TMP122
TMP124

SBOS272B – JUNE 2003 – REVISED DECEMBER 2003

1.5°C Accurate Programmable Digital Temperature Sensors with SPI™ Interface

FEATURES

- **DIGITAL OUTPUT: SPI-Compatible Interface**
- **PROGRAMMABLE RESOLUTION:
9- to 12-Bits + Sign**
- **ACCURACY:
±1.5°C from –25°C to +85°C (max)
±2.0°C from –40°C to +125°C (max)**
- **LOW QUIESCENT CURRENT: 50μA**
- **WIDE SUPPLY RANGE: 2.7V to 5.5V**
- **TINY SOT23-6 AND SO-8 PACKAGES**
- **OPERATION TO 150°C**
- **PROGRAMMABLE HIGH/LOW SETPOINTS**

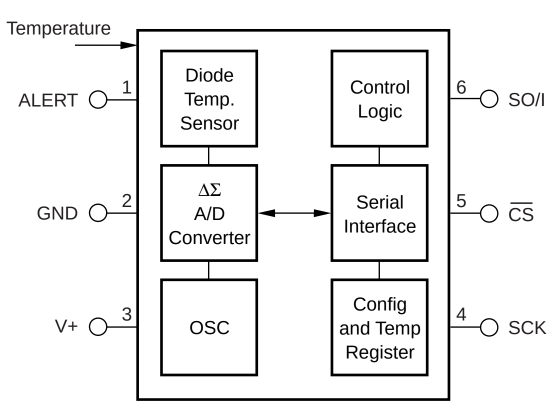
APPLICATIONS

- **POWER-SUPPLY TEMPERATURE MONITORING**
- **COMPUTER PERIPHERAL THERMAL PROTECTION**
- **NOTEBOOK COMPUTERS**
- **CELL PHONES**
- **BATTERY MANAGEMENT**
- **OFFICE MACHINES**
- **THERMOSTAT CONTROLS**
- **ENVIRONMENTAL MONITORING and HVAC**
- **ELECTROMECHANICAL DEVICE TEMPERATURE**

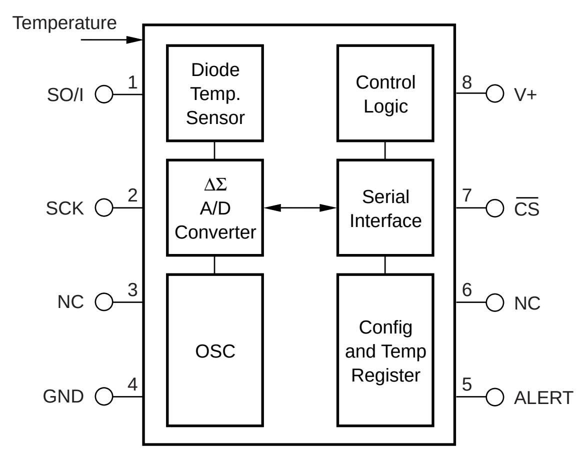
DESCRIPTION

The TMP122 and TMP124 are SPI-compatible temperature sensors available in SOT23-6 and SO-8 packages. Requiring only a pull-up resistor for complete function, the TMP122 and TMP124 temperature sensors are capable of measuring temperatures within 2°C of accuracy over a temperature range of –40°C to +125°C, with operation up to 150°C. Programmable resolution, programmable set points and shut down function provide versatility for any application. Low supply current and a supply range from 2.7V to 5.5V make the TMP122 and TMP124 excellent candidates for low-power applications.

The TMP122 and TMP124 are ideal for extended thermal measurement in a variety of communication, computer, consumer, environmental, industrial, and instrumentation applications.



TMP122



TMP124

ABSOLUTE MAXIMUM RATINGS[1]

Power Supply, V+	7V
Input Voltage[2]	–0.3V to 7V
Input Current	10mA
Operating Temperature Range	–55°C to +150°C
Storage Temperature Range	–60°C to +150°C
Junction Temperature (T_J Max)	+150°C
Lead Temperature (soldering)	+300°C

NOTES: (1) Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. Exposure to absolute maximum conditions for extended periods may affect device reliability. (2) Input voltage rating applies to all TMP122 and TMP124 input voltages.

ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

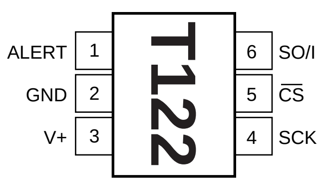
PACKAGE/ORDERING INFORMATION

PRODUCT	PACKAGE-LEAD	PACKAGE DESIGNATOR[1]	SPECIFIED TEMPERATURE RANGE	PACKAGE MARKING	ORDERING NUMBER	TRANSPORT MEDIA, QUANTITY
TMP122	SOT23-6	DBV	–40°C to +125°C	T122	TMP122AIDBVT	Tape and Reel, 250
"	"	"	"	"	TMP122AIDBVR	Tape and Reel, 3000
TMP124	SO-8	D	–40°C to +125°C	T124	TMP124AID	Rails, 100
"	"	"	"	"	TMP124AIDR	Tape and Reel, 2500

NOTE: (1) For the most current specifications and package information, refer to our web site at www.ti.com.

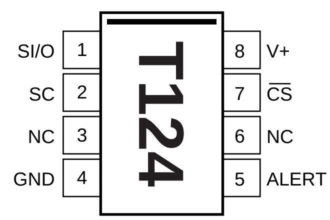
PIN CONFIGURATIONS

Top View **SOT23-6**



TMP122

Top View **SO-8**



TMP124

NC = No Connection

ELECTRICAL CHARACTERISTICS

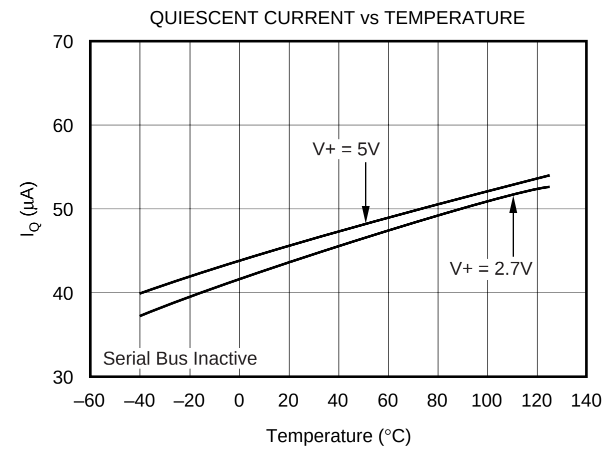
At T_A = –40°C to +125°C, and V+ = 2.7V to 5.5V, unless otherwise noted.

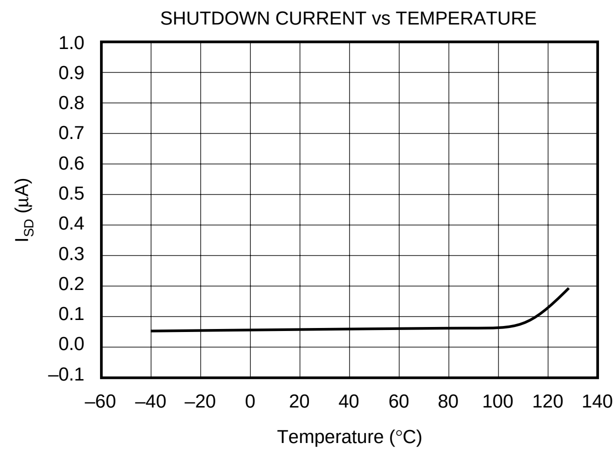
PARAMETER		CONDITION	TMP122, TMP124 MIN	TYP	MAX	UNITS
TEMPERATURE INPUT						
Range			–40		+125	°C
Accuracy (Temperature Error)		–25°C to +85°C		±0.5	±1.5	°C
		–40°C to +125°C		±1.0	±2.0	°C
		–55°C to +150°C		±1.5		°C
vs Supply			–0.3	0.1	+0.3	°C/V
Resolution(1)		Selectable		±0.0625		°C
DIGITAL INPUT/OUTPUT						
Input Logic Levels:						
V_{IH}			0.7(V+)			V
V_{IL}					0.3(V+)	V
Input Current, SO/I, SCK, $\overline{CS}$		0V ≤ V_{IN} ≤ V+			±1	µA
Output Logic Levels:						
V_{OL} SO/I		I_{SINK} = 3mA			0.4	V
V_{OH} SO/I		I_{SOURCE} = 2mA	(V+)–0.4			V
V_{OL} ALERT		I_{SINK} = 4mA			0.4	V
Leakage Current ALERT		0V ≤ V_{IN} ≤ 6V			±1	µA
Input Capacitance, SO/I, SCK, $\overline{CS}$, ALERT				2.5		pF
Resolution		Selectable		9 to 12 + Sign		Bits
Conversion Time		9-Bit + Sign		30	40	ms
		10-Bit + Sign		60	80	ms
		11-Bit + Sign		120	160	ms
		12-Bit + Sign		240	320	ms
POWER SUPPLY						
Operating Range			2.7		5.5	V
Quiescent Current	I_Q	Serial Bus Inactive		50	75	µA
Shutdown Current	I_{SD}	Serial Bus Inactive		0.1	1	µA
TEMPERATURE RANGE						
Specified Range			–40		+125	°C
Operating Range			–55		+150	°C
Storage Range			–60		+150	°C
Thermal Resistance, θ_{JA}		SOT23-6 Surface-Mount		200		°C/W
		SO-8 Surface-Mount		150		°C/W

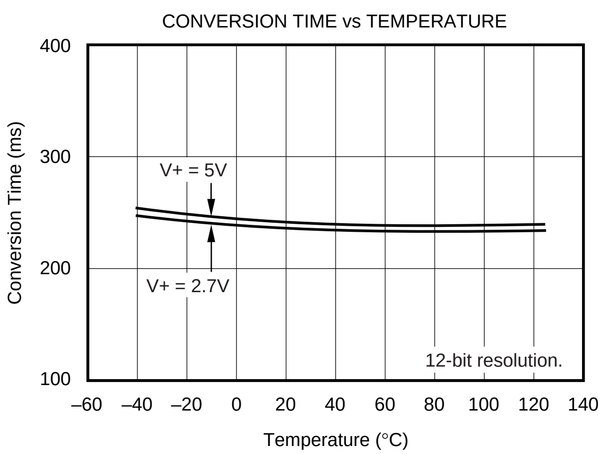
NOTE: (1) Specified for 12-bit resolution.

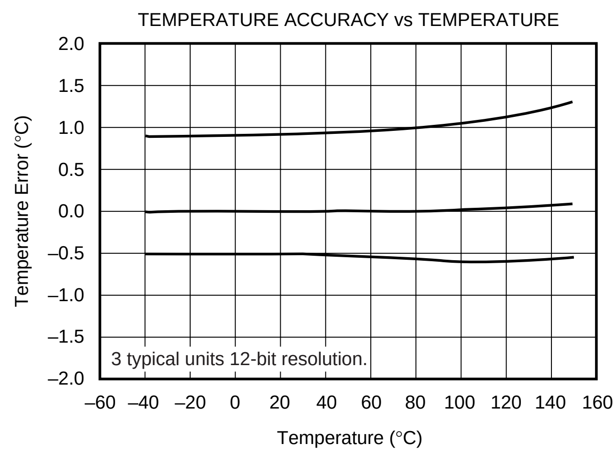
TYPICAL CHARACTERISTICS

At T_A = +25°C, and V+ = 5.0V, unless otherwise noted.









APPLICATIONS INFORMATION

The TMP122 and TMP124 digital temperature sensors are optimal for thermal management and thermal protection applications. The TMP122/TMP124 are SPI interface-compatible and specified for a temperature range of –40°C to +125°C.

The TMP122/TMP124 require minimal external components for operation, needing only a pull-up resistor on the ALERT pin and a bypass capacitor on the supply. Bypass capacitors of 0.1µF is recommended. Figure 1 shows typical connections for the TMP122 and TMP124.

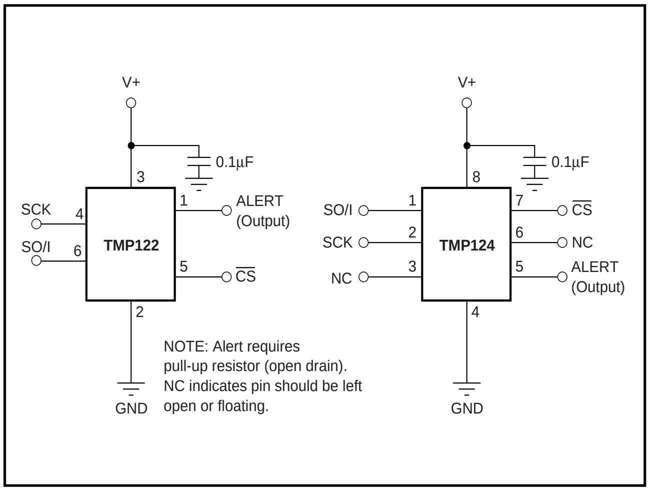


FIGURE 1. Typical Connections of the TMP122 and TMP124.

To maintain accuracy in applications requiring air or surface temperature measurement, care should be taken to isolate the package and leads from ambient air temperature.

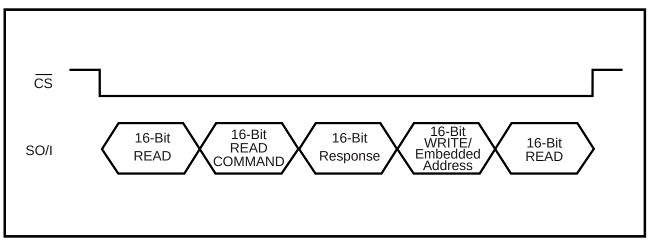


FIGURE 2.Multiple Command Sequence.

COMMUNICATING WITH THE TMP122

The TMP122/TMP124 converts continuously. If $\overline{CS}$ is brought low during a conversion the conversion process continues, but the last completed conversion is available at the output register. Communication with the TMP122/TMP124 is initiated by pulling $\overline{CS}$ low. The first 16 clocks of data transfer will return temperature data from the temperature sensors. The 16-bit data word is clocked out sign bit first, followed by the MSB. Any portion of the 16-bit word may be read before raising $\overline{CS}$. If the user wishes to continue with $\overline{CS}$ low, the following 16 clocks transfer in a READ or WRITE command. READ and WRITE commands are described in Tables I and II.

The READ command contains an embedded address in bits D4 and D3 to identify which register to read. Bits D4 and D3 are internally registered and will hold their value following a READ command until a entire 16-bit read is completed by the user. The completion of the 16-bit READ acknowledges that the READ command has been completed. If the user issues a READ command and then raises $\overline{CS}$ with less than 16 subsequent clocks, the data from that register will be available at the next fall of $\overline{CS}$. The registered READ address will remain in effect until a full 16 clocks have been received. After the completion of a 16-bit READ from the part, the READ address is reset to return data from the Temperature Register. A WRITE command to a register will not change the READ address registered. For further discussion on the READ address register, see the *Read Address Register* section.

Multiple commands may be strung together as illustrated in Figure 2. The TMP122/TMP124 accepts commands alternating with 16-bit response data. On lowering $\overline{CS}$, the part always responds with a READ from the address location indicated by the READ address register. If the next command is a READ command then data is returned from the address specified by the READ command with the 16th clock resetting the READ address register to the default temperature register. The TMP122/TMP124 then expect a 16-bit command. If the command is a WRITE command, then the 16 clocks following the command will again return temperature data.

Figures 3, 4, 5, and 6 detail the communication sequences.

Read Command	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Temperature	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Configuration Register	1	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0
Low Temp Threshold	1	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0
High Temp Threshold	1	0	0	0	0	0	0	0	0	0	0	1	1	0	0	0

TABLE I. Read Command.

Write Command	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Configuration Register	0	0	0	0	D1	D0	R1	R0	F1	F0	POL	TM1	TM0	0	1	0
Low Temp Threshold	T12	T11	T10	T9	T8	T7	T6	T5	T4	T3	T2	T1	T0	1	0	0
High Temp Threshold	T12	T11	T10	T9	T8	T7	T6	T5	T4	T3	T2	T1	T0	1	1	0
Shutdown Command	x	x	x	x	x	x	x	x	1	1	1	1	1	1	1	1

TABLE II. Write Command.

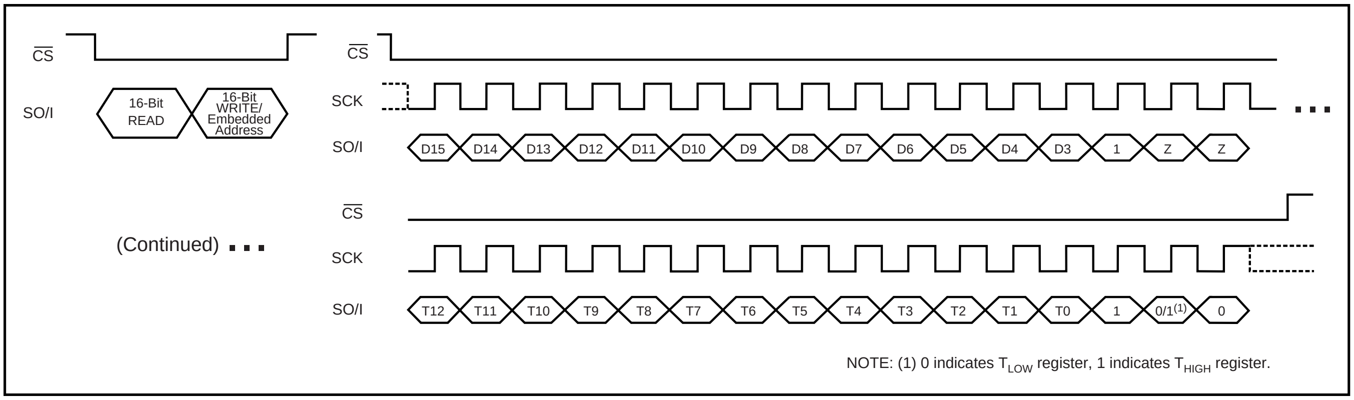


FIGURE 3. READ followed by WRITE COMMAND to T_{LOW}/T_{HIGH} Register.

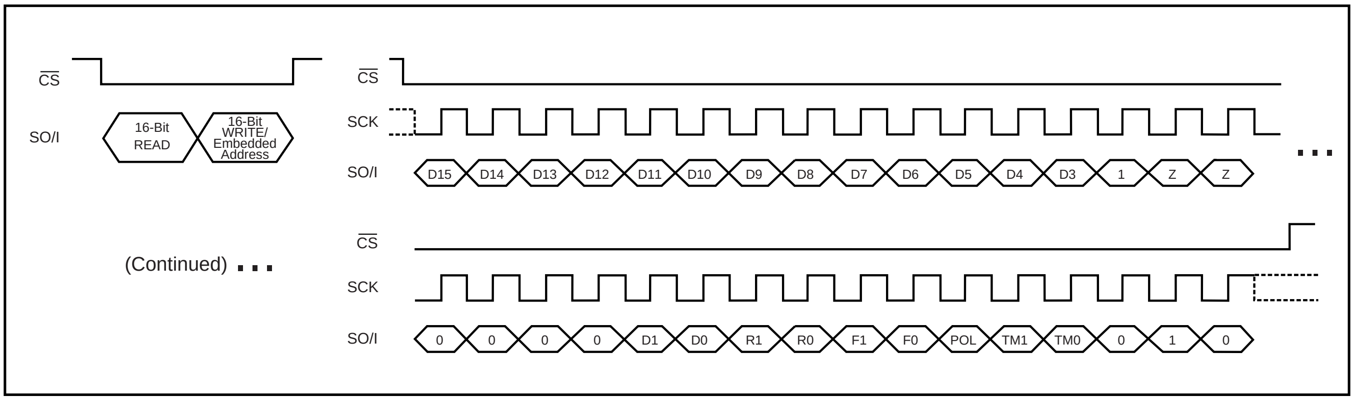


FIGURE 4. READ followed by WRITE COMMAND to Configuration Register.

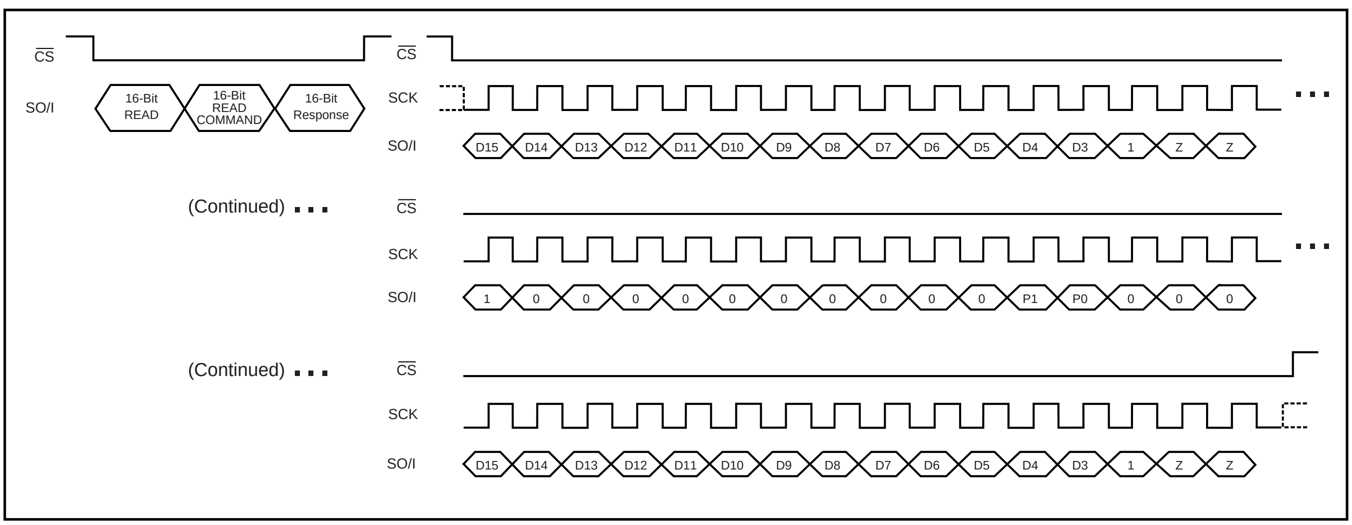


FIGURE 5. READ followed by READ COMMAND and Response.

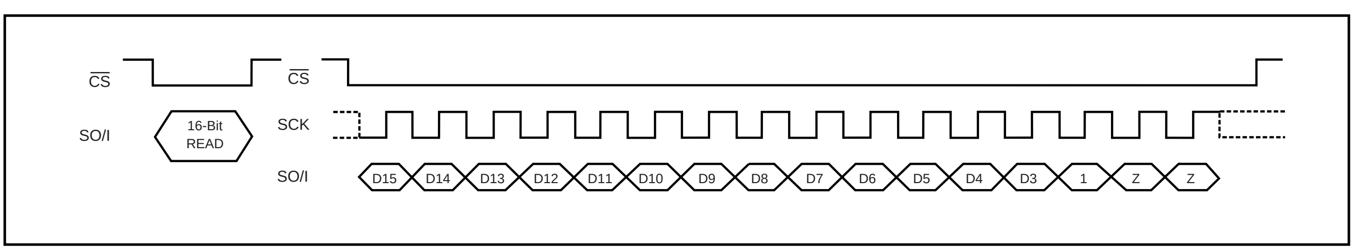


FIGURE 6. Data READ.

READ ADDRESS REGISTER

Figure 7 shows the internal register structure of the TMP122/TMP124. Table III describes the addresses of the registers available. The READ address register uses the two bits to identify which of the data registers should respond to a read command. Following a complete 16-bit read, the READ address register is reset to the default power-up state of P1/P0 equal 0/0.

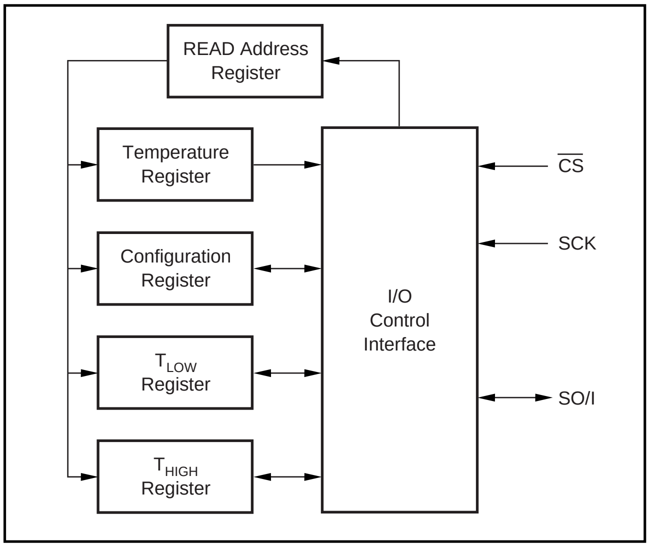


FIGURE 7. Internal Register Structure of the TMP122 and TMP124.

P1	P0	REGISTER
0	0	Temperature Register (READ Only)
0	1	Configuration Register (READ/WRITE)
1	0	T_{LOW} Register (READ/WRITE)
1	1	T_{HIGH} Register (READ/WRITE)

TABLE III. Pointer Addresses of the TMP122 and TMP124 Registers.

TEMPERATURE REGISTER

The Temperature Register of the TMP122/TMP124 is a 16-bit, signed read-only register that stores the output of the most recent conversion. The TMP122/TMP124 are specified for the temperature range of –40°C to +125°C with operation from –55°C to +150°C. Up to 16 bits can be read to obtain data and are described in Table IV. The first 13 bits are used to indicate temperature where bit D2 is 1, and D1, D0 are in a high impedance state. Data format for temperature is summarized in Table V. Following power-up or reset, the Temperature Register will read 0°C until the first conversion is complete.

D15	D14	D13	D12	D11	D10	D9	D8
T12	T11	T10	T9	T8	T7	T6	T5

D7	D6	D5	D4	D3	D2	D1	D0
T4	T3	T2	T1	T0	1	Z	Z

TABLE IV. Temperature Register.

TEMPERATURE (°C)	DIGITAL OUTPUT(1) (BINARY)	HEX
150	0100 1011 0000 0111	4B07
125	0011 1110 1000 0111	3E87
25	0000 1100 1000 0111	0C87
0.0625	0000 0000 0000 1111	000F
0	0000 0000 0000 0111	0007
–0.0625	1111 1111 1111 1111	FFFF
–25	1111 0011 1000 0111	F387
–55	1110 0100 1000 0111	E487

NOTE: (1) The last 2 bits are high impedance and are shown as 11 in the table.

TABLE V. Temperature Data Format.

The user can obtain 9, 10, 11, or 12 bits of resolution by addressing the Configuration Register and setting the resolution bits accordingly. For 9-, 10-, or 11-bit resolution, the most significant bits in the Temperature Register are used with the unused LSBs set to zero.

CONFIGURATION REGISTER

The Configuration Register is a 16-bit read/write register used to store bits that control the operational modes of the temperature sensor. Read/write operations are performed MSB first. The format of the Configuration Register for the TMP122/TMP124 is shown in Table VI, followed by a breakdown of the register bits. The power-up/reset value of the Configuration Register bits R1/R0 equal 1/1, all other bits equal zero.

D15	D14	D13	D12	D11	D10	D9	D8
0	0	0	0	D1	D0	R1	R0

D7	D6	D5	D4	D3	D2	D1	D0
F1	F0	POL	TM1	TM0	0	1	0

TABLE VI. Configuration Register.

SHUTDOWN MODE (SD)

The Shutdown Mode of the TMP122/TMP124 can be used to shut down all device circuitry except the serial interface. Shutdown mode occurs when the last 8 bits of the WRITE command are equal to 1, and will occur once the current conversion is completed, reducing current consumption to less than 1µA. To take the part out of shutdown, send any command or pattern after the 16-bit read with the last 8 bits not equal to one. Power on default is in active mode.

THERMOSTAT MODE (TM1/TM0)

The Thermostat Mode bits of the TMP122/TMP124 indicate to the device whether to operate in Comparator Mode, Interrupt Mode or Interrupt Comparator Mode. For more information on Comparator and Interrupt Mode, see text HIGH and LOW limit registers. The bit assignments for thermostat mode are described in Table VII. Power on default is comparator mode.

TM1	TM0	MODE OF OPERATION
0	0	Comparator Mode
0	1	Interrupt Mode
1	0	Interrupt Comparator Mode
1	1	—

TABLE VII. Mode Settings of the TMP122.

POLARITY (POL)

The Polarity Bit of the TMP122/TMP124 adjusts the polarity of the ALERT pin output. By default, POL = 0 and the ALERT pin will be active LOW, as shown in Figure 8. For POL = 1 the ALERT Pin will be active HIGH, and the state of the ALERT Pin is inverted.

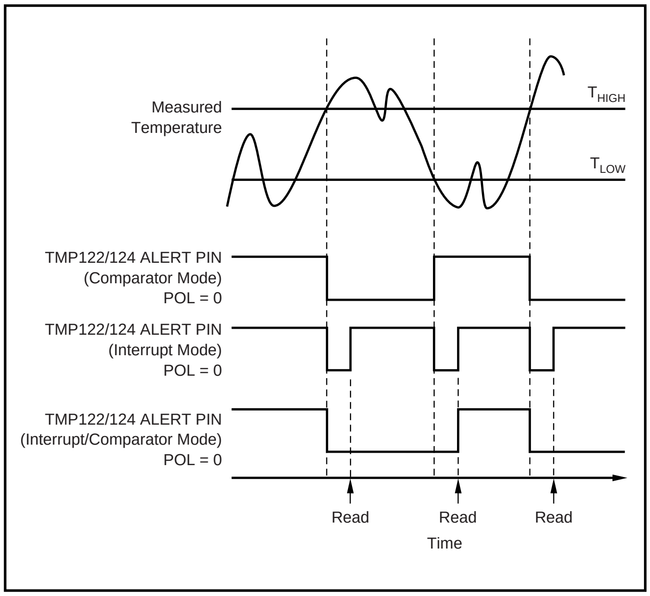


FIGURE 8. ALERT Output Transfer Function Diagrams.

FAULT QUEUE (F1/F0)

A fault condition occurs when the measured temperature exceeds the limits set in the T_{HIGH} and T_{LOW} registers. The Fault Queue is provided to prevent a false alert due to environmental noise and requires consecutive fault measurements to trigger the alert function of the TMP122/TMP124. Table VIII defines the number of consecutive faults required to trigger a consecutive alert condition. Power-on default for F1/F0 is 0/0.

F1	F0	CONSECUTIVE FAULTS
0	0	1
0	1	2
1	0	4
1	1	6

TABLE VIII. Fault Settings of the TMP122 and TMP124.

HIGH AND LOW LIMIT REGISTERS

In Comparator Mode (TM1/TM0 = 0/0), the ALERT Pin of the TMP122/TMP124 becomes active when the temperature equals or exceeds the value in T_{HIGH} and generates a consecutive number of faults according to fault bits F1 and F0. The ALERT pin will remain active until the temperature falls below the indicated T_{LOW} value for the same number of faults.

In Interrupt Mode (TM1/TM0 = 0/1) the ALERT pin becomes active when the temperature equals or exceeds T_{HIGH} for a consecutive number of fault conditions. The ALERT pin remains active until a read operation of any register occurs. The ALERT pin will also be cleared if the device is placed in Shutdown Mode. Once the ALERT pin is cleared, it will only become active again by the temperature falling below T_{LOW}. When the temperature falls below T_{LOW}, the ALERT pin becomes active and remains active until cleared by a read operation of any register. Once the ALERT pin is cleared, the above cycle will repeat with the ALERT pin becoming active when the temperature equals or exceeds T_{HIGH}.

In Interrupt/Comparator Mode (TM1/TM0 = 1/0), the ALERT Pin of the TMP122/TMP124 becomes active when the temperature equals or exceeds the value in T_{HIGH} and generates a consecutive number of faults according to fault bits F1 and F0. The ALERT pin will remain active until the temperature falls below the indicated T_{LOW} value for the same number of faults and a communication with the device has occurred after that point.

Operational modes are represented in Figure 8. Tables IX and X describe the format for the T_{HIGH} and T_{LOW} registers. Power-up reset values for T_{HIGH} and T_{LOW} are: T_{HIGH} = 80°C and T_{LOW} = 75°C. The format of the data for T_{HIGH} and T_{LOW} is the same as for the Temperature Register.

All 13 bits for the Temperature, T_{HIGH}, and T_{LOW} registers are used in the comparisons for the ALERT function for all converter resolutions. The three LSBs in T_{HIGH} and T_{LOW} can affect the ALERT output even if the converter is configured for 9-bit resolution.

D15	D14	D13	D12	D11	D10	D9	D8
H12	H11	H10	H9	H8	H7	H6	H5

D7	D6	D5	D4	D3	D2	D1	D0
H4	H3	H2	H1	H0	1	1	0

TABLE IX. T_{HIGH} Register.

D15	D14	D13	D12	D11	D10	D9	D8
L12	L11	L10	L9	L8	L7	L6	L5

D7	D6	D5	D4	D3	D2	D1	D0
L4	L3	L2	L1	L0	1	0	0

TABLE X. T_{LOW} Register.

CONVERTER RESOLUTION (R1/R0)

The Converter Resolution Bits control the resolution of the internal Analog-to-Digital (A/D) converter. This allows the user to maximize efficiency by programming for higher resolution or faster conversion time. Table XI identifies the Resolution Bits and the relationship between resolution and conversion time. The TMP122/TMP124 have a default resolution of 12 bits.

R1	R0	RESOLUTION	CONVERSION TIME (typical)
0	0	9 Bits (0.5°C) plus sign	30ms
0	1	10 Bits (0.25°C) plus sign	60ms
1	0	11 Bits (0.125°C) plus sign	120ms
1	1	12 Bits (0.0625°C) plus sign	240ms

TABLE XI. Resolution of the TMP122 and TMP124.

DELAY TIME

The Delay Bits control the amount of time delay between each conversion. This feature allows the user to maximize power savings by eliminating unnecessary conversions, and minimizing current consumption. During active conversion the TMP122/TMP124 typically requires 50µA of current for approximately 0.25s conversion time, and approximately 20µA for idle times between conversions. Delay settings are identified in Table XII as conversion time and period, and are shown in Figure 9. Default power up is D1/D0 equal 0/0. Conversion time and conversion periods scale with resolution. Conversion period denotes time between conversion starts.

D1	D0	CONVERSION TIME	CONVERSION PERIOD
0	0	0.25s	0.25s
0	1	0.25s	0.5s
1	0	0.25s	1s
1	1	0.25s	8s

TABLE XII. Conversion Delay for 12-Bit Resolution.

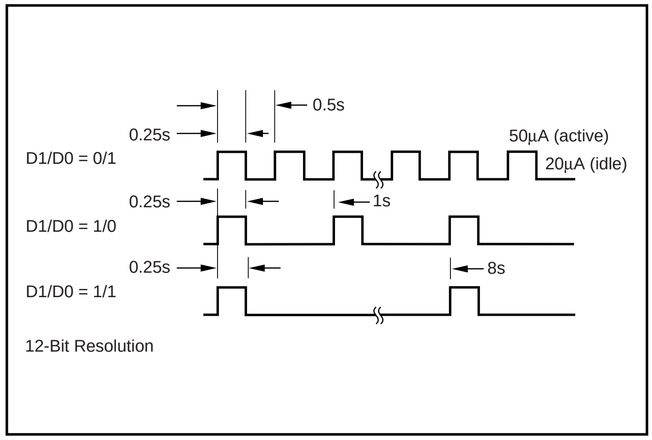


FIGURE 9. Conversion Time and Period Description.

Timing Diagrams

The TMP122/TMP124 are SPI compatible. Figures 10 to 12 describe the various timing parameters of the TMP122/TMP124 with timing definitions in Table XIII.

PARAMETER		MIN	MAX	UNITS
SCK Period	t_1	100		ns
Data In to Rising Edge SCK Setup Time	t_2	20		ns
SCK Falling Edge to Output Data Delay	t_3		30	ns
SCK Rising Edge to Input Data Hold Time	t_4	20		ns
$\overline{CS}$ to Rising Edge SCK Set-Up Time	t_5	40		ns
$\overline{CS}$ to Output Data Delay	t_6		30	ns
$\overline{CS}$ Rising Edge to Output High Impedance	t_7		30	ns

TABLE XIII. Timing Description.

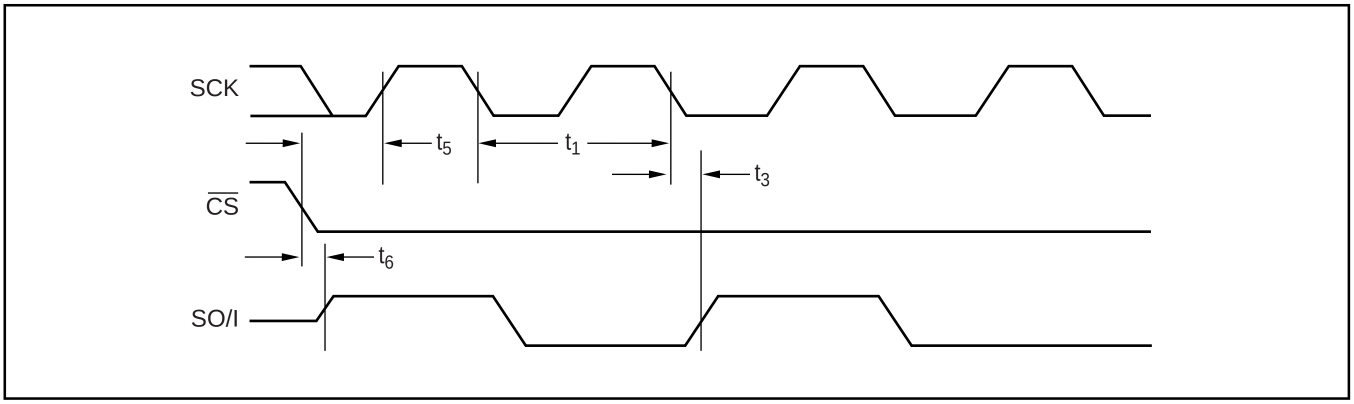


FIGURE 10. Output Data Timing Diagram.

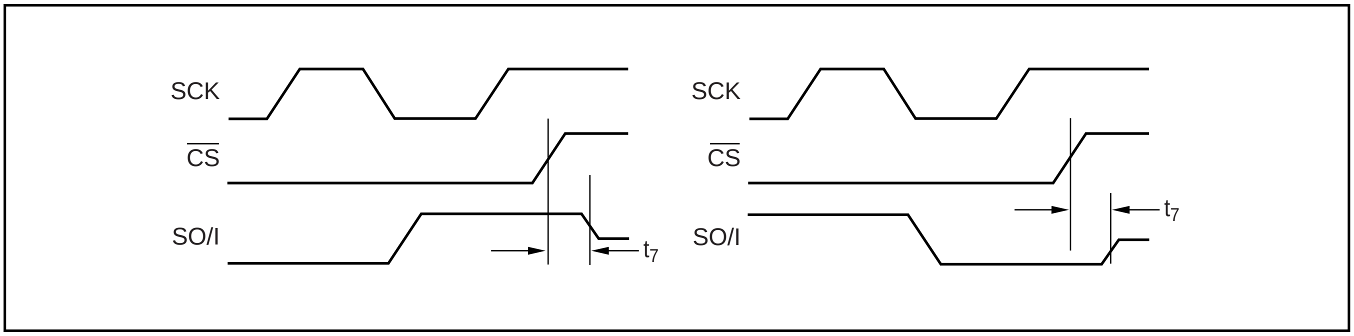


FIGURE 11. High Impedance Output Timing Diagram.

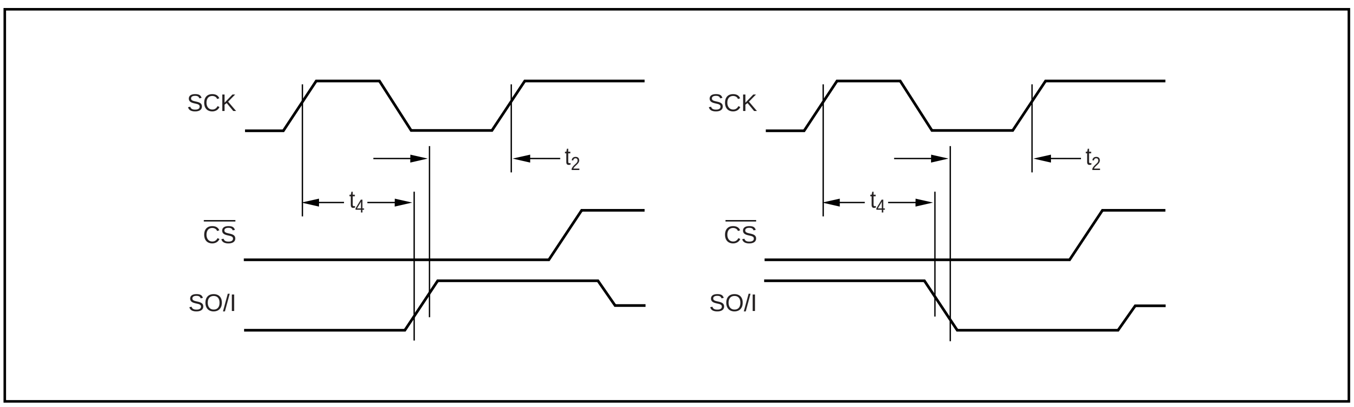


FIGURE 12. Input Data Timing Diagram.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TMP122AIDBVR	ACTIVE	SOT-23	DBV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	T122	Samples
TMP122AIDBVRG4	ACTIVE	SOT-23	DBV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	T122	Samples
TMP122AIDBVT	ACTIVE	SOT-23	DBV	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	T122	Samples
TMP122AIDBVTG4	ACTIVE	SOT-23	DBV	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	T122	Samples
TMP124AID	ACTIVE	SOIC	D	8	96	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	T124	Samples
TMP124AIDG4	ACTIVE	SOIC	D	8	96	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	T124	Samples
TMP124AIDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	T124	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF TMP122 :

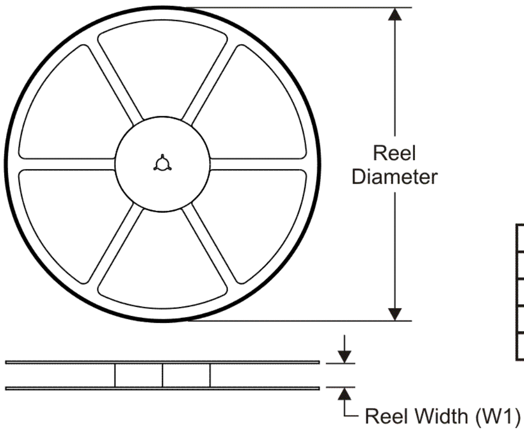
- Enhanced Product: TMP122-EP

NOTE: Qualified Version Definitions:

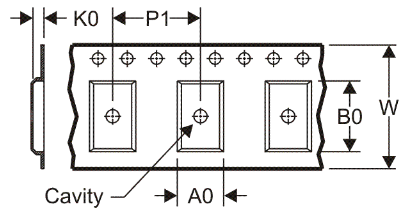
- Enhanced Product - Supports Defense, Aerospace and Medical Applications

TAPE AND REEL INFORMATION

REEL DIMENSIONS

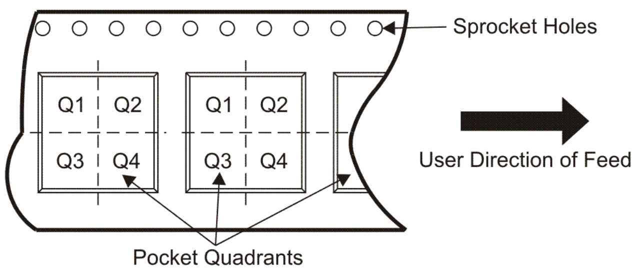


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

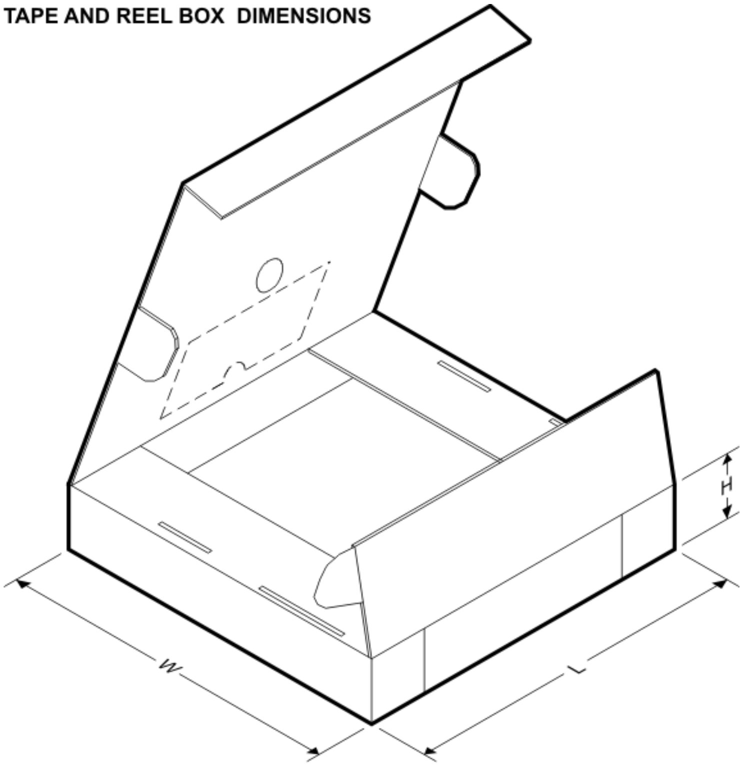
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

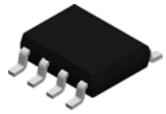
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TMP122AIDBVR	SOT-23	DBV	6	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TMP122AIDBVT	SOT-23	DBV	6	250	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TMP122AIDBVR	SOT-23	DBV	6	3000	180.0	180.0	18.0
TMP122AIDBVT	SOT-23	DBV	6	250	180.0	180.0	18.0

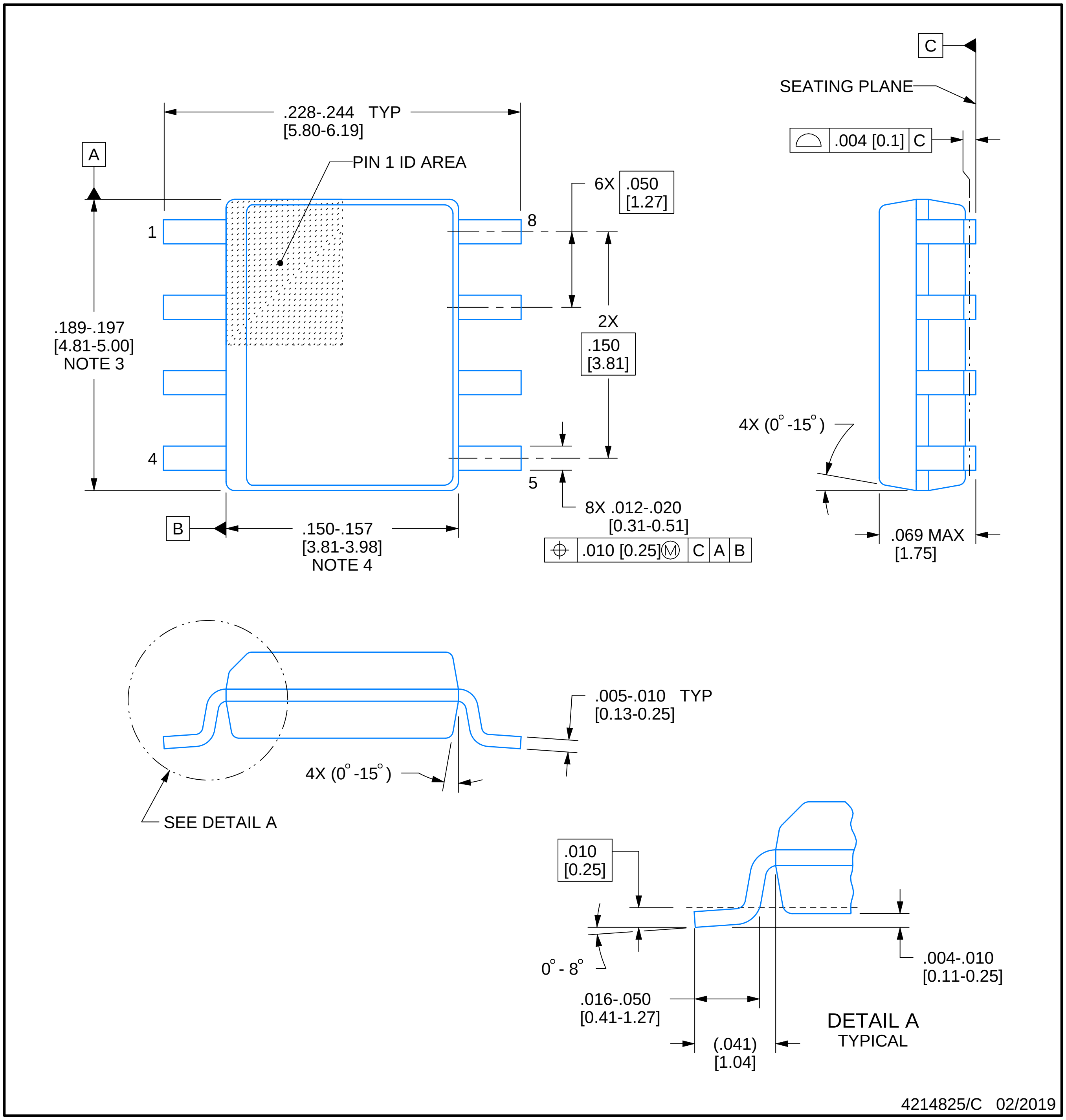


PACKAGE OUTLINE

D0008A

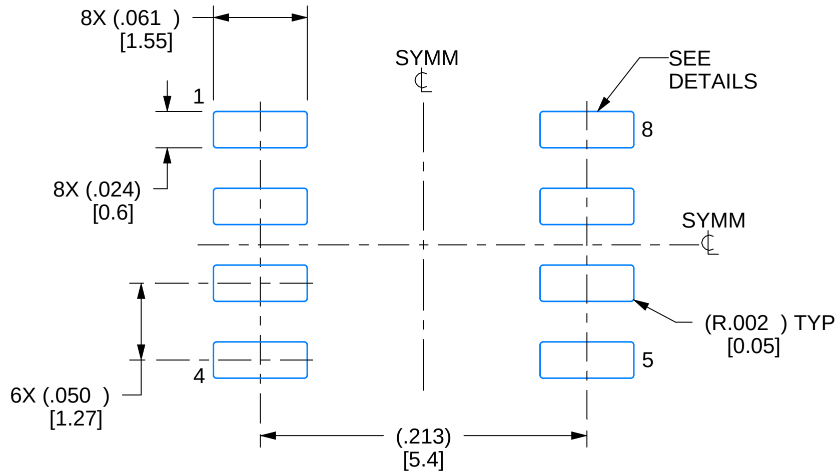
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

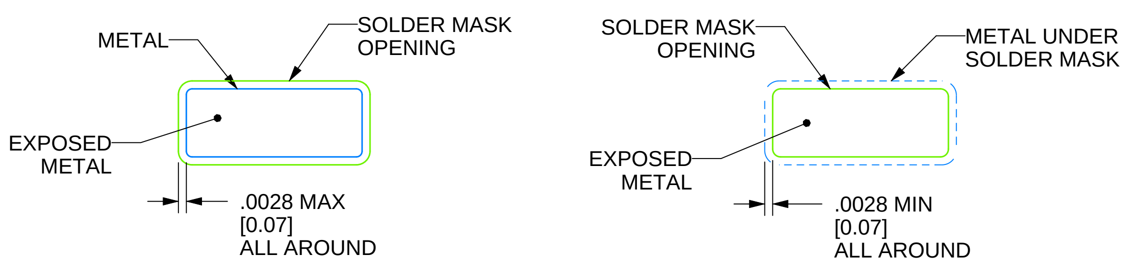


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



NON SOLDER MASK
DEFINED

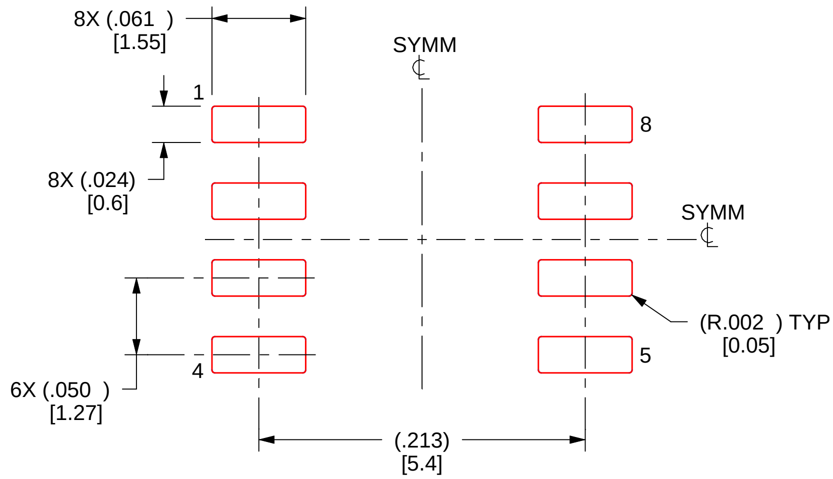
SOLDER MASK
DEFINED

SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

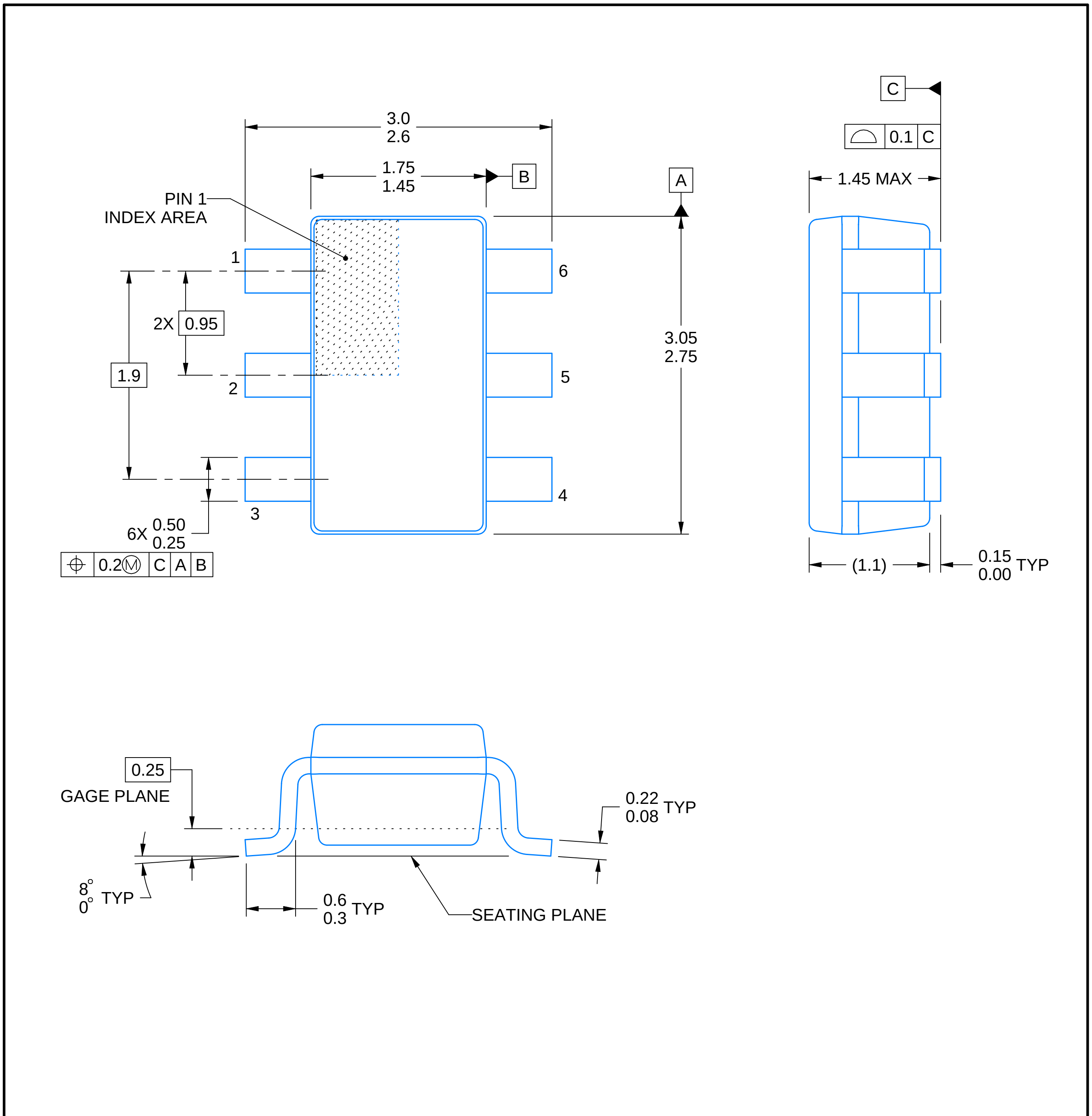


SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

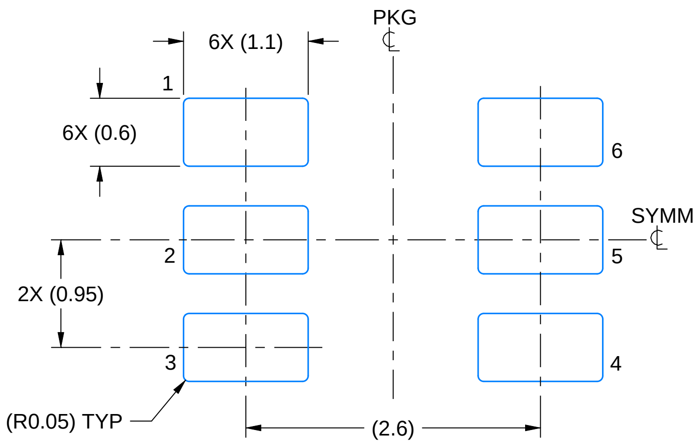
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.



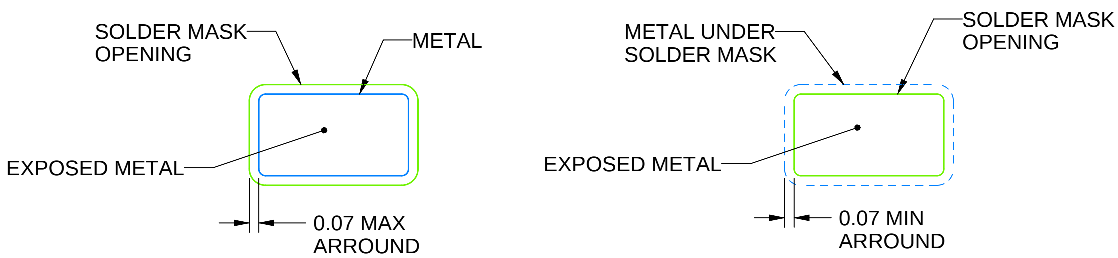
4214840/B 03/2018

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
4. Leads 1,2,3 may be wider than leads 4,5,6 for package orientation.
5. Refernce JEDEC MO-178.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



NON SOLDER MASK DEFINED (PREFERRED)

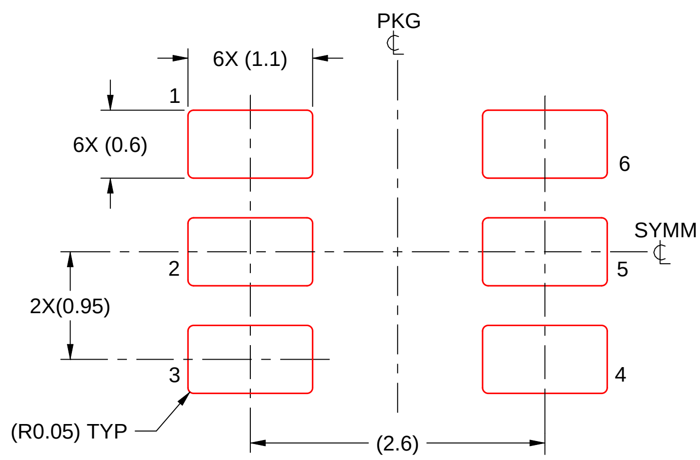
SOLDER MASK DEFINED

SOLDER MASK DETAILS

4214840/B 03/2018

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214840/B 03/2018

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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