1.8V, Resistor-Programmable TEMPERATURE SWITCH and ANALOG OUT TEMPERATURE SENSOR in SC70

Check for Samples: TMP300B-Q1

FEATURES

- **ACCURACY: ±1°C (typical at +25°C)**
- **PROGRAMMABLE TRIP POINT**
- **PROGRAMMABLE HYSTERESIS: 5°C/10°C**
- **OPEN-DRAIN OUTPUTS**
- **LOW-POWER: 110μA (max)**
- **WIDE VOLTAGE RANGE: +1.8V to +18V**
- **OPERATION: –40°C to +150°C**
- **ANALOG OUT: 10mV/°C**
- **SC70-6 PACKAGE**

APPLICATIONS

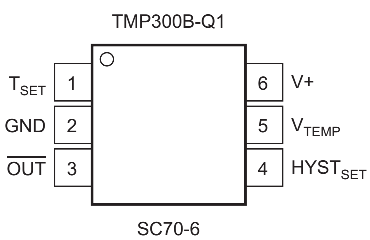
- **QUALIFIED FOR for AUTOMOTIVE APPLICATIONS**
- **POWER-SUPPLY SYSTEMS**
- **DC-DC MODULES**
- **THERMAL MONITORING**
- **ELECTRONIC PROTECTION SYSTEMS**

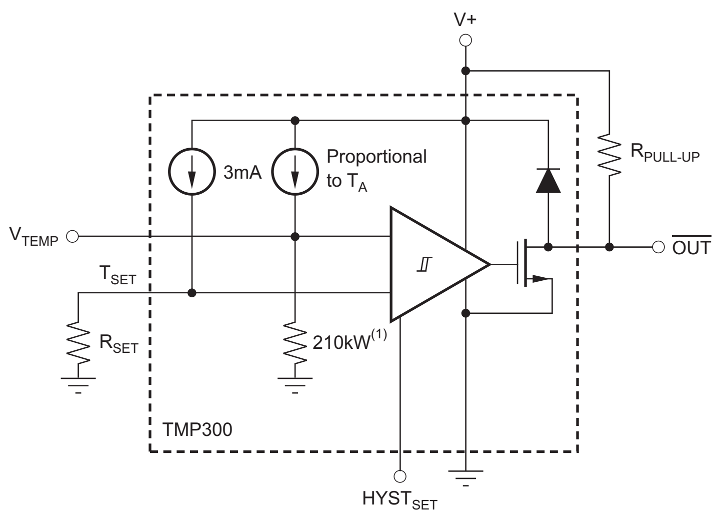
DESCRIPTION

The TMP300B-Q1 is a low-power, resistor-programmable, digital output temperature switch. It allows a threshold point to be set by adding an external resistor. Two levels of hysteresis are available. The TMP300B-Q1 has a V_{TEMP} analog output that can be used as a testing point or in temperature-compensation loops.

With a supply voltage as low as 1.8V and low current consumption, the TMP300B-Q1 is ideal for power-sensitive systems.

Available in two micropackages that have proven thermal characteristics, this part gives a complete and simple solution for users who need simple and reliable thermal management.





NOTE: (1) Thinfilm resistor with approximately 10% accuracy; however, this accuracy error is trimmed out at the factory.

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ORDERING INFORMATION(1)

ORDERABLE P/N	T_A	PACKAGE	TOP SIDE SYMBOL
TMP300BQDCKRQ1 or TMP300B-Q1	-40°C to 125°C	SC70 - DCK | Reel of 3000	SBG

(1) For the most current package and ordering information see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.

ABSOLUTE MAXIMUM RATINGS(1)

		VALUE	UNIT
Supply Voltage	V+	+18	V
Signal Input Terminals, Voltage(2)		–0.5 to (V+) + 0.5	V
Signal Input Terminals, Current(2)		±10	mA
Output Short-Circuit(3)	I_{SC}	Continuous	
Open-Drain Output		(V+) + 0.5	V
Operating Temperature	T_A	–40 to +150	°C
Storage Temperature	T_A	–55 to +150	°C
Junction Temperature	T_J	+150	°C
ESD Rating	Human Body Model (HBM)	4000	V
	Charged Device Model (CDM)	1000	V
	Machine Model (MM)	200	V

(1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not supported.
(2) Input terminals are diode-clamped to the power-supply rails. Input signals that can swing more than 0.5V beyond the supply rails should be current limited to 10mA or less.
(3) Short-circuit to ground.

ELECTRICAL CHARACTERISTICS

At V_S = 3.3V and T_A = –40°C to +125°C, unless otherwise noted.

PARAMETER		TEST CONDITIONS	TMP300B-Q1 MIN	TMP300B-Q1 TYP	TMP300B-Q1 MAX	UNIT
TEMPERATURE MEASUREMENT						
Measurement Range		V_S = 2.35V to 18V	–40		+125	°C
		V_S = 1.8V to 2.35V	–40		100 × (V_S – 0.95)	°C
TRIP POINT						
Total Accuracy		T_A = –40°C to +125°C		±2	±6	°C
R_{SET} Equation		T_C is in °C	R_{SET} = 10 (50 + T_C)/3			kΩ
HYSTERESIS SET INPUT						
LOW Threshold (1)					0.4	V
HIGH Threshold (1)			V_S – 0.4			V
Threshold Hysteresis		$HYST_{SET}$ = GND		5		°C
		$HYST_{SET}$ = V_S		10		°C
DIGITAL OUTPUT						
Logic Family				CMOS		
Open-Drain Leakage Current (1)		OUT = V_S			10	µA
Logic Levels						
V_{OL}		V_S = 1.8V to 18V, I_{SINK} = 5mA			0.3	V
ANALOG OUTPUT						
Accuracy				±2	±5	°C
Temperature Sensitivity				10		mV/°C
Output Voltage (1)		T_A = +25°C	720	750	780	mV
V_{TEMP} Pin Output Resistance				210		kΩ
POWER SUPPLY						
Quiescent Current(2)	I_Q	V_S = 1.8V to 18V, T_A = –40°C to +125°C			110	µA
TEMPERATURE RANGE						
Specified Range	T_A	V_S = 2.35V to 18V	–40		+125	°C
		V_S = 1.8V to 2.35V	–40		100 × (V_S – 0.95)	°C
Operating Range	T_A	V_S = 2.35V to 18V	–40		+150	°C
		V_S = 1.8V to 2.35V	–50		100 × (V_S – 0.95)	°C
Thermal Resistance	θ_{JA}					
SC70				250		°C/W
SOT23-6				180		°C/W

(1) Specified by design. Not production tested.
(2) See Figure 1 for typical quiescent current.

TYPICAL CHARACTERISTICS

At V_S = 5V, unless otherwise noted.

QUIESCENT CURRENT OVER TEMPERATURE AND SUPPLY

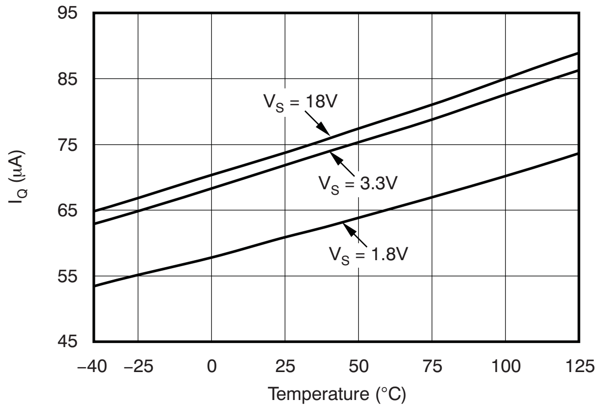


Figure 1.

R_{SET} SHIFT DUE TO R_{SET} TOLERANCE

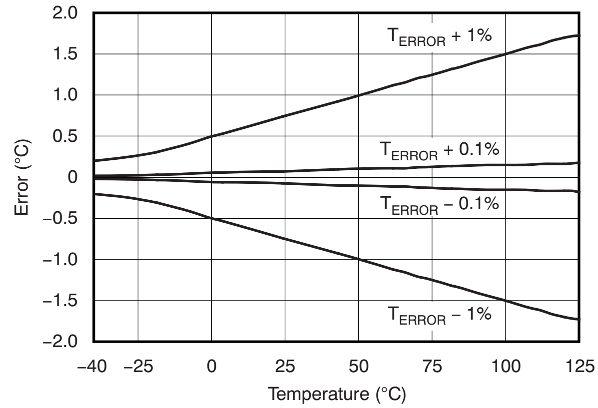


Figure 2.

R_{SET} vs TEMPERATURE

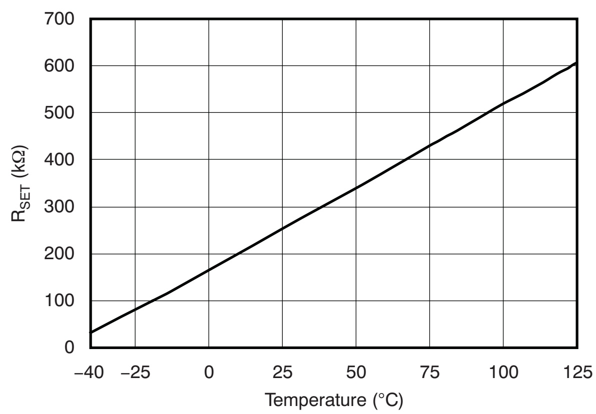


Figure 3.

TYPICAL TRIP ERROR

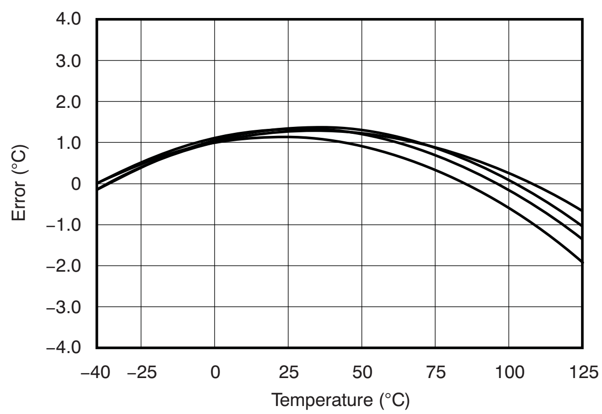


Figure 4.

TYPICAL ANALOG OUTPUT ERROR

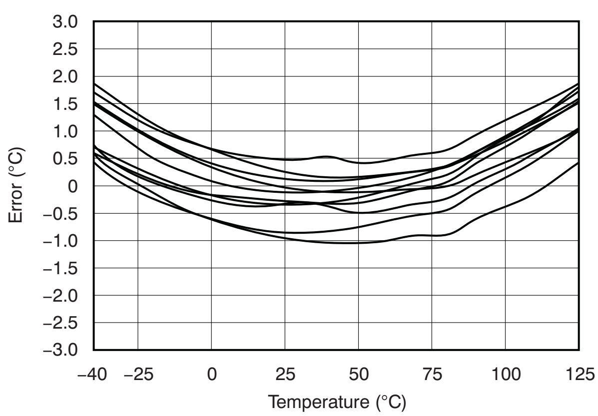


Figure 5.

ANALOG PSR OVER TEMPERATURE

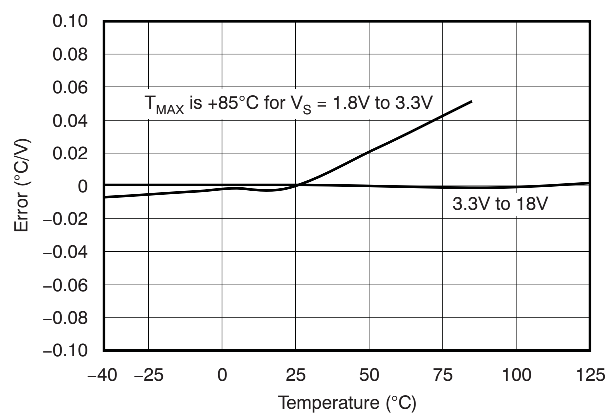


Figure 6.

TYPICAL CHARACTERISTICS (continued)

At V_S = 5V, unless otherwise noted.

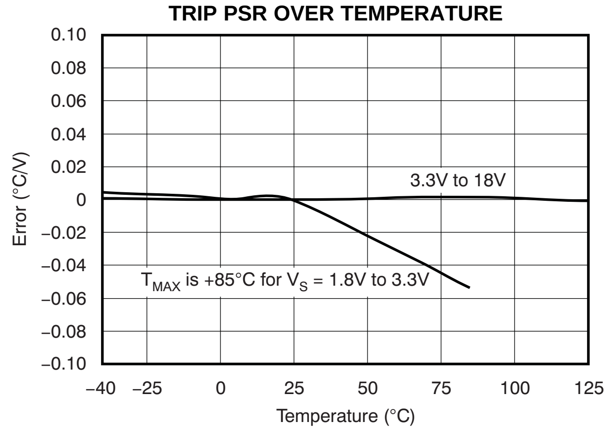


Figure 7.

APPLICATIONS INFORMATION

The TMP300B-Q1 is a thermal sensor designed for over-temperature protection circuits in electronic systems. The TMP300B-Q1 uses a set resistor to program the trip temperature of the digital output. An additional high-impedance (210kΩ) analog voltage output provides the temperature reading.

CALCULATING R_{SET}

The set resistor (R_{SET}) provides a threshold voltage for the comparator input. The TMP300B-Q1 trips when the V_{TEMP} pin exceeds the T_{SET} voltage. The value of the set resistor is determined by the analog output function and the 3µA internal bias current.

To set the TMP300B-Q1 to trip at a preset value, calculate the R_{SET} resistor value according to Equation 1 or Equation 2:

$$R_{SET} = \frac{(T_{SET} \times 0.01 + 0.5)}{3e^{-6}} \quad (1)$$

Where T_{SET} is in °C; or

$$R_{SET} \text{ in k}\Omega = \frac{10(50 + T_{SET})}{3} \quad (2)$$

Where T_{SET} is in °C.

USING V_{TEMP} TO TRIP THE DIGITAL OUTPUT

The analog voltage output can also serve as a voltage input that forces a trip of the digital output to simulate a thermal event. This simulation facilitates easy system design and test of thermal safety circuits, as shown in Figure 8.

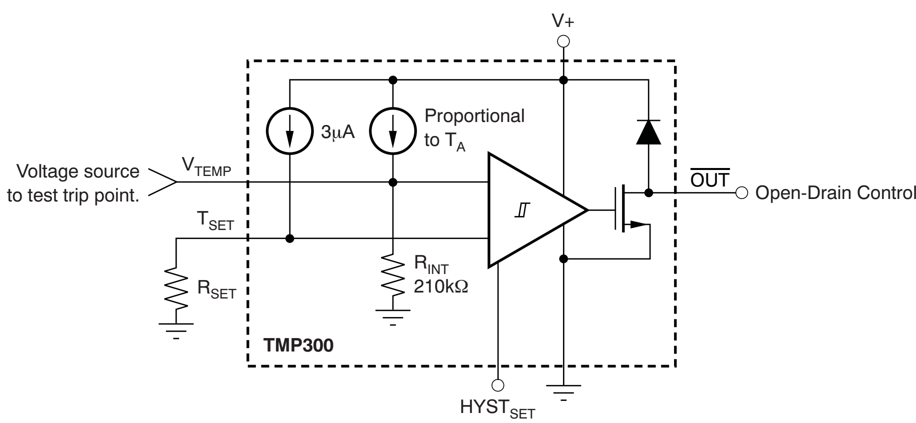


Figure 8. Applying Voltage to Trip Digital Output

ANALOG TEMPERATURE OUTPUT

The analog out or V_{TEMP} pin is high-impedance (210kΩ). Avoid loading this pin to prevent degrading the analog out value or trip point. Buffer the output of this pin when using it for direct thermal measurement. Figure 9 shows buffering of the analog output signal.

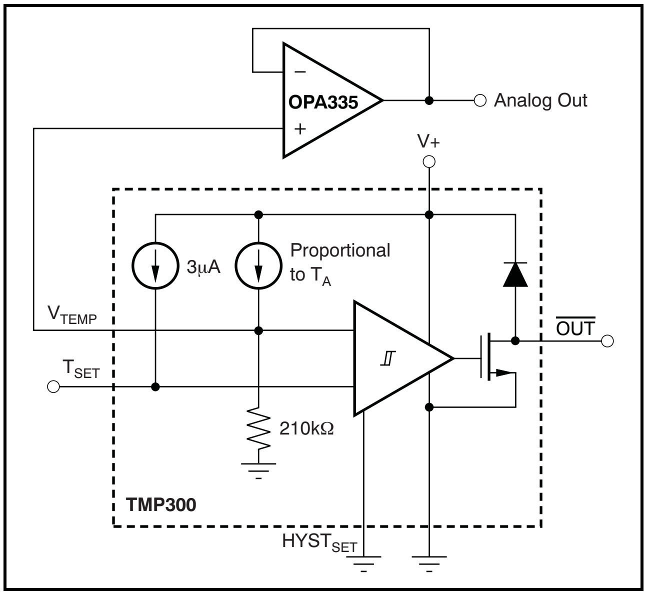


Figure 9. Buffering the Analog Output Signal

USING A DAC TO SET THE TRIP POINT

The trip point is easily converted by changing the digital-to-analog converter (DAC) code. This technique can be useful for control loops where a large thermal mass is being brought up to the set temperature and the $\overline{OUT}$ pin is used to control the heating element. The analog output can be monitored in a control algorithm that adjusts the set temperature to prevent overshoot. Trip set voltage error versus temperature is shown in Figure 10, which shows error in °C of the comparator input over temperature. An alternative method of setting the trip point by using a DAC is shown in Figure 11.

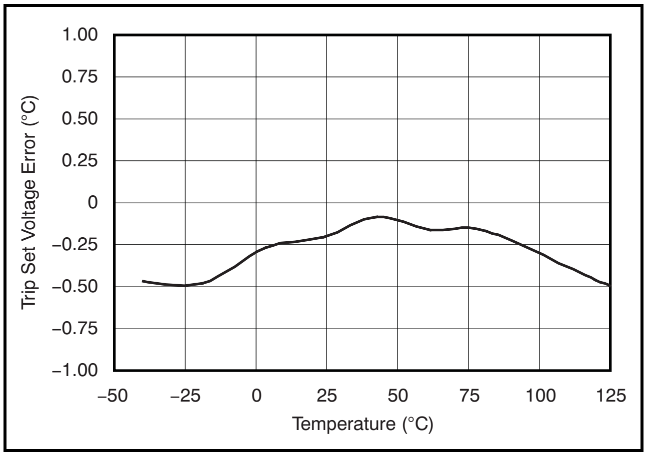


Figure 10. Trip Set Voltage Error vs Temperature

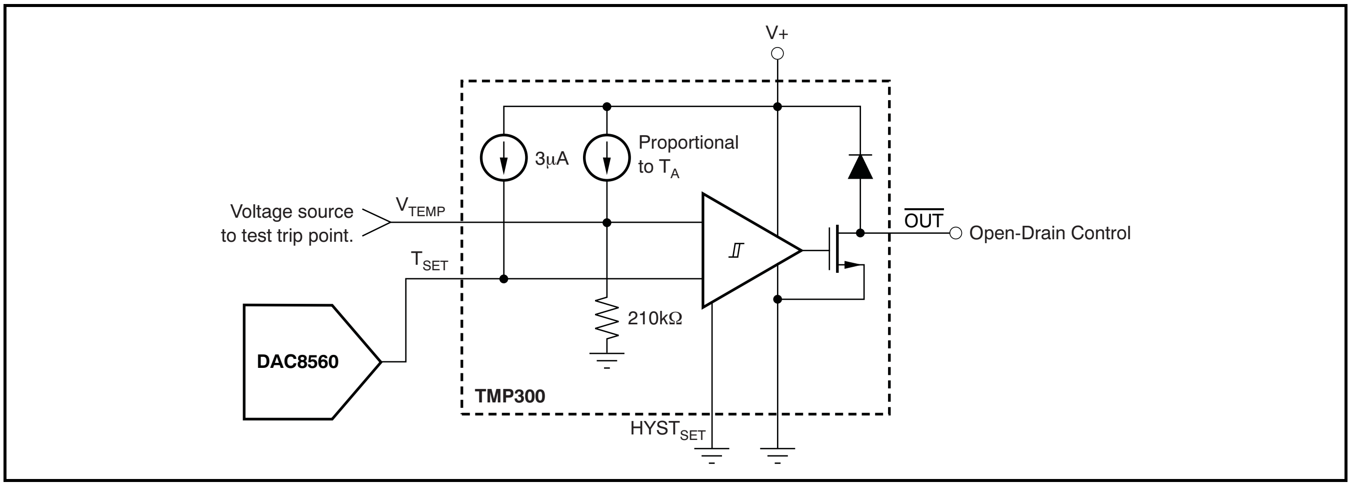


Figure 11. DAC Generates the Voltage-Driving T_{SET} Pin

HYSTERESIS

The hysteresis pin has two settings. Grounding $HYST_{SET}$ results in 5°C of hysteresis. Connecting it to V_S results in 10°C of hysteresis. Hysteresis error variation over temperature is shown in Figure 12 and Figure 13.

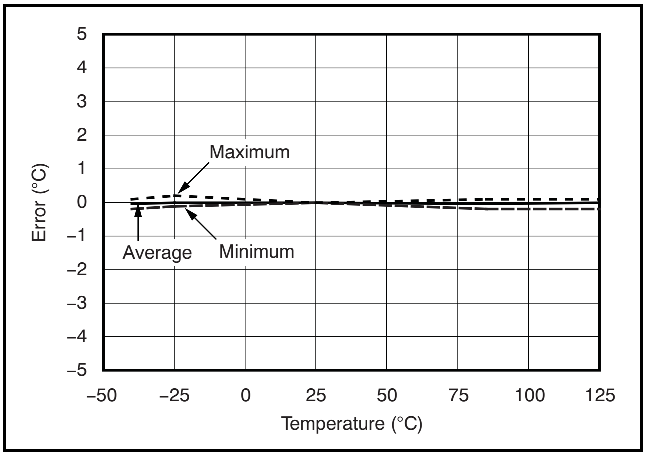


Figure 12. 5°C Hysteresis Error vs Temperature

Bypass capacitors should be used on the supplies as well as on the R_{SET} and analog out (V_{TEMP}) pins when in noisy environments, as shown in Figure 14. These capacitors reduce premature triggering of the comparator.

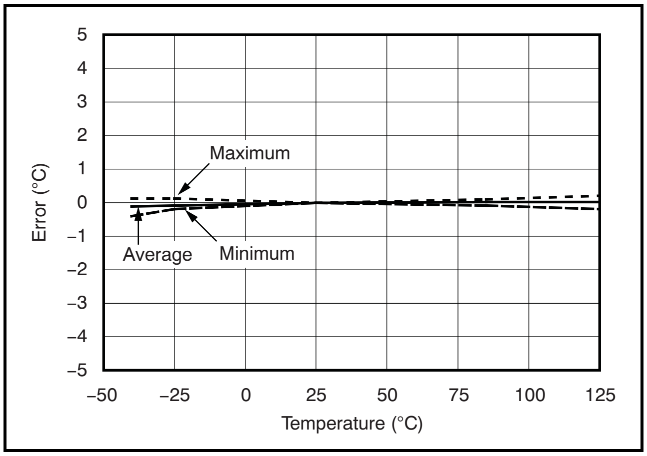


Figure 13. 10°C Hysteresis Error vs Temperature

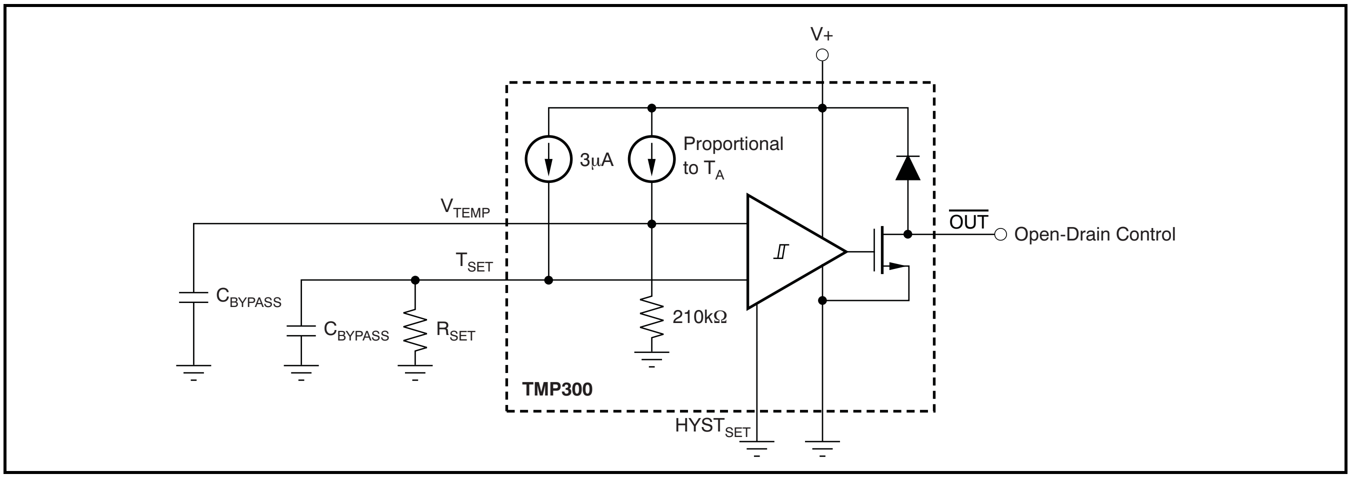


Figure 14. Bypass Capacitors Prevent Early Comparator Toggling Due to Circuit Board Noise

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
TMP300BQDCKRQ1	ACTIVE	SC70	DCK	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	SBG	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

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OTHER QUALIFIED VERSIONS OF TMP300-Q1 :

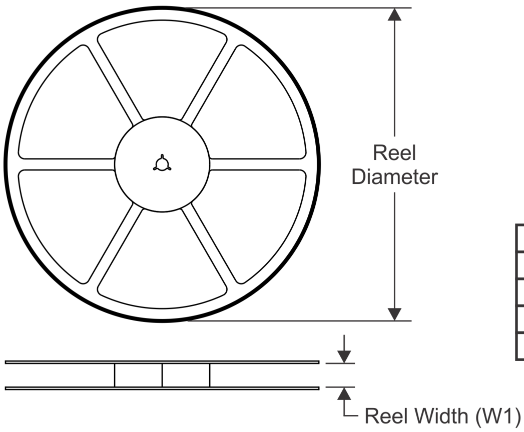
- Catalog: TMP300

NOTE: Qualified Version Definitions:

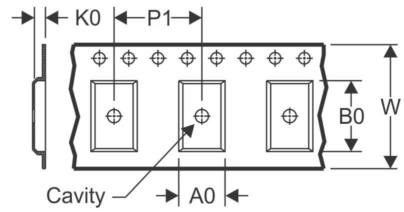
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

REEL DIMENSIONS

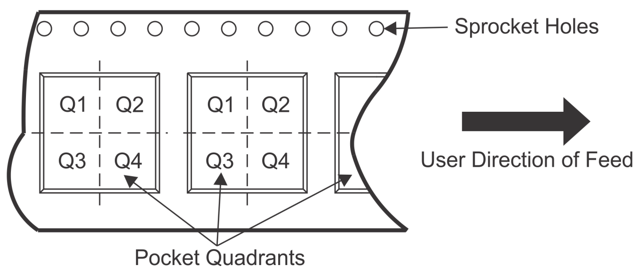


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

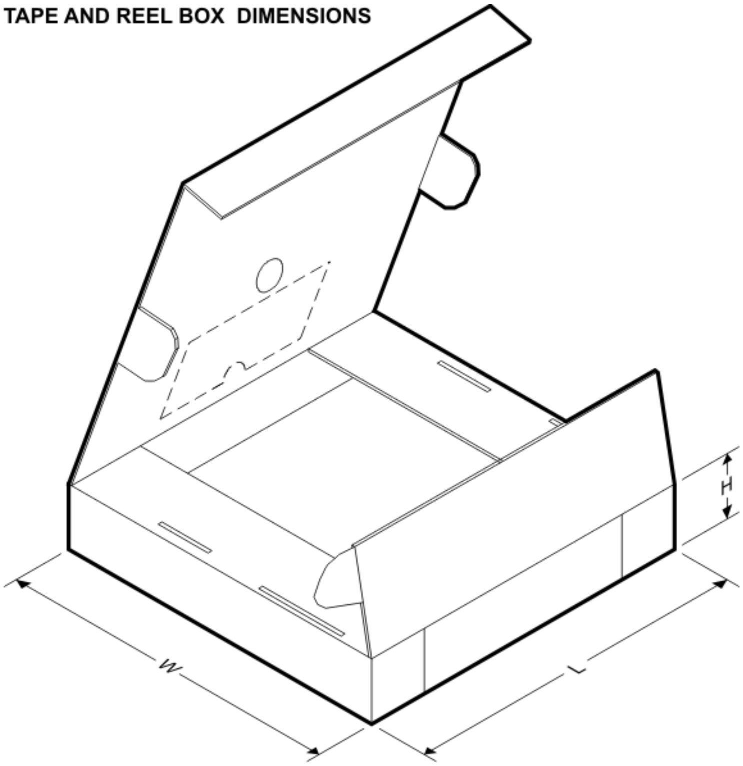
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TMP300BQDCKRQ1	SC70	DCK	6	3000	179.0	8.4	2.2	2.5	1.2	4.0	8.0	Q3

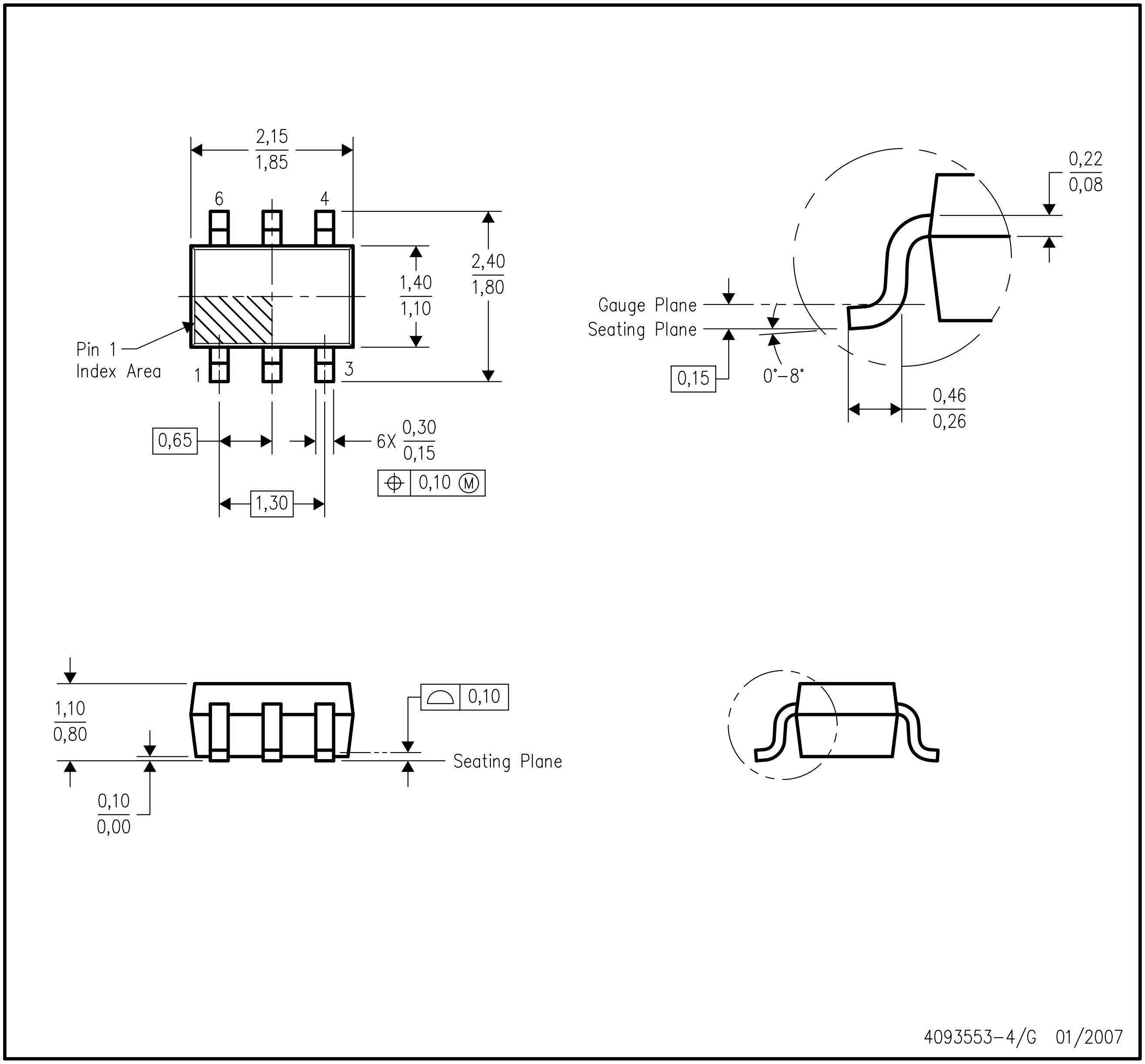
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

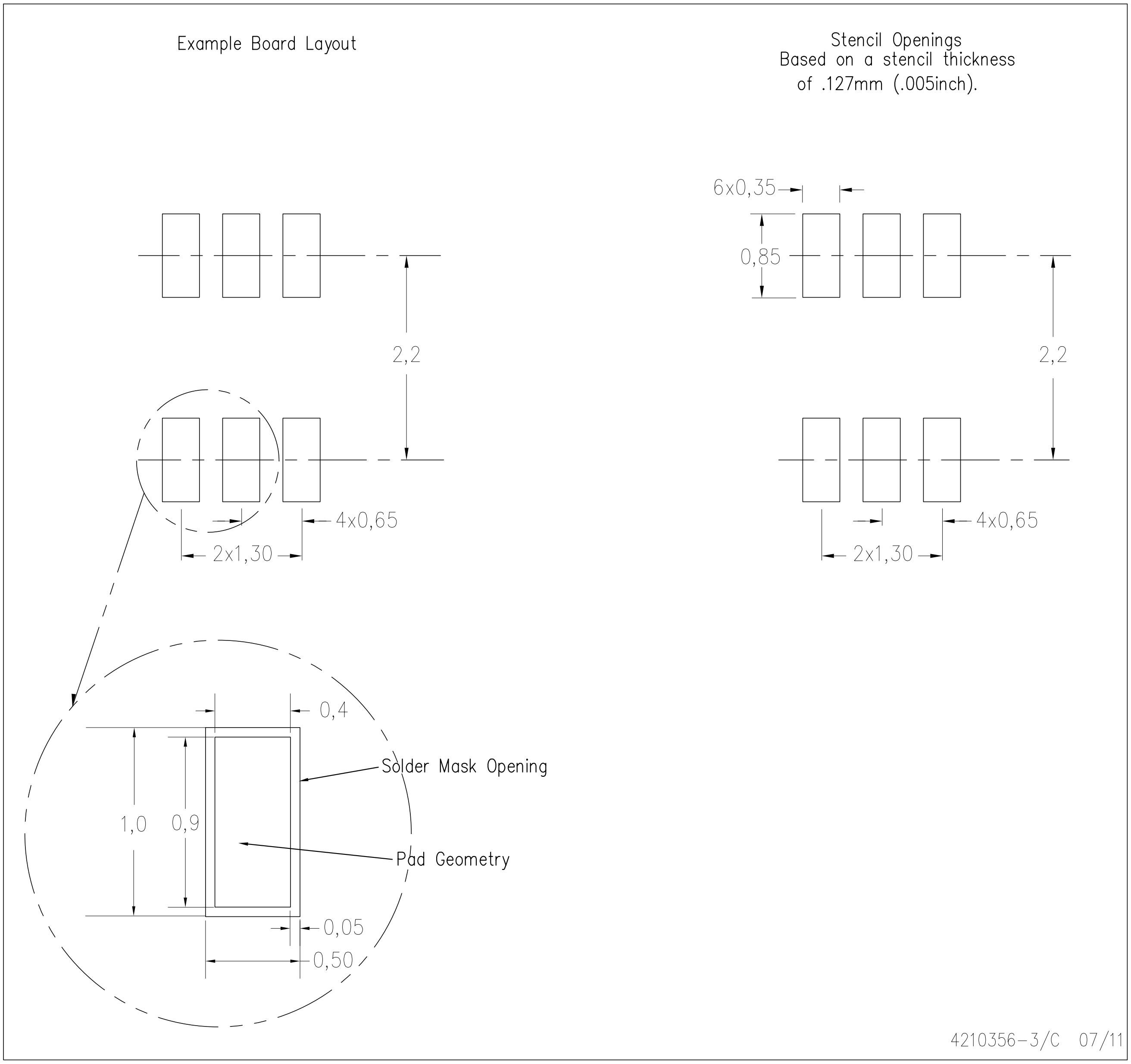
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TMP300BQDCKRQ1	SC70	DCK	6	3000	203.0	203.0	35.0

DCK (R-PDSO-G6) PLASTIC SMALL-OUTLINE PACKAGE



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
D. Falls within JEDEC MO-203 variation AB.

DCK (R–PDSO–G6) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265