TMS320C5545 Fixed-Point Digital Signal Processor

1 Device Overview

1.1 Features

- Core:
  - High-Performance, Low-Power, TMS320C55x Fixed-Point Digital Signal Processor
    - 16.67-, 10-, 8.33-ns Instruction Cycle Time
    - 60-, 100-, 120-MHz Clock Rate
    - One or Two Instructions Executed per Cycle
    - Dual Multiply-and-Accumulate (MAC) Units (up to 200 or 240 Million Multiply-Accumulates per Second [MMACS])
    - Two Arithmetic and Logic Units (ALUs)
    - Three Internal Data and Operand Read Buses and Two Internal Data and Operand Write Buses
    - Software-Compatible With C55x Devices
    - Industrial Temperature Devices Available
  - 320KB of Zero-Wait State On-Chip RAM, Composed of:
    - 64KB of Dual-Access RAM (DARAM), 8 Blocks of 4K × 16-Bit
    - 256KB of Single-Access RAM (SARAM), 32 Blocks of 4K × 16-Bit
  - 128KB of Zero Wait-State On-Chip ROM (4 Blocks of 16K x 16-Bit)
  - Tightly Coupled Fast Fourier transform (FFT) Hardware Accelerator
- Peripheral:
  - Direct Memory Access (DMA) Controller
    - Four DMA With 4 Channels Each (16 Channels Total)
  - Three 32-Bit General-Purpose (GP) Timers
    - One Selectable as a Watchdog or GP
  - Two Embedded Multimedia Card (eMMC) or Secure Digital (SD) Interfaces
  - Universal Asynchronous Receiver/Transmitter (UART)
  - Serial Port Interface (SPI) With Three Chip Selects
  - Master and Slave Inter-Integrated Circuit (I^2C Bus)
  - Four Inter-IC Sound (I2S Bus) for Data Transport
  - Device USB Port With Integrated 2.0 High-Speed PHY That Supports:
    - USB 2.0 Full- and High-Speed Device
  - LCD Bridge With Asynchronous Interface
  - 10-Bit 3-Input Successive Approximation (SAR) Analog-to-Digital Converter (ADC)
  - IEEE 1149.1 (JTAG) Boundary-Scan-Compatible
  - 32 General-Purpose I/O (GPIO) Pins (Multiplexed With Other Device Functions)
    - Configure up to 20 GPIO Pins at the Same Time
- Power:
  - Four Core Isolated Power Supply Domains: Analog, RTC, CPU and Peripherals, and USB
  - Three I/O Isolated Power Supply Domains: RTC I/O, USB PHY, and DV_{DDIO}
  - Three integrated LDOs (DSP_LDO, ANA_LDO, and USB_LDO) to Power the Isolated Domains: DSP Core, Analog, and USB Core, Respectively
  - 1.05-V Core (60 MHz), 1.8-, 2.5-, 2.75-, or 3.3-V I/Os
  - 1.3-V Core (100 or 120 MHz), 1.8-, 2.5-, 2.75-, or 3.3-V I/Os
- Clock:
  - External Clock Source Through CLKIN Pin That Supports 11.2896-, 12.000-, and 12.288-MHz Clock Frequencies
  - Real-Time Clock (RTC) With 32.768-kHz Crystal Input, Separate Clock Domain, and Separate Power Supply
  - Low-Power, Software-Programmable Phase-Locked Loop (PLL) Clock Generator
- Bootloader:
  - On-Chip ROM Bootloader (RBL) to Boot From SPI EEPROM, SPI Serial Flash or I^2C EEPROM eMMC, SD, SDHC, UART, and USB
- Package:
  - 118-Terminal Pb-Free Plastic BGA (Ball Grid Array) (ZQW Suffix)

1.2 Applications

- Wireless Audio Devices (for Example, Headsets, Microphones, Speakerphones)
- Echo Cancellation Headphones
- Portable Medical Devices
- Voice Applications
- Industrial Controls
- Fingerprint Biometrics
- Software-Defined Radio

1.3 Description

These devices are members of TI's C5000™ fixed-point digital signal processor (DSP) product family and are designed for low-power applications.

The fixed-point DSP is based on the TMS320C55x DSP generation CPU processor core. The C55x DSP architecture achieves high performance and low power through increased parallelism and power savings. The CPU supports an internal bus structure composed of one program bus, one 32-bit data read bus, two 16-bit data read buses, two 16-bit data write buses, and additional buses dedicated to peripheral and DMA activity. These buses provide the ability to perform up to four 16-bit data reads and two 16-bit data writes in a single cycle. The device also includes four DMA controllers, each with 4 channels that provide data movement for 16 independent channel contexts without CPU intervention. Each DMA controller can perform one 32-bit data transfer per cycle, both in parallel and independent of the CPU activity.

The C55x CPU provides two multiply-and-accumulate (MAC) units, each capable of 17-bit × 17-bit multiplication and a 32-bit add in a single cycle. A central 40-bit arithmetic and logic unit (ALU) is supported by an additional 16-bit ALU. Used under instruction set control, the ALUs provide the ability to optimize parallel activity and power consumption. These resources are managed in the address unit (AU) and data unit (DU) of the C55x CPU.

The C55x CPU supports a variable byte width instruction set for improved code density. The instruction unit (IU) fetches 32-bit program from internal or external memory and queues instructions for the program unit (PU). The PU decodes the instructions, directs tasks to the AU and DU resources, and manages the fully protected pipeline. Predictive branching avoids pipeline flushes when conditional instructions execute.

The GPIO functions, along with the 10-bit SAR ADC, provide sufficient pins for status, interrupts, and bit I/O for LCD displays, keyboards, and media interfaces. Serial media is supported through two secure digital (SD) peripherals, four Inter-IC Sound (I2S Bus) modules, one serial port interface (SPI) with up to three chip selects, one Inter-Integrated Circuit (I^2C) multimaster and slave interface, and a universal asynchronous receiver/transmitter (UART) interface.

Additional peripherals include: a high-speed universal serial bus (USB 2.0) device mode only, a real-time clock (RTC), three general-purpose (GP) timers with one configurable as a watchdog timer, and an analog phase-locked loop (APLL) clock generator.

In addition, the device includes a tightly coupled FFT hardware accelerator. The tightly coupled FFT hardware accelerator supports 8- to 1024-point (in power of 2) real and complex-valued FFTs.

Furthermore, the device includes the following three integrated LDOs to power different sections of the device:

ANA_LDO provides 1.3 V to the DSP PLL (V_{DDA_PLL}), SAR, and power-management circuits (V_{DDA_ANA}).

DSP_LDO provides 1.3 V or 1.05 V to the DSP core (CV_{DD}), selectable on-the-fly by software as long as operating frequency ranges are observed.

USB_LDO provides 1.3 V to the USB core digital (USB_V_{DD1P3}) and PHY circuits (USB_V_{DDA1P3}).

These devices are supported by the industry's award-winning eXpressDSP™, Code Composer Studio™ Integrated Development Environment (IDE), DSP/BIOS™, Texas Instruments' algorithm standard, and the industry's largest third-party network. Code Composer Studio IDE features code generation tools including a C Compiler and Linker, RTDX™, XDS100, XDS510™, XDS560™ emulation device drivers, and evaluation modules. The devices are also supported by the C55x DSP library, which features more than 50 foundational software kernels (FIR filters, IIR filters, FFTs, and various math functions) and chip support libraries.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE
TMS320C5545A	MicroStar JUNIOR BGA™(118)	7.00 mm × 7.00 mm

(1) For more information, see Section 8, *Mechanical Packaging and Orderable Information*.

1.4 Functional Block Diagram

Figure 1-1 shows the functional block diagram of the devices.

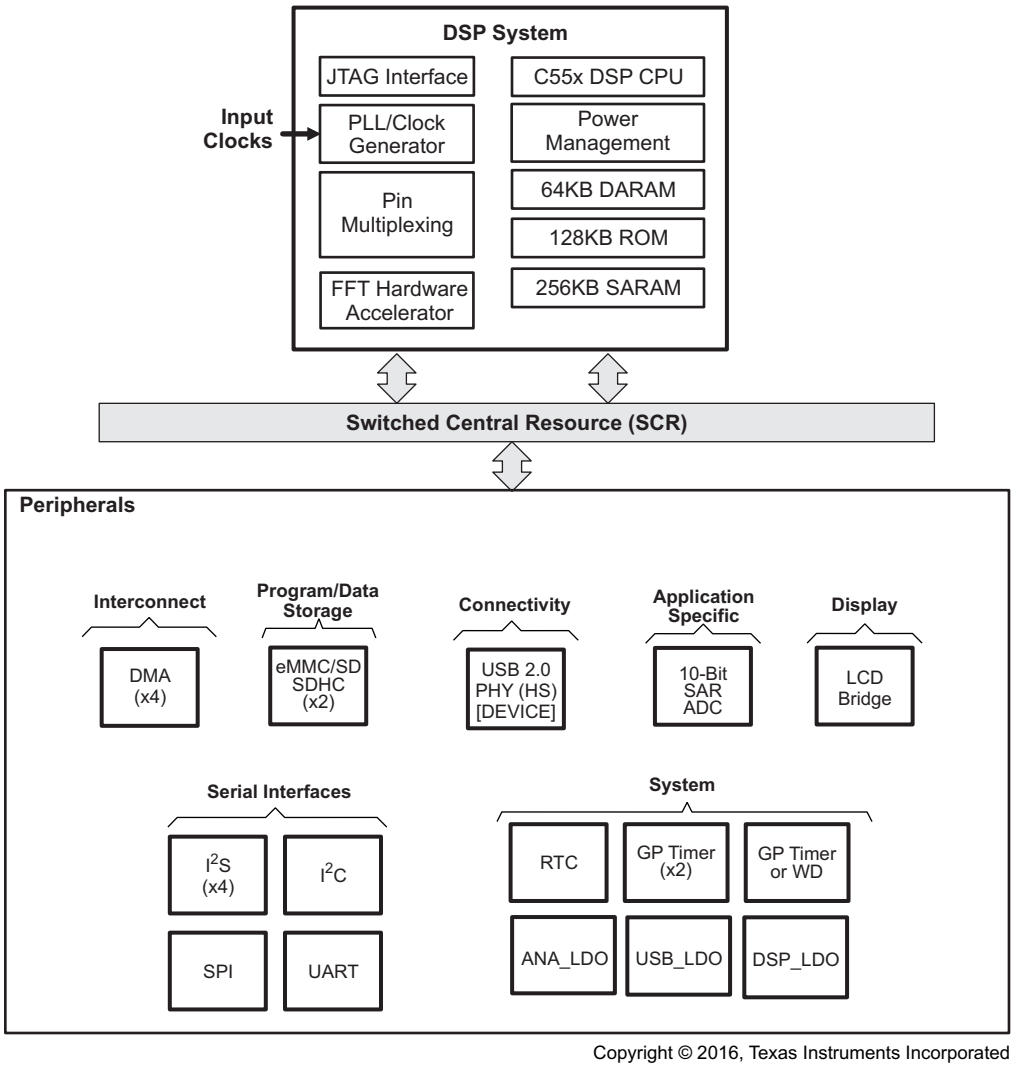

Figure 1-1. Functional Block Diagram

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2 Revision History

Changes from Revision C (February 2016) to Revision D	Page
• Added 120-MHz information that was removed in the previous revision	1
• Updated values in the MIN, TYP, and MAX columns in Section 5.5	37
• Updated/Changed $t_{c(CLKOUT)}$ values in Table 5-9	54
• Updated/Changed footnote 2 in Table 5-21 and Table 5-22	71
• Added Industrial Temperature to Figure 7-1	123
• Added "06" option to DEVICE MAXIMUM OPERATING FREQUENCY in Figure 7-1	123

3 Device Comparison

3.1 Device Characteristics

Table 3-1 lists significant features of each device, including the capacity of on-chip RAM, the peripherals, the CPU frequency, and the package type with pin count. For more detailed information on the actual device part number and maximum device operating frequency, see Section 7.1, *Device and Development-Support Tool Nomenclature*.

Table 3-1. Characteristics of the Processor

HARDWARE FEATURES			TMS320C5545A
Peripherals Not all peripheral pins are available at the same time (for more detail, see Section 6).	DMA		Four DMA controllers each with four channels, for a total of 16 channels
	Timers		Two 32-bit General-Purpose (GP) Timers 1 additional timer configurable as a 32-Bit GP Timer or a watchdog
	UART		1 (with RTS and CTS flow control)
	SPI		1 (with 3 chip selects)
	I^2C		1 (master or slave)
	I2S		4 (2-channel, full-duplex communication)
	USB 2.0 (device only)		High- and full-speed device
	SD		2 SD, 256-byte read and write buffer, maximum 50-MHz clock and signaling for DMA transfers
	LCD bridge		1 (8-bit or 16-bit asynchronous parallel bus)
	ADC (Successive Approximation [SAR])		1 (10-bit, 3-input, 16-µs conversion time)
	RTC		1 (crystal input, separate clock domain, and power supply)
	FFT hardware accelerator		1 (Supports 8- to 1024-point, 16-bit real and complex FFT)
	GPIO port		32 pins and 3 special-purpose outputs for use with SAR Configure up to 20 pins simultaneously
On-Chip Memory	Size (bytes)		320KB of RAM, 128KB of ROM
	Organization		• 64KB of on-chip dual-access RAM (DARAM) • 256KB of on-chip single-access RAM (SARAM) • 128 KB of on-chip single-access ROM (SAROM)
JTAG BSDL_ID	JTAGID register (Value is: 0x1B8F E02F)		See Figure 5-38.
CPU Frequency	MHz	1.05-V Core	60 MHz
		1.3-V Core	100 or 120 MHz
Cycle Time	ns	1.05-V Core	16.67 ns
		1.3-V Core	10 ns, 8.33 ns
Voltage	Core (V)		1.05 V to 60 MHz
			1.3 V to 100 or 120 MHz
	I/O (V)		1.8 V, 2.5 V, 2.75 V, 3.3 V
LDOs	DSP_LDO		1.3 V or 1.05 V, 250 mA maximum current for DSP CPU (CV_{DD})
	ANA_LDO		1.3 V, 4 mA maximum current to supply power to PLL (V_{DDA_PLL}), SAR, and power-management circuits (V_{DDA_ANA})
	USB_LDO		1.3 V, 25 mA maximum current to supply power to USB core digital (USB_V_{DD1P3}) and PHY circuits (USB_V_{DDA1P3})
PLL Options	Software Programmable Multiplier		x4 to x4099 multiplier
BGA Package	7 mm × 7 mm		118-pin BGA (ZQW)

Table 3-1. Characteristics of the Processor (continued)

HARDWARE FEATURES		TMS320C5545A
Product Status(1)	Product Preview (PP), Advance Information (AI), or Production Data (PD)	PD

(1) PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of the Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

3.2 Related Products

For information about other devices in this family of products or related products, see the following links.

Digital Signal Processor DSPs bring computing performance, real-time processing, and power efficiency to diverse applications ranging from sensors to servers. Our product range spans high-performance real-time needs, to power-efficient processors with industry-leading lowest active power needs. Choose one of our scalable solutions below.

C5000™ Ultra Low Power DSP The C5000 ultra-low-power DSP platform includes a broad portfolio of the industry's lowest power 16-bit DSPs with performance up to 300 MHz (600 MIPS). Ideal for portable devices in audio, voice and vision, and other applications requiring analytics with ultra-low power.

4 Terminal Configuration and Functions

4.1 Pin Diagram

Extensive pin multiplexing is used to accommodate the largest number of peripheral functions in the smallest possible package. Pin multiplexing is controlled using software-programmable register settings. For more information on pin muxing, see Section 6.7, *Multiplexed Pin Configurations*.

Figure 4-1 shows the bottom view of the package pin assignments.

	1	2	3	4	5	6	7	8	9	10	11	12	
M	LCD_D[13]/ UART_CTS/ GP[29]/ I2S3_FS	DV_{DDIO}	SD0_D2/ GP[4]	SD1_D2/ GP[10]	RSV17	USB_DM	USB_V_{DDPLL}	USB_V_{DD1P3}	USB_V_{SSOSC}	USB_LDOO	DSP_LDOO	$\overline{DSP\_LDO\_EN}$	M
L	LCD_D[14]/ UART_RXD/ GP[30]/ I2S3_RX	LCD_D[15]/ UART_TXD/ GP[31]/ I2S3_DX	SD1_D0/ I2S1_DX/ GP[8]	SD1_CMD/ I2S1_FS/ GP[7]	USB_V_{DD1P3}	USB_DP	USB_V_{DDA3P3}	USB_V_{SSPLL}	USB_MXI	LDOI	LDOI	RSV0	L
K	LCD_D[9]/ I2S2_FS/ GP[19]/ SPI_CS0	LCD_D[11]/ I2S2_DX/ GP[27]/ SPI_TX		V_{SS}	USB_VBUS	USB_V_{DDA1P3}	USB_R1	USB_V_{DDOSC}	USB_MXO		RSV3	V_{SSA_ANA}	K
J	LCD_D[7]/ GP[17]	SD0_CMD/ I2S0_FS/ GP[1]	LCD_D[12]/ UART_RTS/ GP[28]/ I2S3_CLK						CV_{DD}	RSV5	BG_CAP	GPAIN3	J
H	LCD_D[8]/ I2S2_CLK/ GP[18]/ SPI_CLK	DV_{DDIO}	SD1_D1/ I2S1_RX/ GP[9]		SD1_CLK/ I2S1_CLK/ GP[6]	USB_V_{SS1P3}	USB_V_{SSA3P3}	USB_V_{SSREF}		RSV4	ANA_LDOO	V_{SSA_ANA}	H
G	LCD_D[5]/ GP[15]	SD0_D1/ I2S0_RX/ GP[3]	SD0_D3/ GP[5]		SD1_D3/ GP[11]	V_{SS}	CV_{DD}	V_{SS}		LDOI	V_{DDA_ANA}	V_{SSRTC}	G
F	LCD_D[4]/ GP[14]	$\overline{TRST}$	V_{SS}		LCD_D[10]/ I2S2_RX/ GP[20]/ SPI_RX		V_{SS}	GPAIN1		GPAIN2	RTC_XI	DV_{DDRTC}	F
E	LCD_D[3]/ GP[13]	LCD_D[2]/ GP[12]	LCD_D[6]/ GP[16]		SD0_CLK/ I2S0_CLK/ GP[0]	CV_{DD}		V_{SSA_PLL}		V_{DDA_PLL}	RTC_XO	CLKIN	E
D	TDO	DV_{DDIO}	TMS		SD0_D0/ I2S0_DX/ GP[2]					CV_{DDRTC}	SDA	CLK_SEL	D
C	TCK	LCD_D[1]/ SPI_TX		V_{SS}		CV_{DD}	V_{SS}		V_{SS}		$\overline{INT1}$	CLKOUT	C
B	EMU1	LCD_RW_ WRB/ SPI_CS2	EMU0	TDI	CV_{DD}	V_{SS}	V_{SS}	CV_{DD}	V_{SS}	DV_{DDIO}	SCL	$\overline{INT0}$	B
A	LCD_EN_ RDB/ SPI_CLK	LCD_CS0_E0/ SPI_CS0	LCD_RS/ SPI_CS3	LCD_D[0]/ SPI_RX	V_{SS}	V_{SS}	V_{SS}	V_{SS}	CV_{DD}	V_{SS}	$\overline{RESET}$	V_{SS}	A
	1	2	3	4	5	6	7	8	9	10	11	12	

Figure 4-1. Pin Diagram (Bottom View)

4.2 Terminal Functions

For proper device operation, external pullup and pulldown resistors may be required on some pins. Section 6.8.1, *Pullup and Pulldown Resistors,* discusses situations where external pullup and pulldown resistors are required.

4.2.1 Oscillator and PLL Terminal Functions

Table 4-1 identifies the external signal names, the associated pin (ball) numbers along with the mechanical package designator, the pin type, whether the pin has any internal pullup or pulldown resistors or bus-holders, and a functional pin description. For more detailed information on device configuration, peripheral selection, multiplexed and shared pins, and debugging considerations, see Section 6, *Device Configuration*.

Table 4-1. Oscillator and PLL Terminal Functions

SIGNAL		TYPE (1) (2)	OTHER (3) (4)	DESCRIPTION
NAME	NO.			
CLKOUT	C12	O/Z	– DV_{DDIO} BH	DSP clock output signal. For debug purposes only, the CLKOUT pin can be used to tap different clocks within the system clock generator. The SRC bits in the CLKOUT Control Source Register (CCSSR) can be used to specify the source of the CLKOUT pin. Additionally, the slew rate of the CLKOUT pin can be controlled by the Output Slew Rate Control Register (OSRCR) [1C16h]. The CLKOUT pin is enabled and disabled through the CLKOFF bit in the CPU ST3_55 register. When disabled, the CLKOUT pin is placed in high-impedance (Hi-Z). At reset the CLKOUT pin is enabled until the beginning of the boot sequence, when the on-chip bootloader sets CLKOFF = 1 and the CLKOUT pin is disabled (Hi-Z). For more information on the ST3_55 register, see the *TMS320C55x DSP v3.x CPU Reference Guide*. **Note:** This pin may consume static power if configured as Hi-Z and not externally pulled low or high. Prevent current drain by externally terminating the pin.
CLKIN	E12	I	– DV_{DDIO} BH	Input clock. This signal is used to input an external clock when the 32-kHz on-chip oscillator is not used as the DSP clock (pin CLK_SEL = 1). For boot purposes, the CLKIN frequency is assumed to be either 11.2896, 12, or 12.288 MHz. The CLK_SEL pin (D12) selects between the 32-kHz crystal clock or CLKIN. When the CLK_SEL pin is low, this pin must be tied to ground (V_{SS}). When CLK_SEL is high, this pin must be driven by an external clock source. If CLK_SEL is high, this pin is used as the reference clock for the clock generator. During bootup, the bootloader bypasses the PLL and assumes the CLKIN frequency is one of the following frequencies: 11.2896, 12, or 12.288 MHz. In addition, the bootloader sets the SPI clock rate at 500 kHz and the I2C clock rate at 400 kHz .
CLK_SEL	D12	I	– DV_{DDIO} BH	Clock input select. This pin selects between the 32-kHz crystal clock or CLKIN. 0 = 32-kHz on-chip oscillator drives the RTC timer and the system clock generator while CLKIN is ignored. 1 = CLKIN drives the system clock generator and the 32-kHz on-chip oscillator drives only the RTC timer. This pin is not allowed to change during device operation; it must be tied high or low at the board.
V_{DDA_PLL}	E10	PWR	See Section 5.3, *Recommended Operating Conditions*	1.3-V analog PLL power supply for the system clock generator (PLLOUT ≤ 120 MHz). This signal can be powered from the ANA_LDOO pin.

(1) I = Input, O = Output, Z = High impedance, S = Supply voltage, GND = Ground, A = Analog signal, BH = Bus-holder
(2) Input pins of type I, I/O, and I/O/Z are required to be driven at all times. To achieve the lowest power, these pins must not be allowed to float. When configured as input or high-impedance state, and not driven to a known state, they may cause an excessive I/O-supply current. If this is the case, enable IPD and IPU, if applicable, or externally terminate the pins.
(3) IPD = Internal pulldown, IPU = Internal pullup. For more detailed information on pullup and pulldown resistors and situations where external pullup and pulldown resistors are required, see Section 6.8.1, *Pullup and Pulldown Resistors*.
(4) Specifies the operating I/O supply voltage for each signal

Table 4-1. Oscillator and PLL Terminal Functions (continued)

SIGNAL		TYPE (1) (2)	OTHER (3) (4)	DESCRIPTION
NAME	NO.			
V_{SSA_PLL}	E8	GND	See Section 5.3, *Recommended Operating Conditions*	Analog PLL ground for the system clock generator

4.2.2 RTC Terminal Functions

Table 4-2 identifies the external signal names, the associated pin (ball) numbers along with the mechanical package designator, the pin type, whether the pin has any internal pullup or pulldown resistors or bus-holders, and a functional pin description. For more detailed information on device configuration, peripheral selection, multiplexed and shared pins, and debugging considerations, see Section 6, *Device Configuration*.

Table 4-2. Real-Time Clock Terminal Functions

SIGNAL		TYPE (1) (2)	OTHER (3) (4)	DESCRIPTION
NAME	NO.			
RTC_XO	E11	I/O/Z	– CV_{DDRTC} DV_{DDRTC}	Real-time clock oscillator output. This pin operates at the RTC core voltage, CV_{DDRTC}, and supports a 32.768-kHz crystal. If the RTC oscillator is not used, it can be disabled by connecting RTC_XI to CV_{DDRTC} and RTC_XO to ground (V_{SS}). A voltage must still be applied to CV_{DDRTC} by an external power source (see Section 5.3, *Recommended Operating Conditions*). None of the on-chip LDOs can be used to power CV_{DDRTC}. **Note:** When RTC oscillator is disabled, the RTC registers (I/O address range 1900h to 197Fh) are not accessible.
RTC_XI	F11	I	– CV_{DDRTC} DV_{DDRTC}	Real-time clock oscillator input. If the RTC oscillator is not used, it can be disabled by connecting RTC_XI to CV_{DDRTC} and RTC_XO to ground (V_{SS}). A voltage must still be applied to CV_{DDRTC} by an external power source (see Section 5.3, *Recommended Operating Conditions*). None of the on-chip LDOs can be used to power CV_{DDRTC}. **Note:** When RTC oscillator is disabled, the RTC registers (I/O address range 1900h to 197Fh) are not accessible.

(1) I = Input, O = Output, Z = High impedance, S = Supply voltage, GND = Ground, A = Analog signal, BH = Bus-holder
(2) Input pins of type I, I/O, and I/O/Z are required to be driven at all times. To achieve the lowest power, these pins must not be allowed to float. When configured as input or high-impedance state, and not driven to a known state, they may cause an excessive I/O-supply current. If this is the case, enable IPD and IPU, if applicable, or externally terminate the pins.
(3) IPD = Internal pulldown, IPU = Internal pullup. For more detailed information on pullup and pulldown resistors and situations where external pullup and pulldown resistors are required, see Section 6.8.1, *Pullup and Pulldown Resistors*.
(4) Specifies the operating I/O supply voltage for each signal

4.2.3 RESET, Interrupts, and JTAG Terminal Functions

Table 4-3 identifies the external signal names, the associated pin (ball) numbers along with the mechanical package designator, the pin type, whether the pin has any internal pullup or pulldown resistors or bus-holders, and a functional pin description. For more detailed information on device configuration, peripheral selection, multiplexed and shared pins, and debugging considerations, see Section 6, *Device Configuration*.

Table 4-3. RESET, Interrupts, and JTAG Terminal Functions

SIGNAL		TYPE (1) (2)	OTHER (3) (4)	DESCRIPTION
NAME	NO.			
RESET				
$\overline{\text{RESET}}$	A11	I	IPU DV_{DDIO} BH	Device reset. $\overline{\text{RESET}}$ causes the DSP to terminate execution and loads the program counter with the contents of the reset vector. When $\overline{\text{RESET}}$ is brought to a high level, the reset vector in ROM at FFFF00h forces the program execution to branch to the location of the on-chip ROM bootloader. $\overline{\text{RESET}}$ affects the various registers and status bits. The IPU resistor on this pin can be enabled or disabled through the PDINHIBR2 register but will be forced ON when $\overline{\text{RESET}}$ is asserted.
JTAG				
For more detailed information on emulation header design guidelines, see the *XDS560 Emulator Technical Reference*.				
TMS	D3	I	IPU DV_{DDIO} BH	IEEE standard 1149.1 test mode select. This serial control input is clocked into the TAP controller on the rising edge of TCK. If the emulation header is located more than 6 inches from the device, TMS must be buffered. In this case, the input buffer for TMS needs a pullup resistor connected to DV_{DDIO} to hold the signal at a known value when the emulator is not connected. A resistor value of 4.7 kΩ or greater is suggested. For board design guidelines related to the emulation header, see the *XDS560 Emulator Technical Reference*. The IPU resistor on this pin can be enabled or disabled through the PDINHIBR2 register.
TDO	D1	O/Z	_ DV_{DDIO} BH	IEEE standard 1149.1 test data output. The contents of the selected register (instruction or data) are shifted out of TDO on the falling edge of TCK. TDO is in the high-impedance (Hi-Z) state except when the scanning of data is in progress. For board design guidelines related to the emulation header, see the *XDS560 Emulator Technical Reference*. If the emulation header is located more than 6 inches from the device, TDO must be buffered. **Note:** This pin may consume static power if configured as Hi-Z and not externally pulled low or high. Prevent current drain by externally terminating the pin. TDO pin will be in Hi-Z whenever not doing emulation and boundary scan, so an external pullup is highly recommended.
TDI	B4	I	IPU DV_{DDIO} BH	IEEE standard 1149.1 test data input. TDI is clocked into the selected register (instruction or data) on a rising edge of TCK. If the emulation header is located more than 6 inches from the device, TDI must be buffered. In this case, the input buffer for TDI needs a pullup resistor connected to DV_{DDIO} to hold this signal at a known value when the emulator is not connected. A resistor value of 4.7 kΩ or greater is suggested. The IPU resistor on this pin can be enabled or disabled through the PDINHIBR2 register.

(1) I = Input, O = Output, Z = High impedance, S = Supply voltage, GND = Ground, A = Analog signal, BH = Bus-holder
(2) Input pins of type I, I/O, and I/O/Z are required to be driven at all times. To achieve the lowest power, these pins must not be allowed to float. When configured as input or high-impedance state, and not driven to a known state, they may cause an excessive I/O-supply current. If this is the case, enable IPD and IPU, if applicable, or externally terminate the pins.
(3) IPD = Internal pulldown, IPU = Internal pullup. For more detailed information on pullup and pulldown resistors and situations where external pullup and pulldown resistors are required, see Section 6.8.1, *Pullup and Pulldown Resistors*.
(4) Specifies the operating I/O supply voltage for each signal

Table 4-3. RESET, Interrupts, and JTAG Terminal Functions (continued)

SIGNAL NAME	SIGNAL NO.	TYPE (1) (2)	OTHER (3) (4)	DESCRIPTION
TCK	C1	I	IPU DV_{DDIO} BH	IEEE standard 1149.1 test clock. TCK is normally a free-running clock signal with a 50% duty cycle. The changes on input signals TMS and TDI are clocked into the TAP controller, instruction register, or selected test data register on the rising edge of TCK. Changes at the TAP output signal (TDO) occur on the falling edge of TCK. If the emulation header is located more than 6 inches from the device, TCK must be buffered. For board design guidelines related to the emulation header, see the *XDS560 Emulator Technical Reference*. The IPU resistor on this pin can be enabled or disabled through the PDINHIBR2 register.
$\overline{TRST}$	F2	I	IPD DV_{DDIO} BH	IEEE standard 1149.1 reset signal for test and emulation logic. $\overline{TRST}$, when high, allows the IEEE standard 1149.1 scan and emulation logic to take control of the operations of the device. If $\overline{TRST}$ is not connected or is driven low, the device operates in its functional mode, and the IEEE standard 1149.1 signals are ignored. The device will not operate properly if this reset pin is never asserted low. For board design guidelines related to the emulation header, see the *XDS560 Emulator Technical Reference*. TI recommends using an external pulldown resistor in addition to the IPD, especially if there is a long trace to an emulation header.
EMU1	B1	I/O/Z	IPU DV_{DDIO} BH	Emulator 1 pin. EMU1 is used as an interrupt to or from the emulator system and is defined as input/output by way of the emulation logic. An external pullup to DV_{DDIO} is required to provide a signal rise time of less than 10 μsec. A 4.7-kΩ resistor is suggested for most applications. For board design guidelines related to the emulation header, see the *XDS560 Emulator Technical Reference*. The IPU resistor on this pin can be enabled or disabled through the PDINHIBR2 register.
EMU0	B3	I/O/Z	IPU DV_{DDIO} BH	Emulator 0 pin. When $\overline{TRST}$ is driven low and then high, the state of the EMU0 pin is latched and used to connect the JTAG pins (TCK, TMS, TDI, TDO) to either the IEEE1149.1 Boundary-Scan TAP (when the latched value of EMU0 = 0) or to the DSP Emulation TAP (when the latched value of EMU0 = 1). Once $\overline{TRST}$ is high, EMU0 is used as an interrupt to or from the emulator system and is defined as input/output by way of the emulation logic. An external pullup to DV_{DDIO} is required to provide a signal rise time of less than 10 μsec. A 4.7-kΩ resistor is suggested for most applications. For board design guidelines related to the emulation header, see the *XDS560 Emulator Technical Reference*. The IPU resistor on this pin can be enabled or disabled through the PDINHIBR2 register.
EXTERNAL INTERRUPTS				
$\overline{INT1}$	C11	I	IPU DV_{DDIO} BH	External interrupt inputs ($\overline{INT1}$ and $\overline{INT0}$). These pins are maskable through their specific Interrupt Mask Register (IMR1, IMR0) and the interrupt mode bit. The pins can be polled and reset by their specific Interrupt Flag Register (IFR1, IFR0). The IPU resistor on these pins can be enabled or disabled through the PDINHIBR2 register.
$\overline{INT0}$	B12	I	IPU DV_{DDIO} BH	

4.2.4 I2C Terminal Functions

Table 4-4 identifies the external signal names, the associated pin (ball) numbers along with the mechanical package designator, the pin type, whether the pin has any internal pullup or pulldown resistors or bus-holders, and a functional pin description. For more detailed information on device configuration, peripheral selection, multiplexed and shared pins, and debugging considerations, see Section 6, *Device Configuration*.

Table 4-4. Inter-Integrated Circuit (I2C) Terminal Functions

SIGNAL		TYPE (1) (2)	OTHER (3) (4)	DESCRIPTION
NAME	NO.			
I2C				
SCL	B11	I/O/Z	DV_{DDIO} BH	This pin is the I2C clock output. Per the I2C standard, an external pullup is required on this pin.
SDA	D11	I/O/Z	DV_{DDIO} BH	This pin is the I2C bidirectional data signal. Per the I2C standard, an external pullup is required on this pin.

(1) I = Input, O = Output, Z = High impedance, S = Supply voltage, GND = Ground, A = Analog signal, BH = Bus-holder
(2) Input pins of type I, I/O, and I/O/Z are required to be driven at all times. To achieve the lowest power, these pins must not be allowed to float. When configured as input or high-impedance state, and not driven to a known state, they may cause an excessive IO-supply current. If this is the case, enable IPD and IPU, if applicable, or externally terminate the pins.
(3) IPD = Internal pulldown, IPU = Internal pullup. For more detailed information on pullup and pulldown resistors and situations where external pullup and pulldown resistors are required, see Section 6.8.1, *Pullup and Pulldown Resistors*.
(4) Specifies the operating I/O supply voltage for each signal

4.2.5 I2S0 to I2S3 Terminal Functions

Table 4-5 identifies the external signal names, the associated pin (ball) numbers along with the mechanical package designator, the pin type, whether the pin has any internal pullup or pulldown resistors or bus-holders, and a functional pin description. For more detailed information on device configuration, peripheral selection, multiplexed and shared pins, and debugging considerations, see Section 6, *Device Configuration*.

Table 4-5. Inter-IC Sound (I2S0 to I2S3) Terminal Functions

SIGNAL		TYPE (1) (2)	OTHER (3) (4)	DESCRIPTION
NAME	NO.			
INTERFACE 0 (I2S0)				
SD0_D0/ I2S0_DX/ GP[2]	D5	I/O/Z	IPD DV_{DDIO} BH	This pin is multiplexed between SD0, I2S0, and GPIO. For I2S, it is I2S0 transmit data output I2S0_DX. Mux control through the SP0MODE bits in the EBSR. The IPD resistor on this pin can be enabled or disabled through the PDINHIBR1 register.
SD0_CLK/ I2S0_CLK/ GP[0]	E5	I/O/Z	IPD DV_{DDIO} BH	This pin is multiplexed between SD0, I2S0, and GPIO. For I2S, it is I2S0 clock input/output I2S0_CLK. Mux control through the SP0MODE bits in the EBSR. The IPD resistor on this pin can be enabled or disabled through the PDINHIBR1 register.
SD0_D1/ I2S0_RX/ GP[3]	G2	I/O/Z	IPD DV_{DDIO} BH	This pin is multiplexed between SD0, I2S0, and GPIO. For I2S, it is I2S0 receive data input I2S0_RX. Mux control through the SP0MODE bits in the EBSR. The IPD resistor on this pin can be enabled or disabled through the PDINHIBR1 register.
SD0_CMD/ I2S0_FS/ GP[1]	J2	I/O/Z	IPD DV_{DDIO} BH	This pin is multiplexed between SD0, I2S0, and GPIO. For I2S, it is I2S0 frame synchronization input/output I2S0_FS. Mux control through the SP0MODE bits in the EBSR. The IPD resistor on this pin can be enabled or disabled through the PDINHIBR1 register.
INTERFACE 1 (I2S1)				
SD1_D0/ I2S1_DX/ GP[8]	L3	I/O/Z	IPD DV_{DDIO} BH	This pin is multiplexed between SD1, I2S1, and GPIO. For I2S, it is I2S1 transmit data output I2S1_DX. Mux control through the SP1MODE bits in the EBSR. The IPD resistor on this pin can be enabled or disabled through the PDINHIBR1 register.
SD1_CLK/ I2S1_CLK/ GP[6]	H5	I/O/Z	IPD DV_{DDIO} BH	This pin is multiplexed between SD1, I2S1, and GPIO. For I2S, it is I2S1 clock input/output I2S1_CLK. Mux control through the SP1MODE bits in the EBSR. The IPD resistor on this pin can be enabled or disabled through the PDINHIBR1 register.
SD1_D1/ I2S1_RX/ GP[9]	H3	I/O/Z	IPD DV_{DDIO} BH	This pin is multiplexed between SD1, I2S1, and GPIO. For I2S, it is I2S1 receive data input I2S1_RX. Mux control through the SP1MODE bits in the EBSR. The IPD resistor on this pin can be enabled or disabled through the PDINHIBR1 register.
SD1_CMD/ I2S1_FS/ GP[7]	L4	I/O/Z	IPD DV_{DDIO} BH	This pin is multiplexed between SD1, I2S2, and GPIO. For I2S, it is I2S1 frame synchronization input/output I2S1_FS. Mux control through the SP1MODE bits in the EBSR. The IPD resistor on this pin can be enabled or disabled through the PDINHIBR1 register.

(1) I = Input, O = Output, Z = High impedance, S = Supply voltage, GND = Ground, A = Analog signal, BH = Bus-holder
(2) Input pins of type I, I/O, and I/O/Z are required to be driven at all times. To achieve the lowest power, these pins must not be allowed to float. When configured as input or high-impedance state, and not driven to a known state, they may cause an excessive I/O-supply current. If this is the case, enable IPD and IPU, if applicable, or externally terminate the pins.
(3) IPD = Internal pulldown, IPU = Internal pullup. For more detailed information on pullup and pulldown resistors and situations where external pullup and pulldown resistors are required, see Section 6.8.1, *Pullup and Pulldown Resistors*.
(4) Specifies the operating I/O supply voltage for each signal

Table 4-5. Inter-IC Sound (I2S0 to I2S3) Terminal Functions (continued)

SIGNAL NAME	SIGNAL NO.	TYPE (1) (2)	OTHER (3) (4)	DESCRIPTION
INTERFACE 2 (I2S2)				
LCD_D[11]/ I2S2_DX/ GP[27]/ SPI_TX	K2	I/O/Z	IPD DV_{DDIO} BH	This pin is multiplexed between LCD Bridge, I2S2, GPIO, and SPI. For I2S, it is I2S2 transmit data output I2S2_DX. Mux control through the PPMODE bits in the EBSR. The IPD resistor on this pin can be enabled or disabled through the PDINHIBR3 register.
LCD_D[8]/ I2S2_CLK/ GP[18]/ SPI_CLK	H1	I/O/Z	IPD DV_{DDIO} BH	This pin is multiplexed between LCD Bridge, I2S2, GPIO, and SPI. For I2S, it is I2S2 clock input/output I2S2_CLK. Mux control through the PPMODE bits in the EBSR. The IPD resistor on this pin can be enabled or disabled through the PDINHIBR3 register.
LCD_D[10]/ I2S2_RX/ GP[20]/ SPI_RX	F5	I/O/Z	IPD DV_{DDIO} BH	This pin is multiplexed between LCD Bridge, I2S2, GPIO, and SPI. For I2S, it is I2S2 receive data input I2S2_RX. Mux control through the PPMODE bits in the EBSR. The IPD resistor on this pin can be enabled or disabled through the PDINHIBR3 register.
LCD_D[9]/ I2S2_FS/ GP[19]/ SPI_CS0	K1	I/O/Z	IPD DV_{DDIO} BH	This pin is multiplexed between LCD Bridge, I2S2 and GPIO. For I2S, it is I2S2 frame synchronization input/output I2S2_FS. Mux control through the PPMODE bits in the EBSR. The IPD resistor on this pin can be enabled or disabled through the PDINHIBR3 register.
INTERFACE 3 (I2S3)				
LCD_D[15]/ UART_TXD/ GP[31]/ I2S3_DX	L2	I/O/Z	IPD DV_{DDIO} BH	This pin is multiplexed between LCD Bridge, UART, GPIO, and I2S3. For I2S, it is I2S3 transmit data output I2S3_DX. Mux control through the PPMODE bits in the EBSR. The IPD resistor on this pin can be enabled or disabled through the PDINHIBR3 register.
LCD_D[12]/ UART_RTS/ GP[28]/ I2S3_CLK	J3	I/O/Z	IPD DV_{DDIO} BH	This pin is multiplexed between LCD Bridge, UART, GPIO, and I2S3. For I2S, it is I2S3 clock input/output I2S3_CLK. Mux control through the PPMODE bits in the EBSR. The IPD resistor on this pin can be enabled or disabled through the PDINHIBR3 register.
LCD_D[14]/ UART_RXD/ GP[30]/ I2S3_RX	L1	I/O/Z	IPD DV_{DDIO} BH	This pin is multiplexed between LCD Bridge, UART, GPIO, and I2S3. For I2S, it is I2S3 receive data input I2S3_RX. Mux control through the PPMODE bits in the EBSR. The IPD resistor on this pin can be enabled or disabled through the PDINHIBR3 register.
LCD_D[13]/ UART_CTS/ GP[29]/ I2S3_FS	M1	I/O/Z	IPD DV_{DDIO} BH	This pin is multiplexed between LCD Bridge, UART, GPIO, and I2S3. For I2S, it is I2S3 frame synchronization input/output I2S3_FS. Mux control through the PPMODE bits in the EBSR. The IPD resistor on this pin can be enabled or disabled through the PDINHIBR3 register.

4.2.6 SPI Terminal Functions

Table 4-6 identifies the external signal names, the associated pin (ball) numbers along with the mechanical package designator, the pin type, whether the pin has any internal pullup or pulldown resistors or bus-holders, and a functional pin description. For more detailed information on device configuration, peripheral selection, multiplexed and shared pins, and debugging considerations, see Section 6, *Device Configuration*.

Table 4-6. Serial Peripheral Interface (SPI) Terminal Functions

SIGNAL		TYPE (1) (2)	OTHER (3) (4)	DESCRIPTION
NAME	NO.			
SERIAL PORT INTERFACE (SPI)				
LCD_CS0_E0/ SPI_CS0	A2	I/O/Z	DV_{DDIO} BH	This pin is multiplexed between LCD bridge and SPI. Mux control through the PPMODE bits in the EBSR. For SPI, this pin is SPI chip select SPI_CS0.
LCD_D[9]/ I2S2_FS/ GP[19]/ SPI_CS0	K1	I/O/Z	IPD DV_{DDIO} BH	This pin is multiplexed between LCD bridge, I2S2, GPIO, and SPI. Mux control through the PPMODE bits in the EBSR. For SPI, this pin is SPI chip select SPI_CS0. The IPD resistor on this pin can be enabled or disabled through the PDINHIBR3 register.
LCD_RW_WRB/ SPI_CS2	B2	I/O/Z	DV_{DDIO} BH	This pin is multiplexed between LCD bridge and SPI. Mux control through the PPMODE bits in the EBSR. For SPI, this pin is SPI chip select SPI_CS2.
LCD_RS/ SPI_CS3	A3	I/O/Z	DV_{DDIO} BH	This pin is multiplexed between LCD bridge and SPI. Mux control through the PPMODE bits in the EBSR. For SPI, this pin is SPI chip select SPI_CS3.
LCD_EN_RDB/ SPI_CLK	A1	O/Z	DV_{DDIO} BH	This pin is multiplexed between LCD bridge and SPI. Mux control through the PPMODE bits in the EBSR. For SPI, this pin is clock output SPI_CLK. **Note:** This pin may consume static power if configured as Hi-Z and not externally pulled low or high. Prevent current drain by externally terminating the pin.
LCD_D[8]/ I2S2_CLK/ GP[18]/ SPI_CLK	H1	I/O/Z	IPD DV_{DDIO} BH	This pin is multiplexed between LCD bridge, I2S2, GPIO, and SPI. Mux control through the PPMODE bits in the EBSR. For SPI, this pin is clock output SPI_CLK. The IPD resistor on this pin can be enabled or disabled through the PDINHIBR3 register.
LCD_D[1]/ SPI_TX	C2	I/O/Z	DV_{DDIO} BH	This pin is multiplexed between LCD bridge and SPI. Mux control through the PPMODE bits in the EBSR. For SPI, this pin is SPI transmit data output.
LCD_D[11]/ I2S2_DX/ GP[27]/ SPI_TX	K2	I/O/Z	IPD DV_{DDIO} BH	This pin is multiplexed between LCD bridge, I2S2, GPIO, and SPI. Mux control through the PPMODE bits in the EBSR. For SPI, this pin is SPI transmit data output. The IPD resistor on this pin can be enabled or disabled through the PDINHIBR3 register.

(1) I = Input, O = Output, Z = High impedance, S = Supply voltage, GND = Ground, A = Analog signal, BH = Bus-holder
(2) Input pins of type I, I/O, and I/O/Z are required to be driven at all times. To achieve the lowest power, these pins must not be allowed to float. When configured as input or high-impedance state, and not driven to a known state, they may cause an excessive I/O-supply current. If this is the case, enable IPD and IPU, if applicable, or externally terminate the pins.
(3) IPD = Internal pulldown, IPU = Internal pullup. For more detailed information on pullup and pulldown resistors and situations where external pullup and pulldown resistors are required, see Section 6.8.1, *Pullup and Pulldown Resistors*.
(4) Specifies the operating I/O supply voltage for each signal

Table 4-6. Serial Peripheral Interface (SPI) Terminal Functions (continued)

SIGNAL		TYPE (1) (2)	OTHER (3) (4)	DESCRIPTION
NAME	NO.			
LCD_D[0]/ SPI_RX	A4	I/O/Z	DV_{DDIO} BH	This pin is multiplexed between LCD bridge and SPI. Mux control through the PPMODE bits in the EBSR. For SPI this pin is SPI receive data input.
LCD_D[10]/ I2S2_RX/ GP[20]/ SPI_RX	F5	I/O/Z	IPD DV_{DDIO} BH	This pin is multiplexed between LCD bridge, I2S2, GPIO, and SPI. Mux control through the PPMODE bits in the EBSR. For SPI this pin is SPI receive data input. The IPD resistor on this pin can be enabled or disabled through the PDINHIBR3 register.

4.2.7 UART Terminal Functions

Table 4-7 identifies the external signal names, the associated pin (ball) numbers along with the mechanical package designator, the pin type, whether the pin has any internal pullup or pulldown resistors or bus-holders, and a functional pin description. For more detailed information on device configuration, peripheral selection, multiplexed and shared pins, and debugging considerations, see Section 6, *Device Configuration*.

Table 4-7. Universal Asynchronous Receiver/Transmitter (UART) Terminal Functions

SIGNAL		TYPE (1) (2)	OTHER (3) (4)	DESCRIPTION
NAME	NO.			
UART				
LCD_D[14]/ UART_RXD/ GP[30]/ I2S3_RX	L1	I/O/Z	IPD DV_{DDIO} BH	This pin is multiplexed between LCD bridge, UART, GPIO, and I2S3. When used by UART, it is the receive data input UART_RXD. Mux control through the PPMODE bits in the EBSR. The IPD resistor on this pin can be enabled or disabled through the PDINHIBR3 register.
LCD_D[15]/ UART_TXD/ GP[31]/ I2S3_DX	L2	I/O/Z	IPD DV_{DDIO} BH	This pin is multiplexed between LCD bridge, UART, GPIO, and I2S3. In UART mode, it is the transmit data output UART_TXD. Mux control through the PPMODE bits in the EBSR. The IPD resistor on this pin can be enabled or disabled through the PDINHIBR3 register.
LCD_D[13]/ UART_CTS/ GP[29]/ I2S3_FS	M1	I/O/Z	IPD DV_{DDIO} BH	This pin is multiplexed between LCD bridge, UART, GPIO, and I2S3. In UART mode, it is the clear to send input UART_CTS. Mux control through the PPMODE bits in the EBSR. The IPD resistor on this pin can be enabled or disabled through the PDINHIBR3 register.
LCD_D[12]/ UART_RTS/ GP[28]/ I2S3_CLK	J3	I/O/Z	IPD DV_{DDIO} BH	This pin is multiplexed between LCD bridge, UART, GPIO, and I2S3. In UART mode, it is the ready to send output UART_RTS. Mux control through the PPMODE bits in the EBSR. The IPD resistor on this pin can be enabled or disabled through the PDINHIBR3 register.

(1) I = Input, O = Output, Z = High impedance, S = Supply voltage, GND = Ground, A = Analog signal, BH = Bus-holder
(2) Input pins of type I, I/O, and I/O/Z are required to be driven at all times. To achieve the lowest power, these pins must not be allowed to float. When configured as input or high-impedance state, and not driven to a known state, they may cause an excessive I/O-supply current. If this is the case, enable IPD and IPU, if applicable, or externally terminate the pins.
(3) IPD = Internal pulldown, IPU = Internal pullup. For more detailed information on pullup and pulldown resistors and situations where external pullup and pulldown resistors are required, see Section 6.8.1, *Pullup and Pulldown Resistors*.
(4) Specifies the operating I/O supply voltage for each signal

4.2.8 USB 2.0 Terminal Functions

Table 4-8 identifies the external signal names, the associated pin (ball) numbers along with the mechanical package designator, the pin type, whether the pin has any internal pullup or pulldown resistors or bus-holders, and a functional pin description. For more detailed information on device configuration, peripheral selection, multiplexed and shared pins, and debugging considerations, see Section 6, *Device Configuration*.

Table 4-8. Universal Serial Bus (USB) 2.0 Terminal Functions

SIGNAL		TYPE (1) (2)	OTHER (3) (4)	DESCRIPTION
NAME	NO.			
USB 2.0				
USB_MXI	L9	I	USB_V_{DDOSC}	12-MHz crystal oscillator input When the USB peripheral ***is not*** used, USB_MXI must be connected to ground (V_{SS}). When using an external 12-MHz oscillator, the external oscillator clock signal must be connected to the USB_MXI pin and the amplitude of the oscillator clock signal must meet the V_{IH} requirement (see Section 5.3, *Recommended Operating Conditions*). The USB_MXO remains unconnected and the USB_V_{SSOSC} signal is connected to board ground (V_{SS}).
USB_MXO	K9	O/Z	USB_V_{DDOSC}	12-MHz crystal oscillator output When the USB peripheral ***is not*** used, USB_MXO must be left unconnected. When using an external 12-MHz oscillator, the external oscillator clock signal must be connected to the USB_MXI pin and the amplitude of the oscillator clock signal must meet the V_{IH} requirement (see Section 5.3, *Recommended Operating Conditions*). The USB_MXO remains unconnected and the USB_V_{SSOSC} signal is connected to board ground (V_{SS}).
USB_V_{DDOSC}	K8	S	See Section 5.3, *Recommended Operating Conditions*	3.3-V power supply for USB oscillator. When the USB peripheral ***is not*** used, USB_V_{DDOSC} must be connected to ground (V_{SS}).
USB_V_{SSOSC}	M9	S	See Section 5.3, *Recommended Operating Conditions*	Ground for USB oscillator When the USB peripheral ***is not*** used, USB_V_{SSOSC} must be connected to ground (V_{SS}). When using an external 12-MHz oscillator, the external oscillator clock signal must be connected to the USB_MXI pin and the amplitude of the oscillator clock signal must meet the V_{IH} requirement (see Section 5.3, *Recommended Operating Conditions*). The USB_MXO remains unconnected and the USB_V_{SSOSC} signal is connected to board ground (V_{SS}).
USB_VBUS	K5	A I/O	See Section 5.3, *Recommended Operating Conditions*	USB power detect. 5-V input that signifies that VBUS is connected. This signal must be powered on in the order listed in Section 5.6.5.1, *Power-Supply Sequencing*. When the USB peripheral ***is not*** used, the USB_VBUS signal must be connected to ground (V_{SS}).
USB_DP	L6	A I/O	USB_V_{DDA3P3}	USB bidirectional Data Differential signal pair [positive and negative] When the USB peripheral ***is not*** used, the USB_DP and USB_DM signals should both be tied to ground (V_{SS}).
USB_DM	M6	A I/O	USB_V_{DDA3P3}	

(1) I = Input, O = Output, Z = High impedance, S = Supply voltage, GND = Ground, A = Analog signal, BH = Bus-holder
(2) Input pins of type I, I/O, and I/O/Z are required to be driven at all times. To achieve the lowest power, these pins must not be allowed to float. When configured as input or high-impedance state, and not driven to a known state, they may cause an excessive I/O-supply current. If this is the case, enable IPD and IPU, if applicable, or externally terminate the pins.
(3) IPD = Internal pulldown, IPU = Internal pullup. For more detailed information on pullup and pulldown resistors and situations where external pullup and pulldown resistors are required, see Section 6.8.1, *Pullup and Pulldown Resistors*.
(4) Specifies the operating I/O supply voltage for each signal

Table 4-8. Universal Serial Bus (USB) 2.0 Terminal Functions (continued)

SIGNAL		TYPE (1) (2)	OTHER (3) (4)	DESCRIPTION
NAME	NO.			
USB_R1	K7	A I/O	USB_V_{DDA3P3}	External resistor connect. Reference current output. This must be connected through a 10-kΩ ±1% resistor to USB_V_{SSREF} and placed as close to the device as possible. When the USB peripheral is not used, the USB_R1 signal must be connected through a 10-kΩ resistor to ground (V_{SS}).
USB_V_{SSREF}	H8	GND	See Section 5.3, *Recommended Operating Conditions*	Ground for reference current. This must be connected through a 10-kΩ ±1% resistor to USB_R1. When the USB peripheral is not used, the USB_V_{SSREF} signal must be connected directly to ground (V_{ss}).
USB_V_{DDA3P3}	L7	S	See Section 5.3, *Recommended Operating Conditions*	Analog 3.3-V power supply for USB PHY This signal must be powered on in the order listed in Section 5.6.5.1, *Power-Supply Sequencing*. When the USB peripheral is not used, the USB_V_{DDA3P3} signal must be connected to ground (V_{SS}).
USB_V_{SSA3P3}	H7	GND	See Section 5.3, *Recommended Operating Conditions*	Analog ground for USB PHY
USB_V_{DDA1P3}	K6	S	See Section 5.3, *Recommended Operating Conditions*	Analog 1.3-V power supply for USB PHY (For high-speed sensitive analog circuits) This signal must be powered on in the order listed in Section 5.6.5.1, *Power-Supply Sequencing*. When the USB peripheral is not used, the USB_V_{DDA1P3} signal must be connected to ground (V_{SS}).
USB_V_{DD1P3}	L5, M8	S	See Section 5.3, *Recommended Operating Conditions*	1.3-V digital core power supply for USB PHY. This signal must be powered on in the order listed in Section 5.6.5.1, *Power-Supply Sequencing*. When the USB peripheral is not used, the USB_V_{DD1P3} signal must be connected to ground (V_{SS}).
USB_V_{SS1P3}	H6	GND	See Section 5.3, *Recommended Operating Conditions*	Digital core ground for USB PHY. Analog ground for USB PHY (For high-speed sensitive analog circuits)
USB_V_{DDPLL}	M7	S	See Section 5.3, *Recommended Operating Conditions*	3.3-V USB analog PLL power supply When the USB peripheral ***is not*** used, the USB_V_{DDPLL} signal must be connected to ground (V_{SS}).
USB_V_{SSPLL}	L8	GND	See Section 5.3, *Recommended Operating Conditions*	USB analog PLL ground

4.2.9 LCD Terminal Functions

Table 4-9 identifies the external signal names, the associated pin (ball) numbers along with the mechanical package designator, the pin type, whether the pin has any internal pullup or pulldown resistors or bus-holders, and a functional pin description. For more detailed information on device configuration, peripheral selection, multiplexed and shared pins, and debugging considerations, see Section 6, *Device Configuration*.

Table 4-9. LCD Bridge Terminal Functions

SIGNAL		TYPE (1) (2)	OTHER (3) (4)	DESCRIPTION
NAME	NO.			
LCD_EN_RDB/ SPI_CLK	A1	O/Z	DV_{DDIO} BH	This pin is multiplexed between LCD bridge and SPI. For LCD bridge, this pin is either LCD bridge read and write enable (MPU68 mode) or read strobe (MPU80 mode). Mux control through the PPMODE bits in the EBSR. **Note:** This pin may consume static power if configured as Hi-Z and not externally pulled low or high. Prevent current drain by externally terminating the pin.
LCD_CS0_E0/ SPI_CS0	A2	I/O/Z	DV_{DDIO} BH	This pin is multiplexed between LCD bridge and SPI. For LCD bridge, this pin is either LCD bridge chip select 0 (MPU68 and MPU80 modes) or enable 0 (HD44780 mode). Mux control through the PPMODE bits in the EBSR.
LCD_RW_WRB/ SPI_CS2	B2	I/O/Z	DV_{DDIO} BH	This pin is multiplexed between LCD bridge and SPI. For LCD bridge, this pin is either LCD bridge read and write select (HD44780 and MPU68 modes) or write strobe (MPU80 mode). Mux control through the PPMODE bits in the EBSR.
LCD_RS/ SPI_CS3	A3	I/O/Z	DV_{DDIO} BH	This pin is multiplexed between LCD bridge and SPI. For LCD bridge, this pin is the LCD bridge address setup. Mux control through the PPMODE bits in the EBSR.
LCD_D[15]/ UART_TXD/ GP[31]/ I2S3_DX	L2	I/O/Z	IPD DV_{DDIO} BH	This pin is multiplexed between LCD bridge, UART, GPIO, and I2S3. For LCD bridge, it is LCD data pin 15. Mux control through the PPMODE bits in the EBSR. The IPD resistor on this pin can be enabled or disabled through the PDINHIBR3 register.
LCD_D[14]/ UART_RXD/ GP[30]/ I2S3_RX	L1	I/O/Z	IPD DV_{DDIO} BH	This pin is multiplexed between LCD bridge, UART, GPIO, and I2S3. For LCD bridge, it is LCD data pin 14. Mux control through the PPMODE bits in the EBSR. The IPD resistor on this pin can be enabled or disabled through the PDINHIBR3 register.
LCD_D[13]/ UART_CTS/ GP[29]/ I2S3_FS	M1	I/O/Z	IPD DV_{DDIO} BH	This pin is multiplexed between LCD bridge, UART, GPIO, and I2S3. For LCD bridge, it is LCD data pin 13. Mux control through the PPMODE bits in the EBSR. The IPD resistor on this pin can be enabled or disabled through the PDINHIBR3 register.
LCD_D[12]/ UART_RTS/ GP[28]/ I2S3_CLK	J3	I/O/Z	IPD DV_{DDIO} BH	This pin is multiplexed between LCD bridge, I2S2, and GPIO. For LCD bridge, it is LCD data pin 12. Mux control through the PPMODE bits in the EBSR. The IPD resistor on this pin can be enabled or disabled through the PDINHIBR3 register.

(1) I = Input, O = Output, Z = High impedance, S = Supply voltage, GND = Ground, A = Analog signal, BH = Bus-holder
(2) Input pins of type I, I/O, and I/O/Z are required to be driven at all times. To achieve the lowest power, these pins must not be allowed to float. When configured as input or high-impedance state, and not driven to a known state, they may cause an excessive I/O-supply current. If this is the case, enable IPD and IPU, if applicable, or externally terminate the pins.
(3) IPD = Internal pulldown, IPU = Internal pullup. For more detailed information on pullup and pulldown resistors and situations where external pullup and pulldown resistors are required, see Section 6.8.1, *Pullup and Pulldown Resistors*.
(4) Specifies the operating I/O supply voltage for each signal

Table 4-9. LCD Bridge Terminal Functions (continued)

SIGNAL NAME	SIGNAL NO.	TYPE (1) (2)	OTHER (3) (4)	DESCRIPTION
LCD_D[11]/ I2S2_DX/ GP[27]/ SPI_TX	K2	I/O/Z	IPD DV_{DDIO} BH	This pin is multiplexed between LCD bridge, I2S2, GPIO, and SPI. For LCD bridge, it is LCD data pin 11. Mux control through the PPMODE bits in the EBSR. The IPD resistor on this pin can be enabled or disabled through the PDINHIBR3 register.
LCD_D[10]/ I2S2_RX/ GP[20]/ SPI_RX	F5	I/O/Z	IPD DV_{DDIO} BH	This pin is multiplexed between LCD bridge, I2S2, GPIO, and SPI. For LCD bridge, it is LCD data pin 10. Mux control through the PPMODE bits in the EBSR. The IPD resistor on this pin can be enabled or disabled through the PDINHIBR3 register.
LCD_D[9]/ I2S2_FS/ GP[19]/ SPI_CS0	K1	I/O/Z	IPD DV_{DDIO} BH	This pin is multiplexed between LCD bridge, I2S2, GPIO, and SPI. For LCD bridge, it is LCD data pin 9. Mux control through the PPMODE bits in the EBSR. The IPD resistor on this pin can be enabled or disabled through the PDINHIBR3 register.
LCD_D[8]/ I2S2_CLK GP[18]/ SPI_CLK	H1	I/O/Z	IPD DV_{DDIO} BH	This pin is multiplexed between LCD bridge, I2S2, GPIO, and SPI. For LCD bridge, it is LCD data pin 8. Mux control through the PPMODE bits in the EBSR. The IPD resistor on this pin can be enabled or disabled through the PDINHIBR3 register.
LCD_D[7]/ GP[17]	J1	I/O/Z	IPD DV_{DDIO} BH	This pin is multiplexed between LCD bridge and GPIO. For LCD bridge, it is LCD data pin 7. Mux control through the PPMODE bits in the EBSR. The IPD resistor on this pin can be enabled or disabled through the PDINHIBR3 register.
LCD_D[6]/ GP[16]	E3	I/O/Z	IPD DV_{DDIO} BH	This pin is multiplexed between LCD bridge and GPIO. For LCD bridge, it is LCD data pin 6. Mux control through the PPMODE bits in the EBSR. The IPD resistor on this pin can be enabled or disabled through the PDINHIBR3 register.
LCD_D[5]/ GP[15]	G1	I/O/Z	IPD DV_{DDIO} BH	This pin is multiplexed between LCD bridge and GPIO. For LCD bridge, it is LCD data pin 5. Mux control through the PPMODE bits in the EBSR. The IPD resistor on this pin can be enabled or disabled through the PDINHIBR3 register.
LCD_D[4]/ GP[14]	F1	I/O/Z	IPD DV_{DDIO} BH	This pin is multiplexed between LCD bridge and GPIO. For LCD bridge, it is LCD data pin 4. Mux control through the PPMODE bits in the EBSR. The IPD resistor on this pin can be enabled or disabled through the PDINHIBR3 register.
LCD_D[3]/ GP[13]	E1	I/O/Z	IPD DV_{DDIO} BH	This pin is multiplexed between LCD bridge and GPIO. For LCD bridge, it is LCD data pin 3. Mux control through the PPMODE bits in the EBSR. The IPD resistor on this pin can be enabled or disabled through the PDINHIBR3 register.
LCD_D[2]/ GP[12]	E2	I/O/Z	IPD DV_{DDIO} BH	This pin is multiplexed between LCD bridge and GPIO. For LCD bridge, it is LCD data pin 2. Mux control through the PPMODE bits in the EBSR. The IPD resistor on this pin can be enabled or disabled through the PDINHIBR3 register.
LCD_D[1]/ SPI_TX	C2	I/O/Z	DV_{DDIO} BH	This pin is multiplexed between LCD bridge and SPI. For LCD bridge, it is LCD data pin 1. Mux control through the PPMODE bits in the EBSR.
LCD_D[0]/ SPI_RX	A4	I/O/Z	DV_{DDIO} BH	This pin is multiplexed between LCD bridge and SPI. For LCD bridge, it is LCD data pin 0. Mux control through the PPMODE bits in the EBSR.

4.2.10 SD1 and SD0 Terminal Functions

4.2.10.1 SD1 Terminal Functions

Table 4-10 identifies the external signal names, the associated pin (ball) numbers along with the mechanical package designator, the pin type, whether the pin has any internal pullup or pulldown resistors or bus-holders, and a functional pin description. For more detailed information on device configuration, peripheral selection, multiplexed and shared pins, and debugging considerations, see Section 6, *Device Configuration*.

Table 4-10. SD1 Terminal Functions

SIGNAL		TYPE (1) (2)	OTHER (3) (4)	DESCRIPTION
NAME	NO.			
SD				
SD1_CLK/ I2S1_CLK/ GP[6]	H5	I/O/Z	IPD DV_{DDIO} BH	This pin is multiplexed between SD1, I2S1, and GPIO. For SD, this is the SD1 data clock output SD1_CLK. Mux control through the SP1MODE bits in the EBSR. The IPD resistor on this pin can be enabled or disabled through the PDINHIBR1 register.
SD1_CMD/ I2S1_FS/ GP[7]	L4	I/O/Z	IPD DV_{DDIO} BH	This pin is multiplexed between SD1, I2S1, and GPIO. For SD, this is the SD1 command I/O output SD1_CMD. Mux control through the SP1MODE bits in the EBSR. The IPD resistor on this pin can be enabled or disabled through the PDINHIBR1 register.
SD1_D3/ GP[11]	G5	I/O/Z	IPD DV_{DDIO} BH	The SD1_D3 and SD1_D2 pins are multiplexed between SD1 and GPIO. The SD1_D1 and SD1_D0 pins are multiplexed between SD1, I2S1, and GPIO. In SD mode, all these pins are the SD1 nibble wide bidirectional data bus. Mux control through the SP1MODE bits in the EBSR. The IPD resistor on these pins can be enabled or disabled through the PDINHIBR1 register.
SD1_D2/ GP[10]	M4	I/O/Z	IPD DV_{DDIO} BH	
SD1_D1/ I2S1_RX/ GP[9]	H3	I/O/Z	IPD DV_{DDIO} BH	
SD1_D0/ I2S1_DX/ GP[8]	L3	I/O/Z	IPD DV_{DDIO} BH	

(1) I = Input, O = Output, Z = High impedance, S = Supply voltage, GND = Ground, A = Analog signal, BH = Bus-holder
(2) Input pins of type I, I/O, and I/O/Z are required to be driven at all times. To achieve the lowest power, these pins must not be allowed to float. When configured as input or high-impedance state, and not driven to a known state, they may cause an excessive I/O-supply current. If this is the case, enable IPD and IPU, if applicable, or externally terminate the pins.
(3) IPD = Internal pulldown, IPU = Internal pullup. For more detailed information on pullup and pulldown resistors and situations where external pullup and pulldown resistors are required, see Section 6.8.1, *Pullup and Pulldown Resistors*.
(4) Specifies the operating I/O supply voltage for each signal

4.2.10.2 SD0 Terminal Functions

Table 4-11 identifies the external signal names, the associated pin (ball) numbers along with the mechanical package designator, the pin type, whether the pin has any internal pullup or pulldown resistors or bus-holders, and a functional pin description. For more detailed information on device configuration, peripheral selection, multiplexed and shared pins, and debugging considerations, see Section 6, *Device Configuration*.

Table 4-11. SD0 Terminal Functions

SIGNAL		TYPE (1) (2)	OTHER (3) (4)	DESCRIPTION
NAME	NO.			
SD				
SD0_CLK/ I2S0_CLK/ GP[0]	E5	I/O/Z	IPD DV_{DDIO} BH	This pin is multiplexed between SD0, I2S0, and GPIO. For SD, this is the SD0 data clock output SD0_CLK. Mux control through the SP0MODE bits in the EBSR. The IPD resistor on this pin can be enabled or disabled through the PDINHIBR1 register.
SD0_CMD/ I2S0_FS/ GP[1]	J2	I/O/Z	IPD DV_{DDIO} BH	This pin is multiplexed between SD0, I2S0, and GPIO. For SD, this is the SD0 command I/O output SD0_CMD. Mux control through the SP0MODE bits in the EBSR. The IPD resistor on this pin can be enabled or disabled through the PDINHIBR1 register.
SD0_D3/ GP[5]	G3	I/O/Z	IPD DV_{DDIO} BH	The SD0_D3 and SD0_D2 pins are multiplexed between SD0 and GPIO. The SD0_D1 and SD0_D0 pins are multiplexed between SD0, I2S0, and GPIO. In SD mode, these pins are the SD0 nibble wide bidirectional data bus. Mux control through the SP0MODE bits in the EBSR. The IPD resistor on these pins can be enabled or disabled through the PDINHIBR1 register.
SD0_D2/ GP[4]	M3	I/O/Z	IPD DV_{DDIO} BH	
SD0_D1/ I2S0_RX/ GP[3]	G2	I/O/Z	IPD DV_{DDIO} BH	
SD0_D0/ I2S0_DX/ GP[2]	D5	I/O/Z	IPD DV_{DDIO} BH	

(1) I = Input, O = Output, Z = High impedance, S = Supply voltage, GND = Ground, A = Analog signal, BH = Bus-holder
(2) Input pins of type I, I/O, and I/O/Z are required to be driven at all times. To achieve the lowest power, these pins must not be allowed to float. When configured as input or high-impedance state, and not driven to a known state, they may cause an excessive I/O-supply current. If this is the case, enable IPD and IPU, if applicable, or externally terminate the pins.
(3) IPD = Internal pulldown, IPU = Internal pullup. For more detailed information on pullup and pulldown resistors and situations where external pullup and pulldown resistors are required, see Section 6.8.1, *Pullup and Pulldown Resistors*.
(4) Specifies the operating I/O supply voltage for each signal

4.2.11 SAR ADC Terminal Functions

Table 4-12 identifies the external signal names, the associated pin (ball) numbers along with the mechanical package designator, the pin type, whether the pin has any internal pullup or pulldown resistors or bus-holders, and a functional pin description. For more detailed information on device configuration, peripheral selection, multiplexed and shared pins, and debugging considerations, see Section 6, *Device Configuration*.

Table 4-12. 10-Bit SAR ADC Terminal Functions

SIGNAL		TYPE (1) (2)	OTHER (3) (4)	DESCRIPTION
NAME	NO.			
SAR ADC				
GPAIN1	F8	I/O	V_{DDA_ANA}	GPAIN1: General-Purpose Output and Analog Input pin 1. This pin is connected to ADC Channel 3. GPAIN1 can be used as a general-purpose output if certain requirements are met (see the following note). GPAIN1 can accommodate input voltages from 0 V to V_{DDA_ANA}. **Note:** If the ANA_LDO is used to supply power to V_{DDA_ANA}, this pin must ***not*** be used as a general-purpose output (driving high) because the maximum current capability (see the I_{SD} parameter in Section 5.5, *Electrical Characteristics*) of the ANA_LDO can be exceeded. Doing so may result in the on-chip power-on reset (POR) resetting the chip.
GPAIN2	F10	I/O	V_{DDA_ANA}	GPAIN2: General-Purpose Output and Analog Input pin 2. This pin is connected to ADC Channel 4. GPAIN2 can be used as a general-purpose output if certain requirements are met (see the following note). GPAIN2 can accommodate input voltages from 0 V to V_{DDA_ANA}. **Note:** If the ANA_LDO is used to supply power to V_{DDA_ANA}, this pin must ***not*** be used as a general-purpose output (driving high) because the maximum current capability (see the I_{SD} parameter in Section 5.5, *Electrical Characteristics*) of the ANA_LDO can be exceeded. Doing so may result in the on-chip POR resetting the chip.
GPAIN3	J12	I/O	V_{DDA_ANA}	GPAIN3: General-Purpose Output and Analog Input pin 3. This pin is connected to ADC Channel 5. GPAIN3 can be used as a general-purpose output if certain requirements are met (see the following note). GPAIN3 can accommodate input voltages from 0 V to V_{DDA_ANA}. **Note:** If the ANA_LDO is used to supply power to V_{DDA_ANA}, this pin must ***not*** be used as a general-purpose output (driving high) because the maximum current capability (see the I_{SD} parameter in Section 5.5, *Electrical Characteristics*) of the ANA_LDO can be exceeded. Doing so may result in the on-chip POR resetting the chip.

(1) I = Input, O = Output, Z = High impedance, S = Supply voltage, GND = Ground, A = Analog signal, BH = Bus-holder
(2) Input pins of type I, I/O, and I/O/Z are required to be driven at all times. To achieve the lowest power, these pins must not be allowed to float. When configured as input or high-impedance state, and not driven to a known state, they may cause an excessive I/O-supply current. If this is the case, enable IPD and IPU, if applicable, or externally terminate the pins.
(3) IPD = Internal pulldown, IPU = Internal pullup. For more detailed information on pullup and pulldown resistors and situations where external pullup and pulldown resistors are required, see Section 6.8.1, *Pullup and Pulldown Resistors*.
(4) Specifies the operating I/O supply voltage for each signal

4.2.12 GPIO Terminal Functions

Table 4-13 identifies the external signal names, the associated pin (ball) numbers along with the mechanical package designator, the pin type, whether the pin has any internal pullup or pulldown resistors or bus-holders, and a functional pin description. For more detailed information on device configuration, peripheral selection, multiplexed and shared pins, and debugging considerations, see Section 6, *Device Configuration*.

Table 4-13. General-Purpose Input/Output (GPIO) Terminal Functions

SIGNAL		TYPE (1) (2)	OTHER (3) (4)	DESCRIPTION
NAME	NO.			
GENERAL-PURPOSE INPUT/OUTPUT				
SD0_CLK/ I2S0_CLK/ GP[0]	E5	I/O/Z	IPD DV_{DDIO} BH	This pin is multiplexed between SD0, I2S0, and GPIO. For GPIO, it is general-purpose input/output pin 0 (GP[0]). Mux control through the SP0MODE bits in the EBSR. The IPD resistor on this pin can be enabled or disabled through the PDINHIBR1 register.
SD0_CMD/ I2S0_FS/ GP[1]	J2	I/O/Z	IPD DV_{DDIO} BH	This pin is multiplexed between SD0, I2S0, and GPIO. For GPIO, it is general-purpose input/output pin 1 (GP[1]). Mux control through the SP0MODE bits in the EBSR. The IPD resistor on this pin can be enabled or disabled through the PDINHIBR1 register.
SD0_D0/ I2S0_DX/ GP[2]	D5	I/O/Z	IPD DV_{DDIO} BH	This pin is multiplexed between SD0, I2S0, and GPIO. For GPIO, it is general-purpose input/output pin 2 (GP[2]). Mux control through the SP0MODE bits in the EBSR. The IPD resistor on this pin can be enabled or disabled through the PDINHIBR1 register.
SD0_D1/ I2S0_RX/ GP[3]	G2	I/O/Z	IPD DV_{DDIO} BH	This pin is multiplexed between SD0, I2S0, and GPIO. For GPIO, it is general-purpose input/output pin 3 (GP[3]). Mux control through the SP0MODE bits in the EBSR. The IPD resistor on this pin can be enabled or disabled through the PDINHIBR1 register.
SD0_D2/ GP[4]	M3	I/O/Z	IPD DV_{DDIO} BH	This pin is multiplexed between SD0 and GPIO. For GPIO, it is general-purpose input/output pin 4 (GP[4]). Mux control through the SP0MODE bits in the EBSR. The IPD resistor on this pin can be enabled or disabled through the PDINHIBR1 register.
SD0_D3/ GP[5]	G3	I/O/Z	IPD DV_{DDIO} BH	This pin is multiplexed between SD0 and GPIO. For GPIO, it is general-purpose input/output pin 5 (GP[5]). Mux control through the SP0MODE bits in the EBSR. The IPD resistor on this pin can be enabled or disabled through the PDINHIBR1 register.
SD1_CLK/ I2S1_CLK/ GP[6]	H5	I/O/Z	IPD DV_{DDIO} BH	This pin is multiplexed between SD1, I2S1, and GPIO. For GPIO, it is general-purpose input/output pin 6 (GP[6]). Mux control through the SP1MODE bits in the EBSR.
SD1_CMD/ I2S1_FS/ GP[7]	L4	I/O/Z	IPD DV_{DDIO} BH	This pin is multiplexed between SD1, I2S1, and GPIO. For GPIO, it is general-purpose input/output pin 7 (GP[7]). Mux control through the SP1MODE bits in the EBSR. The IPD resistor on this pin can be enabled or disabled through the PDINHIBR1 register.

(1) I = Input, O = Output, Z = High impedance, S = Supply voltage, GND = Ground, A = Analog signal, BH = Bus-holder
(2) Input pins of type I, I/O, and I/O/Z are required to be driven at all times. To achieve the lowest power, these pins must not be allowed to float. When configured as input or high-impedance state, and not driven to a known state, they may cause an excessive I/O-supply current. If this is the case, enable IPD and IPU, if applicable, or externally terminate the pins.
(3) IPD = Internal pulldown, IPU = Internal pullup. For more detailed information on pullup and pulldown resistors and situations where external pullup and pulldown resistors are required, see Section 6.8.1, *Pullup and Pulldown Resistors*.
(4) Specifies the operating I/O supply voltage for each signal

Table 4-13. General-Purpose Input/Output (GPIO) Terminal Functions (continued)

SIGNAL		TYPE (1) (2)	OTHER (3) (4)	DESCRIPTION
NAME	NO.			
SD1_D0/ I2S1_DX/ GP[8]	L3	I/O/Z	IPD DV_{DDIO} BH	This pin is multiplexed between SD1, I2S1, and GPIO. For GPIO, it is general-purpose input/output pin 8 (GP[8]). Mux control through the SP1MODE bits in the EBSR. The IPD resistor on this pin can be enabled or disabled through the PDINHIBR1 register.
SD1_D1/ I2S1_RX/ GP[9]	H3	I/O/Z	IPD DV_{DDIO} BH	This pin is multiplexed between SD1, I2S1, and GPIO. For GPIO, it is general-purpose input/output pin 9 (GP[9]). Mux control through the SP1MODE bits in the EBSR. The IPD resistor on this pin can be enabled or disabled through the PDINHIBR1 register.
SD1_D2/ GP[10]	M4	I/O/Z	IPD DV_{DDIO} BH	This pin is multiplexed between SD1 and GPIO. For GPIO, it is general-purpose input/output pin 10 (GP[10]). Mux control through the SP1MODE bits in the EBSR. The IPD resistor on this pin can be enabled or disabled through the PDINHIBR1 register.
SD1_D3/ GP[11]	G5	I/O/Z	IPD DV_{DDIO} BH	This pin is multiplexed between SD1 and GPIO. For GPIO, it is general-purpose input/output pin 11 (GP[11]). Mux control through the SP1MODE bits in the EBSR. The IPD resistor on this pin can be enabled or disabled through the PDINHIBR1 register.
LCD_D[2]/ GP[12]	E2	I/O/Z	IPD DV_{DDIO} BH	This pin is multiplexed between LCD bridge and GPIO. For GPIO, it is general-purpose input/output pin 12 (GP[12]). Mux control through the PPMODE bits in the EBSR. The IPD resistor on this pin can be enabled or disabled through the PDINHIBR3 register.
LCD_D[3]/ GP[13]	E1	I/O/Z	IPD DV_{DDIO} BH	This pin is multiplexed between LCD bridge and GPIO. For GPIO, it is general-purpose input/output pin 13 (GP[13]). Mux control through the PPMODE bits in the EBSR. The IPD resistor on this pin can be enabled or disabled through the PDINHIBR3 register.
LCD_D[4]/ GP[14]	F1	I/O/Z	IPD DV_{DDIO} BH	This pin is multiplexed between LCD bridge and GPIO. For GPIO, it is general-purpose input/output pin 14 (GP[14]). Mux control through the PPMODE bits in the EBSR. The IPD resistor on this pin can be enabled or disabled through the PDINHIBR3 register.
LCD_D[5]/ GP[15]	G1	I/O/Z	IPD DV_{DDIO} BH	This pin is multiplexed between LCD bridge and GPIO. For GPIO, it is general-purpose input/output pin 15 (GP[15]). Mux control through the PPMODE bits in the EBSR. The IPD resistor on this pin can be enabled or disabled through the PDINHIBR3 register.
LCD_D[6]/ GP[16]	E3	I/O/Z	IPD DV_{DDIO} BH	This pin is multiplexed between LCD bridge and GPIO. For GPIO, it is general-purpose input/output pin 16 (GP[16]). Mux control through the PPMODE bits in the EBSR. The IPD resistor on this pin can be enabled or disabled through the PDINHIBR3 register.
LCD_D[7]/ GP[17]	J1	I/O/Z	IPD DV_{DDIO} BH	This pin is multiplexed between LCD bridge and GPIO. For GPIO, it is general-purpose input/output pin 17 (GP[17]). Mux control through the PPMODE bits in the EBSR. The IPD resistor on this pin can be enabled or disabled through the PDINHIBR3 register.
LCD_D[8]/ I2S2_CLK/ GP[18]/ SPI_CLK	H1	I/O/Z	IPD DV_{DDIO} BH	This pin is multiplexed between LCD bridge and GPIO. For GPIO, it is general-purpose input/output pin 18 (GP[18]). Mux control through the PPMODE bits in the EBSR. The IPD resistor on this pin can be enabled or disabled through the PDINHIBR3 register.

Table 4-13. General-Purpose Input/Output (GPIO) Terminal Functions (continued)

SIGNAL		TYPE (1) (2)	OTHER (3) (4)	DESCRIPTION
NAME	NO.			
LCD_D[9]/ I2S2_FS/ GP[19]/ SPI_CS0	K1	I/O/Z	IPD DV_{DDIO} BH	This pin is multiplexed between LCD bridge, I2S2, and GPIO. For GPIO, it is general-purpose input/output pin 19 (GP[19]). Mux control through the PPMODE bits in the EBSR. The IPD resistor on this pin can be enabled or disabled through the PDINHIBR3 register.
LCD_D[10]/ I2S2_RX/ GP[20]/ SPI_RX	F5	I/O/Z	IPD DV_{DDIO} BH	This pin is multiplexed between LCD bridge, I2S2, GPIO and SPI. For GPIO, it is general-purpose input/output pin 20 (GP[20]). Mux control through the PPMODE bits in the EBSR. The IPD resistor on this pin can be enabled or disabled through the PDINHIBR3 register.
LCD_D[11]/ I2S2_DX/ GP[27]/ SPI_TX	K2	I/O/Z	IPD DV_{DDIO} BH	This pin is multiplexed between LCD bridge, I2S2, GPIO, and SPI. For GPIO, it is general-purpose input/output pin 27 (GP[27]). Mux control through the PPMODE bits in the EBSR. The IPD resistor on this pin can be enabled or disabled through the PDINHIBR3 register.
LCD_D[12]/ UART_RTS/ GP[28]/ I2S3_CLK	J3	I/O/Z	IPD DV_{DDIO} BH	This pin is multiplexed between LCD bridge, UART, GPIO, and I2S3. For GPIO, it is general-purpose input/output pin 28 (GP[28]). Mux control through the PPMODE bits in the EBSR. The IPD resistor on this pin can be enabled or disabled through the PDINHIBR3 register.
LCD_D[13]/ UART_CTS/ GP[29]/ I2S3_FS	M1	I/O/Z	IPD DV_{DDIO} BH	This pin is multiplexed between LCD bridge, UART, GPIO, and I2S3. For GPIO, it is general-purpose input/output pin 29 (GP[29]). Mux control through the PPMODE bits in the EBSR. The IPD resistor on this pin can be enabled or disabled through the PDINHIBR3 register.
LCD_D[14]/ UART_RXD/ GP[30]/ I2S3_RX	L1	I/O/Z	IPD DV_{DDIO} BH	This pin is multiplexed between LCD bridge, UART, GPIO, and I2S3. For GPIO, it is general-purpose input/output pin 30 (GP[30]). Mux control through the PPMODE bits in the EBSR. The IPD resistor on this pin can be enabled or disabled through the PDINHIBR3 register.
LCD_D[15]/ UART_TXD/ GP[31]/ I2S3_DX	L2	I/O/Z	IPD DV_{DDIO} BH	This pin is multiplexed between LCD bridge, UART, GPIO, and I2S3. For GPIO, it is general-purpose input/output pin 31 (GP[31]). Mux control through the PPMODE bits in the EBSR. The IPD resistor on this pin can be enabled or disabled through the PDINHIBR3 register.

4.2.13 Regulators and Power Management Terminal Functions

Table 4-14 identifies the external signal names, the associated pin (ball) numbers along with the mechanical package designator, the pin type, whether the pin has any internal pullup or pulldown resistors or bus-holders, and a functional pin description. For more detailed information on device configuration, peripheral selection, multiplexed and shared pins, and debugging considerations, see Section 6, *Device Configuration*.

Table 4-14. Regulators and Power Management Terminal Functions

SIGNAL		TYPE (1) (2)	OTHER (3) (4)	DESCRIPTION
NAME	NO.			
REGULATORS				
DSP_LDOO	M11	S		DSP_LDO output. When enabled, this output provides a regulated 1.3- or 1.05-V output and up to 250 mA of current (see the I_{SD} parameter in Section 5.5, *Electrical Characteristics*). The DSP_LDO is intended to supply current to the digital core circuits only (CV_{DD}) and not external devices. For proper device operation, the external decoupling capacitor of this pin must be 5µF ~ 10µF. For more detailed information, see Section 5.6.5.4, *Power-Supply Decoupling*. When disabled, this pin is in the high-impedance (Hi-Z) state. When DSP_LDO comes out of reset, it is enabled to 1.3 V for the bootloader to operate.
LDOI	L10, L11, G10	S		LDO inputs. For proper device operation, LDOI must always be powered. The LDOI pins must be connected to the same power supply source with a voltage range as specified for LDOI in Section 5.3, *Recommended Operating Conditions*. These pins supply power to the internal LDOs, the bandgap reference generator circuits, and serve as the I/O supply for some input pins.
$\overline{\text{DSP\_LDO\_EN}}$	M12	I		DSP_LDO enable input. This signal is not intended to be dynamically switched. 0 = DSP_LDO is enabled. The internal DSP LDO is enabled to regulate power on the DSP_LDOO pin at either 1.3 V or 1.05 V, according to the DSP_LDO_V bit in the LDOCNTL register (see Figure 5-2). At power-on-reset, the internal POR monitors the DSP_LDOO pin voltage and generates the internal POWERGOOD signal when the DSP_LDO voltage is above a minimum threshold voltage. The internal device reset is generated by the AND of POWERGOOD and the $\overline{\text{RESET}}$ pin. 1 = DSP_LDO is disabled and the DSP_LDOO pin is in a high-impedance (Hi-Z) state. The internal voltage monitoring on the DSP_LDOO is bypassed and the internal POWERGOOD signal is immediately set high. The $\overline{\text{RESET}}$ pin (A11) will act as the sole reset source for the device. If an external power supply is used to provide power to CV_{DD}, then $\overline{\text{DSP\_LDO\_EN}}$ must be tied to LDOI, DSP_LDOO must be left unconnected, and the $\overline{\text{RESET}}$ pin must be asserted appropriately for device initialization after power up. **Note:** To pull up this pin, connect it to the same supply as the LDOI pins.
USB_LDOO	M10	S		USB_LDO output. This output provides a regulated 1.3 V output and up to 25 mA of current (see the I_{SD} parameter in Section 5.5, *Electrical Characteristics*). For proper device operation, this pin must be connected to a 1 µF ~ 2 µF decoupling capacitor to V_{SS}. For more detailed information, see Section 5.6.5.4, *Power-Supply Decoupling*. This LDO is intended to supply power to the USB_ V_{DD1P3}, USB_V_{DDA1P3} pins and not external devices.

(1) I = Input, O = Output, Z = High impedance, S = Supply voltage, GND = Ground, A = Analog signal, BH = Bus-holder
(2) Input pins of type I, I/O, and I/O/Z are required to be driven at all times. To achieve the lowest power, these pins must not be allowed to float. When configured as input or high-impedance state, and not driven to a known state, they may cause an excessive IO-supply current. If this is the case, enable IPD and IPU, if applicable, or externally terminate the pins.
(3) IPD = Internal pulldown, IPU = Internal pullup. For more detailed information on pullup and pulldown resistors and situations where external pullup and pulldown resistors are required, see Section 6.8.1, *Pullup and Pulldown Resistors*.
(4) Specifies the operating I/O supply voltage for each signal

Table 4-14. Regulators and Power Management Terminal Functions (continued)

SIGNAL		TYPE (1) (2)	OTHER (3) (4)	DESCRIPTION
NAME	NO.			
ANA_LDOO	H11	S		ANA_LDO output. This output provides a regulated 1.3 V output and up to 4 mA of current (see the I_{SD} parameter in Section 5.5, *Electrical Characteristics*). For proper device operation, this pin must be connected to an ~ 1.0 µF decoupling capacitor to V_{SS}. For more detailed information, see Section 5.6.5.4, *Power-Supply Decoupling*. This LDO is intended to supply power to the V_{DDA_ANA} and V_{DDA_PLL} pins and ***not*** external devices.
BG_CAP	J11	A I/O		Bandgap reference filter signal. For proper device operation, this pin should be bypassed with a 0.1-µF capacitor to analog ground (V_{SSA_ANA}). BG_CAP provides a settling time of 200 ms that must elapse before executing bootloader code. The settling time is used by Timer0. The BG_CAP external capacitor provides filtering for stable reference voltages and currents generated by the bandgap circuit. The bandgap produces the references for use by the System PLL, SAR, and POR circuits.

4.2.14 Reserved and No Connects Terminal Functions

Table 4-15 identifies the external signal names, the associated pin (ball) numbers along with the mechanical package designator, the pin type, whether the pin has any internal pullup or pulldown resistors or bus-holders, and a functional pin description. For more detailed information on device configuration, peripheral selection, multiplexed and shared pins, and debugging considerations, see Section 6, *Device Configuration*.

Table 4-15. Reserved and No Connects Terminal Functions

SIGNAL		TYPE (1) (2)	OTHER (3) (4)	DESCRIPTION
NAME	NO.			
RESERVED				
RSV0	L12	I	–	Reserved. For proper device operation, this pin must be tied directly to V_{SS}.
RSV3	K11	I	–	Reserved. For proper device operation, this pin must be tied directly to V_{SS}.
RSV4	H10	I	–	Reserved. For proper device operation, this pin must be tied directly to V_{SS}.
RSV5	J10	I	–	Reserved. For proper device operation, this pin must be tied directly to V_{SS}.
RSV17	M5	I	–	Reserved. For proper device operation, this pin must be unconnected.

(1) I = Input, O = Output, Z = High impedance, S = Supply voltage, GND = Ground, A = Analog signal, BH = Bus-holder
(2) Input pins of type I, I/O, and I/O/Z are required to be driven at all times. To achieve the lowest power, these pins must not be allowed to float. When configured as input or high-impedance state, and not driven to a known state, they may cause an excessive IO-supply current. If this is the case, enable IPD and IPU, if applicable, or externally terminate the pins.
(3) IPD = Internal pulldown, IPU = Internal pullup. For more detailed information on pullup and pulldown resistors and situations where external pullup and pulldown resistors are required, see Section 6.8.1, *Pullup and Pulldown Resistors*.
(4) Specifies the operating I/O supply voltage for each signal

4.2.15 Supply Voltage Terminal Functions

Table 4-16 identifies the external signal names, the associated pin (ball) numbers along with the mechanical package designator, the pin type, whether the pin has any internal pullup or pulldown resistors or bus-holders, and a functional pin description. For more detailed information on device configuration, peripheral selection, multiplexed and shared pins, and debugging considerations, see Section 6, *Device Configuration*.

Table 4-16. Supply Voltage Terminal Functions

SIGNAL NAME	SIGNAL NO.	TYPE (1) (2)	OTHER (3) (4)	DESCRIPTION
SUPPLY VOLTAGES				
CV_{DD}	A9 B5 B8 C6 E6 G7 J9	PWR		1.05-V Digital Core supply voltage (60 MHz) 1.3-V Digital Core supply voltage (100 or 120 MHz)
DV_{DDIO}	B10 D2 H2 M2	PWR		1.8-V, 2.5-V, 2.75-V, or 3.3-V I/O power supply for non-RTC I/Os The DV_{DDIO} signal must always be powered for proper operation.
CV_{DDRTC}	D10	PWR		1.05-V through 1.3-V RTC digital core and RTC oscillator power supply **Note:** The CV_{DDRTC} must be powered though RTC is not used. **Note:** The CV_{DDRTC} cannot be powered by any of the on-chip LDOs and must be externally powered.
DV_{DDRTC}	F12	PWR		1.8-V, 2.5-V, 2.75-V, or 3.3-V I/O power supply for RTC_XO and RTC_XI pins
V_{DDA_PLL}	E10	PWR	See Section 5.3, *Recommended Operating Conditions*	1.3-V Analog PLL power supply for the system clock generator (PLLOUT ≤ 120 MHz) This signal can be powered from the ANA_LDOO pin.
USB_V_{DDPLL}	M7	S	See Section 5.3, *Recommended Operating Conditions*	3.3-V USB Analog PLL power supply When the USB peripheral is not used, the USB_V_{DDPLL} signal must be connected to ground (V_{SS}).
USB_V_{DD1P3}	L5	S	See Section 5.3, *Recommended Operating Conditions*	1.3-V digital core power supply for USB PHY. This signal must be powered on in the order listed in Section 5.6.5.1, *Power-Supply Sequencing*. When the USB peripheral is not used, the USB_V_{DD1P3} signal must be connected to ground (V_{SS}).
USB_V_{DDA1P3}	K6	S	See Section 5.3, *Recommended Operating Conditions*	Analog 1.3-V power supply for USB PHY (For high-speed sensitive analog circuits) This signal must be powered on in the order listed in Section 5.6.5.1, *Power-Supply Sequencing*. When the USB peripheral is not used, the USB_V_{DDA1P3} signal must be connected to ground (V_{SS}).

(1) I = Input, O = Output, Z = High impedance, S = Supply voltage, GND = Ground, A = Analog signal, BH = Bus-holder
(2) Input pins of type I, I/O, and I/O/Z are required to be driven at all times. To achieve the lowest power, these pins must not be allowed to float. When configured as input or high-impedance state, and not driven to a known state, they may cause an excessive I/O-supply current. If this is the case, enable IPD and IPU, if applicable, or externally terminate the pins.
(3) IPD = Internal pulldown, IPU = Internal pullup. For more detailed information on pullup and pulldown resistors and situations where external pullup and pulldown resistors are required, see Section 6.8.1, *Pullup and Pulldown Resistors*.
(4) Specifies the operating I/O supply voltage for each signal

Table 4-16. Supply Voltage Terminal Functions (continued)

SIGNAL		TYPE (1) (2)	OTHER (3) (4)	DESCRIPTION
NAME	NO.			
USB_V_{DDA3P3}	L7	S	See Section 5.3, *Recommended Operating Conditions*	Analog 3.3 V power supply for USB PHY This signal must be powered on in the order listed in Section 5.6.5.1, *Power-Supply Sequencing*. When the USB peripheral is not used, the USB_V_{DDA3P3} signal must be connected to ground (V_{SS}).
USB_V_{DDOSC}	K8	S	See Section 5.3, *Recommended Operating Conditions*	3.3-V power supply for USB oscillator When the USB peripheral is not used , the USB_V_{DDOSC} signal must be connected to ground (V_{SS}).
V_{DDA_ANA}	G11	PWR		1.3-V supply for power management and 10-bit SAR ADC This signal can be powered from the ANA_LDOO pin.

4.2.16 Ground Terminal Functions

Table 4-17 identifies the external signal names, the associated pin (ball) numbers along with the mechanical package designator, the pin type, whether the pin has any internal pullup or pulldown resistors or bus-holders, and a functional pin description. For more detailed information on device configuration, peripheral selection, multiplexed and shared pins, and debugging considerations, see Section 6, *Device Configuration*.

Table 4-17. Ground Terminal Functions

SIGNAL		TYPE (1) (2)	OTHER (3) (4)	DESCRIPTION
NAME	NO.			
V_{SS}	A5	GND		Ground pins
	A6			
	A7			
	A8			
	A10			
	A12			
	B6			
	B7			
	B9			
	C4			
	C7			
	C9			
	F3			
	F7			
	G6			
	G8			
	K4			
V_{SSRTC}	G12	GND	See Section 5.3, *Recommended Operating Conditions*	Ground for RTC oscillator. When using a 32.768-kHz crystal, this pin is a local ground for the crystal and must not be connected to the board ground (See Figure 5-6 and Figure 5-7). When not using RTC and the crystal is not populated on the board, this pin is connected to the board ground.
V_{SSA_PLL}	E8	GND	See Section 5.3, *Recommended Operating Conditions*	Analog PLL ground for the system clock generator
USB_V_{SSPLL}	L8	GND	See Section 5.3, *Recommended Operating Conditions*	USB analog PLL ground
USB_V_{SS1P3}	H6	GND	See Section 5.3, *Recommended Operating Conditions*	Digital core ground for USB PHY. Analog ground for USB PHY (for high speed sensitive analog circuits).

(1) I = Input, O = Output, Z = High impedance, S = Supply voltage, GND = Ground, A = Analog signal, BH = Bus-holder
(2) Input pins of type I, I/O, and I/O/Z are required to be driven at all times. To achieve the lowest power, these pins must not be allowed to float. When configured as input or high-impedance state, and not driven to a known state, they may cause an excessive I/O-supply current. If this is the case, enable IPD and IPU, if applicable, or externally terminate the pins.
(3) IPD = Internal pulldown, IPU = Internal pullup. For more detailed information on pullup and pulldown resistors and situations where external pullup and pulldown resistors are required, see Section 6.8.1, *Pullup and Pulldown Resistors*.
(4) Specifies the operating I/O supply voltage for each signal

Table 4-17. Ground Terminal Functions (continued)

SIGNAL		TYPE (1) (2)	OTHER (3) (4)	DESCRIPTION
NAME	NO.			
USB_V_{SSA3P3}	H7	GND	See Section 5.3, *Recommended Operating Conditions*	Analog ground for USB PHY
USB_V_{SSOSC}	M9	S	See Section 5.3, *Recommended Operating Conditions*	Ground for USB oscillator
USB_V_{SSREF}	H8	GND	See Section 5.3, *Recommended Operating Conditions*	Ground for reference current. This signal must be connected through a 10-kΩ ±1% resistor to USB_R1. When the USB peripheral is not used, the USB_V_{SSREF} signal must be connected directly to ground (V_{SS}).
V_{SSA_ANA}	H12 K12	0		Ground pins for power management (POR and Bandgap circuits) and 10-bit SAR ADC

5 Specifications

For the device maximum operating frequency, see Section 7.1, *Device and Development-Support Tool Nomenclature*.

5.1 Absolute Maximum Ratings (1)

over operating free-air temperature range (unless otherwise noted)

		VALUE	UNIT
Supply voltage	Digital Core (CV_{DD}, CV_{DDRTC}, USB_V_{DD1P3})(2)	–0.5 to 1.7	V
	I/O, 1.8 V, 2.5 V, 2.75 V, 3.3 V (DV_{DDIO}, DV_{DDRTC}) 3.3 V USB supplies USB PHY (USB_V_{DDOSC}, USB_V_{DDPLL}, USB_V_{DDA3P3})(2)	–0.5 to 4.2	
	LDOI	–0.5 to 4.2	
	Analog, 1.3 V (V_{DDA_PLL}, USB_V_{DDA1P3}, V_{DDA_ANA})(2)	–0.5 to 1.7	
Input and Output voltage ranges:	V_I I/O, all pins with DV_{DDIO} or USB_V_{DDOSC} or USB_V_{DDPLL} or USB_V_{DDA3P3} as supply source	–0.5 to 4.2	V
	V_O I/O, all pins with DV_{DDIO} or USB_V_{DDOSC} or USB_V_{DDPLL}or USB_V_{DDA3P3} as supply source	–0.5 to 4.2	
	RTC_XI and RTC_XO	–0.5 to 1.7	
	V_I and V_O, GPAIN[3:1]	–0.5 to 1.7	
	V_O, BG_CAP	–0.5 to 1.7	
	USB_V_{BUS} Input	–0.5 to 5.5	
	ANA_LDOO, DSP_LDOO, and USB_LDOO	–0.5 to 1.7	
Operating case temperature, T_c	Commercial temperature (default)	–10 to 70	°C
	Industrial temperature	–40 to 85	°C
Storage temperature, T_{stg}		–65 to 150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to V_{SS}.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±1000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±250	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 500-V HBM is possible with the necessary precautions. Pins listed as ±1000 V may actually have higher performance.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 250-V CDM is possible with the necessary precautions. Pins listed as ±250 V may actually have higher performance.

5.3 Recommended Operating Conditions

				MIN	NOM	MAX	UNIT
Core Supplies	CV_{DD}	Supply voltage, Digital Core	60 MHz	0.998	1.05	1.15	V
			100 or 120 MHz	1.24	1.3	1.43	
	CV_{DDRTC}	Supply voltage, RTC and RTC OSC	32.768 kHz	0.998		1.43	
	USB_V_{DD1P3}	Supply voltage, Digital USB		1.24	1.3	1.43	
	USB_V_{DDA1P3}	Supply voltage, 1.3-V Analog USB		1.24	1.3	1.43	
	V_{DDA_ANA}	Supply voltage, 1.3-V SAR and Power Management		1.24	1.3	1.43	
	V_{DDA_PLL}	Supply voltage, System PLL		1.24	1.3	1.43	
	USB_V_{DDPLL}	Supply voltage, 3.3-V USB PLL		2.97	3.3	3.63	
I/O Supplies	DV_{DDIO} DV_{DDRTC}	Supply voltage, I/O, 3.3-V		2.97	3.3	3.63	V
		Supply voltage, I/O, 2.75-V		2.48	2.75	3.02	
		Supply voltage, I/O, 2.5-V		2.25	2.5	2.75	
		Supply voltage, I/O, 1.8-V		1.65	1.8	1.98	
	USB_V_{DDOSC}	Supply voltage, I/O, 3.3-V USB OSC		2.97	3.3	3.63	
	USB_V_{DDA3P3}	Supply voltage, I/O, 3.3-V Analog USB PHY		2.97	3.3	3.63	
	LDOI	Supply voltage, Analog Power Management and LDO Inputs		1.75	1.8	1.85	
GND	V_{SS}	Supply ground, Digital I/O		0	0	0	V
	V_{SSRTC}	Supply ground, RTC					
	USB_V_{SSOSC}	Supply ground, USB OSC					
	USB_V_{SSPLL}	Supply ground, USB PLL					
	USB_V_{SSA3P3}	Supply ground, 3.3-V Analog USB PHY					
	USB_V_{SSREF}	Supply ground, USB Reference Current					
	V_{SSA_PLL}	Supply ground, System PLL					
	USB_V_{SS1P3}	Supply ground, 1.3-V Digital USB PHY					
	V_{SSA_ANA}	Supply ground, SAR and Power Management					
V_{IH} (1)		High-level input voltage, 3.3-, 2.75-, 2.5-, 1.8-V I/O (except GPAIN[3:1] pins) (2)		0.7 × DV_{DD}		DV_{DD} + 0.3	V
V_{IL} (1)		Low-level input voltage, 3.3-, 2.75-, 2.5-, 1.8-V I/O (except GPAIN[3:1] pins) (2)		–0.3		0.3 × DV_{DD}	V
V_{IN}		Input voltage, GPAIN[3:1] pins		–0.3		V_{DDA_ANA} + 0.3	V
T_c		Operating case temperature	Default (Commercial)	–10		70	°C
			Industrial	–40		85	°C
F_{SYSCLK}		DSP Operating Frequency (SYSCLK)	1.05-V	0		60	MHz
			1.3-V	0		100 or 120	

(1) DV_{DD} refers to the pin I/O supply voltage. To determine the I/O supply voltage for each pin, see Section 4.2, *Terminal Functions*.
(2) The I2C pins SDA and SCL do not feature fail-safe I/O buffers. These pins could potentially draw current when the DV_{DDIO} is powered down. Due to the fact that different voltage devices can be connected to I^2C bus and that the I^2C inputs are LVCMOS, the level of logic 0 (low) and logic 1 (high) are not fixed and depend on DV_{DDIO}.

5.4 Power Consumption Summary

NOTE

Power consumption on this device depends on several operating parameters such as operating voltage, operating frequency, and temperature. Power consumption also varies by end applications that determine the overall processor, CPU, and peripheral activity. For more specific power consumption details, see Power Estimation and Power Consumption Summary for TMS320C5504/05/14/15/32/33/34/35/45. This document includes a spreadsheet for estimating power based on parameters that closely resemble the end application to generate a realistic estimate of power consumption on this device based on use-case and operating conditions.

5.5 Electrical Characteristics

Over Recommended Ranges of Supply Voltage and Operating Temperature (Unless Otherwise Noted)

PARAMETER		TEST CONDITIONS (1)	MIN	TYP	MAX	UNIT
V_{OH}	Full speed: USB_DN and USB_DP (2)		2.8		USB_V_{DDA3P3}	V
	High speed: USB_DN and USB_DP (2)		360		440	mV
	High-level output voltage, 3.3-, 2.75-, 2.5-, 1.8-V I/O (except GPAIN[3: 1] pins)	IO = I_{OH}	0.8 × DV_{DD}			V
	High-level output voltage, GPAIN[3:1] pins	IO = I_{OH}	0.8 × V_{DDA_ANA}			
V_{OL}	Full speed: USB_DN and USB_DP (2)		0.0		0.3	V
	High speed: USB_DN and USB_DP (2)		–10		10	mV
	Low-level output voltage, 3.3-, 2.75-, 2.5-, 1.8-V I/O (except I2C and GPAIN[3:1] pins)	IO = I_{OL}			0.2 × DV_{DD}	V
	Low-level output voltage, I2C pins (3)	V_{DD} > 2 V, $I_{O\ L}$ = 3 mA	0		0.4	V
	Low-level output voltage, GPAIN[3:1] pins	IO = I_{OL}			0.2 × V_{DDA_ANA}	
V_{HYS}	Input hysteresis (4)	DV_{DD} = 3.3-V		162		mV
		DV_{DD} = 2.5-V		141		
		DV_{DD} = 1.8-V		122		
V_{LDO}	USB_LDOO voltage		1.24	1.3	1.43	V
	ANA_LDOO voltage		1.24	1.3	1.43	
	DSP_LDOO voltage	DSP_LDO_V bit in the LDOCNTL register = 1	1.24	1.3	1.43	
		DSP_LDO_V bit in the LDOCNTL register = 0	0.998	1.05	1.15	
I_{SD}	DSP_LDO shutdown current (5)	LDOI = V_{MIN}			250	mA
	ANA_LDO shutdown current (5)	LDOI = V_{MIN}			4	
	USB_LDO shutdown current (5)	LDOI = V_{MIN}			25	
I_{ILPU} (6)(7)	Input current [DC] (except I2C and GPAIN[3:1] pins)	Input only pin, internal pulldown or pullup disabled	–5		5	µA
		DV_{DD} = 3.3 V with internal pullup enabled (8)	–59		–161	
		DV_{DD} = 2.5 V with internal pullup enabled (8)	–31		–93	
		DV_{DD} = 1.8 V with internal pullup enabled (8)	–14		–44	
I_{IHPD} (6)(7)	Input current [DC] (except I2C and GPAIN[3:1] pins)	Input only pin, internal pulldown or pullup disabled	–5		5	
		DV_{DD} = 3.3 V with internal pulldown enabled (8)	52		158	
		DV_{DD} = 2.5 V with internal pulldown enabled (8)	27		83	
		DV_{DD} = 1.8 V with internal pulldown enabled (8)	11		35	
I_{IH}/ I_{IL} (7)	Input current [DC], ALL pins	V_I = V_{SS} to DV_{DD} with internal pullups and pulldowns disabled.	–5		5	

(1) For test conditions shown as MIN, MAX, or TYP, use the appropriate value specified in the recommended operating conditions table.
(2) The USB I/Os adhere to the universal bus specification revision 2.0 (USB 2.0 specifications).
(3) V_{DD} is the voltage to which the I2C bus pullup resistors are connected.
(4) Applies to all input pins except I2C pins, GPAIN[3:1], RTC_XI, and USB_MXI.
(5) I_{SD} is the amount of current the LDO is ensured to deliver before shutting down to protect itself.
(6) I_I applies to input-only pins and bidirectional pins. For input-only pins, I_I indicates the input leakage current. For bidirectional pins, I_I indicates the input leakage current and off-state (Hi-Z) output leakage current.
(7) When CV_{DD} power is ON, the pin bus-holders are disabled. For more detailed information, see Section 5.6.5.2, *Digital I/O Behavior When Core Power (CV_{DD}) is Down*.
(8) Applies only to pins with an internal pullup (IPU) or pulldown (IPD) resistor.

Electrical Characteristics *(continued)*

Over Recommended Ranges of Supply Voltage and Operating Temperature (Unless Otherwise Noted)

PARAMETER		TEST CONDITIONS (1)		MIN	TYP	MAX	UNIT
I_{OH} (7)	High-level output current [DC]	All Pins (except USB, CLKOUT, and GPAIN[3:1] pins)		–4			mA
		CLKOUT pin	DV_{DD} = 3.3 V	–6			
			DV_{DD} = 1.8 V	–4			
		GPAIN[3:1] pins	DV_{DD} = V_{DDA_ANA} = 1.3 V, external regulator (9)	–4			
			DV_{DD} = V_{DDA_ANA} = 1.3 V, internal regulator (9)	–100			µA
I_{OL} (7)	Low-level output current [DC]	All pins (except USB, CLKOUT, and GPAIN[3:1])				4	mA
		CLKOUT pin	DV_{DD} = 3.3 V			6	
			DV_{DD} = 1.8 V			4	
I_{OZ} (10)	I/O off-state output current	All pins (except USB and GPAIN[3:1])		–10		10	µA
		GPAIN [3:1] pins		–10		10	
I_{OLBH} (11)	Bus-holder pull low current when CV_{DD} is powered off	Supply voltage, I/O, 3.3-V				2.2	mA
		Supply voltage, I/O, 2.75-V				1.6	
		Supply voltage, I/O, 2.5-V				1.4	
		Supply voltage, I/O, 1.8-V				0.72	
I_{OHBH} (11)	Bus-holder pull high current when CV_{DD} is powered off	Supply voltage, I/O, 3.3-V		–1.3			
		Supply voltage, I/O, 2.75-V		–0.97			
		Supply voltage, I/O, 2.5-V		–0.83			
		Supply voltage, I/O, 1.8-V		–0.46			
I	Analog PLL (V_{DDA_PLL}) supply current	V_{DDA_PLL} = 1.3 V Room temp (25°C), Phase detector = 170 kHz, VCO = 100 MHz			0.7		mA
I	SAR Analog (V_{DDA_ANA}) supply current	V_{DDA_ANA} = 1.3 V, SAR clock = 2 MHz, Temp (70 °C)				1	mA
C_I	Input capacitance					4	pF
C_o	Output capacitance					4	pF

(9) When the ANA_LDO supplies V_{DDA_ANA}, it is not recommended to use the GPAIN[3:1] signals for general-purpose outputs (driving high). The I_{SD} parameter of the ANA_LDO is too low to drive any realistic load on the GPAIN[3:1] pins while also supplying the PLL through V_{DDA_PLL} and the SAR through V_{DDA_ANA} .
(10) I_{OZ} applies to output-only pins, indicating off-state (Hi-Z) output leakage current.
(11) This parameter specifies the maximum strength of the bus-holder and is needed to calculate the minimum strength of external pullups and pulldowns.

Table 5-1. Thermal Resistance Characteristics (PBGA Package) [ZQW]

NAME	DESCRIPTION	VELOCITY (m/s) (1)	1S0P	2S2P
Θ_{JA} (°C/W) (2)	Junction-to-free air	0	74.21	39.53
		1	58.98	34.82
		2	51.54	32.75
		3	45.27	30.66
Psi $_{JT}$ (°C/W)	Junction-to-package top	0	0.33	0.15
		1	0.59	0.38
		2	1.04	0.68
		3	1.90	1.30

(1) m/s = meters per second
(2) These measurements were conducted in a JEDEC-defined 1S0P/2S2P system and will change based on environment as well as application. For more information, see these EIA/JEDEC standards – EIA/JESD51-2, *Integrated Circuits Thermal Test Method Environment Conditions - Natural Convection (Still Air)* and JESD51-7, *High Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages*.

Table 5-1. Thermal Resistance Characteristics (PBGA Package) [ZQW] (continued)

NAME	DESCRIPTION	VELOCITY (m/s)(1)	1S0P	2S2P
Psi $_{JB}$ (°C/W)	Junction-to-board	0	15.28	16.28
		1	14.99	16.01
		2	14.45	15.69
		3	13.72	15.08
Θ_{JC} (°C/W)	Junction-to-case		11.12	N/A
Θ_{JB} (°C/W)	Junction-to-board		14.99	16.21

5.6 Timing and Switching Characteristics

5.6.1 Power Considerations

The device provides several means of managing power consumption.

To minimize power consumption, the device divides its circuits into eight main isolated supply domains:

- LDOI (LDOs and bandgap power supply)
- Analog POR, SAR, and PLL (V_{DDA_ANA} and V_{DDA_PLL})
- RTC Core (CV_{DDRTC})

NOTE

CV_{DDRTC} must always be powered by an external power source and none of the on-chip LDOs can be used to power CV_{DDRTC}.

- Digital Core (CV_{DD})
- USB Core (USB_ V_{DD1P3} and USB_V_{DDA1P3})
- USB PHY and USB PLL (USB_V_{DDOSC}, USB_V_{DDA3P3}, and USB_V_{DDPLL})
- RTC I/O (DV_{DDRTC})
- Rest of the I/O (DV_{DDIO})

5.6.1.1 LDO Configuration

The device includes low-dropout regulators (LDOs) that regulate the power supplies of the analog PLL and SAR ADC and power management (ANA_LDO), digital core (DSP_LDO), and USB core (USB_LDO).

A combination of pin configuration and register settings control these LDOs. For more detailed information see the following sections.

5.6.1.1.1 LDO Inputs

The LDOI pins (G10, L10, L11) provide power to the internal ANA_LDO, DSP_LDO, USB_LDO, the bandgap reference generator, and some I/O input pins, and range as specified for LDOI in Section 5.3, *Recommended Operating Conditions*. The bandgap provides accurate voltage and current references to the POR, LDOs, PLL, and SAR. Even if the LDO outputs are unused, power must always be applied to the LDOI pins .

5.6.1.1.2 LDO Outputs

The ANA_LDOO pin (H11) is the output of the internal ANA_LDO and can provide regulated 1.3 V power of up to 4 mA. On the board, the ANA_LDOO pin is intended to be connected to the V_{DDA_ANA} and V_{DDA_PLL} pins to provide a regulated 1.3 V to the 10-bit SAR ADC, Power Management Circuits, and System PLL. TI recommends powering V_{DDA_ANA} and V_{DDA_PLL} by this LDO output to take advantage of the device's power management techniques or by an external power supply. The ANA_LDO cannot be disabled individually (see Section 5.6.1.1.3, *LDO Control*).

The DSP_LDOO pin (M11) is the output of the internal DSP_LDO and provides software-selectable regulated 1.3 V or regulated 1.05 V power of up to 250 mA. On the board, TI intends the DSP_LDOO pin to connect to the CV_{DD} pins. In this configuration, the $\overline{\text{DSP\_LDO\_EN}}$ pin must be tied to the board V_{SS}, enabling DSP_LDO. Optionally, the CV_{DD} pins may be powered by an external power supply; the $\overline{\text{DSP\_LDO\_EN}}$ pin must be tied (high) to LDOI, disabling DSP_LDO. The $\overline{\text{DSP\_LDO\_EN}}$ pin also affects how reset is generated to the chip (for more details, see the $\overline{\text{DSP\_LDO\_EN}}$ pin description in Table 4-14). When DSP_LDO is disabled, its output pin is in a high-impedance state.

NOTE

$\overline{\text{DSP\_LDO\_EN}}$ is not intended to be changed dynamically.

When DSP_LDO comes out of reset, it is enabled to 1.3 V for the bootloader to operate.

The USB_LDOO pin (M10) is the output of the internal USB_LDO and provides regulated 1.3 V, software-switchable (on and off) power of up to 25 mA. On the board, TI intends the USB_LDOO pin to connect to the USB_V_{DD1P3} and USB_V_{DDA1P3} pins to provide power to portions of the USB. Optionally, the USB_V_{DD1P3} and USB_V_{DDA1P3} may be powered by an external power supply and the USB_LDO can be left disabled. When the USB_LDO is disabled, its output pin is in a high-impedance state.

5.6.1.1.3 LDO Control

All LDOs can be simultaneously disabled through software by writing to either the BG_PD bit or the LDO_PD bit in the RTCPMGT register (see Figure 5-1). When the LDOs are disabled through this mechanism, the only way to re-enable them is by an RTC alarm interrupt or by cycling power to the CV_{DDRTC} pin.

ANA_LDO: ANA_LDO is only disabled by the BG_PD and the LDO_PD mechanism described above. If not, ANA_LDO is always enabled.

DSP_LDO: DSP_LDO can be statically disabled by the $\overline{\text{DSP\_LDO\_EN}}$ pin as described in Section 5.6.1.1.2, *LDO Outputs*. DSP_LDO can be also dynamically disabled through the BG_PD and the LDO_PD mechanism described above. DSP_LDO can change its output voltage dynamically by software through the DSP_LDO_V bit in the LDOCNTL register (see Figure 5-2). The DSP_LDO output voltage is set to 1.3 V at reset.

USB_LDO: USB_LDO can be independently and dynamically enabled or disabled by software through the USB_LDO_EN bit in the LDOCNTL register (see Figure 5-2). USB _LDO is disabled at reset.

The RTCPMGT register is shown in Figure 5-1 and described in Table 5-2. The LDOCNTL register is shown in Figure 5-2 and described in Table 5-3.

Table 5-4 lists the ON and OFF control of each LDO and its register control bit configurations.

Figure 5-1. RTC Power Management Register (RTCPMGT) [1930h]

15						8
Reserved						
R-0						
7	5	4	3	2	1	0
Reserved		Reserved	Reserved	BG_PD	LDO_PD	Reserved
		R-0	R-0	R/W-0	R/W-0	R-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 5-2. RTCPMGT Register Bit Descriptions

BIT	NAME	DESCRIPTION
15:5	RESERVED	Reserved. Read-only, writes have no effect.
4	RESERVED	Reserved. For proper operation, default value cannot be changed.
3	RESERVED	Reserved. For proper operation, default value cannot be changed.
2	BG_PD	Bandgap, on-chip LDOs, and the analog POR power down bit This bit shuts down the on-chip LDOs (ANA_LDO, DSP_LDO, and USB_LDO), the analog POR, and bandgap reference. TI intends using BG_PD and LDO_PD only when the internal LDOs supply power to the chip. If the internal LDOs are bypassed and unused then the BG_PD and LDO_PD power down mechanisms should not be used because POR gets powered down and the POWERGOOD signal is not generated properly. After this bit is asserted, the on-chip LDOs, analog POR, and the Bandgap reference can be reenabled by the RTC alarm interrupt. The bandgap circuit will take about 100 msec to charge the external 0.1-µF capacitor through the internal 326-kΩ resistor. 0 = On-chip LDOs, analog POR, and bandgap reference are enabled. 1 = On-chip LDOs, analog POR, and bandgap reference are disabled (shutdown).
1	LDO_PD	On-chip LDOs and analog POR power down bit This bit shuts down the on-chip LDOs (ANA_LDO, DSP_LDO, and USB_LDO). TI intends using the analog POR. BG_PD and LDO_PD only when the internal LDOs supply power to the chip. If the internal LDOs are bypassed and not used then the BG_PD and LDO_PD power down mechanisms should not be used because POR gets powered down and the POWERGOOD signal is not generated properly. After this bit is asserted, the on-chip LDOs and analog POR can be re-enabled by the RTC alarm interrupt. This bit keeps the bandgap reference turned on to allow a faster wake-up time with the expense power consumption of the bandgap reference. 0 = On-chip LDOs and analog POR are enabled. 1 = On-chip LDOs and analog POR are disabled (shutdown).
0	RESERVED	Reserved. For proper operation, default value cannot be changed.

Figure 5-2. LDO Control Register (LDOCNTL) [7004h]

15	8
Reserved	
R-0	

7	2	1	0
Reserved		DSP_LDO_V	USB_LDO_EN
R-0		R/W-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; *-n* = value after reset

Table 5-3. LDOCNTL Register Bit Descriptions

BIT	NAME	DESCRIPTION
15:2	Reserved	Reserved. read-only, writes have no effect
1	DSP_LDO_V	DSP_LDO voltage select bit 0 = DSP_LDOO is regulated to 1.3 V. 1 = DSP_LDOO is regulated to 1.05 V
0	USB_LDO_EN	USB_LDO enable bit 0 = USB_LDO output is disabled. USB_LDOO pin is placed in high-impedance (Hi-Z) state. 1 = USB_LDO output is enabled. USB_LDOO is regulated to 1.3 V.

Table 5-4. LDO Controls Matrix

RTCPMGT REGISTER (1930h)		LDOCNTL REGISTER (7004h)	$\overline{\text{DSP\_LDO\_EN}}$ (PIN M12)	ANA_LDO	DSP_LDO	USB_LDO
BG_PD BIT	LDO_PD BIT	USB_LDO_EN BIT				
1	Don't Care	Don't Care	Don't Care	OFF	OFF	OFF
0	1	Don't Care	Don't Care	OFF	OFF	OFF
0	0	0	Low	ON	ON	OFF
0	0	0	High	ON	OFF	OFF
0	0	1	Low	ON	ON	ON

5.6.2 Clock Considerations

Used by the CPU and most of the DSP peripherals, the system clock is controlled by the system clock generator. The system clock generator features a software-programmable PLL multiplier and several dividers. The clock generator accepts an input reference clock from the CLKIN pin or the output clock of the 32.768-kHz real-time clock (RTC) oscillator. The selection of the input reference clock is based on the state of the CLK_SEL pin. The CLK_SEL pin is required to be statically tied high or low and cannot change dynamically after reset.

The DSP requires a reference clock for USB applications. The USB reference clock is generated using a dedicated on-chip oscillator with a 12-MHz external crystal connected to the USB_MXI and USB_MXO pins.

The USB reference clock is not required if the USB peripheral is unused. To completely disable the USB oscillator, connect the USB_MXI pin to ground (V_{SS}) and leave the USB_MXO pin unconnected. The USB oscillator power pins (USB_V_{DDOSC} and USB_V_{SSOSC}) should also be connected to ground.

The RTC oscillator generates a clock when a 32.768-kHz crystal is connected to the RTC_XI and RTC_XO pins. The 32.768-kHz crystal can be disabled if CLKIN is used as the clock source for the DSP. When the RTC oscillator is disabled, the RTC peripheral will not operate and the RTC registers (I/O address range 1900h to 197Fh) will not be accessible. To disable the RTC oscillator, connect the RTC_XI pin to CV_{DDRTC} and the RTC_XO pin to ground.

For more information on crystal specifications for the RTC oscillator and the USB oscillator, see Section 5.6.6, *External Clock Input From RTC_XI, CLKIN, and USB_MXI Pins*.

5.6.2.1 Clock Configurations After Device Reset

After reset, the on-chip bootloader programs the system clock generator based on the input clock selected through the CLK_SEL pin.

If CLK_SEL = 0, the bootloader programs the system clock generator and sets the system clock to 12.288 MHz (multiply the 32.768-kHz RTC oscillator clock by 375).

If CLK_SEL = 1, the bootloader bypasses the system clock generator altogether and the system clock is driven by the CLKIN pin. In this case, the CLKIN frequency is expected to be 11.2896 MHz, 12.000 MHz, or 12.288 MHz. While the bootloader tries to boot from the USB, the clock generator will be programmed to output approximately 36 MHz.

5.6.2.1.1 Device Clock Frequency

After the boot process is complete, reprogram the system clock generator to bring the device up to the desired clock frequency and the desired peripheral clock state (clock gating or not). Adhere to the clock requirements when programming the system clock generator. For more information, see Section 5.6.7, *Clock PLLs*.

NOTE

The on-chip bootloader allows for DSP registers to be configured during the boot process. Do not use this feature to change the output frequency of the system clock generator during the boot process. The bootloader also uses Timer0 to calculate the settling time of BG_CAP until executing bootloader code. The bootloader register modification feature must not modify the Timer0 registers.

5.6.2.1.2 Peripheral Clock State

The clock and reset state of each of peripheral is controlled through a set of system registers. The peripheral clock gating control registers (PCGCR1 and PCGCR2) enable and disable peripheral clocks. The peripheral software reset counter register (PSRCR) and the peripheral reset control register (PRCR) assert and deassert peripheral reset signals.

At hardware reset, all of the peripheral clocks are off to conserve power. After hardware reset, the DSP boots through the bootloader code in ROM. During the boot process, the bootloader queries each peripheral to determine if it can boot from that peripheral. In this process, the bootloader reads each peripheral searching for a valid boot image file. At that time, the individual peripheral clocks will be enabled for the query and then disabled again when the bootloader is finished with the peripheral. When the bootloader releases control to the user code, all peripheral clocks will be off and all domains in the ICR will be idled except for the CPU domain.

5.6.2.1.3 USB Oscillator Control

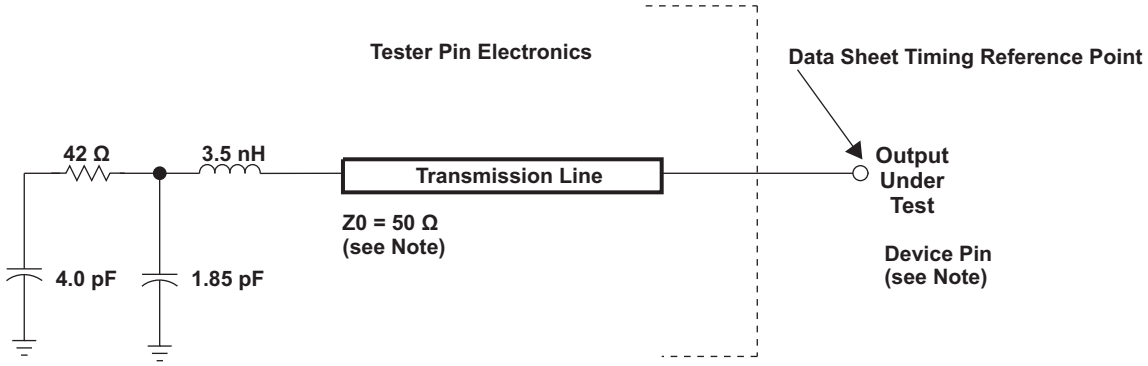
The USB system control register (USBSCR) controls the USB oscillator. To enable the oscillator, the USBOSCDIS and USBOSCBIASDIS bits must be cleared to 0. Wait until the USB oscillator stabilizes before proceeding with the USB configuration. The USB oscillator stabilization time is typically 100 μs, with a 10 ms maximum.

NOTE

The start-up time is dependent on the ESR and capacitive load on the crystal.

5.6.3 Parameter Information

Figure 5-3 shows the test load circuit for AC timing measurements.



NOTE: The data sheet provides timing at the device pin. For output timing analysis, the tester pin electronics and its transmission line effects must be taken into account. A transmission line with a delay of 2 ns can be used to produce the desired transmission line effect. The transmission line is intended as a load only. It is not necessary to add or subtract the transmission line delay (2 ns) from the data sheet timings.

Input requirements in this data sheet are tested with an input slew rate of < 4 Volts per nanosecond (4 V/ns) at the device pin.

Figure 5-3. 3.3-V Test Load Circuit for AC Timing Measurements

The load capacitance value stated is only for characterization and measurement of AC timing signals. This load capacitance value does not indicate the maximum load the device is capable of driving.

5.6.3.1 1.8-V, 2.5-V, 2.75-V, and 3.3-V Signal Transit n Levels

All rise and fall transition timing parameters are referenced to V_{IL} MAX and V_{IH} MIN for input clocks, V_{OL} MAX and V_{OH} MIN for output clocks.

Figure 5-4 shows the rise and fall transition time of the voltage reference levels.

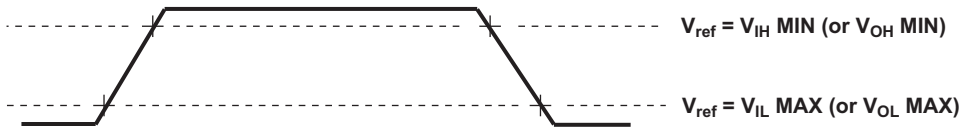


Figure 5-4. Rise and Fall Transition Time Voltage Reference Levels

5.6.3.2 3.3-V Signal Transition Rates

All timings are tested with an input edge rate of 4 volts per nanosecond (4 V/ns).

5.6.3.3 Timing Parameters and Board Routing Analysis

The timing parameter values specified in this data manual do not include delays by board routing. As a good practice, always take delays into account. Increase or decrease delays to adjust timing values. TI recommends using the available I/O buffer information specification (IBIS) models to analyze the timing characteristics correctly. To properly use IBIS models to attain accurate timing analysis for a given system, see *Using IBIS Models for Timing Analysis*. If needed, external logic hardware such as buffers may be used to compensate any timing differences.

5.6.4 Recommended Clock and Control Signal Transition Behavior

All clocks and control signals must transition between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.

5.6.5 Power Supplies

The device includes four core voltage-level supplies (CV_{DD}, CV_{DDRTC}, USB_V_{DD1P3}, USB_V_{DDA1P3}), and four I/O supplies (DV_{DDIO}, DV_{DDRTC} , USB_V_{DDOSC}, and USB_V_{DDA3P3}), as well as four analog supplies (LDOI, V_{DDA_PLL}, V_{DDA_ANA}, and USB_V_{DDPLL}). Some TI power-supply devices include features that facilitate power sequencing—for example, Auto-Track and Slow-Start and Enable features. For more information regarding TI's power management products and suggested devices to power TI DSPs, see www.ti.com/processorpower.

5.6.5.1 Power-Supply Sequencing

NOTE

The external reset signal on the $\overline{\text{RESET}}$ pin must be held low until all of the external power supplies reach their operating voltage conditions.

The device includes four core voltage-level supplies (CV_{DD}, CV_{DDRTC}, USB_V_{DD1P3}, USB_V_{DDA1P3}), and four I/O supplies (DV_{DDIO}, DV_{DDRTC}, USB_V_{DDOSC}, and USB_V_{DDA3P3}).

If the DSP_LDO is disabled ($\overline{\text{DSP\_LDO\_EN}}$ = high) and an external regulator supplies power to the CPU Core (CV_{DD}), the external reset signal ($\overline{\text{RESET}}$) must be held asserted until all of the supply voltages reach their valid operating ranges.

The I/O design allows either the core supplies (CV_{DD}, CV_{DDRTC} , USB_V_{DD1P3}, USB_V_{DDA1P3}) or the I/O supplies (DV_{DDIO}, DV_{DDRTC} , USB_V_{DDOSC}, and USB_V_{DDA3P3}) to be powered up for an indefinite period of time while the other supply is not powered if the following constraints are met:

1. All maximum ratings and recommended operating conditions are satisfied.
2. All warnings about exposure to maximum rated and recommended conditions, particularly junction temperature are satisfied. These apply to power transitions as well as normal operation.
3. Bus contention while core supplies are powered must be limited to 100 hours over the projected lifetime of the device.
4. Bus contention while core supplies are powered down does not violate the absolute maximum ratings.

If the USB subsystem is used, the subsystem must be powered up in the following sequence:

1. USB_V_{DDA1P3} and USB_V_{DD1P3}
2. USB_V_{DDA3P3}
3. USB_V_{BUS}

If the USB subsystem is unused, the following can be powered off:

- USB Core
  - USB_V_{DD1P3}
  - USB_V_{DDA1P3}
- USB PHY and I/O level supplies
  - USB_V_{DDOSC}
  - USB_V_{DDA3P3}
  - USB_V_{DDPLL}

A supply bus is powered up when the voltage is within the TI-recommended operating range. The supply bus is powered down when the voltage is below that range, either stable or while in transition.

5.6.5.2 Digital I/O Behavior When Core Power (CV_{DD}) is Down

With some exceptions, all digital I/O pins on the device have special features to allow powering down of the digital core domain (CV_{DD}) without causing I/O contentions or floating inputs at the pins (see Figure 5-5). The device asserts the internal signal called HHV high when power has been removed from the digital core domain (CV_{DD}). Asserting the internal HHV signal causes the following conditions to occur in any order:

- All output pin strong drivers to go to the high-impedance (Hi-Z) state
- Weak bus-holders to be enabled to hold the pin at a valid high or low
- The internal pullups or pulldowns (IPUs and IPDs) on the I/O pins will be disabled

The exception pins that do not have this special feature are:

- Pins driven by the CV_{DDRTC} Power Domain [This power domain is Always On; therefore, the pins driven by CV_{DDRTC} do not need these special features]:
  - RTC_XI and RTC_XO
- USB Pins:
  - USB_DP, USB_DM, USB_R1, USB_VBUS, USB_MXI, and USB_MXO

NOTE

The USB oscillator consumes power when core voltage is removed. For more information, see TMS320C5545A Fixed-Point DSP Silicon Errata.

- Pins for the Analog Block:
  - GPAIN[3:1], $\overline{\text{DSP\_LDO\_EN}}$ and BG_CAP

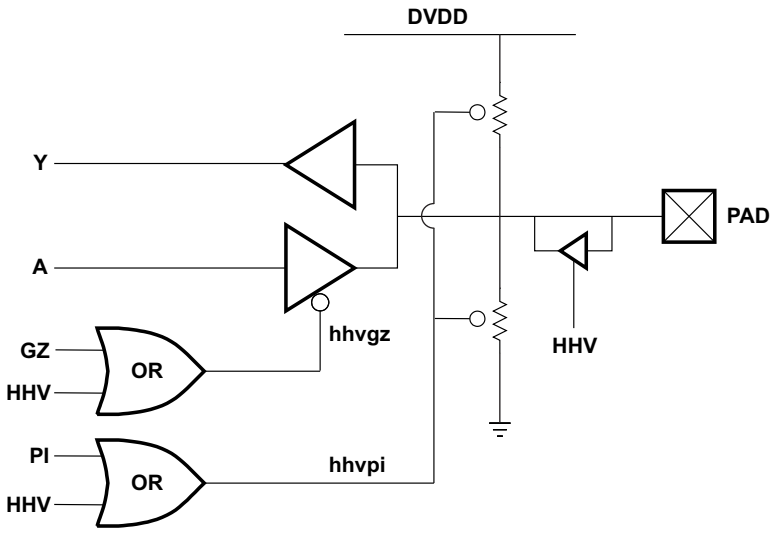


Figure 5-5. Bus-Holder I/O Circuit

NOTE

Figure 5-5 shows both a pullup and pulldown but pins have only one, not both.

PI = Pullup and pulldown Inhibit

GZ = Output enable (active low)

HHV = Described in Section 5.6.5.2

5.6.5.3 Power-Supply Design Considerations

Core and I/O supply voltage regulators should be located close to the DSP (or DSP array) to minimize inductance and resistance in the power delivery path. When designing for high-performance applications using the device, the PC board should include separate power planes for core, I/O, V_{DDA_ANA} and V_{DDA_PLL} (which can share the same PCB power plane), and ground; all bypassed with high–quality low–ESL and ESR capacitors.

5.6.5.4 Power-Supply Decoupling

To properly decouple the supply planes from system noise, place capacitors (caps) as close as possible to the device. These caps should be no more than 1.25 cm maximum distance from the device power pins to be effective. Physically smaller caps, like 0402, are better but must be evaluated from a yield and manufacturing point-of-view. Parasitic inductance limits the effectiveness of the decoupling capacitors; physically smaller capacitors must be used while maintaining the largest available capacitance value.

Larger caps for each supply can be placed further away for bulk decoupling. Large bulk caps (on the order of 10 μF) should be furthest away, but still as close as possible. Large caps for each supply should be placed outside of the BGA footprint.

As with the selection of any component, verification of capacitor availability over the product's production lifetime must be considered.

The recommended decoupling capacitance for the DSP core supplies should be 1 μF in parallel with 0.01-μF capacitor per supply pin.

5.6.5.5 LDO Input Decoupling

The LDO inputs should follow the same decoupling guidelines as other power-supply pins.

5.6.5.6 LDO Output Decoupling

The LDO circuits implement a voltage feedback control system which TI has designed to optimize gain and stability tradeoffs. Design assumptions exist for the amount of capacitance on the LDO outputs. For proper device operation, the following external decoupling capacitors must be used when the on-chip LDOs are enabled:

- ANA_LDOO– 1 μF
- DSP_LDOO – 5 μF to 10 μF
- USB_LDOO – 1 μF to 2 μF

5.6.6 External Clock Input From RTC_XI, CLKIN, and USB_MXI Pins

The device DSP includes two options to provide an external clock input to the system clock generator:

- Use the on-chip RTC oscillator with an external 32.768-kHz crystal connected to the RTC_XI and RTC_XO pins.
- Use an external 11.2896-, 12.0-, or 12.288-MHz LVCMOS clock input fed into the CLKIN pin that operates at the same voltage as the DV_{DDIO} supply (1.8-, 2.5-, 2.75-, or 3.3-V).

The CLK_SEL pin determines which input is used as the clock source for the system clock generator. For more details, see Section 6.5.1, *Device and Peripheral Configurations at Device Reset*. The crystal for the RTC oscillator is not required if CLKIN is used as the system reference clock but the RTC must still be powered by an external power source. None of the on-chip LDOs can power CV_{DDRTC}. The RTC registers starting at I/O address 1900h will be inaccessible without an RTC clock. Section 5.6.6.1, *Real-Time Clock (RTC) On-Chip Oscillator With External Crystal* provides more details on using the RTC on-chip oscillator with an external crystal. Section 5.6.6.2, *CLKIN Pin With LVCMOS-Compatible Clock Input* provides details on using an external LVCMOS-compatible clock input fed into the CLKIN pin.

The USB requires a reference clock generated using a dedicated on-chip oscillator with a 12-MHz external crystal connected to the USB_MXI and USB_MXO pins. The USB reference clock is not required if the USB peripheral is unused. Section 5.6.6.3, *USB On-Chip Oscillator With External Crystal* provides details on using the USB on-chip oscillator with an external crystal.

5.6.6.1 Real-Time Clock (RTC) On-Chip Oscillator With External Crystal

The on-chip oscillator requires an external 32.768-kHz crystal connected across the RTC_XI and RTC_XO pins, along with two load capacitors, as shown in Figure 5-6. The external crystal load capacitors must be connected only to the RTC oscillator ground pin (V_{SSRTC}). Do not connect to board ground (V_{SS}). Position the V_{SS} lead on the board between RTC_XI and RTC_XO as a shield to reduce direct capacitance between RTC_XI and RTC_XO leads on the board. The CV_{DDRTC} pin can be connected to the same power supply as CV_{DD} , or may be connected to a different supply that meets the recommended operating conditions (see Section 5.3, *Recommended Operating Conditions*), if desired. However, the CV_{DDRTC} pin must not be supplied by any on-chip LDOs.

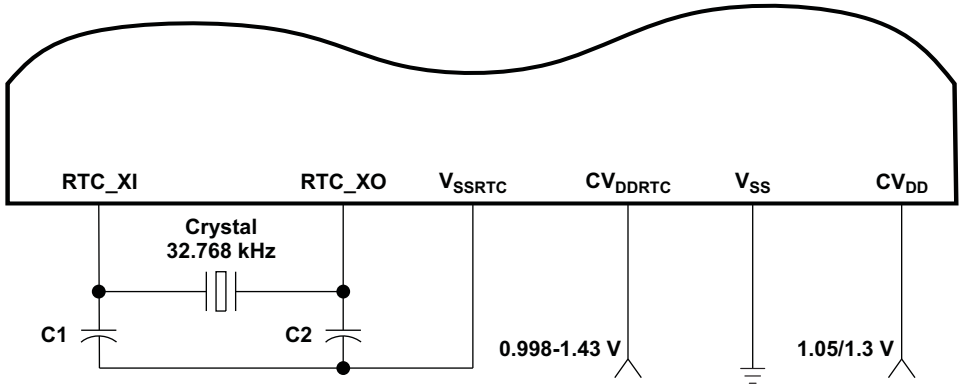


Figure 5-6. 32.768-kHz RTC Oscillator

The crystal should be in fundamental-mode function, and parallel resonant, with a maximum effective series resistance (ESR) specified in Table 5-5. The load capacitors, C1 and C2, are the total capacitance of the circuit board and components, excluding the IC and crystal. The load capacitors values are usually approximately twice the value of the load capacitance (CL) of the crystal, specified in the crystal manufacturer's data sheet and should be chosen to satisfy the equation.

$$C_L = \frac{C_1 C_2}{(C_1 + C_2)}$$

All discrete components used to implement the oscillator circuit must be placed as close as possible to the associated oscillator pins (RTC_XI and RTC_XO) and to the V_{SSRTC} pin.

Table 5-5. Input Requirements for Crystal on the 32.768-kHz RTC Oscillator

PARAMETER	MIN	NOM	MAX	UNIT
Start-up time (from power up until oscillating at stable frequency of 32.768-kHz)(1)	0.2		2	sec
Oscillation frequency		32.768		kHz
ESR			100	kΩ
Maximum shunt capacitance			1.6	pF
Maximum crystal drive			1.0	µW

(1) The start-up time is highly dependent on the ESR and the capacitive load of the crystal.

5.6.6.2 CLKIN Pin With LVCMOS-Compatible Clock Input (Optional)

NOTE

If CLKIN is not used, the pin must be tied low.

A LVCMOS-compatible clock input of a frequency less than 24 MHz can be fed into the CLKIN pin for use by the DSP system clock generator. The external connections are shown in Figure 5-7 and Figure 5-8. The bootloader assumes that the CLKIN pin is connected to the LVCMOS-compatible clock source with a frequency of 11.2896-, 12.0-, or 12.288-MHz. These frequencies were selected to support boot mode peripheral speeds of 500 kHz for SPI and 400 kHz for I2C and UART. These clock frequencies are achieved by dividing the CLKIN value by 25 for SPI and by 32 for I2C and UART. If a faster external clock is input, then these boot modes will run at faster clock speeds. If the system design uses faster peripherals or these boot modes are not used, CLKIN values higher than 12.288 MHz can be used.

NOTE

The CLKIN pin operates at the same voltage as the DV_{DDIO} supply (1.8-, 2.5-, 2.75-, or 3.3-V).

In this configuration the RTC oscillator can be optionally disabled by connecting RTC_XI to CV_{DDRTC} and RTC_XO to ground (V_{SS}). However, when the RTC oscillator is disabled the RTC registers starting at I/O address 1900h will not be accessible.

NOTE

The RTC core must still be powered by an external power source even if the RTC oscillator is disabled. None of the on-chip LDOs can power CV_{DDRTC}.

For more details on the RTC on-chip oscillator, see Section 5.6.6.1, *Real-Time Clock (RTC) On-Chip Oscillator With External Crystal*.

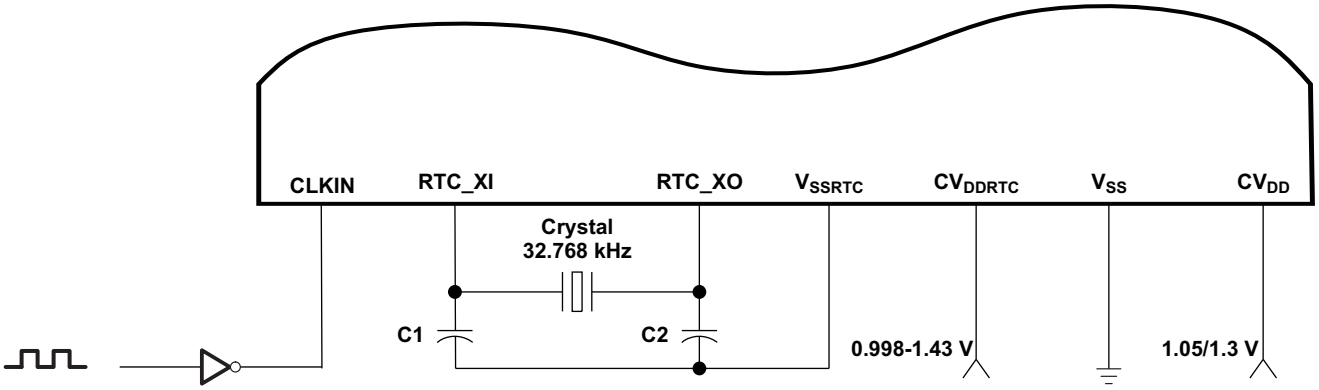


Figure 5-7. LVCMOS-Compatible Clock Input With RTC Oscillator Enabled

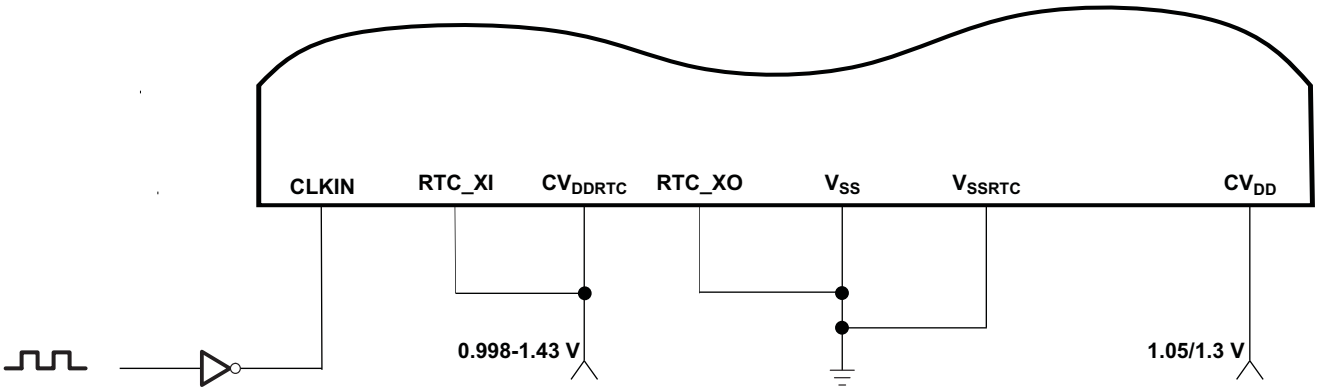


Figure 5-8. LVCMOS-Compatible Clock Input With RTC Oscillator Disabled

5.6.6.3 USB On-Chip Oscillator With External Crystal (Optional)

When using the USB, the USB on-chip oscillator requires an external 12-MHz crystal connected across the USB_MXI and USB_MXO pins, along with two load capacitors, as shown in Figure 5-9. The external crystal load capacitors must be connected only to the USB oscillator ground pin (USB_V_{SSOSC}). Do not connect to board ground (V_{SS}). The USB_V_{DDOSC} pin can be connected to the same power supply as USB_V_{DDA3P3}.

The USB on-chip oscillator can be permanently disabled, through tie-offs, if the USB peripheral is unused. To permanently disable the USB oscillator, connect the USB_MXI pin to ground (V_{SS}) and leave the USB_MXO pin unconnected. The USB oscillator power pins (USB_V_{DDOSC} and USB_V_{SSOSC}) should also be connected to ground, as shown in Figure 5-10.

When using an external 12-MHz oscillator, the external oscillator clock signal must be connected to the USB_MXI pin and the amplitude of the oscillator clock signal must meet the V_{IH} requirement (see Section 5.3, *Recommended Operating Conditions*). The USB_MXO remains unconnected and the USB_V_{SSOSC} signal is connected to board ground (V_{SS}).

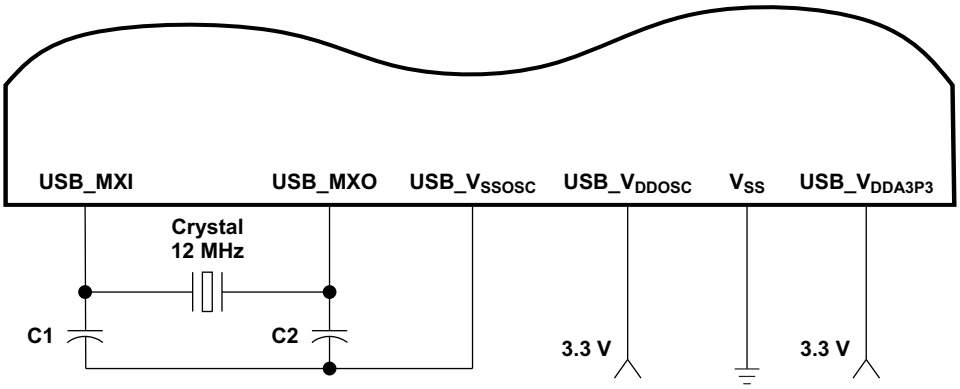


Figure 5-9. 12-MHz USB Oscillator

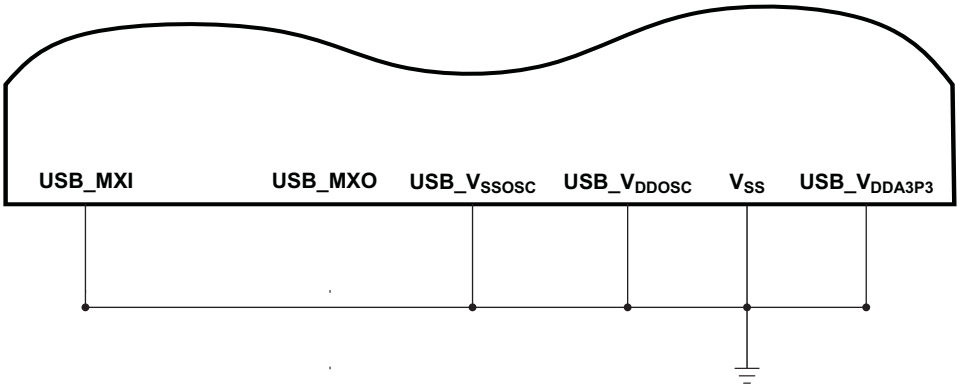


Figure 5-10. Connections When USB Oscillator is Permanently Disabled

The crystal should be in fundamental-mode operation and parallel resonant, with a maximum effective series resistance (ESR) specified in Table 5-6. The load capacitors, C1 and C2 are the total capacitance of the circuit board and components, excluding the IC and crystal. The load capacitor value is usually approximately twice the value of the load capacitance (CL) of the crystal, specified in the crystal manufacturer's data sheet and should be chosen such that the equation below is satisfied. All discrete components used to implement the oscillator circuit should be placed as close as possible to the associated oscillator pins (USB_MXI and USB_MXO) and to the USB_V_{SSOSC} pin.

$$C_L = \frac{C_1 C_2}{(C_1 + C_2)} \quad (1)$$

Table 5-6. Input Requirements for Crystal on the 12-MHz USB Oscillator

PARAMETER	MIN	NOM	MAX	UNIT
Start-up time (from power up until oscillating at stable frequency of 12 MHz)(1)		0.100	10	ms
Oscillation frequency		12		MHz
ESR			100	Ω
Frequency stability (2)			±100	ppm
Maximum shunt capacitance			5	pF
Maximum crystal drive			330	μW

(1) The start-up time is highly dependent on the ESR and the capacitive load of the crystal.
(2) If the USB is used, a 12-MHz, ±100-ppm crystal is recommended.

5.6.7 Clock PLLs

The DSP uses a software-programmable PLL to generate frequencies required by the CPU, DMA, and peripherals. The reference clock for the PLL is taken from either the CLKIN pin or the RTC on-chip oscillator (specified through the CLK_SEL pin).

5.6.7.1 PLL Device-Specific Information

Table 5-7 lists the PLL clock frequency ranges.

Table 5-7. PLL Clock Frequency Ranges

CLOCK SIGNAL NAME	CV_{DD} = 1.05 V V_{DDA_PLL} = 1.3 V		CV_{DD} = 1.3 V V_{DDA_PLL} = 1.3 V		UNIT
	MIN	MAX	MIN	MAX	
CLKIN(1)		11.2896 12 12.288		11.2896 12 12.288	MHz
RTC Clock		32.768		32.768	kHz
PLLIN	32.768	170	32.768	170	kHz
PLLOUT	60	120	60	120	MHz
SYSCLK	0.032768	60	0.032768	100 or 120	MHz
PLL_LOCKTIME		4		4	ms

(1) These CLKIN values are used when the CLK_SEL pin = 1.

Follow the lock time requirements for the PLL. The PLL lock time is the amount of time needed for the PLL to complete its phase-locking sequence.

5.6.7.2 Clock PLL Considerations With External Clock Sources

If the CLKIN pin provides the reference clock to the PLL, a single clean power supply should power both the device and the external clock oscillator circuit to minimize the clock jitter. Observe the minimum CLKIN rise and fall times. For the input clock timing requirements, see Section 5.6.7.3, *Clock PLL Electrical Data and Timing (Input and Output Clocks)*.

Rise and fall times, duty cycles (high and low pulse durations), and the load capacitance of the external clock source must meet the device requirements in this data manual (see Section 5.5, *Electrical Characteristics Over Recommended Ranges of Supply Voltage and Operating Temperature*, and Section 5.6.7.3, *Clock PLL Electrical Data and Timing (Input and Output Clocks)*.

5.6.7.3 Clock PLL Electrical Data and Timing (Input and Output Clocks)

Table 5-8 and Table 5-9 list the timing and switching requirements for CLKIN and CLKOUT, respectively.

Table 5-8. Timing Requirements for CLKIN(1) (2) (see Figure 5-11)

NO.			CV_{DD} = 1.05 V			CV_{DD} = 1.3 V			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
1	$t_{c(CLKIN)}$	Cycle time, external clock driven on CLKIN		88.577, 83.333, or 81.380			88.577, 83.333, or 81.380		ns
2	$t_{w(CLKINH)}$	Pulse width, CLKIN high	0.466 × $t_{c(CLKIN)}$			0.466 × $t_{c(CLKIN)}$			ns
3	$t_{w(CLKINL)}$	Pulse width, CLKIN low	0.466 × $t_{c(CLKIN)}$			0.466 × $t_{c(CLKIN)}$			ns
4	$t_{t(CLKIN)}$	Transition time, CLKIN			4			4	ns

(1) The CLKIN frequency and PLL multiply factor must be chosen so that the resulting clock frequency is within the specific range for CPU operating frequency.
(2) The reference points for the rise and fall transitions are measured at V_{IL} MAX and V_{IH} MIN.

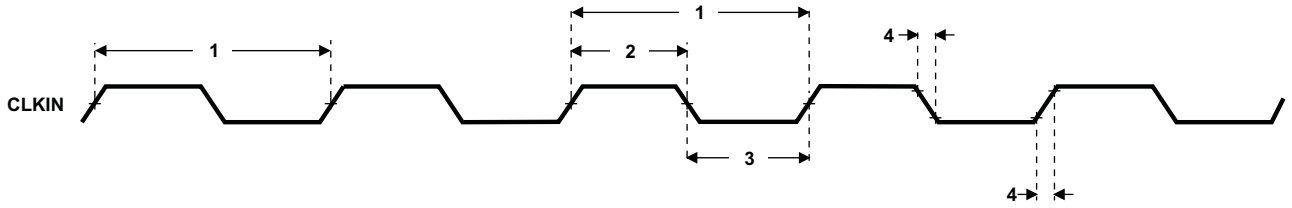


Figure 5-11. CLKIN Timing

Table 5-9. Switching Characteristics Over Recommended Operating Conditions for CLKOUT(1) (2) (see Figure 5-12)

NO.	PARAMETER		CV_{DD} = 1.05 V V_{DDA_PLL} = 1.3 V		CV_{DD} = 1.3 V V_{DDA_PLL} = 1.3 V		UNIT
			MIN	MAX	MIN	MAX	
1	$t_{c(CLKOUT)}$	Cycle time, CLKOUT	16.67	P	8.33	P	ns
2	$t_{w(CLKOUTH)}$	Pulse duration, CLKOUT high	0.466 × $t_{c(CLKOUT)}$		0.466 × $t_{c(CLKOUT)}$		ns
3	$t_{w(CLKOUTL)}$	Pulse duration, CLKOUT low	0.466 × $t_{c(CLKOUT)}$		0.466 × $t_{c(CLKOUT)}$		ns
4	$t_{t(CLKOUTR)}$	Transition time (rise), CLKOUT(3)		5		5	ns
5	$t_{t(CLKOUTF)}$	Transition time (fall), CLKOUT(3)		5		5	ns

(1) The reference points for the rise and fall transitions are measured at V_{OL} MAX and V_{OH} MIN.
(2) P = 1/SYSCLK clock frequency in nanoseconds (ns). For example, when SYSCLK frequency is 100 MHz, use P = 10 ns.
(3) Transition time is measured with the slew rate set to FAST and DV_{DDIO} = 1.65 V. (For more detailed information, see the Section 6.6.6, *Output Slew Rate Control Register (OSRCR) [1C16h].*).

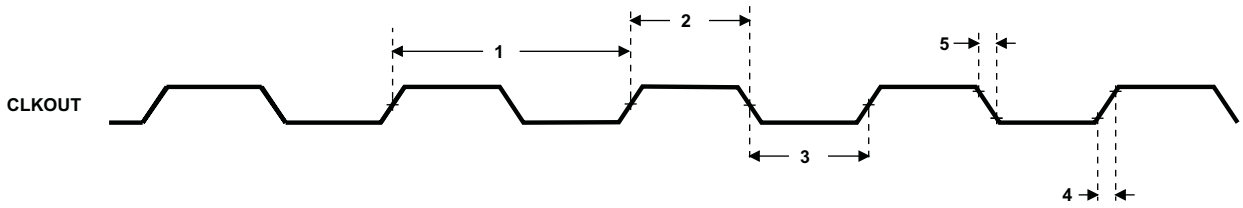


Figure 5-12. CLKOUT Timing

5.6.8 Direct Memory Access (DMA) Controller

The DMA controller moves data among internal memory, external memory, and peripherals without intervention from the CPU and in the background of CPU operation.

The DSP includes a total of four DMA controllers. Aside from the DSP resources they can access, all four DMA controllers are identical.

The DMA controller has the following features:

- Operation that is independent of the CPU.
- Four channels, which allow the DMA controller to keep track of the context of four independent block transfers.
- Event synchronization. DMA transfers in each channel can be made dependent on the occurrence of selected events.
- An interrupt for each channel. Each channel can send an interrupt to the CPU on completion of the programmed transfer.
- Ping-Pong mode allows the DMA controller to keep track of double-buffering context without CPU intervention.
- A dedicated clock idle domain. The four device DMA controllers can be put into a low-power state by independently turning off their input clocks.

5.6.8.1 DMA Channel Synchronization Events

The DMA controllers allow activity in their channels to be synchronized to selected events. The DSP supports 20 separate synchronization events and each channel can be tied to separate sync events independent of the other channels. Synchronization events are selected by programming the CHnEVT field in the DMAn channel event source registers (DMAnCESR1 and DMAnCESR2).

5.6.9 Reset

The device has two main types of reset: hardware reset and software reset.

Hardware reset is responsible for initializing all key states of the device. The hardware reset occurs whenever the RESET pin is asserted or when the internal power-on-reset (POR) circuit deasserts an internal signal called POWERGOOD. The device's internal POR is a voltage comparator that monitors the DSP_LDOO pin voltage and generates the internal POWERGOOD signal when the DSP_LDO is enabled externally by the DSP_LDO_EN pin. POWERGOOD is asserted when the DSP_LDOO voltage is above a minimum threshold voltage provided by the bandgap. When the DSP_LDO is disabled (DSP_LDO_EN is high), the internal voltage comparator becomes inactive, and the POWERGOOD signal logic level is immediately set high. The RESET pin and the POWERGOOD signal are internally combined with a logical AND gate to produce an (active low) hardware reset (see Figure 5-13 and Figure 5-14).

There are two types of software reset: the software reset instruction of the CPU and the software control of the peripheral reset signals. For more information on the software reset instruction of the CPU, see the *TMS320C55x CPU 3.0 CPU Reference Guide*. In all the device documentation, all references to reset refer to hardware reset. Any references to software reset will explicitly state software reset.

The device RTC has one additional type of reset, a power-on-reset (POR) for the registers in the RTC core. This POR monitors the voltage of CV_{DDRTC} and resets the RTC registers when power is first applied to the RTC core.

5.6.9.1 Power-On Reset (POR) Circuits

The device includes two power-on reset (POR) circuits, one for the RTC (RTC POR) and another for the rest of the chip (MAIN POR).

5.6.9.1.1 RTC Power-On Reset (POR)

The RTC POR ensures that the flip-flops in the CV_{DDRTC} power domain have an initial state upon power-up. In particular, the RTCNOPWR register is reset by this POR and is used to indicate that the RTC time registers must be initialized with the current time and date when power is first applied.

5.6.9.1.2 Main Power-On Reset (POR)

The device includes an analog power-on reset (POR) circuit that keeps the DSP in reset until specific voltages have reached predetermined levels. When the DSP_LDO is enabled externally by the DSP_LDO_EN pin, the output of the POR circuit, POWERGOOD, is held low until the following conditions are satisfied:

- LDOI is powered
- The bandgap is active for at least approximately 8 ms
- VDD_ANA is powered for at least approximately 4 ms
- DSP_LDOO is above approximately 950 mV

NOTE

The POR comparator has hysteresis, so the threshold voltage becomes approximately 850 mV after POWERGOOD signal is set high.

When these conditions are met, the internal POWERGOOD signal is set high. The POWERGOOD signal is internally combined with the RESET pin signal, through an AND-gate, to produce the DSP subsystem's global reset. This global reset is the hardware reset for the whole chip, except the RTC. When the global reset is deasserted (high), the boot sequence starts. For more detailed information on the boot sequence, see Section 6.4, *Boot Sequence*.

When the DSP_LDO is disabled (DSP_LDO_EN pin = 1), the voltage monitoring on the DSP_LDOO pin is deactivated and the POWERGOOD signal is immediately set high. The RESET pin will be the sole source of hardware reset.

5.6.9.1.3 Reset Pin (RESET)

The device can receive an external reset signal on the RESET pin. As specified in Section 5.6.9.1.2, *Main Power-On Reset*, the RESET pin is combined with the internal POWERGOOD signal, generated by the MAIN POR through an AND-gate. The output of the AND gate provides the hardware reset to the chip. The RESET pin may be tied high and the MAIN POR can provide the hardware reset in case DSP_LDO is enabled (DSP_LDO_EN = 0), but an external hardware reset must be provided through the RESET pin when the DSP_LDO is disabled (DSP_LDO_EN = 1).

When the hardware reset is applied, the system clock generator is enabled and the DSP starts the boot sequence. For more information on the boot sequence, see Section 6.4, *Boot Sequence*.

5.6.9.2 Pin Behavior at Reset

Pins are controlled by the respective peripheral selected in the external bus selection register (EBSR) register. During power-on reset and reset, the behavior of the output pins changes. These changes are categorized as follows:

- **High Group:** LCD_RS/SPI_CS3
- **Low Group:** LCD_EN_RDB/ SPI_CLK, SD0_CLK/I2S0_CLK/GP[0], SD1_CLK/I2S1_CLK/GP[6]
- **Z Group:** EMU[1:0], SCL, SDA, LCD_D[0]/SPI_RX, LCD_D[1]/ SPI_TX, LCD_D[10]/ I2S2_RX/GP[20]/SPI_RX, LCD_D[11]/I2S2_DX/GP[27]/SPI_TX, LCD_D[12]/UART_RTS/GP[28]/I2S3_CLK, LCD_D[13]/ UART_CTS/GP[29]/I2S3_FS,

  LCD_D[14]/UART_RXD/GP[30]/I2S3_RX, LCD_D[15]/UART_TXD/GP[31]/I2S3_DX, LCD_D[2]/ GP[12], LCD_D[3]/ GP[13], LCD_D[4]/ GP[14], LCD_D[5]/ GP[15], LCD_D[6]/ GP[16], LCD_D[7]/ GP[17], LCD_D[8]/ I2S2_CLK/GP[18]/SPI_CLK, LCD_D[9] I2S2_FS/GP[19]/SPI_CS0,

  SD0_CMD/I2S0_FS/GP[1], SD0_D0/I2S0_DX/GP[2], SD0_D1/I2S0_RX/GP[3], SD0_D2/GP[4], SD0_D3/GP[5], SD1_CMD/I2S1_FS/GP[7], SD1_D0/I2S1_DX/GP[8], SD1_D1/I2S1_RX/GP[9], SD1_D2/GP[10], SD1_D3/GP[11], TDO
- **CLKOUT Group:** CLKOUT
- **SYNCH 0→1 Group:** LCD_CS0_E0/SPI_CS0, LCD_RW_WRB/SPI_CS2

5.6.9.3 Reset Electrical Data and Timing

Table 5-10 lists the timing requirements for resets.

Table 5-10. Timing Requirements for Reset(1) (see Figure 5-13 and Figure 5-14)

NO.			CV_{DD} = 1.05 V		CV_{DD} = 1.3 V		UNIT
			MIN	MAX	MIN	MAX	
1	$t_{w(RSTL)}$	Pulse duration, $\overline{\text{RESET}}$ low	3P		3P		ns

(1) P = 1/SYSCLK clock frequency in ns. For example, if SYSCLK = 12 MHz, use P = 83.3 ns. In IDLE3 mode the system clock generator is bypassed and the SYSCLK frequency is equal to either CLKIN or the RTC clock frequency depending on CLK_SEL.

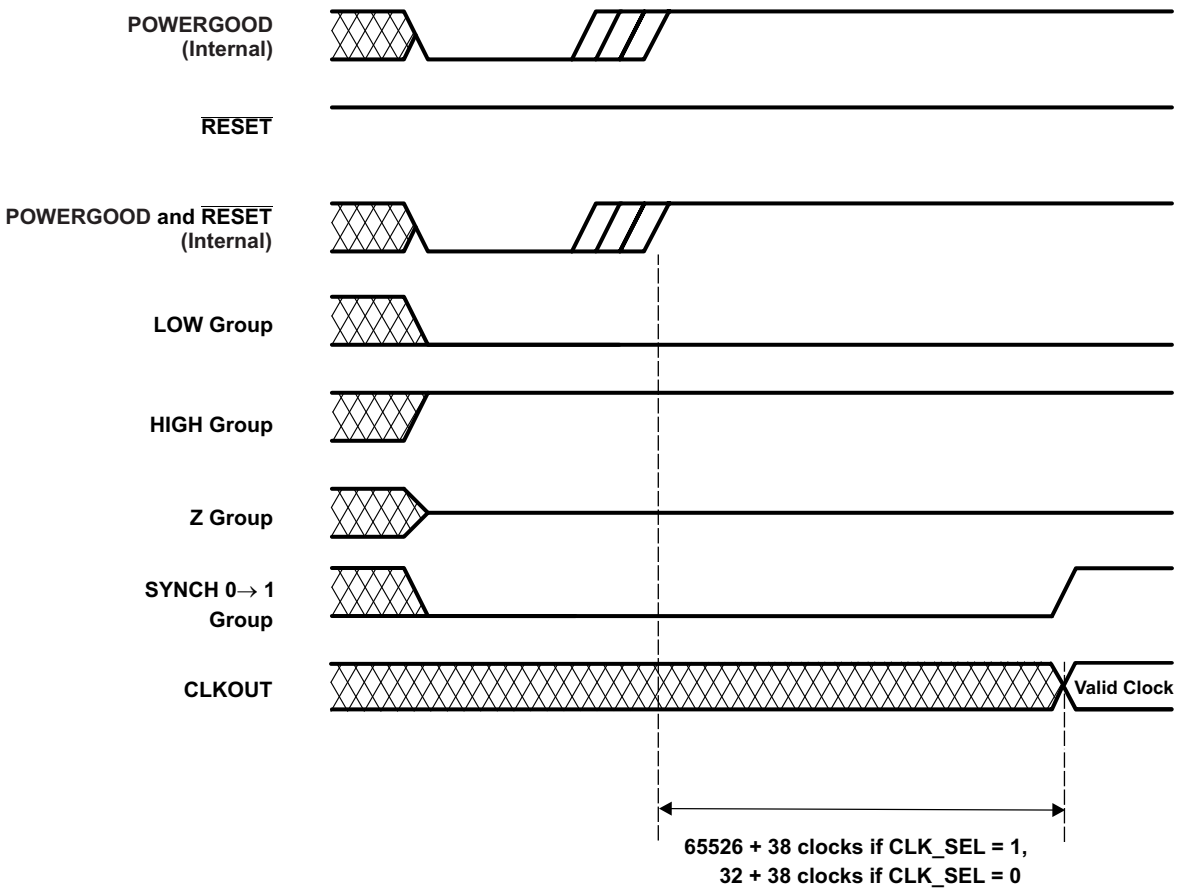


Figure 5-13. Power-On Reset Timing Requirements

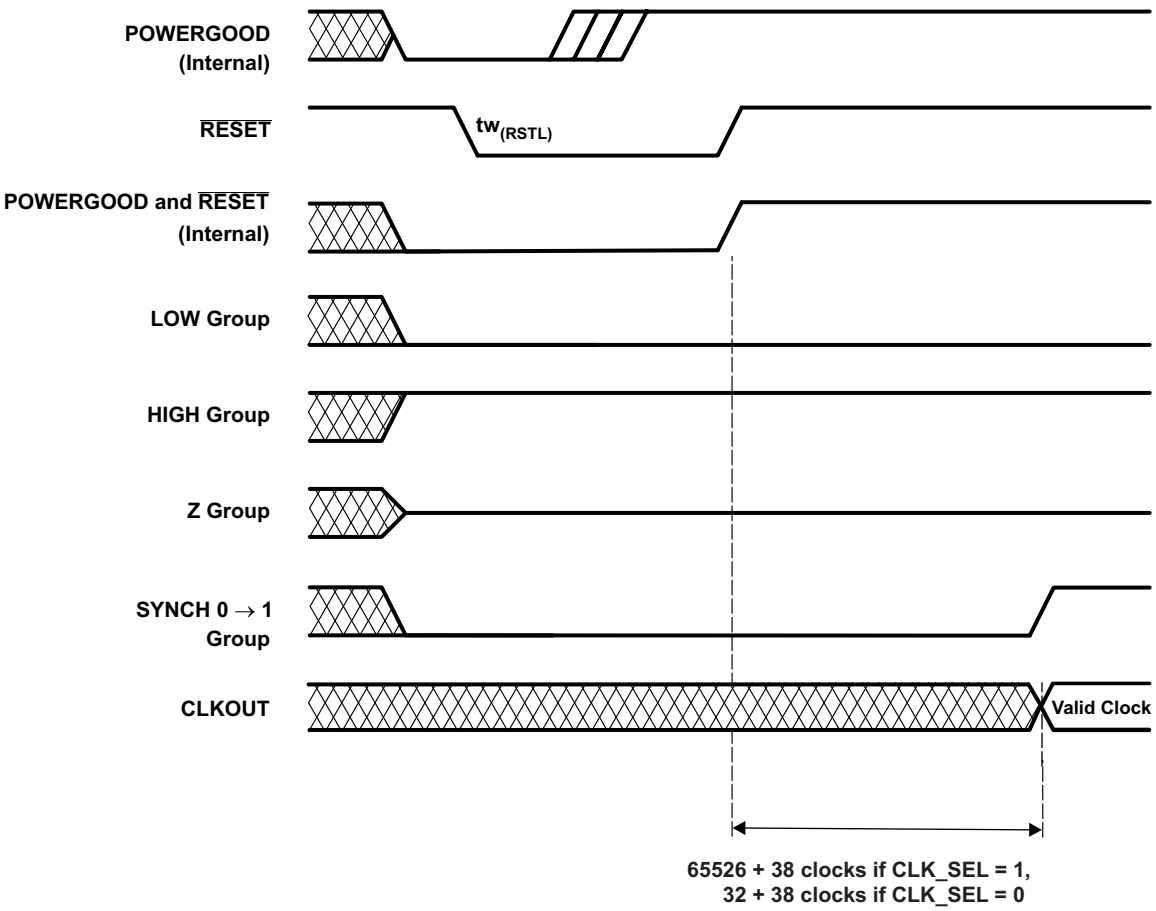


Figure 5-14. Reset Timing Requirements

5.6.10 Interrupts

The device has interrupts to service its peripherals. The interrupts can be selectively enabled or disabled.

5.6.10.1 Interrupts Electrical Data and Timing

Table 5-11 lists the timing requirements for interrupts.

Table 5-11. Timing Requirements for Interrupts(1) (see Figure 5-15)

NO.			CV_{DD} = 1.05 V CV_{DD} = 1.3 V		UNIT
			MIN	MAX	
1	$t_{w(INTH)}$	Pulse duration, interrupt high CPU active	2P		ns
2	$t_{w(INTL)}$	Pulse duration, interrupt low CPU active	2P		ns

(1) P = 1/SYSCLK clock frequency in ns. For example, when the CPU core is clocked at 100 MHz, use P = 10 ns. For example, when the CPU core is clocked at 120 MHz, use P = 8.3 ns.

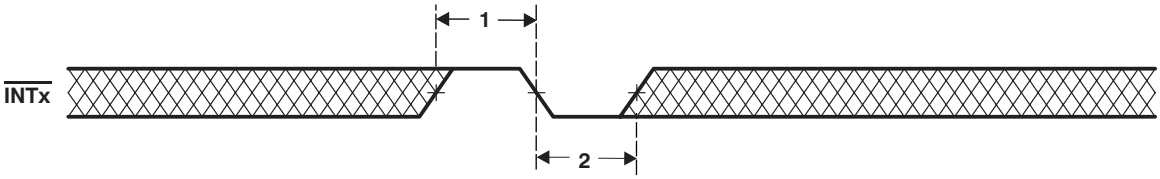


Figure 5-15. External Interrupt Timings

5.6.11 Secure Digital (SD)

The device includes two SD controllers that are compliant with Secure Digital Part 1 Physical Layer Specification V2.0 and Secure Digital Input Output (SDIO) V2.0 and eMMC V4.3 specifications. The SD card controller supports these industry standards and assumes the reader also supports these standards.

Each SD controller in the device has the following features:

- Embedded multimedia card and secure digital (eMMC, SD, HCSD, and HSSD) protocol support
- Programmable clock frequency
- 512-bit read and write FIFO to lower system overhead
- Slave DMA transfer capability

The SD card controller transfers data between the CPU and DMA controller on one side and the SD card on the other side. The CPU and DMA controller can read and write the data in the card by accessing the registers in the SD controller.

The SD controller on this device does not support the SPI mode of operation.

5.6.11.1 SD Peripheral Register Descriptions

Table 5-12 and Table 5-13 list the SD registers. The SD0 registers start at address 3A00h and the SD1 registers start at address 3B00h.

Table 5-12. SD0 Registers

HEX ADDRESS RANGE	ACRONYM	REGISTER NAME
3A00h	SDCTL	SD Control Register
3A04h	SDCLK	SD Memory Clock Control Register
3A08h	SDST0	SD Status Register 0
3A0Ch	SDST1	SD Status Register 1
3A10h	SDIM	SD Interrupt Mask Register
3A14h	SDTOR	SD Response Time-Out Register
3A18h	SDTOD	SD Data Read Time-Out Register
3A1Ch	SDBLEN	SD Block Length Register
3A20h	SDNBLK	SD Number of Blocks Register
3A24h	SDNBLC	SD Number of Blocks Counter Register
3A28h	SDDRR1	SD Data Receive 1 Register
3A29h	SDDRR2	SD Data Receive 2 Register
3A2Ch	SDDXR1	SD Data Transmit 1 Register
3A2Dh	SDDXR2	SD Data Transmit 2 Register
3A30h	SDCMD	SD Command Register
3A34h	SDARGHL	SD Argument Register
3A38h	SDRSP0	SD Response Register 0
3A39h	SDRSP1	SD Response Register 1
3A3Ch	SDRSP2	SD Response Register 2
3A3Dh	SDRSP3	SD Response Register 3
3A40h	SDRSP4	SD Response Register 4
3A41h	SDRSP5	SD Response Register 5
3A44h	SDRSP6	SD Response Register 6
3A45h	SDRSP7	SD Response Register 7
3A48h	SDDRSP	SD Data Response Register
3A50h	SDCIDX	SD Command Index Register
3A64h to 3A70h	–	Reserved
3A74h	SDFIFOCTL	SD FIFO Control Register

Table 5-13. SD1 Registers

HEX ADDRESS RANGE	ACRONYM	REGISTER NAME
3B00h	SDCTL	SD Control Register
3B04h	SDCLK	SD Memory Clock Control Register
3B08h	SDST0	SD Status Register 0
3B0Ch	SDST1	SD Status Register 1
3B10h	SDIM	SD Interrupt Mask Register
3B14h	SDTOR	SD Response Time-Out Register
3B18h	SDTOD	SD Data Read Time-Out Register
3B1Ch	SDBLEN	SD Block Length Register
3B20h	SDNBLK	SD Number of Blocks Register
3B24h	SDNBLC	SD Number of Blocks Counter Register
3B28h	SDDRR1	SD Data Receive 1 Register
3B29h	SDDRR2	SD Data Receive 2 Register
3B2Ch	SDDXR1	SD Data Transmit 1 Register
3B2Dh	SDDXR2	SD Data Transmit 2 Register
3B30h	SDCMD	SD Command Register
3B34h	SDARGHL	SD Argument Register
3B38h	SDRSP0	SD Response Register 0
3B39h	SDRSP1	SD Response Register 1
3B3Ch	SDRSP2	SD Response Register 2
3B3Dh	SDRSP3	SD Response Register 3
3B40h	SDRSP4	SD Response Register 4
3B41h	SDRSP5	SD Response Register 5
3B44h	SDRSP6	SD Response Register 6
3B45h	SDRSP7	SD Response Register 7
3B48h	SDDRSP	SD Data Response Register
3B50h	SDCIDX	SD Command Index Register
3B74h	SDFIFOCTL	SD FIFO Control Register

5.6.11.2 SD Electrical Data and Timing

Table 5-14 and Table 5-15 list the timing and switching requirements for SD, respectively.

Table 5-14. Timing Requirements for SD (see Figure 5-16, Figure 5-17, Figure 5-18, and Figure 5-19)

NO.			CV_{DD} = 1.3 V FAST MODE		CV_{DD} = 1.05 V STD MODE		UNIT
			MIN	MAX	MIN	MAX	
1	$t_{su(CMDV-CLKH)}$	Setup time, SDx_CMD data input valid before SDx_CLK high	3		3		ns
2	$t_{h(CLKH-CMDV)}$	Hold time, SDx_CMD data input valid after SDx_CLK high	3		3		ns
3	$t_{su(DATV-CLKH)}$	Setup time, SD_Dx data input valid before SDx_CLK high	3		3		ns
4	$t_{h(CLKH-DATV)}$	Hold time, SD_Dx data input valid after SDx_CLK high	3		3		ns

Table 5-15. Switching Characteristics Over Recommended Operating Conditions for SD Output(1) (see Figure 5-16, Figure 5-17, Figure 5-18, and Figure 5-19)

NO.	PARAMETER		CV_{DD} = 1.3 V FAST MODE		CV_{DD} = 1.05 V STD MODE		UNIT
			MIN	MAX	MIN	MAX	
7	$f_{(CLK)}$	Operating frequency, SDx_CLK	0	50(2)	0	25(2)	MHz
8	$f_{(CLK\_ID)}$	Identification mode frequency, SDx_CLK	0	400	0	400	kHz
9	$t_{w(CLKL)}$	Pulse width, SDx_CLK low	7		10		ns
10	$t_{w(CLKH)}$	Pulse width, SDx_CLK high	7		10		ns
11	$t_{r(CLK)}$	Rise time, SDx_CLK		3		3	ns
12	$t_{f(CLK)}$	Fall time, SDx_CLK		3		3	ns
13	$t_{d(MDCLKL-CMDIV)}$	Delay time, SDx_CLK low to SD_CMD data output invalid	–4		–4.1		ns
14	$t_{d(MDCLKL-CMDV)}$	Delay time, SDx_CLK low to SD_CMD data output valid		4		5.1	ns
15	$t_{d(MDCLKL-DATIV)}$	Delay time, SDx_CLK low to SD_Dx data output invalid	–4		–4.1		ns
16	$t_{d(MDCLKL-DATV)}$	Delay time, SDx_CLK low to SD_Dx data output valid		4		5.1	ns

(1) For SD, the parametric values are measured at DV_{DDIO} = 3.3 V and 2.75 V.
(2) Use this value or SYS_CLK/2 whichever is smaller.

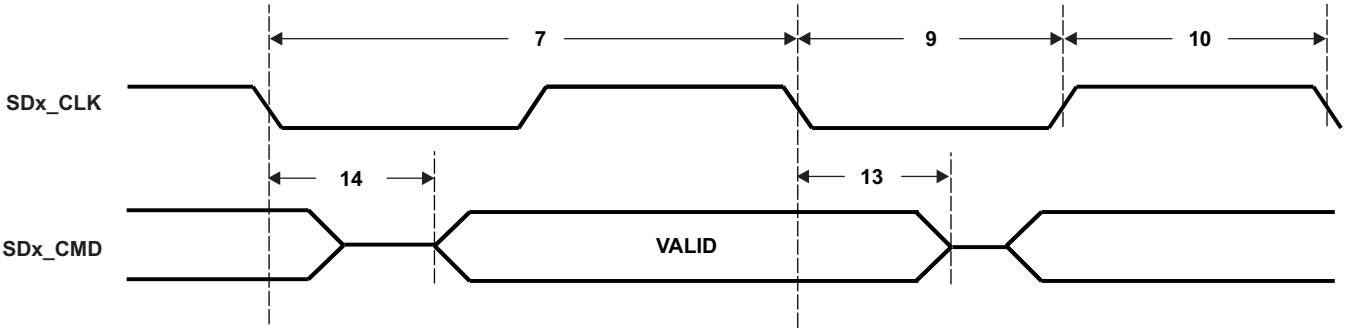


Figure 5-16. SD Host Command Write Timing

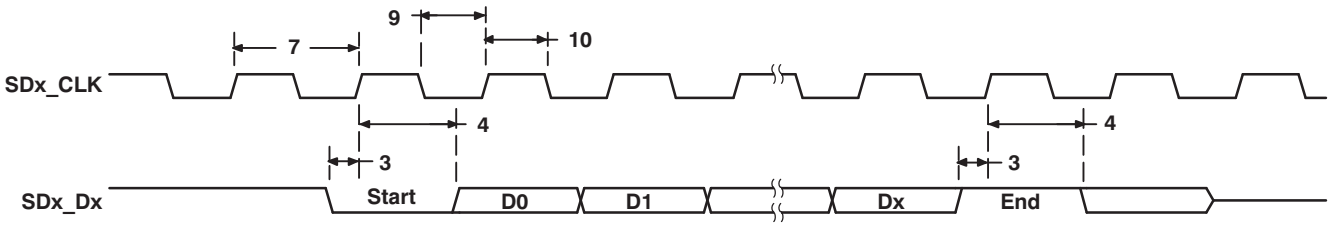


Figure 5-17. SD Card Response Timing

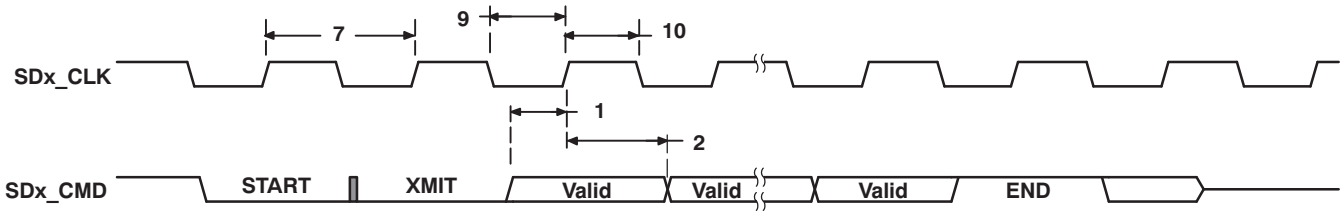


Figure 5-18. SD Host Write Timing

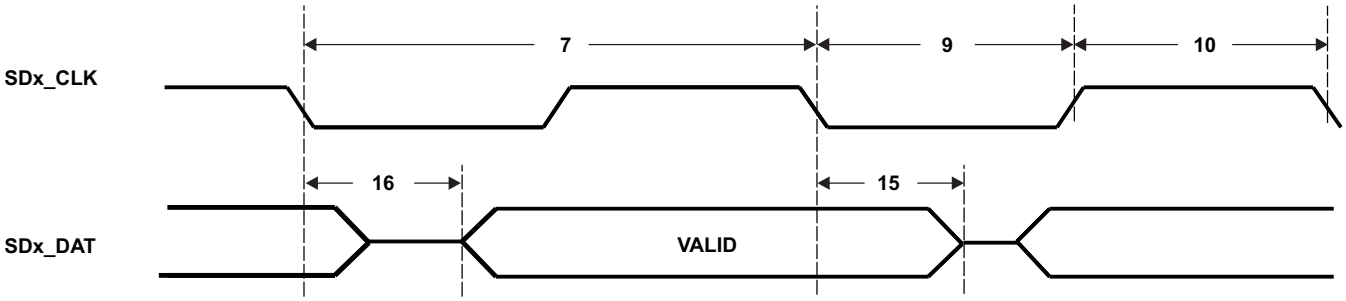


Figure 5-19. SD Data Write Timing

5.6.12 Real-Time Clock (RTC)

The device includes an RTC with its own separated power supply and isolation circuits. All RTC registers are preserved (except for RTC Control and RTC Update Registers) and the counter continues to operate when the device is powered off.

The RTC also has the capability to wake up the device from idle states through alarms and periodic interrupts.

NOTE

The RTC Core (CV_{DDRTC}) must be properly powered by an external power source even though RTC is not used. None of the on-chip LDOs can power CV_{DDRTC}.

The device RTC provides the following features:

- 100-year calendar up to year 2099.
- Counts seconds, minutes, hours, day of the week, date, month, and year with leap year compensation
- Millisecond time correction
- Binary-coded-decimal (BCD) representation of time, calendar, and alarm
- 24-hour clock mode
- Second, minute, hour, day, or week alarm interrupt
- Periodic interrupt: every millisecond, second, minute, hour, or day
- Alarm interrupt: precise time of day
- Single interrupt to the DSP CPU
- 32.768-kHz crystal oscillator with frequency calibration

Control of the RTC is maintained through a set of I/O memory mapped registers (see Table 5-16). Any write to these registers will be synchronized to the RTC 32.768-kHz clock; the CPU must run at least 3X faster than the RTC. Writes to these registers will not be apparent until the next two 32.768-kHz clock cycles later. If the RTC oscillator is disabled, no RTC register can be written to.

The RTC has its own power-on-reset (POR) circuit that resets the registers in the RTC core domain when power is first applied to the CV_{DDRTC} power pin. The RTC flops are not reset by the device's $\overline{\text{RESET}}$ pin nor the digital core's POR (powergood signal).

The scratch registers in the RTC can take advantage of this unique reset domain to keep track of when the DSP boots and whether the RTC time registers have already been initialized to the current clock time or whether the software must go into a routine to prompt the user to set the time and date.

5.6.12.1 RTC Peripheral Register Descriptions

Table 5-16 lists the RTC registers.

Table 5-16. RTC Registers

HEX ADDRESS RANGE	ACRONYM	REGISTER NAME
1900h	RTCINTEN	RTC Interrupt Enable Register
1901h	RTCUPDATE	RTC Update Register
1904h	RTCMIL	Milliseconds Register
1905h	RTCMILA	Milliseconds Alarm Register
1908h	RTCSEC	Seconds Register
1909h	RTCSECA	Seconds Alarm Register
190Ch	RTCMIN	Minutes Register
190Dh	RTCMINA	Minutes Alarm Register
1910h	RTCHOUR	Hours Register
1911h	RTCHOURA	Hours Alarm Register
1914h	RTCDAY	Days Register
1915h	RTCDAYA	Days Alarm Register
1918h	RTCMONTH	Months Register
1919h	RTCMONTHA	Months Alarm Register
191Ch	RTCYEAR	Years Register
191Dh	RTCYEARA	Years Alarm Register
1920h	RTCINTFL	RTC Interrupt Flag Register
1921h	RTCNOPWR	RTC Lost Power Status Register
1924h	RTCINTREG	RTC Interrupt Register
1928h	RTCDRIFT	RTC Compensation Register
192Ch	RTCOSC	RTC Oscillator Register
1930h	RTCPMGT	RTC Power Management Register
1960h	RTCSCR1	RTC LSW Scratch Register 1
1961h	RTCSCR2	RTC MSW Scratch Register 2
1964h	RTCSCR3	RTC LSW Scratch Register 3
1965h	RTCSCR4	RTC MSW Scratch Register 4

5.6.12.1.1 RTC Electrical Data and Timing

For more detailed information on RTC electrical timings, see the Section 5.6.9.3, *Reset Electrical Data and Timing*.

5.6.13 Inter-Integrated Circuit (I2C)

The inter-integrated circuit (I2C) module provides an interface between the device and other devices compliant with Philips Semiconductors Inter-IC bus (I^2C-bus™) specification version 2.1. External components attached to this 2-wire serial bus can transmit and receive 2 to 8-bit data to and from the DSP through the I2C module. The I2C port does not support CBUS compatible devices.

The I2C port supports the following features:

- Compatible with Philips I2C Specification Revision 2.1 (January 2000)
- Data Transfer Rate from 10 kbps to 400 kbps (Philips Fast-Mode Rate)
- Noise Filter to Remove Noise 50 ns or Less
- 7- and 10-Bit Device Addressing Modes
- Master (Transmit and Receive) and Slave (Transmit and Receive) Functionality
- One Read DMA Event and One Write DMA Event That the DMA Controller Can Use
- One Interrupt That the CPU Can Use
- Slew-Rate Limited Open-Drain Output Buffers

The I2C module clock must be in the range from 6.7 MHz to 13.3 MHz. With the I2C module clock in this range, the noise filters on the SDA and SCL pins suppress noise that has a duration of 50 ns or shorter. The I2C module clock is derived from the DSP clock divided by a programmable prescaler.

5.6.13.1 I2C Peripheral Register Descriptions

Table 5-17 lists the I2C registers.

Table 5-17. I2C Registers

HEX ADDRESS RANGE	ACRONYM	REGISTER NAME
1A00h	ICOAR	I2C Own Address Register
1A04h	ICIMR	I2C Interrupt Mask Register
1A08h	ICSTR	I2C Interrupt Status Register
1A0Ch	ICCLKL	I2C Clock Low-Time Divider Register
1A10h	ICCLKH	I2C Clock High-Time Divider Register
1A14h	ICCNT	I2C Data Count Register
1A18h	ICDRR	I2C Data Receive Register
1A1Ch	ICSAR	I2C Slave Address Register
1A20h	ICDXR	I2C Data Transmit Register
1A24h	ICMDR	I2C Mode Register
1A28h	ICIVR	I2C Interrupt Vector Register
1A2Ch	ICEMDR	I2C Extended Mode Register
1A30h	ICPSC	I2C Prescaler Register
1A34h	ICPID1	I2C Peripheral Identification Register 1
1A38h	ICPID2	I2C Peripheral Identification Register 2

5.6.13.2 I2C Electrical Data and Timing

Table 5-18 and Table 5-19 list the timing and switching requirements for I2C, respectively.

Table 5-18. Timing Requirements for I2C Timings(1) (see Figure 5-20)

NO.			CV_{DD} = 1.05 V, CV_{DD} = 1.3 V				UNIT
			STANDARD MODE		FAST MODE		
			MIN	MAX	MIN	MAX	
1	$t_{c(SCL)}$	Cycle time, SCL	10		2.5		µs
2	$t_{su(SCLH-SDAL)}$	Setup time, SCL high before SDA low (for a repeated START condition)	4.7		0.6		µs
3	$t_{h(SCLL-SDAL)}$	Hold time, SCL low after SDA low (for a START and a repeated START condition)	4		0.6		µs
4	$t_{w(SCLL)}$	Pulse duration, SCL low	4.7		1.3		µs
5	$t_{w(SCLH)}$	Pulse duration, SCL high	4		0.6		µs
6	$t_{su(SDAV-SCLH)}$	Setup time, SDA valid before SCL high	250		100(2)		ns
7	$t_{h(SDA-SCLL)}$	Hold time, SDA valid after SCL low	0(3)		0(3)	0.9(4)	µs
8	$t_{w(SDAH)}$	Pulse duration, SDA high between STOP and START conditions	4.7		1.3		µs
9	$t_{r(SDA)}$	Rise time, SDA(5)		1000	20 + 0.1C_b (6)	300	ns
10	$t_{r(SCL)}$	Rise time, SCL(5)		1000	20 + 0.1C_b (6)	300	ns
11	$t_{f(SDA)}$	Fall time, SDA(5)		300	20 + 0.1C_b (6)	300	ns
12	$t_{f(SCL)}$	Fall time, SCL(5)		300	20 + 0.1C_b (6)	300	ns
13	$t_{su(SCLH-SDAH)}$	Setup time, SCL high before SDA high (for STOP condition)	4		0.6		µs
14	$t_{w(SP)}$	Pulse duration, spike (must be suppressed)			0	50	ns
15	C_b (6)	Capacitive load for each bus line		400		400	pF

(1) The I2C pins SDA and SCL do not feature fail-safe I/O buffers. These pins could potentially draw current when the device is powered down. Also these pins are not 3.6 V-tolerant (their V_{IH} cannot go above DV_{DDIO} + 0.3 V).
(2) A Fast-mode I^2C-bus device can be used in a Standard-mode I^2C-bus system, but the requirement $t_{su(SDA-SCLH)} \geq$ 250 ns must then be met. This will automatically be the case if the device does not stretch the LOW period of the SCL signal. If such a device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line t_r max + $t_{su(SDA-SCLH)}$= 1000 + 250 = 1250 ns (according to the Standard-mode I^2C-Bus Specification) before the SCL line is released.
(3) A device must internally provide a hold time of at least 300 ns for the SDA signal (referred to the V_{IHmin} of the SCL signal) to bridge the undefined region of the falling edge of SCL.
(4) The maximum $t_{h(SDA-SCLL)}$ only has to be met if the device does not stretch the low period [$t_{w(SCLL)}$] of the SCL signal.
(5) The rise and fall times are measured at 30% and 70% of DV_{DDIO}. The fall time is only slightly influenced by the external bus load (C_b) and external pullup resistor. The rise time (t_r) is mainly determined by the bus load capacitance and the value of the pullup resistor. The pullup resistor must be selected to meet the I2C rise and fall time values specified.
(6) C_b = total capacitance of one bus line in pF. If mixed with HS-mode devices, faster fall-times are allowed.

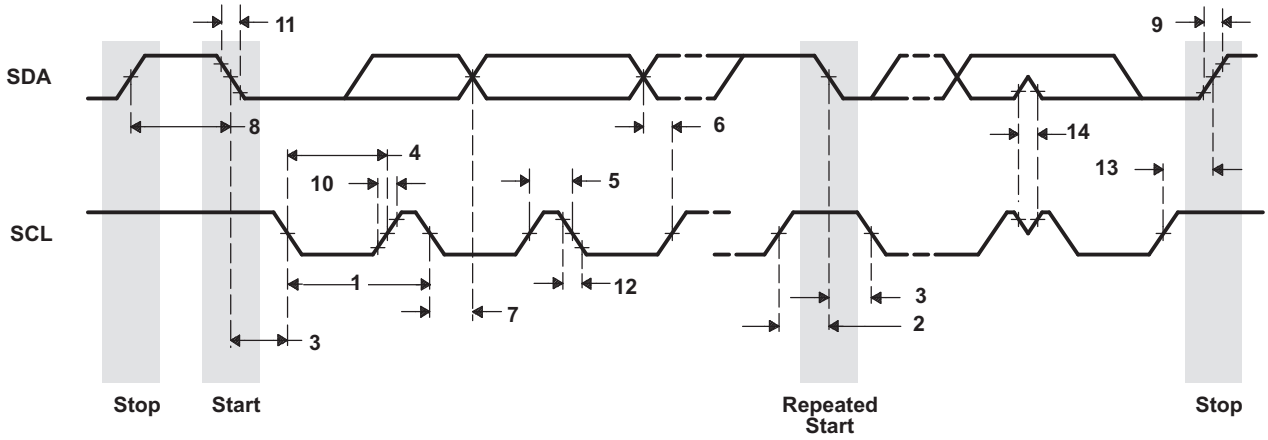


Figure 5-20. I2C Receive Timings

Table 5-19. Switching Characteristics for I2C Timings[1] (see Figure 5-21)

NO.	PARAMETER		CV_{DD} = 1.05 V, CV_{DD} = 1.3 V				UNIT
			STANDARD MODE		FAST MODE		
			MIN	MAX	MIN	MAX	
16	$t_{c(SCL)}$	Cycle time, SCL	10		2.5		µs
17	$t_{d(SCLH-SDAL)}$	Delay time, SCL high to SDA low (for a repeated START condition)	4.7		0.6		µs
18	$t_{d(SDAL-SCLL)}$	Delay time, SDA low to SCL low (for a START and a repeated START condition)	4		0.6		µs
19	$t_{w(SCLL)}$	Pulse duration, SCL low	4.7		1.3		µs
20	$t_{w(SCLH)}$	Pulse duration, SCL high	4		0.6		µs
21	$t_{d(SDAV-SCLH)}$	Delay time, SDA valid to SCL high	250		100		ns
22	$t_{v(SCLL-SDAV)}$	Valid time, SDA valid after SCL low	0		0	0.9	µs
23	$t_{w(SDAH)}$	Pulse duration, SDA high between STOP and START conditions	4.7		1.3		µs
24	$t_{r(SDA)}$	Rise time, SDA[2]		1000	20 + 0.1C_b [1]	300	ns
25	$t_{r(SCL)}$	Rise time, SCL[2]		1000	20 + 0.1C_b [1]	300	ns
26	$t_{f(SDA)}$	Fall time, SDA[2]		300	20 + 0.1C_b [1]	300	ns
27	$t_{f(SCL)}$	Fall time, SCL[2]		300	20 + 0.1C_b [1]	300	ns
28	$t_{d(SCLH-SDAH)}$	Delay time, SCL high to SDA high (for STOP condition)	4		0.6		µs
29	C_p	Capacitance for each I2C pin		10		10	pF

(1) C_b = total capacitance of one bus line in pF. If mixed with HS-mode devices, faster fall-times are allowed.
(2) The rise and fall times are measured at 30% and 70% of DV_{DDIO}. The fall time is only slightly influenced by the external bus load (C_b) and external pullup resistor. The rise time (t_r) is determined by the bus load capacitance and the value of the pullup resistor. The pullup resistor must be selected to meet the I2C rise and fall time values specified.

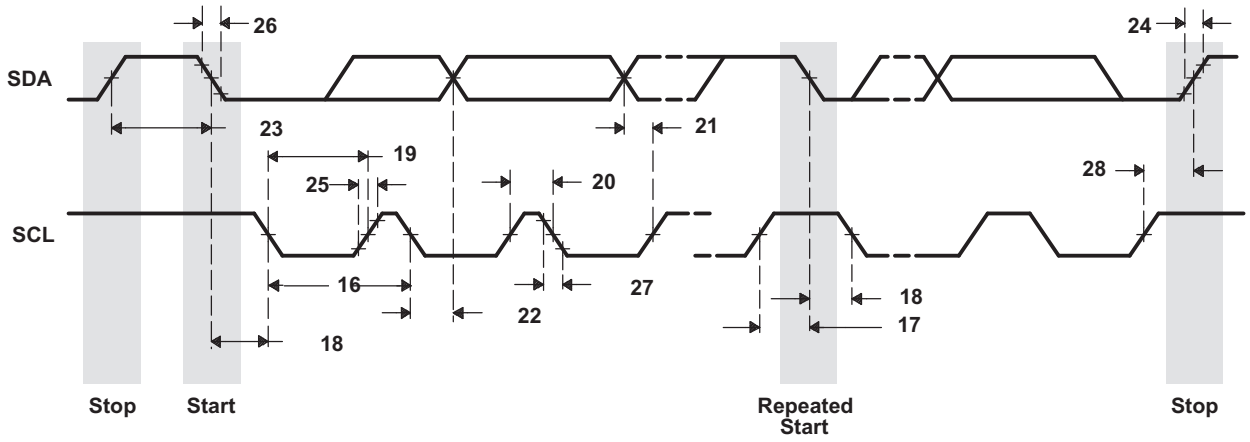


Figure 5-21. I2C Transmit Timings

5.6.14 Universal Asynchronous Receiver/Transmitter (UART)

The UART performs serial-to-parallel conversions on data received from an external peripheral device and parallel-to-serial conversions on data transmitted to an external peripheral device through a serial bus.

The device has one UART peripheral with the following features:

- Programmable baud rates (frequency prescale values from 1 to 65535)
- Fully programmable serial interface characteristics:
  - 5, 6, 7, or 8-bit characters
  - Even, odd, or no PARITY bit generation and detection
  - 1, 1.5, or 2 STOP bit generation
- 16-byte depth transmitter and receiver FIFOs:
  - The UART can be operated with or without the FIFOs
  - 1, 4, 8, or 14 byte selectable receiver FIFO trigger level for autoflow control and DMA
- DMA signaling capability for both received and transmitted data
- CPU interrupt capability for both received and transmitted data
- False START bit detection
- Line break generation and detection
- Internal diagnostic capabilities:
  - Loopback controls for communications link fault isolation
  - Break, parity, overrun, and framing error simulation
- Programmable autoflow control using CTS and RTS signals

5.6.14.1 UART Peripheral Register Descriptions

Table 5-20 lists the UART registers.

Table 5-20. UART Registers

HEX ADDRESS RANGE	ACRONYM	REGISTER NAME
1B00h	RBR	Receiver Buffer Register (read only)
1B00h	THR	Transmitter Holding Register (write only)
1B02h	IER	Interrupt Enable Register
1B04h	IIR	Interrupt Identification Register (read only)
1B04h	FCR	FIFO Control Register (write only)
1B06h	LCR	Line Control Register
1B08h	MCR	Modem Control Register
1B0Ah	LSR	Line Status Register
1B0Ch	MSR	Modem Status Register
1B0Eh	SCR	Scratch Register
1B10h	DLL	Divisor LSB Latch
1B12h	DLH	Divisor MSB Latch
1B18h	PWREMU_MGMT	Power and Emulation Management Register

5.6.14.2 UART Electrical Data and Timing [Receive and Transmit]

Table 5-21 and Table 5-22 list the timing and switching requirements of UART, respectively.

Table 5-21. Timing Requirements for UART Receive(1) (2) (see Figure 5-22)

NO.			CV_{DD} = 1.05 V		CV_{DD} = 1.3 V		UNIT
			MIN	MAX	MIN	MAX	
4	$t_{w(URXDB)}$	Pulse duration, receive data bit (UART_RXD) [15/30 pF]	U - 3.5	U + 3	U - 3.5	U + 3	ns
5	$t_{w(URXSB)}$	Pulse duration, receive start bit [15/30 pF]	U - 3.5	U + 3	U - 3.5	U + 3	ns

(1) U = UART baud time = 1/programmed baud rate.
(2) These parametric values are measured at DVDDIO = 3.3 V, 2.75 V, and 2.5 V.

Table 5-22. Switching Characteristics Over Recommended Operating Conditions for UART Transmit(1) (2) (see Figure 5-22)

NO.	PARAMETER		CV_{DD} = 1.05 V		CV_{DD} = 1.3 V		UNIT
			MIN	MAX	MIN	MAX	
1	$f_{(baud)}$	Maximum programmable bit rate		3.75		6.25	MHz
2	$t_{w(UTXDB)}$	Pulse duration, transmit data bit (UART_TXD) [15/30 pF]	U - 3.5	U + 4	U - 3.5	U + 4	ns
3	$t_{w(UTXSB)}$	Pulse duration, transmit start bit [15/30 pF]	U - 3.5	U + 4	U - 3.5	U + 4	ns

(1) U = UART baud time = 1/programmed baud rate.
(2) These parametric values are measured at DVDDIO = 3.3 V, 2.75 V, and 2.5 V.

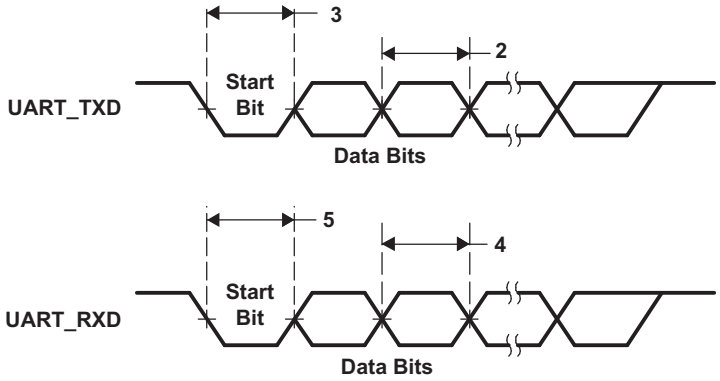


Figure 5-22. UART Transmit and Receive Timing

5.6.15 Inter-IC Sound (I2S)

The device I2S peripherals allow serial transfer of full-duplex streaming data, usually audio data, between the device and an external I2S peripheral device such as an audio codec.

The device supports four independent dual-channel I2S peripherals, each with the following features:

- Full-duplex (transmit and receive) dual-channel communication
- Double-buffered data registers that allow for continuous data streaming
- I2S/Left-justified and DSP data format with a data delay of 1 or 2 bits
- Data word-lengths of 8, 10, 12, 14, 16, 18, 20, 24, or 32 bits
- Ability to sign-extend received data samples for easy use in signal processing algorithms
- Programmable polarity for both frame synchronization and bit clocks
- Stereo (in I2S/Left-justified or DSP data formats) or mono (in DSP data format) mode
- Detection of overrun, underrun, and frame-sync error conditions

5.6.15.1 I2S Peripheral Register Descriptions

Table 5-23, Table 5-24, Table 5-25, and Table 5-26 list the I2S0, I2S1, I2S2, and I2S3 registers, respectively.

Table 5-23. I2S0 Registers

HEX ADDRESS RANGE	ACRONYM	REGISTER NAME
2800h	I2S0SCTRL	I2S0 Serializer Control Register
2804h	I2S0SRATE	I2S0 Sample Rate Generator Register
2808h	I2S0TXLT0	I2S0 Transmit Left Data 0 Register
2809h	I2S0TXLT1	I2S0 Transmit Left Data 1 Register
280Ch	I2S0TXRT0	I2S0 Transmit Right Data 0 Register
280Dh	I2S0TXRT1	I2S0 Transmit Right Data 1 Register
2810h	I2S0INTFL	I2S0 Interrupt Flag Register
2814h	I2S0INTMASK	I2S0 Interrupt Mask Register
2828h	I2S0RXLT0	I2S0 Receive Left Data 0 Register
2829h	I2S0RXLT1	I2S0 Receive Left Data 1 Register
282Ch	I2S0RXRT0	I2S0 Receive Right Data 0 Register
282Dh	I2S0RXRT1	I2S0 Receive Right Data 1 Register

Table 5-24. I2S1 Registers

HEX ADDRESS RANGE	ACRONYM	REGISTER NAME
2900h	I2S1SCTRL	I2S1 Serializer Control Register
2904h	I2S1SRATE	I2S1 Sample Rate Generator Register
2908h	I2S1TXLT0	I2S1 Transmit Left Data 0 Register
2909h	I2S1TXLT1	I2S1 Transmit Left Data 1 Register
290Ch	I2S1TXRT0	I2S1 Transmit Right Data 0 Register
290Dh	I2S1TXRT1	I2S1 Transmit Right Data 1 Register
2910h	I2S1INTFL	I2S1 Interrupt Flag Register
2914h	I2S1INTMASK	I2S1 Interrupt Mask Register
2928h	I2S1RXLT0	I2S1 Receive Left Data 0 Register
2929h	I2S1RXLT1	I2S1 Receive Left Data 1 Register
292Ch	I2S1RXRT0	I2S1 Receive Right Data 0 Register
292Dh	I2S1RXRT1	I2S1 Receive Right Data 1 Register

Table 5-25. I2S2 Registers

HEX ADDRESS RANGE	ACRONYM	REGISTER NAME
2A00h	I2S2SCTRL	I2S2 Serializer Control Register
2A04h	I2S2SRATE	I2S2 Sample Rate Generator Register
2A08h	I2S2TXLT0	I2S2 Transmit Left Data 0 Register
2A09h	I2S2TXLT1	I2S2 Transmit Left Data 1 Register
2A0Ch	I2S2TXRT0	I2S2 Transmit Right Data 0 Register
2A0Dh	I2S2TXRT1	I2S2 Transmit Right Data 1 Register
2A10h	I2S2INTFL	I2S2 Interrupt Flag Register
2A14h	I2S2INTMASK	I2S2 Interrupt Mask Register
2A28h	I2S2RXLT0	I2S2 Receive Left Data 0 Register
2A29h	I2S2RXLT1	I2S2 Receive Left Data 1 Register
2A2Ch	I2S2RXRT0	I2S2 Receive Right Data 0 Register
2A2Dh	I2S2RXRT1	I2S2 Receive Right Data 1 Register

Table 5-26. I2S3 Registers

HEX ADDRESS RANGE	ACRONYM	REGISTER NAME
2B00h	I2S3SCTRL	I2S3 Serializer Control Register
2B04h	I2S3SRATE	I2S3 Sample Rate Generator Register
2B08h	I2S3TXLT0	I2S3 Transmit Left Data 0 Register
2B09h	I2S3TXLT1	I2S3 Transmit Left Data 1 Register
2B0Ch	I2S3TXRT0	I2S3 Transmit Right Data 0 Register
2B0Dh	I2S3TXRT1	I2S3 Transmit Right Data 1 Register
2B10h	I2S3INTFL	I2S3 Interrupt Flag Register
2B14h	I2S3INTMASK	I2S3 Interrupt Mask Register
2B28h	I2S3RXLT0	I2S3 Receive Left Data 0 Register
2B29h	I2S3RXLT1	I2S3 Receive Left Data 1 Register
2B2Ch	I2S3RXRT0	I2S3 Receive Right Data 0 Register
2B2Dh	I2S3RXRT1	I2S3 Receive Right Data 1 Register

5.6.15.2 I2S Electrical Data and Timing

Table 5-27, Table 5-28, Table 5-29, and Table 5-30 list the timing and switching requirements for I2S.

Table 5-27. Timing Requirements for I2S [I/O = 3.3 V, 2.75 V, and 2.5 V](1) (see Figure 5-23)

NO.			MASTER				SLAVE				UNIT
			CV_{DD} = 1.05 V		CV_{DD} = 1.3 V		CV_{DD} = 1.05 V		CV_{DD} = 1.3 V		
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
1	$t_{c(CLK)}$	Cycle time, I2S_CLK	40 or 2P(1) (2)		40 or 2P(1) (2)		40 or 2P(1) (2)		40 or 2P(1) (2)		ns
2	$t_{w(CLKH)}$	Pulse duration, I2S_CLK high	20		20		20		20		ns
3	$t_{w(CLKL)}$	Pulse duration, I2S_CLK low	20		20		20		20		ns
7	$t_{su(RXV-CLKH)}$	Setup time, I2S_RX valid before I2S CLK high (CLKPOL = 0)	5		5		5		5		ns
	$t_{su(RXV-CLKL)}$	Setup time, I2S_RX valid before I2S_CLK low (CLKPOL = 1)	5		5		5		5		ns
8	$t_{h(CLKH-RXV)}$	Hold time, I2S_RX valid after I2S_CLK high (CLKPOL = 0)	3		3		3		3		ns
	$t_{h(CLKL-RXV)}$	Hold time, I2S_RX valid after I2S_CLK low (CLKPOL = 1)	3		3		3		3		ns
9	$t_{su(FSV-CLKH)}$	Setup time, I2S_FS valid before I2S_CLK high (CLKPOL = 0)	–		–		15		15		ns
	$t_{su(FSV-CLKL)}$	Setup time, I2S_FS valid before I2S_CLK low (CLKPOL = 1)	–		–		15		15		ns
10	$t_{h(CLKH-FSV)}$	Hold time, I2S_FS valid after I2S_CLK high (CLKPOL = 0)	–		–		$t_{w(CLKH)}$ + 0.6(3)		$t_{w(CLKH)}$ + 0.6(3)		ns
	$t_{h(CLKL-FSV)}$	Hold time, I2S_FS valid after I2S_CLK low (CLKPOL = 1)	–		–		$t_{w(CLKL)}$ + 0.6(3)		$t_{w(CLKL)}$ + 0.6(3)		ns

(1) P = SYSCLK period in ns. For example, when the CPU core is clocked at 100 MHz, use P = 10 ns.
(2) Use the greater value.
(3) In slave mode, I2S_FS must be latched on both edges of I2S input clock (I2S_CLK).

Table 5-28. Timing Requirements for I2S [I/O = 1.8 V](1) (see Figure 5-23)

NO.			MASTER				SLAVE				UNIT
			CV_{DD} = 1.05 V		CV_{DD} = 1.3 V		CV_{DD} = 1.05 V		CV_{DD} = 1.3 V		
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
1	$t_{c(CLK)}$	Cycle time, I2S_CLK	50 or 2P(1) (2)		40 or 2P(1) (2)		50 or 2P(1) (2)		40 or 2P(1) (2)		ns
2	$t_{w(CLKH)}$	Pulse duration, I2S_CLK high	25		20		25		20		ns
3	$t_{w(CLKL)}$	Pulse duration, I2S_CLK low	25		20		25		20		ns
7	$t_{su(RXV-CLKH)}$	Setup time, I2S_RX valid before I2S CLK high (CLKPOL = 0)	5		5		5		5		ns
	$t_{su(RXV-CLKL)}$	Setup time, I2S_RX valid before I2S_CLK low (CLKPOL = 1)	5		5		5		5		ns
8	$t_{h(CLKH-RXV)}$	Hold time, I2S_RX valid after I2S_CLK high (CLKPOL = 0)	3		3		3		3		ns
	$t_{h(CLKL-RXV)}$	Hold time, I2S_RX valid after I2S_CLK low (CLKPOL = 1)	3		3		3		3		ns
9	$t_{su(FSV-CLKH)}$	Setup time, I2S_FS valid before I2S_CLK high (CLKPOL = 0)	–		–		15		15		ns
	$t_{su(FSV-CLKL)}$	Setup time, I2S_FS valid before I2S_CLK low (CLKPOL = 1)	–		–		15		15		ns
10	$t_{h(CLKH-FSV)}$	Hold time, I2S_FS valid after I2S_CLK high (CLKPOL = 0)	–		–		$t_{w(CLKH)}$ + 0.6(3)		$t_{w(CLKH)}$ + 0.6(3)		ns
	$t_{h(CLKL-FSV)}$	Hold time, I2S_FS valid after I2S_CLK low (CLKPOL = 1)	–		–		$t_{w(CLKL)}$ + 0.6(3)		$t_{w(CLKL)}$ + 0.6(3)		ns

(1) P = SYSCLK period in ns. For example, when the CPU core is clocked at 100 MHz, use P = 10 ns.
(2) Use the greater value.
(3) In slave mode, I2S_FS is required to be latched on both edges of I2S input clock (I2S_CLK).

Table 5-29. Switching Characteristics Over Recommended Operating Conditions for I2S Output [I/O = 3.3 V, 2.75 V, or 2.5 V] (see Figure 5-23)

NO.	PARAMETER		MASTER				SLAVE				UNIT
			CV_{DD} = 1.05 V		CV_{DD} = 1.3 V		CV_{DD} = 1.05 V		CV_{DD} = 1.3 V		
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
1	$t_{c(CLK)}$	Cycle time, I2S_CLK	40 or 2P(1) (2)		40 or 2P(1) (2)		40 or 2P(1) (2)		40 or 2P(1) (2)		ns
2	$t_{w(CLKH)}$	Pulse duration, I2S_CLK high (CLKPOL = 0)	20		20		20		20		ns
	$t_{w(CLKL)}$	Pulse duration, I2S_CLK low (CLKPOL = 1)	20		20		20		20		ns
3	$t_{w(CLKL)}$	Pulse duration, I2S_CLK low (CLKPOL = 0)	20		20		20		20		ns
	$t_{w(CLKH)}$	Pulse duration, I2S_CLK high (CLKPOL = 1)	20		20		20		20		ns
4	$t_{dmax(CLKL-DXV)}$	Output Delay time, I2S_CLK low to I2S_DX valid (CLKPOL = 0)	0	15	0	14	0	15	0	15	ns
	$t_{dmax(CLKH-DXV)}$	Output Delay time, I2S_CLK high to I2S_DX valid (CLKPOL = 1)	0	15	0	14	0	15	0	15	ns
5	$t_{dmax(CLKL-FSV)}$	Delay time, I2S_CLK low to I2S_FS valid (CLKPOL = 0)	–1.1	14	–1.1	14		–		–	ns
	$t_{dmax(CLKH-FSV)}$	Delay time, I2S_CLK high to I2S_FS valid (CLKPOL = 1)	–1.1	14	–1.1	14		–		–	ns

(1) P = SYSCLK period in ns. For example, when the CPU core is clocked at 100 MHz, use P = 10 ns.
(2) Use the greater value.

Table 5-30. Switching Characteristics Over Recommended Operating Conditions for I2S Output [I/O = 1.8 V] (see Figure 5-23)

NO.	PARAMETER		MASTER				SLAVE				UNIT
			CV_{DD} = 1.05 V		CV_{DD} = 1.3 V		CV_{DD} = 1.05 V		CV_{DD} = 1.3 V		
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
1	$t_{c(CLK)}$	Cycle time, I2S_CLK	50 or 2P(1) (2)		40 or 2P(1) (2)		50 or 2P(1) (2)		40 or 2P(1) (2)		ns
2	$t_{w(CLKH)}$	Pulse duration, I2S_CLK high (CLKPOL = 0)	25		20		25		20		ns
	$t_{w(CLKL)}$	Pulse duration, I2S_CLK low (CLKPOL = 1)	25		20		25		20		ns
3	$t_{w(CLKL)}$	Pulse duration, I2S_CLK low (CLKPOL = 0)	25		20		25		20		ns
	$t_{w(CLKH)}$	Pulse duration, I2S_CLK high (CLKPOL = 1)	25		20		25		20		ns
4	$t_{dmax(CLKL-DXV)}$	Output Delay time, I2S_CLK low to I2S_DX valid (CLKPOL = 0)	0	19	0	14	0	19	0	16.5	ns
	$t_{dmax(CLKH-DXV)}$	Output Delay time, I2S_CLK high to I2S_DX valid (CLKPOL = 1)	0	19	0	14	0	19	0	16.5	ns
5	$t_{dmax(CLKL-FSV)}$	Delay time, I2S_CLK low to I2S_FS valid (CLKPOL = 0)	–1.1	14	–1.1	14		–		–	ns
	$t_{dmax(CLKH-FSV)}$	Delay time, I2S_CLK high to I2S_FS valid (CLKPOL = 1)	–1.1	14	–1.1	14		–		–	ns

(1) P = SYSCLK period in ns. For example, when the CPU core is clocked at 100 MHz, use P = 10 ns.
(2) Use the greater value.

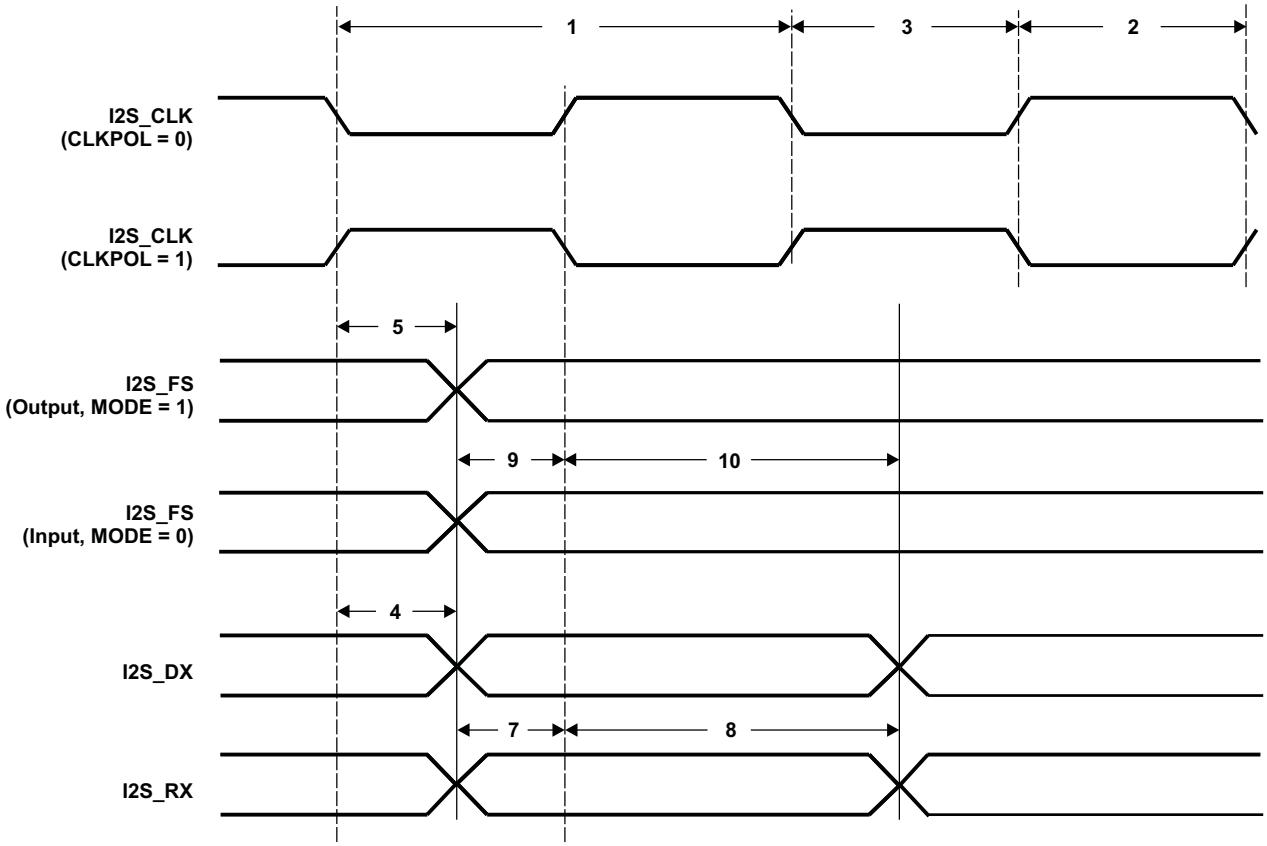


Figure 5-23. I2S Input and Output Timings

5.6.16 Liquid Crystal Display Controller (LCDC)

The device includes a LCD interface display driver (LIDD) controller.

The LIDD controller supports the asynchronous LCD interface and has the following features:

- Provides full-timing programmability of control signals and output data

NOTE

Raster mode is not supported on this device.

The LCD controller generates the correct external timing. The DMA engine provides a constant flow of data from the frame buffer to the external LCD panel through the LIDD controller. CPU access is provided to read and write registers.

5.6.16.1 LCDC Peripheral Register Descriptions

Table 5-31 lists the LCDC peripheral registers.

Table 5-31. LCD Controller Registers

CPU WORD ADDRESS	ACRONYM	REGISTER DESCRIPTION
2E00h	LCDREVMIN	LCD Minor Revision Register
2E01h	LCDREVMAJ	LCD Major Revision Register
2E04h	LCDCR	LCD Control Register
2E08h	LCDSR	LCD Status Register
2E0Ch	LCDLIDDCR	LCD LIDD Control Register
2E10h	LCDLIDDCS0CONFIG0	LCD LIDD CS0 Configuration Register 0
2E11h	LCDLIDDCS0CONFIG1	LCD LIDD CS0 Configuration Register 1
2E14h	LCDLIDDCS0ADDR	LCD LIDD CS0 Address Read and Write Register
2E18h	LCDLIDDCS0DATA	LCD LIDD CS0 Data Read and Write Register
2E1Ch	LCDLIDDCS1CONFIG0	LCD LIDD CS1 Configuration Register 0
2E1Dh	LCDLIDDCS1CONFIG1	LCD LIDD CS1 Configuration Register 1
2E20h	LCDLIDDCS1ADDR	LCD LIDD CS1 Address Read and Write Register
2E24h	LCDLIDDCS1DATA	LCD LIDD CS1 Data Read and Write Register
2E28h to 2E3Ah	—	Reserved
2E40h	LCDDMACR	LCD DMA Control Register
2E44h	LCDDMAFB0BAR0	LCD DMA Frame Buffer 0 Base Address Register 0
2E45h	LCDDMAFB0BAR1	LCD DMA Frame Buffer 0 Base Address Register 1
2E48h	LCDDMAFB0CAR0	LCD DMA Frame Buffer 0 Ceiling Address Register 0
2E49h	LCDDMAFB0CAR1	LCD DMA Frame Buffer 0 Ceiling Address Register 1
2E4Ch	LCDDMAFB1BAR0	LCD DMA Frame Buffer 1 Base Address Register 0
2E4Dh	LCDDMAFB1BAR1	LCD DMA Frame Buffer 1 Base Address Register 1
2E50h	LCDDMAFB1CAR0	LCD DMA Frame Buffer 1 Ceiling Address Register 0
2E51h	LCDDMAFB1CAR1	LCD DMA Frame Buffer 1 Ceiling Address Register 1

5.6.16.2 LCDC Electrical Data and Timing

Table 5-32 and Table 5-33 list the timing and switching requirements for LCDC, respectively.

Table 5-32. Timing Requirements for LCD LIDD Mode(1) (see Figure 5-24, Figure 5-25, Figure 5-26, Figure 5-27, Figure 5-28, Figure 5-29, Figure 5-30, and Figure 5-31)

NO.			CV_{DD} = 1.05 V		CV_{DD} = 1.3 V		UNIT
			MIN	MAX	MIN	MAX	
16	$t_{su(LCD\_D-CLK)}$	Setup time, LCD_D[15:0] valid before LCD_CLK rising edge	27		42		ns
17	$t_{h(CLK-LCD\_D)}$	Hold time, LCD_D[15:0] valid after LCD_CLK rising edge	0		0		ns

(1) Over operating free-air temperature range (unless otherwise noted)

Table 5-33. Switching Characteristics Over Recommended Operating Conditions for LCD LIDD Mode (see Figure 5-24, Figure 5-25, Figure 5-26, Figure 5-27, Figure 5-28, Figure 5-29, Figure 5-30, and Figure 5-31)

NO.	PARAMETER		CV_{DD} = 1.05 V		CV_{DD} = 1.3 V		UNIT
			MIN	MAX	MIN	MAX	
4	$t_{d(LCD\_D\_V)}$	Delay time, LCD_CLK rising edge to LCD_D[15:0] valid (write)		5		7	ns
5	$t_{d(LCD\_D\_I)}$	Delay time, LCD_CLK rising edge to LCD_D[15:0] invalid (write)	–6		–6		ns
6	$t_{d(LCD\_E\_A)}$	Delay time, LCD_CLK rising edge to LCD_CSx_Ex low		5		7	ns
7	$t_{d(LCD\_E\_I)}$	Delay time, LCD_CLK rising edge to LCD_CSx_Ex high	–6		–6		ns
8	$t_{d(LCD\_A\_A)}$	Delay time, LCD_CLK rising edge to LCD_RS low		5		7	ns
9	$t_{d(LCD\_A\_I)}$	Delay time, LCD_CLK rising edge to LCD_RS high	–6		–6		ns
10	$t_{d(LCD\_W\_A)}$	Delay time, LCD_CLK rising edge to LCD_RW_WRB low		5		7	ns
11	$t_{d(LCD\_W\_I)}$	Delay time, LCD_CLK rising edge to LCD_RW_WRB high	–6		–6		ns
12	$t_{d(LCD\_STRB\_A)}$	Delay time, LCD_CLK rising edge to LCD_EN_RDB high		5		7	ns
13	$t_{d(LCD\_STRB\_I)}$	Delay time, LCD_CLK rising edge to LCD_EN_RDB low	–6		–6		ns
14	$t_{d(LCD\_D\_Z)}$	Delay time, LCD_CLK rising edge to LCD_D[15:0] in 3-state		5		7	ns
15	$t_{d(Z\_LCD\_D)}$	Delay time, LCD_CLK rising edge to LCD_D[15:0] valid from 3-state	–6		–6		ns

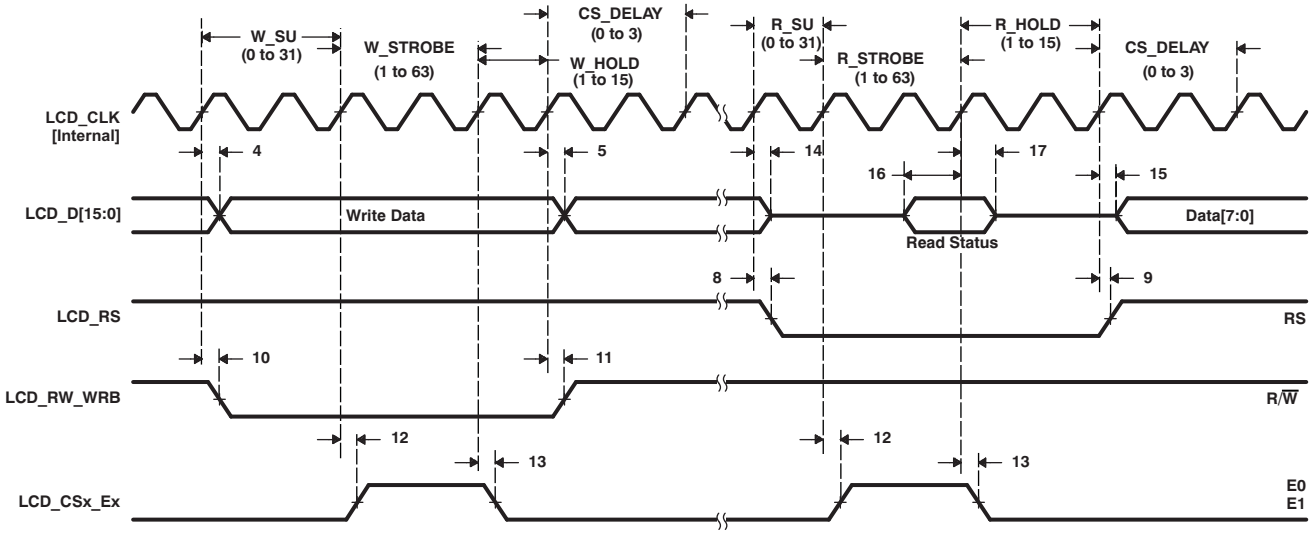


Figure 5-24. Character Display HD44780 Write

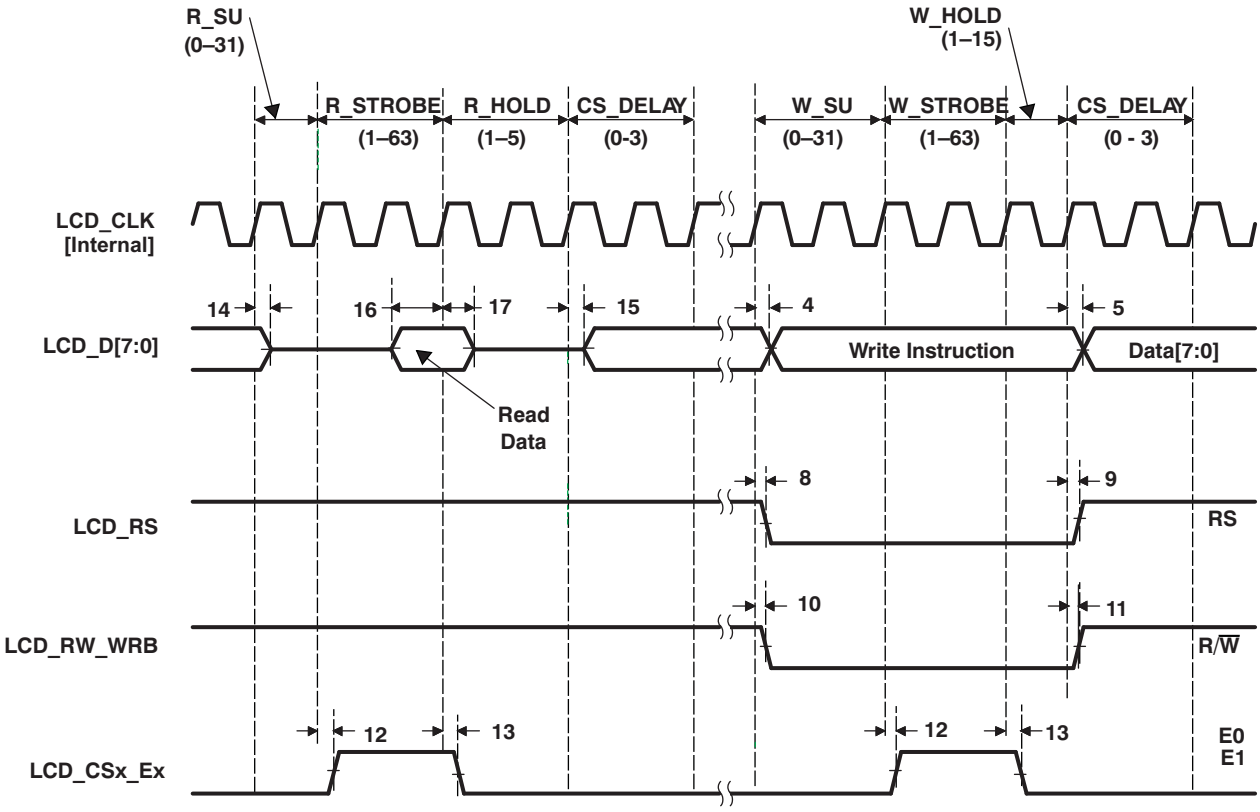


Figure 5-25. Character Display HD44780 Read

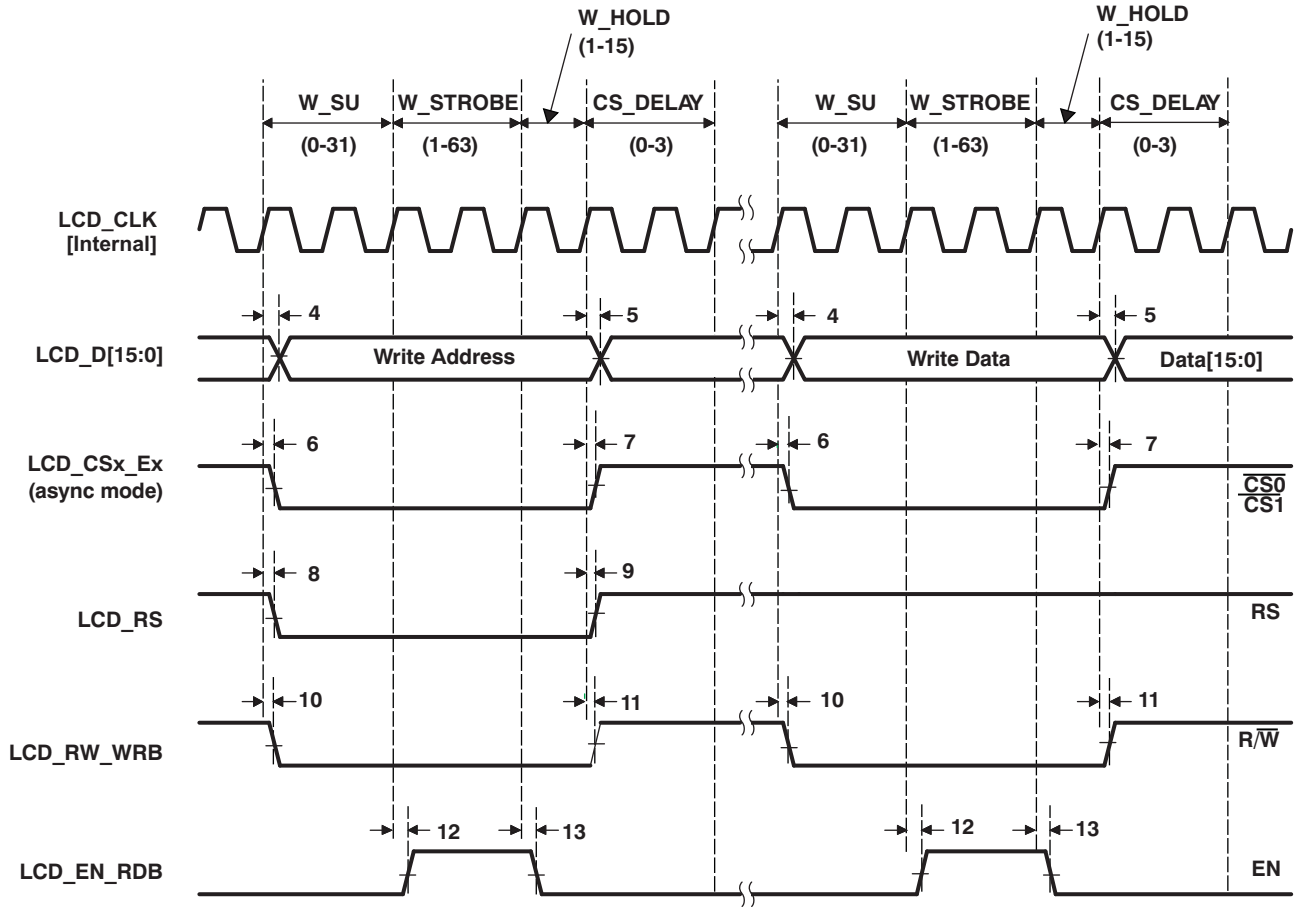


Figure 5-26. Micro-Interface Graphic Display 6800 Write

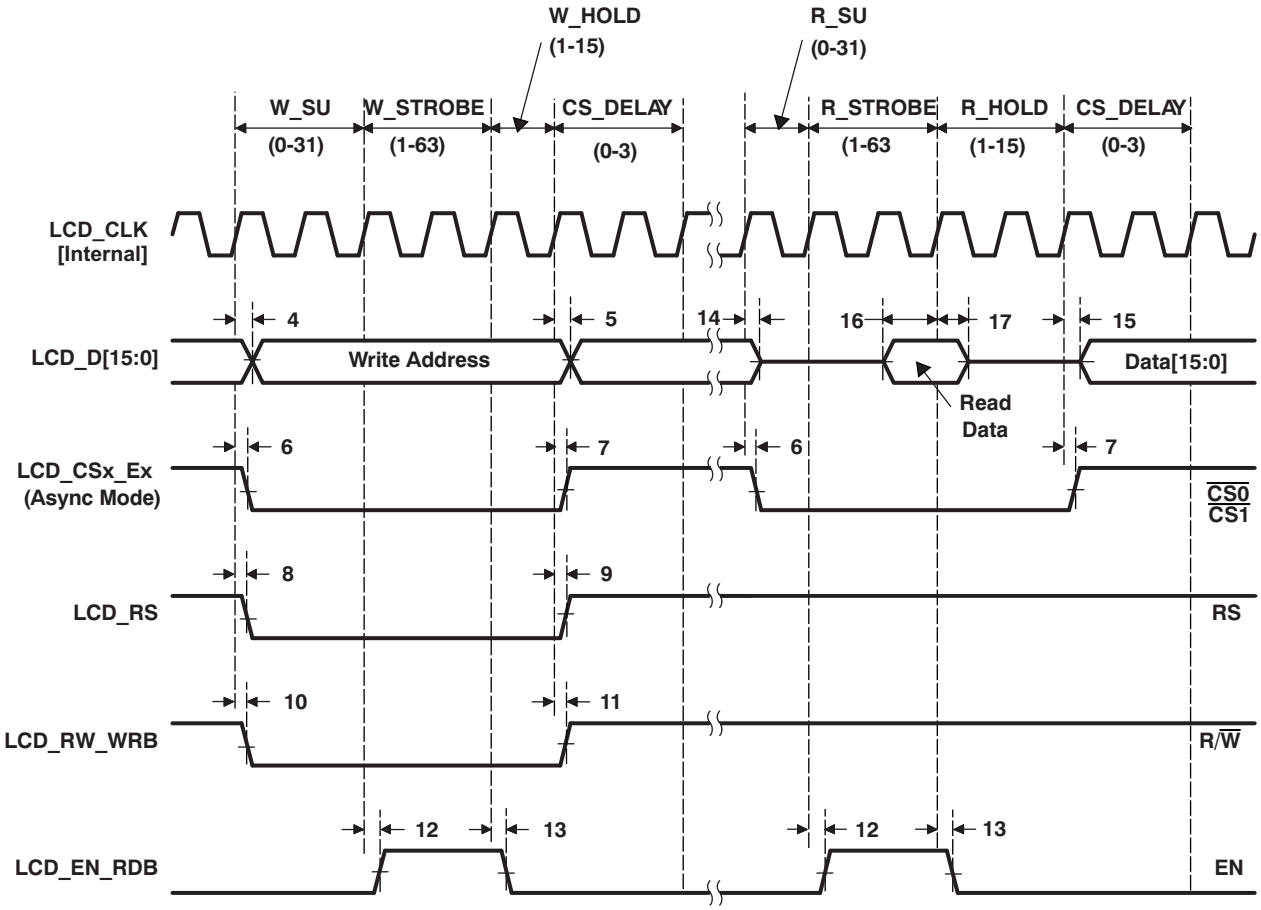


Figure 5-27. Micro-Interface Graphic Display 6800 Read

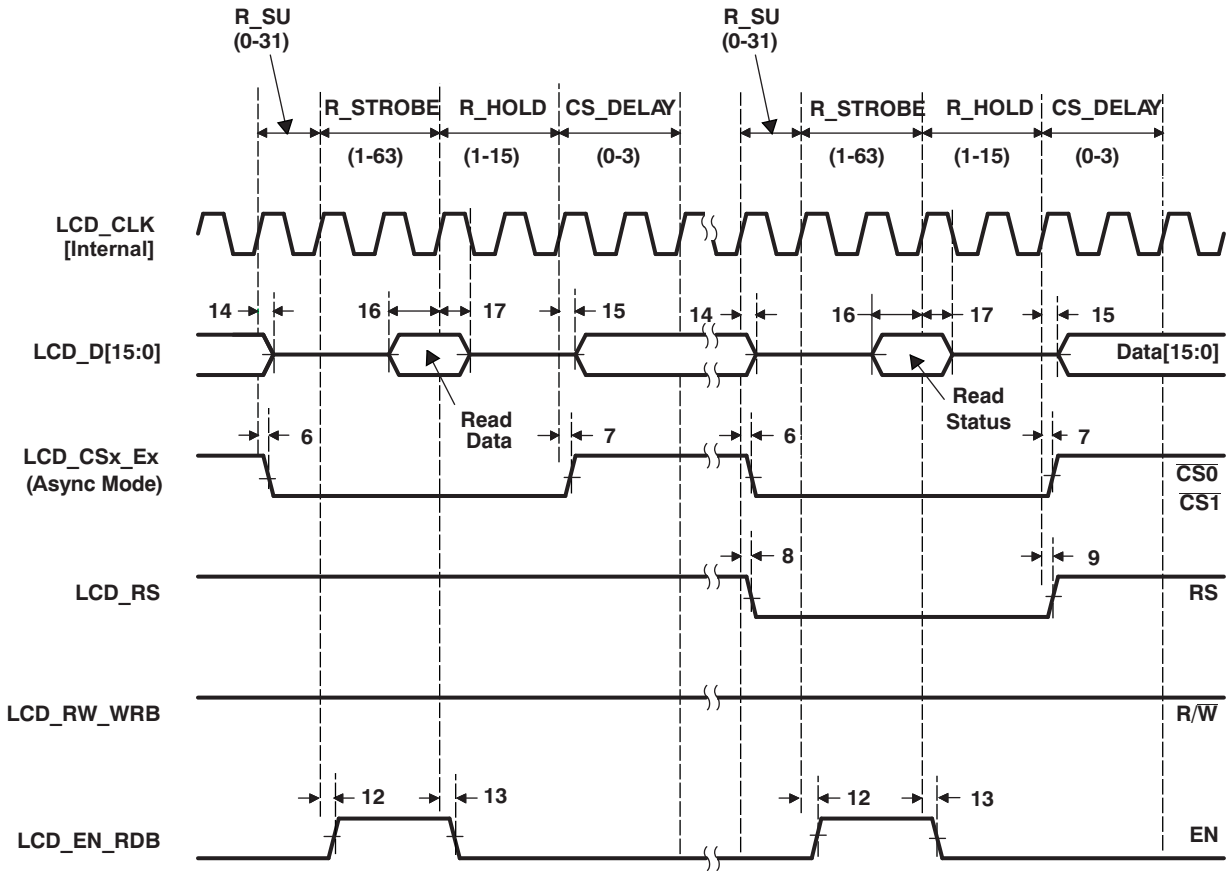


Figure 5-28. Micro-Interface Graphic Display 6800 Status

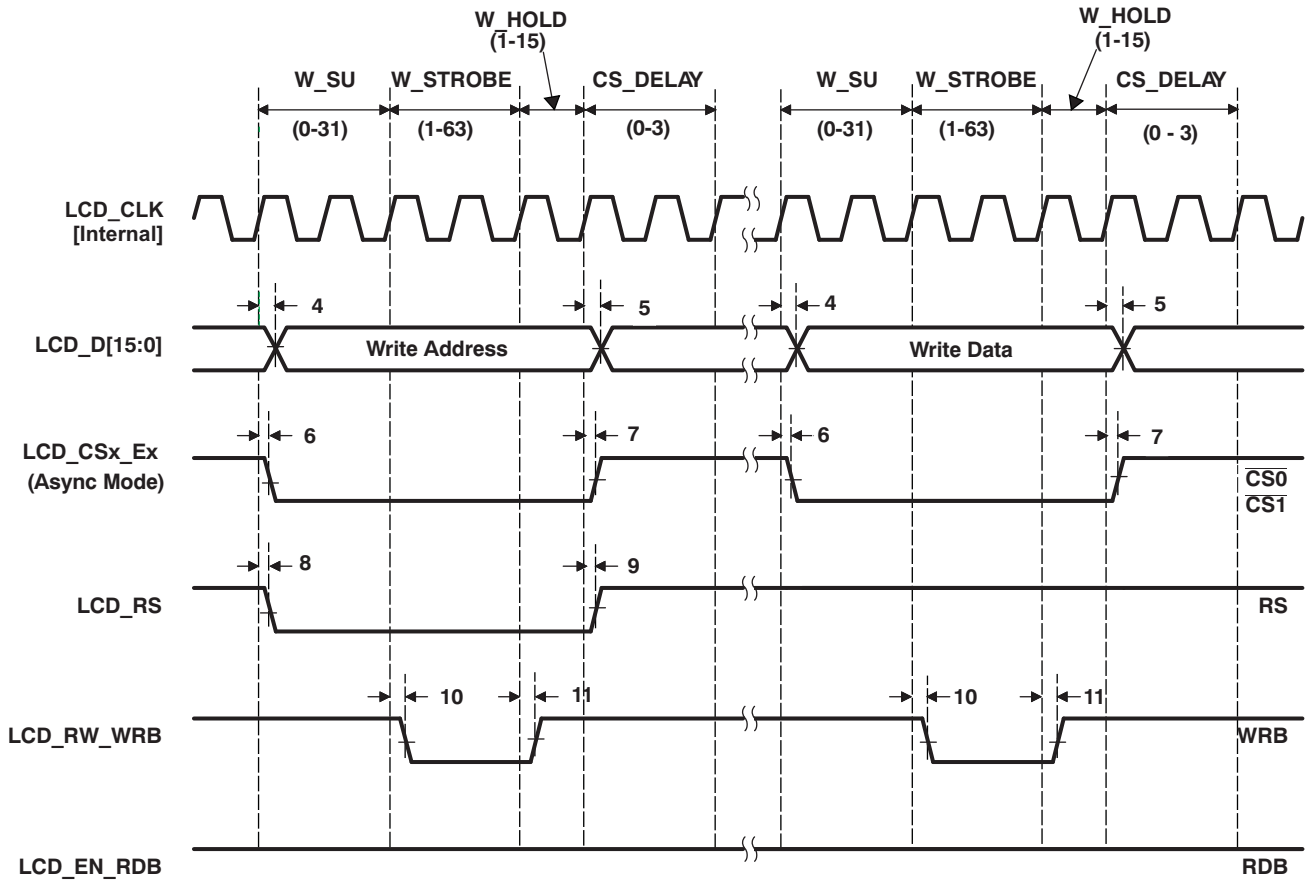


Figure 5-29. Micro-Interface Graphic Display 8080 Write

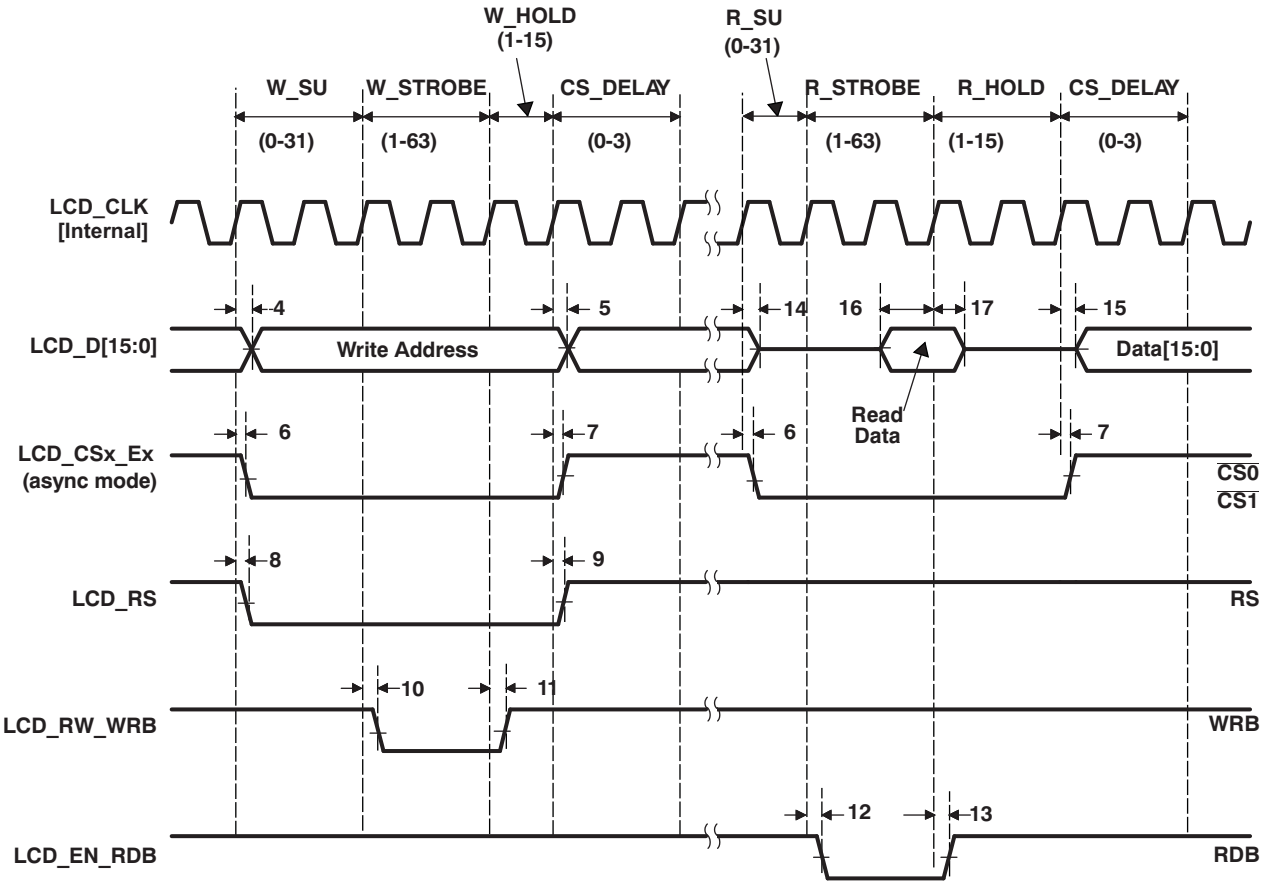


Figure 5-30. Micro-Interface Graphic Display 8080 Read

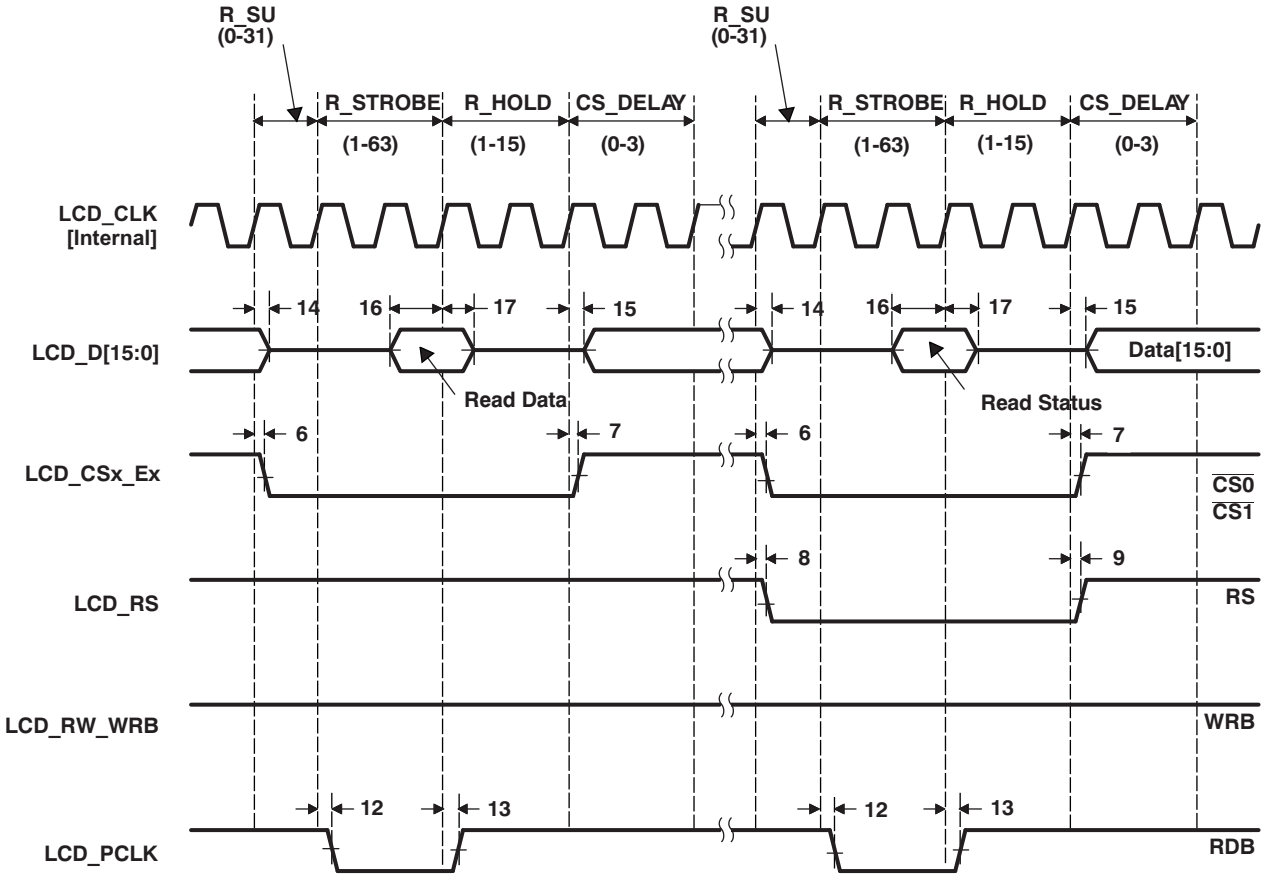


Figure 5-31. Micro-Interface Graphic Display 8080 Status

5.6.17 10-Bit SAR ADC

The device includes a 10-bit SAR ADC using a switched capacitor architecture that converts an analog input signal to a digital value at a maximum rate of 62.5-k samples per second (ksps) for the DSP. This SAR module supports six channels connected to three general purpose analog pins (GPAIN[3:1]) which can be used as general purpose outputs.

The device SAR supports the following features:

- Up to 62.5 ksps (2-MHz clock with 32 cycles per conversion)
- Single conversion and continuous back-to-back conversion modes
- Interrupt driven or polling conversion or DMA event generation
- Internal configurable bandgap reference voltages of 1 V or 0.8 V; or external V_{ref} of V_{DDA_ANA}
- Software controlled power down
- Individually configurable general-purpose digital outputs

5.6.17.1 SAR ADC Peripheral Register Descriptions

Table 5-34 lists the SAR ADC peripheral registers.

Table 5-34. SAR Analog Control Registers

CPU WORD ADDRESS	ACRONYM	REGISTER DESCRIPTION
7012h	SARCTRL	SAR A/D Control Register
7014h	SARDATA	SAR A/D Data Register
7016h	SARCLKCTRL	SAR A/D Clock Control Register
7018h	SARPINCTRL	SAR A/D Reference and Pin Control Register
701Ah	SARGPOCTRL	SAR A/D GPO Control Register

5.6.17.2 SAR ADC Electrical Data and Timing

Table 5-35 lists the switching characteristics for ADC.

Table 5-35. Switching Characteristics Over Recommended Operating Conditions for ADC Characteristics

NO.	PARAMETER		CV_{DD} = 1.3 V, CV_{DD} = 1.05 V			UNIT
			MIN	TYP	MAX	
1	$t_{C(SCLC)}$	Cycle time, ADC internal conversion clock			2	MHz
3	$t_{d(CONV)}$	Delay time, ADC conversion time			$32t_{C(SCLC)}$	ns
4	S_{DNL}	Static differential nonlinearity error (DNL measured for 9 bits)		±0.6		LSB
5	S_{INL}	Static integral nonlinearity error		±1		LSB
6	Z_{set}	Zero-scale offset error (INL measured for 9 bits)			2	LSB
7	F_{set}	Full-scale offset error			2	LSB
8		Analog input impedance	1			MΩ
9		Signal-to-noise ratio		54		dB

5.6.18 Serial Port Interface (SPI)

The device serial port interface (SPI) is a high-speed synchronous serial input/output port that allows a serial bit stream of programmed length (1 to 32 bits) to be shifted into and out of the device at a programmed bit-transfer rate. The SPI supports multi-chip operation of up to three SPI slave devices. The SPI can operate as a master device only, slave mode is not supported.

NOTE

The SPI is not supported by the device DMA controller, so DMA cannot be used in transferring data between the SPI and the on-chip RAM.

The DSP and external peripherals use the SPI to communicate. Typical applications include an interface to external I/O or peripheral expansion through devices such as shift registers, display drivers, SPI EEPROMs, and ADCs.

The SPI has the following features:

- Programmable divider for serial data clock generation
- Four pin interface (SPI_CLK, SPI_CSn, SPI_RX, and SPI_TX)
- Programmable data length (1 to 32 bits)
- Three external chip select signals
- Programmable transfer or frame size (1 to 4096 characters)
- Optional interrupt generation on character completion
- Programmable SPI_CSn to SPI_TX delay from 0 to 3 SPI_CLK cycles
- Programmable signal polarities
- Programmable active clock edge
- Internal loopback mode for testing

5.6.18.1 SPI Peripheral Register Descriptions

Table 5-36 lists the SPI registers.

Table 5-36. SPI Module Registers

CPU WORD ADDRESS	ACRONYM	REGISTER NAME
3000h	SPICDR	Clock Divider Register
3001h	SPICCR	Clock Control Register
3002h	SPIDCR1	Device Configuration Register 1
3003h	SPIDCR2	Device Configuration Register 2
3004h	SPICMD1	Command Register 1
3005h	SPICMD2	Command Register 2
3006h	SPISTAT1	Status Register 1
3007h	SPISTAT2	Status Register 2
3008h	SPIDAT1	Data Register 1
3009h	SPIDAT2	Data Register 2

5.6.18.2 SPI Electrical Data and Timing

Table 5-37 and Table 5-38 list the timing and switching requirements for the SPI, respectively.

Table 5-37. Timing Requirements for SPI Inputs (see Figure 5-32, Figure 5-33, Figure 5-34, and Figure 5-35)

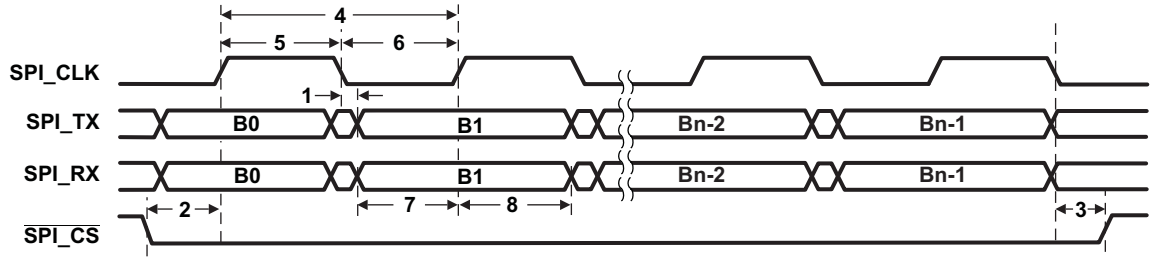
NO.			CV_{DD} = 1.05 V		CV_{DD} = 1.3 V		UNIT
			MIN	MAX	MIN	MAX	
4	$t_{C(SCLK)}$	Cycle time, SPI_CLK	66.4 or 4P(1) (2)		40 or 4P(1) (2)		ns
5	$t_{w(SCLKH)}$	Pulse duration, SPI_CLK high	30		19		ns
6	$t_{w(SCLKL)}$	Pulse duration, SPI_CLK low	30		19		ns
7	$t_{su(SRXV-SCLK)}$	Setup time, SPI_RX valid before SPI_CLK high, SPI Mode 0	16.1		13.9		ns
		Setup time, SPI_RX valid before SPI_CLK low, SPI Mode 1	16.1		13.9		ns
		Setup time, SPI_RX valid before SPI_CLK high, SPI Mode 2	16.1		13.9		ns
		Setup time, SPI_RX valid before SPI_CLK high, SPI Mode 3	16.1		13.9		ns
8	$t_{h(SCLK-SRXV)}$	Hold time, SPI_RX valid after SPI_CLK high, SPI Mode 0	0		0		ns
		Hold time, SPI_RX valid after SPI_CLK low, SPI Mode 1	0		0		ns
		Hold time, SPI_RX valid after SPI_CLK low, SPI Mode 2	0		0		ns
		Hold time, SPI_RX valid after SPI_CLK high, SPI Mode 3	0		0		ns

(1) P = SYSCLK period in ns. For example, when the CPU core is clocked at 100 MHz, use P = 10 ns.
(2) Use whichever value is greater.

Table 5-38. Switching Characteristics Over Recommended Operating Conditions for SPI Outputs (see Figure 5-32, Figure 5-33, Figure 5-34, and Figure 5-35)

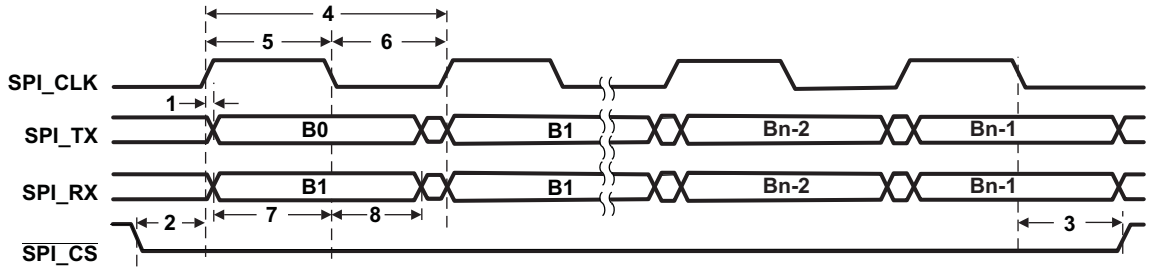
NO.	PARAMETER		CV_{DD} = 1.05 V		CV_{DD} = 1.3 V		UNIT
			MIN	MAX	MIN	MAX	
1	$t_{d(SCLK-STXV)}$	Delay time, SPI_CLK low to SPI_TX valid, SPI Mode 0	–4.2	8.9	–4.9	5.3	ns
		Delay time, SPI_CLK high to SPI_TX valid, SPI Mode 1	–4.2	8.9	–4.9	5.3	ns
		Delay time, SPI_CLK high to SPI_TX valid, SPI Mode 2	–4.2	8.9	–4.9	5.3	ns
		Delay time, SPI_CLK low to SPI_TX valid, SPI Mode 3	–4.2	8.9	–4.9	5.3	ns
2	$t_{d(SPICS-SCLK)}$	Delay time, $\overline{SPI\_CS}$ active to SPI_CLK active		t_C – 8 + D(1)		t_C – 8 + D(1)	ns
3	$t_{oh(SCLKI-SPICSI)}$	Output hold time, $\overline{SPI\_CS}$ inactive to SPI_CLK inactive	$0.5t_C$ - 2.2		$0.5t_C$ - 2.2		ns

(1) D is the programable data delay in ns. Data delay can be programmed to 0, 1, 2, or 3 SPICLK clock cycles.



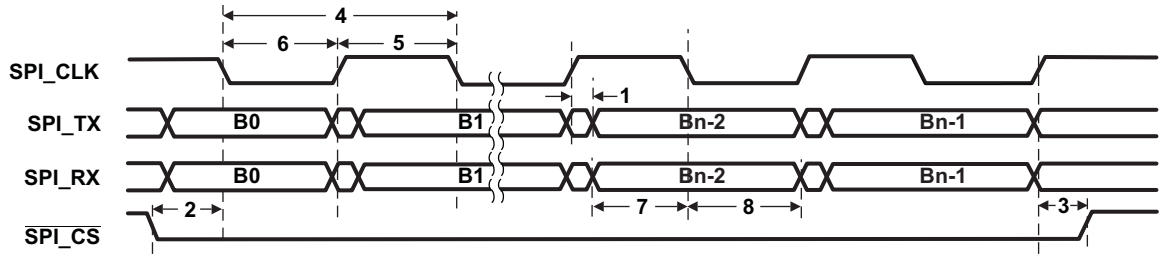
A. Character length is programmable between 1 and 32 bits; 8-bit character length shown.
B. Polarity of SPI_CSn is configurable, active-low polarity is shown.

Figure 5-32. SPI Mode 0 Transfer (CKP*n* = 0, CKPH*n* = 0)



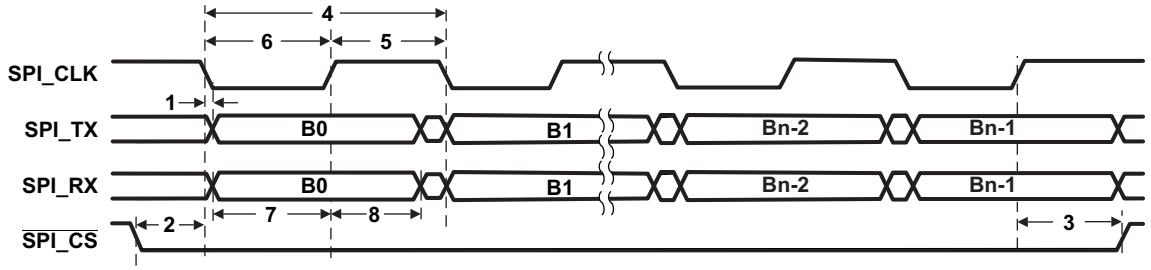
A. Character length is programmable between 1 and 32 bits; 8-bit character length shown.
B. Polarity of SPI_CSn is configurable, active-low polarity is shown.

Figure 5-33. SPI Mode 1 Transfer (CKP*n* = 0, CKPH*n* = 1)



A. Character length is programmable between 1 and 32 bits; 8-bit character length shown.
B. Polarity of SPI_CSn is configurable, active-low polarity is shown.

Figure 5-34. SPI Mode 2 Transfer (CKP*n* = 1, CKPH*n* = 0)



A. Character length is programmable between 1 and 32 bits; 8-bit character length shown.
B. Polarity of SPI_CSn is configurable, active-low polarity is shown.

Figure 5-35. SPI Mode 3 Transfer (CKP*n* = 1, CKPH*n* = 1)

5.6.19 Universal Serial Bus (USB) 2.0 Controller

The device USB 2.0 peripheral supports the following features:

- USB 2.0 peripheral at speeds high-speed (480 Mbps) and full-speed (12 Mbps)
- All transfer modes (control, bulk, interrupt, and isochronous asynchronous mode)
- Four transmit (TX) and four receive (RX) Endpoints in addition to Control Endpoint 0
- FIFO RAM
  - 4K endpoint
  - Programmable size
- Integrated USB 2.0 high-speed PHY
- RNDIS mode for accelerating RNDIS type protocols using short packet termination over USB

The USB 2.0 peripheral on this device, does not support:

- Host mode (only peripheral and device modes are supported)
- On-Chip Charge Pump
- On-the-Go (OTG) mode

5.6.19.1 USB 2.0 Peripheral Register Descriptions

Table 5-39 lists of the USB 2.0 peripheral registers.

Table 5-39. Universal Serial Bus (USB) Registers(1)

CPU WORD ADDRESS	ACRONYM	REGISTER DESCRIPTION
8000h	REVID1	Revision Identification Register 1
8001h	REVID2	Revision Identification Register 2
8004h	CTRLR	Control Register
8008h	STATR	Status Register
800Ch	EMUR	Emulation Register
8010h	MODER1	Mode Register 1
8011h	MODER2	Mode Register 2
8014h	AUTOREQ	Auto Request Register
8018h	SRPFIXTIME1	SRP Fix Time Register 1
8019h	SRPFIXTIME2	SRP Fix Time Register 2
801Ch	TEARDOWN1	Teardown Register 1
801Dh	TEARDOWN2	Teardown Register 2
8020h	INTSRCR1	USB Interrupt Source Register 1
8021h	INTSRCR2	USB Interrupt Source Register 2
8024h	INTSETR1	USB Interrupt Source Set Register 1
8025h	INTSETR2	USB Interrupt Source Set Register 2
8028h	INTCLRR1	USB Interrupt Source Clear Register 1
8029h	INTCLRR2	USB Interrupt Source Clear Register 2
802Ch	INTMSKR1	USB Interrupt Mask Register 1
802Dh	INTMSKR2	USB Interrupt Mask Register 2
8030h	INTMSKSETR1	USB Interrupt Mask Set Register 1
8031h	INTMSKSETR2	USB Interrupt Mask Set Register 2
8034h	INTMSKCLRR1	USB Interrupt Mask Clear Register 1
8035h	INTMSKCLRR2	USB Interrupt Mask Clear Register 2
8038h	INTMASKEDR1	USB Interrupt Source Masked Register 1
8039h	INTMASKEDR2	USB Interrupt Source Masked Register 2
803Ch	EOIR	USB End of Interrupt Register
8040h	INTVECTR1	USB Interrupt Vector Register 1
8041h	INTVECTR2	USB Interrupt Vector Register 2
8050h	GREP1SZR1	Generic RNDIS EP1Size Register 1
8051h	GREP1SZR2	Generic RNDIS EP1Size Register 2
8054h	GREP2SZR1	Generic RNDIS EP2 Size Register 1
8055h	GREP2SZR2	Generic RNDIS EP2 Size Register 2
8058h	GREP3SZR1	Generic RNDIS EP3 Size Register 1
8059h	GREP3SZR2	Generic RNDIS EP3 Size Register 2
805Ch	GREP4SZR1	Generic RNDIS EP4 Size Register 1
805Dh	GREP4SZR2	Generic RNDIS EP4 Size Register 2

(1) Before reading or writing to the USB registers, be sure to set the BYTEMODE bits to 00b in the USB system control register to enable word accesses to the USB registers .

Table 5-39. Universal Serial Bus (USB) Registers[1] (continued)

CPU WORD ADDRESS	ACRONYM	REGISTER DESCRIPTION
		Common USB Registers
8401h	FADDR_POWER	Function Address Register, Power Management Register
8402h	INTRTX	Interrupt Register for Endpoint 0 plus Transmit Endpoints 1 to 4
8405h	INTRRX	Interrupt Register for Receive Endpoints 1 to 4
8406h	INTRTXE	Interrupt enable register for INTRTX
8409h	INTRRXE	Interrupt Enable Register for INTRRX
840Ah	INTRUSB_INTRUSBE	Interrupt Register for Common USB Interrupts, Interrupt Enable Register
840Dh	FRAME	Frame Number Register
840Eh	INDEX_TESTMODE	Index Register for Selecting the Endpoint Status and Control Registers, Register to Enable the USB 2.0 Test Modes
		USB Indexed Registers
8411h	TXMAXP_INDX	Maximum Packet Size for Peripheral and Host Transmit Endpoint. (Index register set to select Endpoints 1-4)
8412h	PERI_CSR0_INDX	Control Status Register for Endpoint 0 in Peripheral Mode. (Index register set to select Endpoint 0)
	PERI_TXCSR_INDX	Control Status Register for Peripheral Transmit Endpoint. (Index register set to select Endpoints 1-4)
8415h	RXMAXP_INDX	Maximum Packet Size for Peripheral and Host Receive Endpoint. (Index register set to select Endpoints 1-4)
8416h	PERI_RXCSR_INDX	Control Status Register for Peripheral Receive Endpoint. (Index register set to select Endpoints 1-4)
8419h	COUNT0_INDX	Number of Received Bytes in Endpoint 0 FIFO. (Index register set to select Endpoint 0)
	RXCOUNT_INDX	Number of Bytes in Host Receive Endpoint FIFO. (Index register set to select Endpoints 1- 4)
841Ah	–	Reserved
841Dh	–	Reserved
841Eh	CONFIGDATA_INDC (Upper byte of 841Eh)	Returns details of core configuration. (index register set to select Endpoint 0)
		USB FIFO Registers
8421h	FIFO0R1	Transmit and Receive FIFO Register 1 for Endpoint 0
8422h	FIFO0R2	Transmit and Receive FIFO Register 2 for Endpoint 0
8425h	FIFO1R1	Transmit and Receive FIFO Register 1 for Endpoint 1
8426h	FIFO1R2	Transmit and Receive FIFO Register 2 for Endpoint 1
8429h	FIFO2R1	Transmit and Receive FIFO Register 1 for Endpoint 2
842Ah	FIFO2R2	Transmit and Receive FIFO Register 2 for Endpoint 2
842Dh	FIFO3R1	Transmit and Receive FIFO Register 1 for Endpoint 3
842Eh	FIFO3R2	Transmit and Receive FIFO Register 2 for Endpoint 3
8431h	FIFO4R1	Transmit and Receive FIFO Register 1 for Endpoint 4
8432h	FIFO4R2	Transmit and Receive FIFO Register 2 for Endpoint 4
		Dynamic FIFO Control Registers
8461h	DEVCTL	Device Control Register
8462h	TXFIFOSZ_RXFIFOSZ	Transmit Endpoint FIFO Size, Receive Endpoint FIFO Size (Index register set to select Endpoints 1-4)
8465h	TXFIFOADDR	Transmit Endpoint FIFO Address (Index register set to select Endpoints 1-4)
8466h	RXFIFOADDR	Receive Endpoint FIFO Address (Index register set to select Endpoints 1-4)
846Dh	–	Reserved

Table 5-39. Universal Serial Bus (USB) Registers[1] (continued)

CPU WORD ADDRESS	ACRONYM	REGISTER DESCRIPTION
		Control and Status Register for Endpoint 0
8501h	–	Reserved
8502h	PERI_CSR0	Control Status Register for Peripheral Endpoint 0
8505h	–	Reserved
8506h	–	Reserved
8509h	COUNT0	Number of Received Bytes in Endpoint 0 FIFO
850Ah	–	Reserved
850Dh	–	Reserved
850Eh	CONFIGDATA (Upper byte of 850Eh)	Returns details of core configuration.
		Control and Status Register for Endpoint 1
8511h	TXMAXP	Maximum Packet Size for Peripheral and Host Transmit Endpoint
8512h	PERI_TXCSR	Control Status Register for Peripheral Transmit Endpoint (peripheral mode)
8515h	RXMAXP	Maximum Packet Size for Peripheral and Host Receive Endpoint
8516h	PERI_RXCSR	Control Status Register for Peripheral Receive Endpoint (peripheral mode)
8519h	RXCOUNT	Number of Bytes in the Receiving Endpoint's FIFO
851Ah	–	Reserved
851Dh	–	Reserved
851Eh	–	Reserved
		Control and Status Register for Endpoint 2
8521h	TXMAXP	Maximum Packet Size for Peripheral and Host Transmit Endpoint
8522h	PERI_TXCSR	Control Status Register for Peripheral Transmit Endpoint (peripheral mode)
8525h	RXMAXP	Maximum Packet Size for Peripheral and Host Receive Endpoint
8526h	PERI_RXCSR	Control Status Register for Peripheral Receive Endpoint (peripheral mode)
8529h	RXCOUNT	Number of Bytes in Host Receive endpoint FIFO
852Ah	–	Reserved
852Dh	–	Reserved
852Eh	–	Reserved
		Control and Status Register for Endpoint 3
8531h	TXMAXP	Maximum Packet Size for Peripheral and Host Transmit Endpoint
8532h	PERI_TXCSR	Control Status Register for Peripheral Transmit Endpoint (peripheral mode)
8535h	RXMAXP	Maximum Packet Size for Peripheral and Host Receive Endpoint
8536h	PERI_RXCSR	Control Status Register for Peripheral Receive Endpoint (peripheral mode)
8539h	RXCOUNT	Number of Bytes in Host Receive endpoint FIFO
853Ah	–	Reserved
853Dh	–	Reserved
853Eh	–	Reserved
		Control and Status Register for Endpoint 4
8541h	TXMAXP	Maximum Packet Size for Peripheral and Host Transmit Endpoint
8542h	PERI_TXCSR	Control Status Register for Peripheral Transmit Endpoint (peripheral mode)
8545h	RXMAXP	Maximum Packet Size for Peripheral and Host Receive Endpoint
8546h	PERI_RXCSR	Control Status Register for Peripheral Receive Endpoint (peripheral mode)
8549h	RXCOUNT	Number of Bytes in Host Receive endpoint FIFO
854Ah	–	Reserved
854Dh	–	Reserved
854Eh	–	Reserved

Table 5-39. Universal Serial Bus (USB) Registers[1] (continued)

CPU WORD ADDRESS	ACRONYM	REGISTER DESCRIPTION
		CPPI DMA (CMDA) Registers
9000h	–	Reserved
9001h	–	Reserved
9004h	TDFDQ	CDMA Teardown Free Descriptor Queue Control Register
9008h	DMAEMU	CDMA Emulation Control Register
9800h	TXGCR1[0]	Transmit Channel 0 Global Configuration Register 1
9801h	TXGCR2[0]	Transmit Channel 0 Global Configuration Register 2
9808h	RXGCR1[0]	Receive Channel 0 Global Configuration Register 1
9809h	RXGCR2[0]	Receive Channel 0 Global Configuration Register 2
980Ch	RXHPCR1A[0]	Receive Channel 0 Host Packet Configuration Register 1 A
980Dh	RXHPCR2A[0]	Receive Channel 0 Host Packet Configuration Register 2 A
9810h	RXHPCR1B[0]	Receive Channel 0 Host Packet Configuration Register 1 B
9811h	RXHPCR2B[0]	Receive Channel 0 Host Packet Configuration Register 2 B
9820h	TXGCR1[1]	Transmit Channel 1 Global Configuration Register 1
9821h	TXGCR2[1]	Transmit Channel 1 Global Configuration Register 2
9828h	RXGCR1[1]	Receive Channel 1 Global Configuration Register 1
9829h	RXGCR2[1]	Receive Channel 1 Global Configuration Register 2
982Ch	RXHPCR1A[1]	Receive Channel 1 Host Packet Configuration Register 1 A
982Dh	RXHPCR2A[1]	Receive Channel 1 Host Packet Configuration Register 2 A
9830h	RXHPCR1B[1]	Receive Channel 1 Host Packet Configuration Register 1 B
9831h	RXHPCR2B[1]	Receive Channel 1 Host Packet Configuration Register 2 B
9840h	TXGCR1[2]	Transmit Channel 2 Global Configuration Register 1
9841h	TXGCR2[2]	Transmit Channel 2 Global Configuration Register 2
9848h	RXGCR1[2]	Receive Channel 2 Global Configuration Register 1
9849h	RXGCR2[2]	Receive Channel 2 Global Configuration Register 2
984Ch	RXHPCR1A[2]	Receive Channel 2 Host Packet Configuration Register 1 A
984Dh	RXHPCR2A[2]	Receive Channel 2 Host Packet Configuration Register 2 A
9850h	RXHPCR1B[2]	Receive Channel 2 Host Packet Configuration Register 1 B
9851h	RXHPCR2B[2]	Receive Channel 2 Host Packet Configuration Register 2 B
9860h	TXGCR1[3]	Transmit Channel 3 Global Configuration Register 1
9861h	TXGCR2[3]	Transmit Channel 3 Global Configuration Register 2
9868h	RXGCR1[3]	Receive Channel 3 Global Configuration Register 1
9869h	RXGCR2[3]	Receive Channel 3 Global Configuration Register 2
986Ch	RXHPCR1A[3]	Receive Channel 3 Host Packet Configuration Register 1 A
986Dh	RXHPCR2A[3]	Receive Channel 3 Host Packet Configuration Register 2 A
9870h	RXHPCR1B[3]	Receive Channel 3 Host Packet Configuration Register 1 B
9871h	RXHPCR2B[3]	Receive Channel 3 Host Packet Configuration Register 2 B
A000h	DMA_SCHED_CTRL1	CDMA Scheduler Control Register 1
A001h	DMA_SCHED_CTRL2	CDMA Scheduler Control Register 1
A800h + 4 × *N*	ENTRYLSW[*N*]	CDMA Scheduler Table Word *N* Registers LSW (*N* = 0 to 63)
A801h + 4 × *N*	ENTRYMSW[*N*]	CDMA Scheduler Table Word *N* Registers MSW (*N* = 0 to 63)

Table 5-39. Universal Serial Bus (USB) Registers[(1)] (continued)

CPU WORD ADDRESS	ACRONYM	REGISTER DESCRIPTION
		Queue Manager (QMGR) Registers
C000h	–	Reserved
C001h	–	Reserved
C008h	DIVERSION1	Queue Manager Queue Diversion Register 1
C009h	DIVERSION2	Queue Manager Queue Diversion Register 2
C020h	FDBSC0	Queue Manager Free Descriptor and Buffer Starvation Count Register 0
C021h	FDBSC1	Queue Manager Free Descriptor and Buffer Starvation Count Register 1
C024h	FDBSC2	Queue Manager Free Descriptor and Buffer Starvation Count Register 2
C025h	FDBSC3	Queue Manager Free Descriptor and Buffer Starvation Count Register 3
C028h	FDBSC4	Queue Manager Free Descriptor and Buffer Starvation Count Register 4
C029h	FDBSC5	Queue Manager Free Descriptor and Buffer Starvation Count Register 5
C02Ch	FDBSC6	Queue Manager Free Descriptor and Buffer Starvation Count Register 6
C02Dh	FDBSC7	Queue Manager Free Descriptor and Buffer Starvation Count Register 7
C080h	LRAM0BASE1	Queue Manager Linking RAM Region 0 Base Address Register 1
C081h	LRAM0BASE2	Queue Manager Linking RAM Region 0 Base Address Register 2
C084h	LRAM0SIZE	Queue Manager Linking RAM Region 0 Size Register
C085h	–	Reserved
C088h	LRAM1BASE1	Queue Manager Linking RAM Region 1 Base Address Register 1
C089h	LRAM1BASE2	Queue Manager Linking RAM Region 1 Base Address Register 2
C090h	PEND0	Queue Manager Queue Pending 0
C091h	PEND1	Queue Manager Queue Pending 1
C094h	PEND2	Queue Manager Queue Pending 2
C095h	PEND3	Queue Manager Queue Pending 3
C098h	PEND4	Queue Manager Queue Pending 4
C099h	PEND5	Queue Manager Queue Pending 5
D000h + 16 × *R*	QMEMRBASE1[*R*]	Queue Manager Memory Region *R* Base Address Register 1 (*R* = 0 to 15)
D001h + 16 × *R*	QMEMRBASE2[*R*]	Queue Manager Memory Region *R* Base Address Register 2 (*R* = 0 to 15)
D004h + 16 × *R*	QMEMRCTRL1[*R*]	Queue Manager Memory Region *R* Control Register (*R* = 0 to 15)
D005h + 16 × *R*	QMEMRCTRL2[*R*]	Queue Manager Memory Region *R* Control Register (*R* = 0 to 15)
E000h + 16 × *N*	CTRL1A	Queue Manager Queue *N* Control Register 1A (*N* = 0 to 63)
E001h + 16 × *N*	CTRL2A	Queue Manager Queue *N* Control Register 2A (*N* = 0 to 63)
E004h + 16 × *N*	CTRL1B	Queue Manager Queue *N* Control Register 1B (*N* = 0 to 63)
E005h + 16 × *N*	CTRL2B	Queue Manager Queue *N* Control Register 2B (*N* = 0 to 63)
E008h + 16 × *N*	CTRL1C	Queue Manager Queue *N* Control Register 1C (*N* = 0 to 63)
E009h + 16 × *N*	CTRL2C	Queue Manager Queue *N* Control Register 2C (*N* = 0 to 63)
E00Ch + 16 × *N*	CTRL1D	Queue Manager Queue *N* Control Register 1D (*N* = 0 to 63)
E00Dh + 16 × *N*	CTRL2D	Queue Manager Queue *N* Control Register 2D (*N* = 0 to 63)
E800h + 16 × *N*	QSTAT1A	Queue Manager Queue *N* Status Register 1A (*N* = 0 to 63)
E801h + 16 × *N*	QSTAT2A	Queue Manager Queue *N* Status Register 2A (*N* = 0 to 63)
E804h + 16 × *N*	QSTAT1B	Queue Manager Queue *N* Status Register 1B (*N* = 0 to 63)
E805h + 16 × *N*	QSTAT2B	Queue Manager Queue *N* Status Register 2B (*N* = 0 to 63)
E808h + 16 × *N*	QSTAT1C	Queue Manager Queue *N* Status Register 1C (*N* = 0 to 63)
E809h + 16 × *N*	QSTAT1C	Queue Manager Queue *N* Status Register 2C (*N* = 0 to 63)

5.6.19.2 USB 2.0 Electrical Data and Timing

Table 5-40 lists the switching characteristics USB 2.0.

Table 5-40. Switching Characteristics Over Recommended Operating Conditions for USB 2.0 (see Figure 5-36)

NO.	PARAMETER		CV_{DD} = 1.05 V, CV_{DD} = 1.3 V				UNIT
			FULL SPEED 12 Mbps		HIGH SPEED 480 Mbps(1)		
			MIN	MAX	MIN	MAX	
1	$t_{r(D)}$	Rise time, USB_DP and USB_DM signals(2)	4	20	0.5		ns
2	$t_{f(D)}$	Fall time, USB_DP and USB_DM signals(2)	4	20	0.5		ns
3	t_{rfM}	Rise and Fall time, matching(3)	90	111	–	–	
4	V_{CRS}	Output signal cross-over voltage(2)	1.3	2	–	–	V
7	$t_{w(EOPT)}$	Pulse duration, EOP transmitter(4)	160	175	–	–	ns
8	$t_{w(EOPR)}$	Pulse duration, EOP receiver(4)	82		–		ns
9	$t_{(DRATE)}$	Data Rate		12		480	Mbps
10	Z_{DRV}	Driver Output Resistance	40.5	49.5	40.5	49.5	Ω
11	Z_{INP}	Receiver Input Impedance	100k		–	–	Ω

(1) For more detailed information, see the Universal Serial Bus Specification, Revision 2.0, Chapter 7.
(2) Full speed and high speed C_L = 50 pF
(3) $t_{RFM} = (t_r/t_f) \times 100$. [Excluding the first transaction from the IDLE state.]
(4) Must accept as valid EOP.

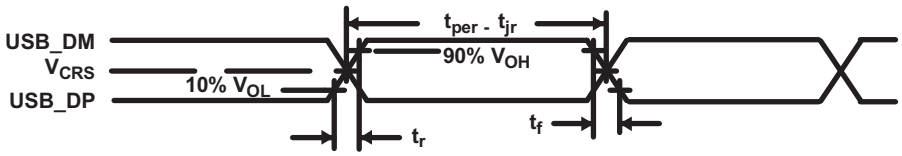


Figure 5-36. USB 2.0 Integrated Transceiver Interface Timing

5.6.20 General-Purpose Timers

The device has three 32-bit software programmable timers. Each timer can be used as a general-purpose (GP) timer. Timer2 can be configured as either a GP or a Watchdog (WD) or both. General-purpose timers are typically used to provide interrupts to the CPU to schedule periodic tasks or a delayed task. A watchdog timer is used to reset the CPU in case it gets into an infinite loop. The GP timers are 32-bit timers with a 13-bit prescaler that can divide the CPU clock and uses this scaled value as a reference clock. These timers can be used to generate periodic interrupts. The watchdog timer is a 16-bit counter with a 16-bit prescaler used to provide a recovery mechanism for the device in the event of a fault condition, such as a nonexiting code loop.

The device timers support the following:

- A 32-bit programmable countdown timer
- A 13-bit prescaler divider
- Timer modes:
  - 32-bit general-purpose timer
  - 32-bit watchdog timer (Timer2 only)
- An auto-reload option
- Generating a single interrupt to CPU (The interrupt is individually latched to determine which timer triggered the interrupt.)
- Generating an active low pulse to the hardware reset (watchdog only)
- Using an interrupt for a DMA event

5.6.20.1 Timers Peripheral Register Descriptions

Table 5-41, Table 5-42, Table 5-43, and Table 5-44 list the timer and watchdog registers.

Table 5-41. Watchdog Timer Registers (Timer2 Only)

CPU WORD ADDRESS	ACRONYM	REGISTER DESCRIPTION
1880h	WDKCKLK	Watchdog Kick Lock Register
1882h	WDKICK	Watchdog Kick Register
1884h	WDSVLR	Watchdog Start Value Lock Register
1886h	WDSVR	Watchdog Start Value Register
1888h	WDENLOK	Watchdog Enable Lock Register
188Ah	WDEN	Watchdog Enable Register
188Ch	WDPSLR	Watchdog Prescale Lock Register
188Eh	WDPS	Watchdog Prescale Register

Table 5-42. General-Purpose Timer 0 Registers

CPU WORD ADDRESS	ACRONYM	REGISTER DESCRIPTION
1810h	TCR	Timer 0 Control Register
1812h	TIMPRD1	Timer 0 Period Register 1
1813h	TIMPRD2	Timer 0 Period Register 2
1814h	TIMCNT1	Timer 0 Counter Register 1
1815h	TIMCNT2	Timer 0 Counter Register 2

Table 5-43. General-Purpose Timer 1 Registers

CPU WORD ADDRESS	ACRONYM	REGISTER DESCRIPTION
1850h	TCR	Timer 1 Control Register
1852h	TIMPRD1	Timer 1 Period Register 1
1853h	TIMPRD2	Timer 1 Period Register 2
1854h	TIMCNT1	Timer 1 Counter Register 1
1855h	TIMCNT2	Timer 1 Counter Register 2

Table 5-44. General-Purpose Timer 2 Registers

CPU WORD ADDRESS	ACRONYM	REGISTER DESCRIPTION
1890h	TCR	Timer 2 Control Register
1892h	TIMPRD1	Timer 2 Period Register 1
1893h	TIMPRD2	Timer 2 Period Register 2
1894h	TIMCNT1	Timer 2 Counter Register 1
1895h	TIMCNT2	Timer 2 Counter Register 2

5.6.21 General-Purpose Input and Output

The GPIO peripheral provides general-purpose pins that can be configured as either inputs or outputs. When configured as an output, you can write to an internal register to control the state driven on the output pin. When configured as an input, you can detect the state of the input by reading the state of the internal register. The GPIO can also send interrupts to the CPU.

The GPIO peripheral supports the following:

- 32 GPIO pins and 3 special-purpose outputs for use with SAR
  - Configure up to 20 GPIO pins simultaneously
- Each GPIO pin has internal pulldowns (IPDs) which can be individually disabled
- Each GPIO pin can be configured to generate edge detected interrupts to the CPU on either the rising or falling edge

The device GPIO pin functions are multiplexed with various other signals. For more detailed information on what signals are multiplexed with the GPIO and how to configure them, see Section 4.2, *Terminal Functions* and Section 6, *Device Configuration* of this document.

5.6.21.1 General-Purpose Input and Output Peripheral Register Descriptions

The external parallel port interface includes a 16-bit general purpose I/O that can be individually programmed as input or output with interrupt capability. Control of the general purpose I/O is maintained through a set of I/O memory-mapped registers listed in Table 5-45.

Table 5-45. GPIO Registers

HEX ADDRESS RANGE	ACRONYM	REGISTER NAME
1C06h	IODIR1	GPIO Direction Register 1
1C07h	IODIR2	GPIO Direction Register 2
1C08h	IOINDATA1	GPIO Data In Register 1
1C09h	IOINDATA2	GPIO Data In Register 2
1C0Ah	IODATAOUT1	GPIO Data Out Register 1
1C0Bh	IODATAOUT2	GPIO Data Out Register 2
1C0Ch	IOINTEDG1	GPIO Interrupt Edge Trigger Enable Register 1
1C0Dh	IOINTEDG2	GPIO Interrupt Edge Trigger Enable Register 2
1C0Eh	IOINTEN1	GPIO Interrupt Enable Register 1
1C0Fh	IOINTEN2	GPIO Interrupt Enable Register 2
1C10h	IOINTFLG1	GPIO Interrupt Flag Register 1
1C11h	IOINTFLG2	GPIO Interrupt Flag Register 2

5.6.21.2 GPIO Peripheral Input and Output Electrical Data and Timing

Table 5-46 and Table 5-47 lists the timing and switching requirements for GPIO, respectively.

Table 5-46. Timing Requirements for GPIO Inputs(1) (see Figure 5-37)

NO.			CV_{DD} = 1.05 V CV_{DD} = 1.3 V		UNIT
			MIN	MAX	
1	$t_{w(ACTIVE)}$	Pulse duration, GPIO input and external interrupt pulse active	2C(1) (2)		ns
2	$t_{w(INACTIVE)}$	Pulse duration, GPIO input and external interrupt pulse inactive	C (1) (2)		ns

(1) The pulse width given is sufficient to get latched into the GPIO_IFR register and to generate an interrupt. If you want the device recognize the GPIO changes through software polling of the GPIO Data In (GPIO_DIN) register, the GPIO duration must be extended to allow the device enough time to access the GPIO register through the internal bus.
(2) C = SYSCLK period in ns. For example, when running parts at 100 MHz, use C = 10 ns.

Table 5-47. Switching Characteristics Over Recommended Operating Conditions for GPIO Outputs (see Figure 5-37)

NO.	PARAMETER		CV_{DD} = 1.05 V CV_{DD} = 1.3 V		UNIT
			MIN	MAX	
3	$t_{w(GPOH)}$	Pulse duration, GP[x] output high	3C(1) (2)		ns
4	$t_{w(GPOL)}$	Pulse duration, GP[x] output low	3C(1) (2)		ns

(1) This parameter value should not be used as a maximum performance specification. Actual performance of back-to-back accesses of the GPIO is dependent upon internal bus activity.
(2) C = SYSCLK period in ns. For example, when running parts at 100 MHz, use C = 10 ns.

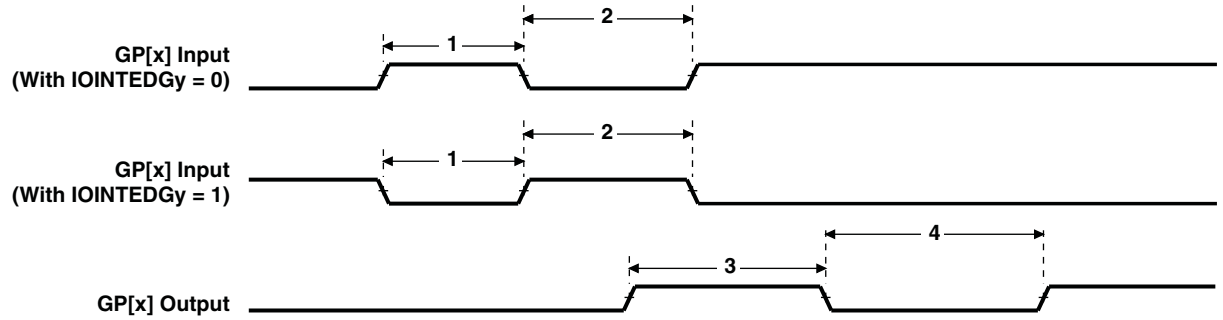


Figure 5-37. GPIO Port Timing

5.6.21.3 GPIO Peripheral Input Latency Electrical Data and Timing

Table 5-48 lists the iming requirements for GPIO input latency.

Table 5-48. Timing Requirements for GPIO Input Latency(1)

NO.			CV_{DD} = 1.05 V CV_{DD} = 1.3 V		UNIT
			MIN	MAX	
1	$t_{L(GPI)}$ Latency, GP[x] input	Polling GPIO_DIN register	5		cyc
		Polling GPIO_IFR register	7		cyc
		Interrupt detection	8		cyc

(1) The pulse width given is sufficient to generate a CPU interrupt. However, if a user wants to have the device recognize the GP[x] input changes through software polling of the GPIO register, the GP[x] input duration must be extended to allow device enough time to access the GPIO register through the internal bus.

5.6.22 IEEE 1149.1 JTAG

The JTAG interface is used for boundary-scan testing and emulation of the device.

$\overline{\text{TRST}}$ should only to be deasserted when it is necessary to use a JTAG controller to debug the device or exercise the boundary-scan functionality of the device.

The device includes an internal pulldown (IPD) on the $\overline{\text{TRST}}$ pin to ensure that $\overline{\text{TRST}}$ will always be asserted upon power up and the internal emulation logic of the device will always be properly initialized. TI also recommends an external pulldown to ensure proper device operation when an emulation or boundary-scan JTAG controller is not connected to the JTAG pins. JTAG controllers from TI actively drive $\overline{\text{TRST}}$ high. However, some third-party JTAG controllers may not drive $\overline{\text{TRST}}$ high but expect the use of a pullup resistor on $\overline{\text{TRST}}$. When using this type of JTAG controller, assert $\overline{\text{TRST}}$ to initialize the device after powerup and externally drive $\overline{\text{TRST}}$ high before trying any emulation or boundary-scan operations. The device will not operate properly if $\overline{\text{TRST}}$ is not asserted low during power up.

5.6.22.1 JTAG ID (JTAGID) Register Descriptions

The JTAGID register is provided in Table 5-49 and Figure 5-38 and described in Table 5-50.

Table 5-49. JTAG ID Register

HEX ADDRESS RANGE	ACRONYM	REGISTER NAME	COMMENTS
N/A	JTAGID	JTAG Identification Register	Read-only. Provides 32-bit JTAG ID of the device.

The JTAG ID register is a read-only register that identifies to the customer the JTAG/Device ID. The register hex value for the device is: 0x1B8F E02F. For the actual register bit names and their associated bit field descriptions, see Figure 5-38 and Table 5-50.

31-28	27-12	11-1	0
VARIANT (4-Bit)	PART NUMBER (16-Bit)	MANUFACTURER (11-Bit)	LSB
R-0001	R-1011 1000 1111 1110	R-0000 0010 111	R-1

LEGEND: R = Read, W = Write, n = value at reset

Figure 5-38. JTAG ID Register Description — 0x1B8F E02F

Table 5-50. JTAG ID Register Selection Bit Descriptions

BIT	NAME	DESCRIPTION
31:28	VARIANT	Variant (4-bit) value: 0001.
27:12	PART NUMBER	Part Number (16-bit) value: 1011 1000 1111 1110.
11:1	MANUFACTURER	Manufacturer (11-bit) value: 0000 0010 111.
0	LSB	LSB. This bit is read as 1.

5.6.22.2 JTAG Test_port Electrical Data and Timing

Table 5-51 and Table 5-52 list the timing and switching requirements for JTAG test port.

Table 5-51. Timing Requirements for JTAG Test Port (see Figure 5-39)

NO.			CV_{DD} = 1.05 V CV_{DD} = 1.3 V		UNIT
			MIN	MAX	
2	$t_{c(TCK)}$	Cycle time, TCK	60		ns
3	$t_{w(TCKH)}$	Pulse duration, TCK high	24		ns
4	$t_{w(TCKL)}$	Pulse duration, TCK low	24		ns
5	$t_{su(TDIV-TCKH)}$	Setup time, TDI valid before TCK high	10		ns
6	$t_{su(TMSV-TCKH)}$	Setup time, TMS valid before TCK high	6		ns
7	$t_{h(TCKH-TDIV)}$	Hold time, TDI valid after TCK high	5		ns
8	$t_{h(TCKH-TDIV)}$	Hold time, TMS valid after TCK high	4		ns

Table 5-52. Switching Characteristics Over Recommended Operating Conditions for JTAG Test Port (see Figure 5-39)

NO.	PARAMETER		CV_{DD} = 1.05 V CV_{DD} = 1.3 V		UNIT
			MIN	MAX	
1	$t_{d(TCKL-TDOV)}$	Delay time, TCK low to TDO valid		30.5	ns

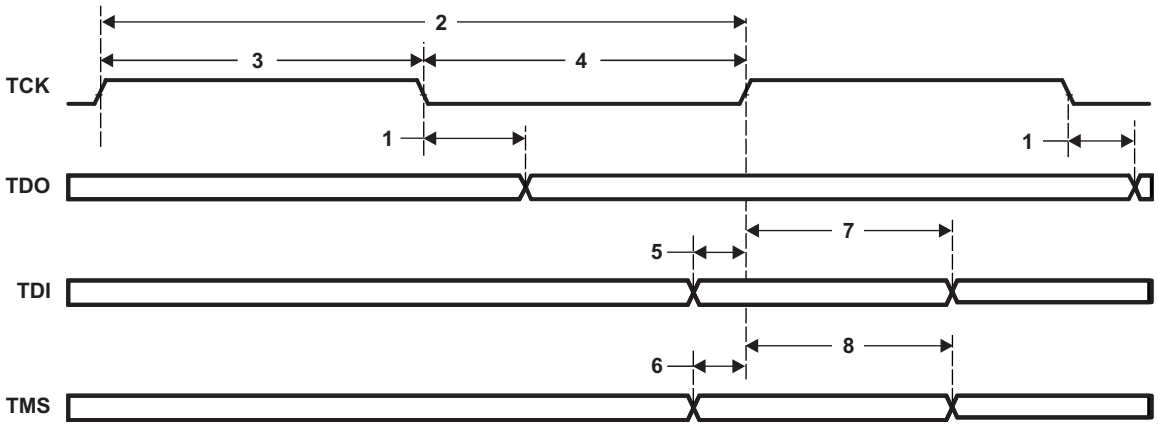


Figure 5-39. JTAG Test-Port Timing

6 Detailed Description

6.1 C55x CPU

The fixed-point digital signal processors (DSPs) are based on the C55x CPU 3.3 generation processor core. The C55x DSP architecture achieves high performance and low power through increased parallelism and total focus on power savings. The CPU supports an internal bus structure that is composed of one program bus, three data read buses (one 32-bit data read bus and two 16-bit data read buses), two 16-bit data write buses, and additional buses dedicated to peripheral and DMA activity. These buses provide the ability to perform up to four data reads and two data writes in a single cycle. Each DMA controller can perform one 32-bit data transfer per cycle, in parallel and independent of the CPU activity.

The C55x CPU provides two multiply-and-accumulate (MAC) units, each capable of 17-bit × 17-bit multiplication in a single cycle. A central 40-bit arithmetic and logic unit (ALU) is supported by an additional 16-bit ALU. Use of the ALUs is under instruction set control, providing the ability to optimize parallel activity and power consumption. These resources are managed in the address unit (AU) and data unit (DU) of the C55x CPU.

The C55x DSP generation supports a variable byte width instruction set for improved code density. The instruction unit (IU) performs 32-bit program fetches from internal or external memory, stores them in a 128-byte instruction buffer queue, and queues instructions for the program unit (PU). The PU decodes the instructions, directs tasks to AU and DU resources, and manages the fully protected pipeline. Predictive branching capability avoids pipeline flushes on execution of conditional instruction calls.

For more detailed information on the CPU, see the TMS320C55x CPU 3.0 CPU Reference Guide.

6.1.1 On-Chip Dual-Access RAM (DARAM)

The DARAM is in the byte address range 000000h to 00FFFFh and is composed of eight blocks of 4K words each (see Table 6-1). Each DARAM block can perform two accesses per cycle (two reads, two writes, or a read and a write). The DARAM can be accessed by the internal program, data, or DMA buses.

Table 6-1. DARAM Blocks

CPU BYTE ADDRESS RANGE	DMA CONTROLLER BYTE ADDRESS RANGE	MEMORY BLOCK
000000h to 001FFFh	0001 0000h to 0001 1FFFh	DARAM 0 (1)
002000h to 003FFFh	0001 2000h to 0001 3FFFh	DARAM 1
004000h to 005FFFh	0001 4000h to 0001 5FFFh	DARAM 2
006000h to 007FFFh	0001 6000h to 0001 7FFFh	DARAM 3
008000h to 009FFFh	0001 8000h to 0001 9FFFh	DARAM 4
00A000h to 00BFFFh	0001 A000h to 0001 BFFFh	DARAM 5
00C000h to 00DFFFh	0001 C000h to 0001 DFFFh	DARAM 6
00E000h to 00FFFFh	0001 E000h to 0001 FFFFh	DARAM 7

(1) The first 192 bytes are reserved for memory-mapped registers (MMRs). See Section 6.2, *Memory Map Summary*.

6.1.2 On-Chip Read-Only Memory (ROM)

The zero-wait-state ROM is located at the byte address range FE0000h to FFFFFFh. The ROM is composed of four 16K-word blocks, for a total of 128KB of ROM. The ROM address space can be mapped by software to the internal ROM.

The standard device includes a bootloader program resident in the ROM.

When the MPNMC bit field of the ST3 status register is cleared (by default), the byte address range FE0000h to FFFFFFh is reserved for the on-chip ROM. When software sets the MPNMC bit field of the ST3 status register, the on-chip ROM is disabled and not present in the memory map, and byte address range FE0000h to FFFFFFh is unmapped. A hardware reset always clears the MPNMC bit, so the ROM at reset cannot be disabled. The software reset instruction does not affect the MPNMC bit. The ROM can be accessed by the program and data buses. Each on-chip ROM block is a one cycle per word access memory.

6.1.3 On-Chip Single-Access RAM (SARAM)

6.1.3.1 SARAM

The SARAM is located at the byte address range 010000h to 04FFFFh and is composed of 32 blocks of 4K words each (see Table 6-2). Each SARAM block can perform one access per cycle (one read or one write). SARAM can be accessed by the internal program, data, or DMA buses.

SARAM is also accessed by the USB and LCD DMA buses.

Table 6-2. SARAM Blocks

CPU BYTE ADDRESS RANGE	DMA and USB CONTROLLER BYTE ADDRESS RANGE	MEMORY BLOCK
010000h to 011FFFh	0009 0000h to 0009 1FFFh	SARAM 0
012000h to 013FFFh	0009 2000h to 0009 3FFFh	SARAM 1
014000h to 015FFFh	0009 4000h to 0009 5FFFh	SARAM 2
016000h to 017FFFh	0009 6000h to 0009 7FFFh	SARAM 3
018000h to 019FFFh	0009 8000h to 0009 9FFFh	SARAM 4
01A000h to 01BFFFh	0009 A000h to 0009 BFFFh	SARAM 5
01C000h to 01DFFFh	0009 C000h to 0009 DFFFh	SARAM 6
01E000h to 01FFFFh	0009 E000h to 0009 FFFFh	SARAM 7
020000h to 021FFFh	000A 0000h to 000A 1FFFh	SARAM 8
022000h to 023FFFh	000A 2000h to 000A 3FFFh	SARAM 9
024000h to 025FFFh	000A 4000h to 000A 5FFFh	SARAM 10
026000h to 027FFFh	000A 6000h to 000A 7FFFh	SARAM 11
028000h to 029FFFh	000A 8000h to 000A 9FFFh	SARAM 12
02A000h to 02BFFFh	000A A000h to 000A BFFFh	SARAM 13
02C000h to 02DFFFh	000A C000h to 000A DFFFh	SARAM 14
02E000h to 02FFFFh	000A E000h to 000A FFFFh	SARAM 15
030000h to 031FFFh	000B 0000h to 000B 1FFFh	SARAM 16
032000h to 033FFFh	000B 2000h to 000B 3FFFh	SARAM 17
034000h to 035FFFh	000B 4000h to 000B 5FFFh	SARAM 18
036000h to 037FFFh	000B 6000h to 000B 7FFFh	SARAM 19
038000h to 039FFFh	000B 8000h to 000B 9FFFh	SARAM 20
03A000h to 03BFFFh	000B A000h to 000B BFFFh	SARAM 21
03C000h to 03DFFFh	000B C000h to 000B DFFFh	SARAM 22
03E000h to 03FFFFh	000B E000h to 000B FFFFh	SARAM 23

Table 6-2. SARAM Blocks (continued)

CPU BYTE ADDRESS RANGE	DMA and USB CONTROLLER BYTE ADDRESS RANGE	MEMORY BLOCK
040000h to 041FFFh	000C 0000h to 000C 1FFFh	SARAM 24
042000h to 043FFFh	000C 2000h to 000C 3FFFh	SARAM 25
044000h to 045FFFh	000C 4000h to 000C 5FFFh	SARAM 26
046000h to 047FFFh	000C 6000h to 000C 7FFFh	SARAM 27
048000h to 049FFFh	000C 8000h to 000C 9FFFh	SARAM 28
04A000h to 04BFFFh	000C A000h to 000C BFFFh	SARAM 29
04C000h to 04DFFFh	000C C000h to 000C DFFFh	SARAM 30
04E000h to 04FFFFh	000C E000h to 000C FFFFh	SARAM 31 (1)

(1) SARAM31 (byte address range: 0x4E000 to 0x4EFFF) is reserved for the bootloader. After the boot process completes, this memory space can be used.

6.1.4 I/O Memory

Each device includes a 64-KB I/O space for the memory-mapped registers of the DSP peripherals and system registers used for idle control, status monitoring, and system configuration. I/O space is separate from program and memory space and is accessed with separate instruction opcodes or through the DMAs.

Table 6-3 lists the memory-mapped registers of each device. Not all addresses in the 64-KB I/O space are used; these addresses must be treated as reserved and not accessed by the CPU or DMA. For the expanded tables of each peripheral, see Section 5.6, *Peripheral Information and Electrical Specifications* of this document.

Some DMA controllers have access to the I/O-Space memory-mapped registers of the following peripherals registers: I2C, UART, I2S, SD, USB, and SAR ADC.

Before accessing any peripheral memory-mapped register, ensure the peripheral being accessed is not held in reset through the Peripheral Reset Control Register (PRCR) and its internal clock is enabled through the Peripheral Clock Gating Control Registers (PCGCR1 and PCGCR2).

Table 6-3. Peripheral I/O-Space Control Registers

WORD ADDRESS	PERIPHERAL
0x0000 to 0x0004	Idle Control
0x0005 to 0x000D through 0x0803 to 0x0BFF	Reserved
0x0C00 to 0x0C7F	DMA0
0x0C80 to 0x0CFF	Reserved
0x0D00 to 0x0D7F	DMA1
0x0D80 to 0x0DFF	Reserved
0x0E00 to 0x0E7F	DMA2
0x0E80 to 0x0EFF	Reserved
0x0F00 to 0x0F7F	DMA3
0x0F80 to 0x17FF	Reserved
0x1800 to 0x181F	Timer0
0x1820 to 0x183F	Reserved
0x1840 to 0x185F	Timer1
0x1860 to 0x187F	Reserved
0x1880 to 0x189F	Timer2
0x1900 to 0x197F	RTC
0x1980 to 0x19FF	Reserved

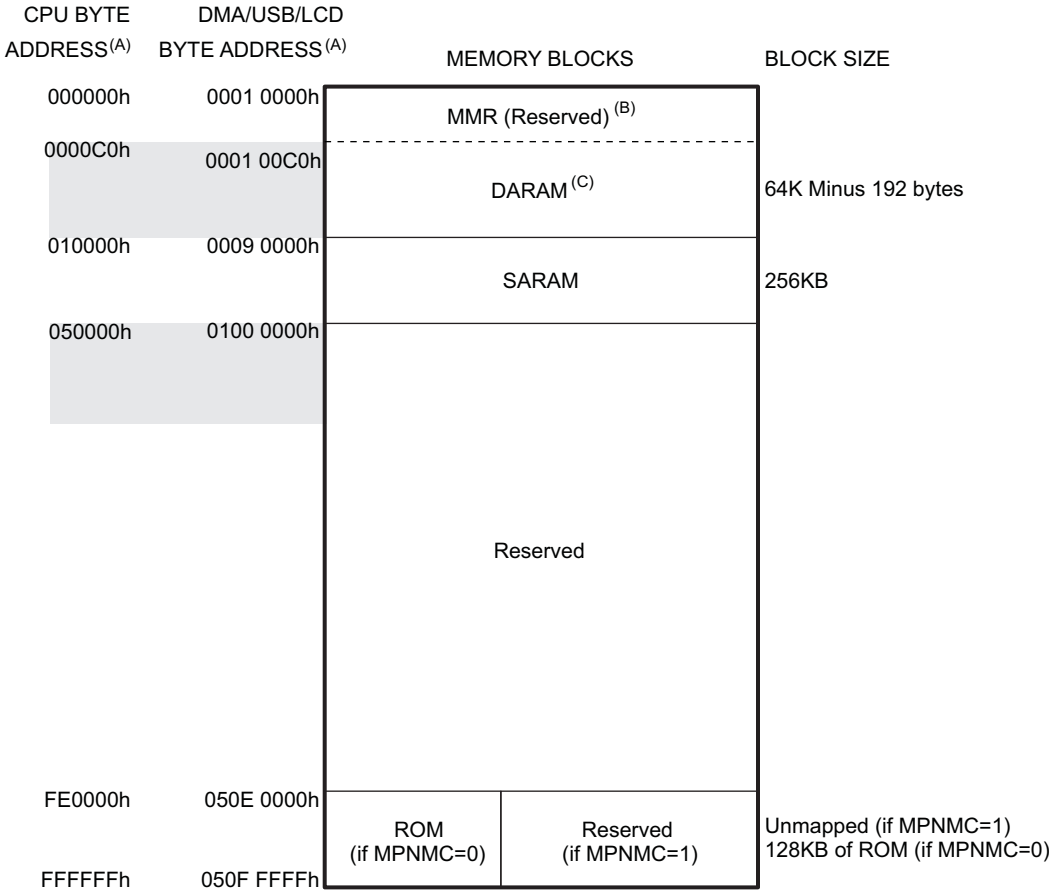
Table 6-3. Peripheral I/O-Space Control Registers (continued)

WORD ADDRESS	PERIPHERAL
0x1A00 to 0x1A6C	I2C
0x1A6D to 0x1AFF	Reserved
0x1B00 to 0x1B1F	UART
0x1B80 to 0x1BFF	Reserved
0x1C00 to 0x1CFF	System Control
0x1D00 to 0x1FFF through 0x2600 to 0x27FF	Reserved
0x2800 to 0x2840	I2S0
0x2900 to 0x2940	I2S1
0x2A00 to 0x2A40	I2S2
0x2B00 to 0x2B40	I2S3
0x2C41 to 0x2DFF	Reserved
0x2E00 to 0x2E40	LCD
0x2E41 to 0x2FFF	Reserved
0x3000 to 0x300F	SPI
0x3010 to 0x39FF	Reserved
0x3A00 to 0x3A7F	SD0
0x3A80 to 0x3AFF	Reserved
0x3B00 to 0x3B7F	SD1
0x3B80 to 0x6FFF	Reserved
0x7000 to 0x70FF	SAR and Analog Control Registers
0x7100 to 0x7FFF	Reserved
0x8000 to 0xFFFF	USB

6.2 Memory Map Summary

The on-chip, dual-access RAM allows two accesses to a given block during the same cycle. There are eight blocks of 8KB of dual-access RAM and thirty-two blocks of 8KB of single-access RAM. The on-chip, single-access RAM allows one access to a given block per cycle.

The DSP memory can be accessed by different master modules within the DSP. These master modules include the C55x CPU, the four DMA controllers, LCD, and CDMA of the USB (see Figure 6-1).



A. Address shown represents the first byte address in each block.
B. The first 192 bytes are reserved for memory-mapped registers (MMRs).
C. The USB and LCD controllers do not have access to DARAM.

Figure 6-1. Memory Map Summary

6.3 System Registers

The system registers configure the device and monitor its status. Brief descriptions of the various system registers are provided in Table 6-4.

Table 6-4. Idle Control, Status, and System Registers

CPU WORD ADDRESS	ACRONYM	REGISTER DESCRIPTION	COMMENTS
0001h	ICR	Idle Control Register	
0002h	ISTR	Idle Status Register	
1C00h	EBSR	External Bus Selection Register	See Section 6.6.1.
1C02h	PCGCR1	Peripheral Clock Gating Control Register 1	
1C03h	PCGCR2	Peripheral Clock Gating Control Register 2	
1C04h	PSRCR	Peripheral Software Reset Counter Register	
1C05h	PRCR	Peripheral Reset Control Register	
1C14h	TIAFR	Timer Interrupt Aggregation Flag Register	
1C16h	ODSCR	Output Drive Strength Control Register	
1C17h	PDINHIBR1	Pulldown Inhibit Register 1	
1C18h	PDINHIBR2	Pulldown Inhibit Register 2	
1C19h	PDINHIBR3	Pulldown Inhibit Register 3	
1C1Ah	DMA0CESR1	DMA0 Channel Event Source Register 1	
1C1Bh	DMA0CESR2	DMA0 Channel Event Source Register 2	
1C1Ch	DMA1CESR1	DMA1 Channel Event Source Register 1	
1C1Dh	DMA1CESR2	DMA1 Channel Event Source Register 2	
1C28h	RAMSLPMDCNTLR1	RAM Sleep Mode Control Register 1	
1C2Ah	RAMSLPMDCNTLR2	RAM Sleep Mode Control Register 2	
1C2Bh	RAMSLPMDCNTLR3	RAM Sleep Mode Control Register 3	
1C2Ch	RAMSLPMDCNTLR4	RAM Sleep Mode Control Register 4	
1C2Dh	RAMSLPMDCNTLR5	RAM Sleep Mode Control Register 5	
1C30h	DMAIFR	DMA Interrupt Flag Aggregation Register	
1C31h	DMAIER	DMA Interrupt Enable Register	
1C32h	USBSCR	USB System Control Register	
1C36h	DMA2CESR1	DMA2 Channel Event Source Register 1	
1C37h	DMA2CESR2	DMA2 Channel Event Source Register 2	
1C38h	DMA3CESR1	DMA3 Channel Event Source Register 1	
1C39h	DMA3CESR2	DMA3 Channel Event Source Register 2	
1C3Ah	CLKSTOP	Peripheral Clock Stop Request and Acknowledge Register	
1C40h	DIEIDR0(1)	Die ID Register 0	
1C41h	DIEIDR1(1)	Die ID Register 1	
1C42h	DIEIDR2(1)	Die ID Register 2	
1C43h	DIEIDR3(1)	Die ID Register 3	
1C44h	DIEIDR4(1)	Die ID Register 4	
1C45h	DIEIDR5(1)	Die ID Register 5	
1C46h	DIEIDR6(1)	Die ID Register 6	
1C47h	DIEIDR7(1)	Die ID Register 7	
7004h	LDOCNTL	LDO Control Register	See Section 5.6.1.1.3.

(1) This register is reserved.

6.4 Boot Sequence

The boot sequence is when the on-chip memory of the device is loaded with program and data sections from an external image file (in flash memory, for example). The boot sequence lets you program some internal registers of the device with predetermined values. The boot sequence is started automatically after each device reset. For more details on device reset, see Section 5.6.9, *Reset.*

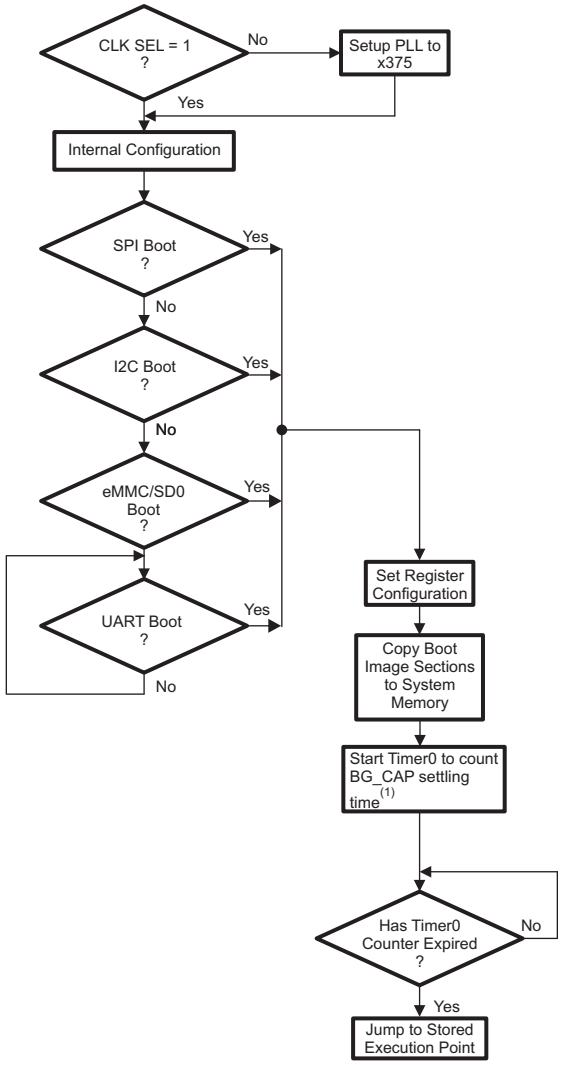
There are several methods by which the memory and register initialization can occur. Each of these methods is referred to as a boot mode. At reset, the device cycles through different boot modes until it finds an image with a valid boot signature. The on-chip bootloader allows the DSP registers to be configured during the boot process, if the optional register configuration section is present in the boot image (see Figure 6-2). For more information on the boot modes supported, see Section 6.4.1, *Boot Modes*.

After reset, the CPU gets the reset vector from 0xFFFF00. MP or $\overline{MC}$ is 0 by default, so 0xFFFF00 is mapped to internal ROM. The PLL is in bypass mode.

The device bootloader follows the following steps (see Figure 6-2.)

1. After reset, the CPU gets the reset vector from 0xFFFF00. MP or MC is 0 by default, so 0xFFFF00 is mapped to internal ROM. The PLL is in bypass mode.
2. Set CLKOUT slew rate control to slow slew rate.
3. Idle all peripherals, MPORT, and HWA.
4. If CLK_SEL = 0, the bootloader powers up the PLL and sets its output frequency to 12.288 MHz (with a 375x multiplier using VP = 749, VS = 0, input divider disabled, output divide-by-8 enabled, and output divider enabled with VO = 0). If CLK_SEL = 1, the bootloader keeps the PLL bypassed. Enable Timer0 to count the settling time of BG_CAP
5. Apply manufacturing trim to the bandgap references.
6. Disable CLKOUT.
7. Test for the 16-bit and 24-bit SPI EEPROM boot on SPI_CS[0] with a 500-kHz clock rate and set to parallel port mode on the EBSR to 5, then set to 6:
   (a) Check the first 2 bytes read from boot table for a boot signature match using 16-bit address mode.
   (b) If the boot signature is not valid, read the first 2 bytes again using 24-bit address mode.
   (c) If the boot signature is not valid from either case (16-bit and 24-bit address modes), go to Step 8.
   (d) Set Register Configuration, if present in boot image.
   (e) Attempt SPI Serial Memory boot, go to Step 12.
8. Test for I2C EEPROM boot with a 7-bit slave address 0x50 and 400-kHz clock rate.
   (a) Check the first 2 bytes read from boot table for a boot signature match.
   (b) If the boot signature is not valid, go to Step 9.
   (c) Set Register Configuration, if present in boot image.
   (d) Attempt I2C EEPROM boot, go to Step 12.
9. Test for eMMC partitions, eMMC, SD0 boot:
   – For an eMMC, SD, or SDHC card, the card must be formatted to FAT16 or FAT32. The boot image file must be renamed bootimg.bin and copied to the foot directory of the formatted card.
   – If an eMMC boot partition is desired (for only eMMC 4.3 and up), then the boot image file must be programmed to one of the two boot partitions (1 or 2) on the eMMC card. PARTITION_CONFIG in the EXT_CSD must be set accordingly.
   – If the boot signature is found, attempt eMMC, SD, or SDHC boot and go to Step 12. If boot signature is not found, go to Step 10.
10. Set the PLL output to approximately 36 MHz. If CLK_SEL = 1, CLKIN multiplied by 3x. If CLK_SEL = 0, CLKIN is multiplied by 1125x. Re-enable TIMER0 to start counting the settling time of BG_CAP due to the PLL change.

11. Test for UART or USB boot:
    - The USB internal LDO will be enabled and the device is configured to accept a boot image on EP1 OUT.
    - UART will be set to 57600 baud, 8 bit, 1 stop bit, CTS or RTS auto flow control, and odd parity will be enabled to accept a boot image from the UART transmitter.
    - The device will poll UART and USB in turns. If a valid boot signature is detected on either device, a boot image will attempt to download on that device. Go to Step 12. If a valid signature is not detected, return to the start of this step.
12. Copy the boot image sections to system memory.
13. Verify the settling time of BG_CAP has elapsed before executing application code.
14. Jump to the entry point specified in the boot image.



(1) See settling time of BG_CAP in Table 4-14.

Figure 6-2. Bootloader Software Architecture

6.4.1 Boot Modes

The DSP supports the following boot modes in the following device order: SPI 16-bit EEPROM, SPI 24-bit Flash, I2C EEPROM, and eMMC boot partition, eMMC, SD or SDHC card. The boot mode is determined by checking for a valid boot signature on each supported boot device. The first boot device with a valid boot signature will be used to load and execute the user code. If none of the supported boot devices have a valid boot signature, the bootloader goes into an endless loop checking the UART or USB boot mode and the device must be reset to search for another valid boot image in the supported boot modes.

Note: For detailed information on eMMC boot partition, eMMC, SD, or SDHC and UART or USB boot modes, contact your local sales representative.

6.4.2 Boot Configuration

After reset, the on-chip bootloader programs the system clock generator based on the input clock selected through the CLK_SEL pin. If CLK_SEL = 0, the bootloader programs the system clock generator and sets the system clock to 12.288 MHz (multiply the 32.768-kHz RTC oscillator clock by 375). If CLK_SEL = 1, the bootloader bypasses the system clock generator altogether and the system clock is driven by the CLKIN pin.

Note:

- When CLK_SEL = 1, the CLKIN frequency is expected to be 11.2896 MHz, 12.0 MHz, or 12.288 MHz.
- The on-chip bootloader allows for DSP registers to be configured during the boot process. However, this feature must not be used to change the output frequency of the system clock generator during the boot process. Timer0 is also used by the bootloader to allow for 200 ms of BG_CAP settling time. The bootloader register modification feature must not modify the PLL or Timer0 registers.

After hardware reset, the DSP boots through the bootloader code in ROM. During the boot process, the bootloader queries each peripheral to determine if it can boot from that peripheral. At that time, the individual peripheral clocks will be enabled for the query and then disabled when the bootloader is finished with the peripheral. By the time the bootloader releases control to the user code, all peripheral clocks will be off and all domains in the ICR will be idled except the CPU domain.

6.4.3 DSP Resources Used By the Bootloader

The bootloader uses SARAM block 31 for the storing of temporary data. This block of memory is reserved during the boot process. After the boot process is complete, it can be used by the user application.

6.5 Configurations at Reset

Some device configurations are determined at reset. The following subsections give more details.

6.5.1 Device and Peripheral Configurations at Device Reset

Table 6-5 summarizes the device boot and configuration pins that are required to be statically tied high, tied low, or remain unconnected during device operation. For proper operation, a device reset must be initiated after changing any of these pin functions.

Table 6-5. Default Functions Affected by Device Configuration Pins

CONFIGURATION PINS	SIGNAL NO.	IPU and IPD	FUNCTIONAL DESCRIPTION
$\overline{\text{DSP\_LDO\_EN}}$	M12	–	DSP_LDO enable input. This signal is not intended to be dynamically switched. 0 = DSP_LDO is enabled. The internal DSP LDO is enabled to regulate power on the DSP_LDOO pin at either 1.3 V or 1.05 V according to the DSP_LDO_V bit in the LDOCNTL register, see Figure 5-2). At power-on reset, the internal POR monitors the DSP_LDOO pin voltage and generates the internal POWERGOOD signal when the DSP_LDO voltage is above a minimum threshold voltage. The internal device reset is generated by the AND of POWERGOOD and the $\overline{\text{RESET}}$ pin. 1 = DSP_LDO is disabled and the DSP_LDOO pin is in a high-impedance (Hi-Z) state. The internal voltage monitoring on the DSP_LDOO is bypassed and the internal POWERGOOD signal is immediately set high. The $\overline{\text{RESET}}$ pin will act as the sole reset source for the device. If an external power supply is used to provide power to CV_{DD}, then $\overline{\text{DSP\_LDO\_EN}}$ must be tied to LDOI, DSP_LDOO must be left unconnected, and the $\overline{\text{RESET}}$ pin must be asserted appropriately for device initialization after powerup. **Note:** To pullup this pin, connect it to the same supply as LDOI pins.
CLK_SEL	D12	–	Clock input select. 0 = 32-kHz on-chip oscillator drives the RTC timer and the system clock generator. CLKIN is ignored. 1 = CLKIN drives the system clock generator and the 32-kHz on-chip oscillator drives only the RTC timer. This pin is not allowed to change during device operation; it must be tied to DV_{DDIO} or GND at the board.

For proper device operation, external pullup and pulldown resistors may be required on these device configuration pins. For discussion on situations where external pullup and pulldown resistors are required, see Section 6.8.1, *Pullup and Pulldown Resistors*.

This device also has RESERVED pins that must be configured correctly for proper device operation (statically tied high, tied low, or remain unconnected at all times). For more details on these pins, see Table 4-15.

6.6 Configurations After Reset

The following sections provide details on configuring the device after reset. Multiplexed pin functions are selected by software after reset. For more details on multiplexed pin function control, see Section 6.7, *Multiplexed Pin Configurations*.

6.6.1 External Bus Selection Register (EBSR)

The External Bus Selection Register (EBSR) determines the mapping of the LCD Controller, I2S2, I2S3, UART, SPI, and GPIO signals to 21 signals of the external parallel port pins. The EBSR also determines the mapping of the I2S or SD ports to serial port 0 pins and serial port pins. The EBSR is at port address 1C00h. Once the bit fields of this register are changed, the routing of the signals occurs on the next CPU clock cycle.

Before modifying the values of the EBSR, you must clock gate all affected peripherals through the PCGCR. After the EBSR has been modified, you must reset the peripherals before using them through the peripheral software reset counter register.

Figure 6-3. External Bus Selection Register (EBSR) [1C00h]

15	14	13	12	11	10	9	8
Reserved	PPMODE			SP1MODE		SP0MODE	
R-0	R/W-000			R/W-00		R/W-00	

7	6	5	4	3	2	1	0
Reserved	Reserved						
R-0	R-0						

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 6-6. EBSR Register Bit Descriptions

BIT	NAME	DESCRIPTION
15	RESERVED	Reserved. Read-only, writes have no effect.
14:12	PPMODE	Parallel port mode control bits. These bits control the pin multiplexing of the LCD Controller, SPI, UART, I2S2, I2S3, and GP[31:27, 20:18] pins on the parallel port. For more details, see Table 6-7.
		000 = Mode 0 (16-bit LCD Controller). All 20 signals of the LCD bridge module are routed to the 20 external signals of the parallel port.
		001 = Mode 1 (SPI, GPIO, UART, and I2S2). 6 signals of the SPI module, 6 GPIO signals, 4 signals of the UART module and 4 signals of the I2S2 module are routed to the 20 external signals of the parallel port.
		010 = Mode 2 (8-bit LCD Controller and GPIO). 8 bits of pixel data of the LCD controller module and 8 GPIO are routed to the 20 external signals of the parallel port.
		011 = Mode 3 (8-bit LCD Controller, SPI and I2S3). 8 bits of pixel data of the LCD controller module, 4 signals of the SPI module and 4 signals of the I2S3 module are routed to the 20 external signals of the parallel port.
		100 = Mode 4 (8-bit LCD Controller, I2S2 and UART). 8 bits of pixel data of the LCD controller module, 4 signals of the I2S2 module and 4 signals of the UART module are routed to the 20 external signals of the parallel port.
		101 = Mode 5 (8-bit LCD Controller, SPI and UART). 8 bits of pixel data of the LCD controller module, 4 signals of the SPI module and 4 signals of the UART module are routed to the 20 external signals of the parallel port.
		110 = Mode 6 (SPI, I2S2, I2S3, and GPIO). 6 signals of the SPI module, 4 signals of the I2S2 module, 4 signals of the I2S3 module, and 6 GPIO are routed to the 20 external signals of the parallel port.
		111 = Reserved.

Table 6-6. EBSR Register Bit Descriptions (continued)

BIT	NAME	DESCRIPTION
11:10	SP1MODE	Serial port 1 mode control bits. The bits control the pin multiplexing of the SD1, I2S1, and GPIO pins on serial port 1. For more details, see Table 6-8.
		00 = Mode 0 (SD1). All 6 signals of the SD1 module are routed to the 6 external signals of the serial port 1.
		01 = Mode 1 (I2S1 and GP[11:10]). 4 signals of the I2S1 module and 2 GP[11:10] signals are routed to the 6 external signals of the serial port 1.
		10 = Mode 2 (GP[11:6]). 6 GPIO signals (GP[11:6]) are routed to the 6 external signals of the serial port 1.
		11 = Reserved.
9:8	SP0MODE	Serial port 0 mode control bits. The bits control the pin multiplexing of the SD0, I2S0, and GPIO pins on serial port 0. For more details, see Section 6.7.1.3.
		00 = Mode 0 (SD0). All 6 signals of the SD0 module are routed to the 6 external signals of the serial port 0.
		01 = Mode 1 (I2S0 and GP[5:0]). 4 signals of the I2S0 module and 2 GP[5:4] signals are routed to the 6 external signals of the serial port 0.
		10 = Mode 2 (GP[5:0]). 6 GPIO signals (GP[5:0]) are routed to the 6 external signals of the serial port 0.
		11 = Reserved.
7	RESERVED	Reserved. Read-only, writes have no effect.
6	RESERVED	Reserved. Read-only, writes have no effect.
5	RESERVED	Reserved
4	RESERVED	Reserved
3	RESERVED	Reserved
2	RESERVED	Reserved
1	RESERVED	Reserved
0	RESERVED	Reserved

6.6.2 LDO Control Register [7004h]

When the DSP_LDO is enabled by the $\overline{\text{DSP\_LDO\_EN}}$ pin [M12], by default, the DSP_LDOO voltage is set to 1.3 V. The DSP_LDOO voltage can be programmed to be either 1.05 V or 1.3 V through the DSP_LDO_V bit (bit 1) in the LDO Control Register (LDOCNTL).

At reset, the USB_LDO is turned off. The USB_LDO can be enabled through the USBLDOEN bit (bit 0) in the LDOCNTL register.

For more detailed information on the LDOs, see Section 5.6.1.1 *LDO Configuration*.

6.6.3 USB System Control Registers (USBSCR) [1C32h]

After reset, by default, the CPU performs 16-bit accesses to the USB register and data space. To perform 8-bit accesses to the USB data space, set the BYTEMODE bits to 01b for the high byte or 10b for the low byte in the USB System Control Register (USBSCR).

6.6.4 Peripheral Clock Gating Control Registers (PCGCR1 and PCGCR2) [1C02h and 1C03h]

After hardware reset, the DSP executes the on-chip bootloader from ROM. As the bootloader executes, it selectively enables the clock of the peripheral being queried for a valid boot. If a valid boot source is not found, the bootloader disables the clock to that peripheral and moves on to the next peripheral in the boot order. After the boot process is complete, all of the peripheral clocks will be off and all domains in the ICR, except for the CPU domain, will be idled (including the MPORT and HWA). The user must enable the clocks to the peripherals and CPU ports that are going to be used. PCGCR1 and PCGCR2 are used to enable and disable the peripheral clocks.

6.6.5 Pullup and Pulldown Inhibit Registers (PDINHIBR1, 2, and 3) [1C17h, 1C18h, and 1C19h]

Each internal pullup (IPU) and internal pulldown (IPD) resistor on the device DSP, except for the IPD on $\overline{\text{TRST}}$, can be individually controlled through the IPU and IPD registers (PDINHIBR1 [1C17h], PDINHIBR2 [1C18h], and PDINHIBR3 [1C19h]). To minimize power consumption, IPU or IPD resistors must be disabled in the presence of an external pullup or pulldown resistor or external driver. Section 6.8.1, *Pullup and Pulldown Resistors*, describes other situations in which an pullup and pulldown resistors are required.

When CV_{DD} is powered down, pullup and pulldown resistors will be forced disabled and an internal bus-holder will be enabled. For more detailed information, see Section 5.6.5.2, *Digital I/O Behavior When Core Power (CV_{DD}) is Down*.

6.6.6 Output Slew Rate Control Register (OSRCR) [1C16h]

To provide the lowest power consumption setting, the DSP has configurable slew rate control on the CLKOUT output pin. The OSRCR is used to set a subset of the device I/O pins, namely the CLKOUT pin, to either fast or slow slew rate. The slew rate feature is implemented by staging or delaying turnon times of the parallel P-channel drive transistors and parallel N-channel drive transistors of the output buffer. In the slow slew rate configuration, the delay is longer but the same number of parallel transistors are used to drive the output high or low. In the slow slew rate configuration, the drive strength is the same. The slower slew rate control can be used for power savings and has the greatest effect at lower DV_{DDIO} voltages.

6.7 Multiplexed Pin Configurations

The device DSP uses pin multiplexing to accommodate a larger number of peripheral functions in the smallest possible package, providing the ultimate flexibility for end applications. The EBSR controls all the pin multiplexing functions on the device.

6.7.1 Pin Multiplexing Details

This section discusses how to program the EBSR to select the desired peripheral functions and pin muxing. See the individual pin mux sections for pin muxing details for a specific muxed pin. After changing any of the pin mux control registers, it will be necessary to reset the peripherals that are affected.

6.7.1.1 LCD Controller, SPI, UART, I2S2, I2S3, and GP[31:27, 20:18] Pin Multiplexing [EBSR.PPMODE Bits]

The LCD controller, SPI, UART, I2S2, I2S3, and GPIO signal muxing is determined by the value of the PPMODE bit fields in the EBSR. For more details on the actual pin functions, see Table 6-7.

Table 6-7. LCD Controller, SPI, UART, I2S2, I2S3, and GP[31:27, 20:18] Pin Multiplexing

PDINHIBR3 REGISTER BIT FIELDS(1)	PIN NAME	EBSR PPMODE BITS						
		MODE 0	MODE 1	MODE 2	MODE 3	MODE 4	MODE 5	MODE 6
		000 (Reset default)	001	010	011	100	101	110
	LCD_EN_RDB/SPI_CLK	LCD_EN_RDB	SPI_CLK	LCD_EN_RDB	LCD_EN_RDB	LCD_EN_RDB	LCD_EN_RDB	SPI_CLK
	LCD_D[0]/SPI_RX	LCD_D[0]	SPI_RX	LCD_D[0]	LCD_D[0]	LCD_D[0]	LCD_D[0]	SPI_RX
	LCD_D[1]/SPI_TX	LCD_D[1]	SPI_TX	LCD_D[1]	LCD_D[1]	LCD_D[1]	LCD_D[1]	SPI_TX
P2PD	LCD_D[2]/GP[12]	LCD_D[2]	GP[12]	LCD_D[2]	LCD_D[2]	LCD_D[2]	LCD_D[2]	GP[12]
P3PD	LCD_D[3]/GP[13]	LCD_D[3]	GP[13]	LCD_D[3]	LCD_D[3]	LCD_D[3]	LCD_D[3]	GP[13]
P4PD	LCD_D[4]/GP[14]	LCD_D[4]	GP[14]	LCD_D[4]	LCD_D[4]	LCD_D[4]	LCD_D[4]	GP[14]
P5PD	LCD_D[5]/GP[15]	LCD_D[5]	GP[15]	LCD_D[5]	LCD_D[5]	LCD_D[5]	LCD_D[5]	GP[15]
P6PD	LCD_D[6]/GP[16]	LCD_D[6]	GP[16]	LCD_D[6]	LCD_D[6]	LCD_D[6]	LCD_D[6]	GP[16]
P7PD	LCD_D[7]/GP[17]	LCD_D[7]	GP[17]	LCD_D[7]	LCD_D[7]	LCD_D[7]	LCD_D[7]	GP[17]
P8PD	LCD_D[8]/I2S2_CLK/GP[18]/SPI_CLK	LCD_D[8]	I2S2_CLK	GP[18]	SPI_CLK	I2S2_CLK	SPI_CLK	I2S2_CLK
P9PD	LCD_D[9]/I2S2_FS/GP[19]/SPI_CS0	LCD_D[9]	I2S2_FS	GP[19]	SPI_CS0	I2S2_FS	SPI_CS0	I2S2_FS
P10PD	LCD_D[10]/I2S2_RX/GP[20]/SPI_RX	LCD_D[10]	I2S2_RX	GP[20]	SPI_RX	I2S2_RX	SPI_RX	I2S2_RX
P11PD	LCD_D[11]/I2S2_DX/GP[27]/SPI_TX	LCD_D[11]	I2S2_DX	GP[27]	SPI_TX	I2S2_DX	SPI_TX	I2S2_DX
P12PD	LCD_D[12]/UART_RTS/GP[28]/I2S3_CLK	LCD_D[12]	UART_RTS	GP[28]	I2S3_CLK	UART_RTS	UART_RTS	I2S3_CLK
P13PD	LCD_D[13]/UART_CTS/GP[29]/I2S3_FS	LCD_D[13]	UART_CTS	GP[29]	I2S3_FS	UART_CTS	UART_CTS	I2S3_FS
P14PD	LCD_D[14]/UART_RXD/GP[30]/I2S3_RX	LCD_D[14]	UART_RXD	GP[30]	I2S3_RX	UART_RXD	UART_RXD	I2S3_RX
P15PD	LCD_D[15]/UART_TXD/GP[31]/I2S3_DX	LCD_D[15]	UART_TXD	GP[31]	I2S3_DX	UART_TXD	UART_TXD	I2S3_DX
	LCD_CS0_E0/SPI_CS0	LCD_CS0_E0	SPI_CS0	LCD_CS0_E0	LCD_CS0_E0	LCD_CS0_E0	LCD_CS0_E0	SPI_CS0
	LCD_RW_WRB/SPI_CS2	LCD_RW_WRB	SPI_CS2	LCD_RW_WRB	LCD_RW_WRB	LCD_RW_WRB	LCD_RW_WRB	SPI_CS2
	LCD_RS/SPI_CS3	LCD_RS	SPI_CS3	LCD_RS	LCD_RS	LCD_RS	LCD_RS	SPI_CS3

(1) The pin names with PDINHIBR3 register bit field references can have the pulldown resistor enabled or disabled through this register.

6.7.1.2 SD1, I2S1, and GP[11:6] Pin Multiplexing [EBSR.SP1MODE Bits]

The SD1, I2S1, and GPIO signal muxing is determined by the value of the SP1MODE bit fields in the EBSR. For more details on the actual pin functions, see Table 6-8.

Table 6-8. SD1, I2S1, and GP[11:6] Pin Multiplexing

PDINHIBR1 REGISTER BIT FIELDS(1)	PIN NAME	EBSR SP1MODE BITS		
		MODE 0	MODE 1	MODE 2
		00 (Reset default)	01	10
S10PD	SD1_CLK/I2S1_CLK/GP[6]	SD1_CLK	I2S1_CLK	GP[6]
S11PD	SD1_CMD/I2S1_FS/GP[7]	SD1_CMD	I2S1_FS	GP[7]
S12PD	SD1_D0/I2S1_DX/GP[8]	SD1_D0	I2S1_DX	GP[8]
S13PD	SD1_D1/I2S1_RX/GP[9]	SD1_D1	I2S1_RX	GP[9]
S14PD	SD1_D2/GP[10]	SD1_D2	GP[10]	GP[10]
S15PD	SD1_D3/GP[11]	SD1_D3	GP[11]	GP[11]

(1) The pin names with PDINHIBR1 register bit field references can have the pulldown register enabled or disabled through this register.

6.7.1.3 SD0, I2S0, and GP[5:0] Pin Multiplexing [EBSR.SP0MODE Bits]

The SD0, I2S0, and GPIO signal muxing is determined by the value of the SP0MODE bit fields in the EBSR. For more details on the actual pin functions, see Table 6-9.

Table 6-9. SD0, I2S0, and GP[5:0] Pin Multiplexing

PDINHIBR1 REGISTER BIT FIELDS(1)	PIN NAME	EBSR SP0MODE BITS		
		MODE 0	MODE 1	MODE 2
		00 (Reset default)	01	10
S00PD	SD0_CLK/I2S0_CLK/GP[0]	SD0_CLK	I2S0_CLK	GP[0]
S01PD	SD0_CMD/I2S0_FS/GP[1]	SD0_CMD	I2S0_FS	GP[1]
S02PD	SD0_D0/I2S0_DX/GP[2]	SD0_D0	I2S0_DX	GP[2]
S03PD	SD0_D1/I2S0_RX/GP[3]	SD0_D1	I2S0_RX	GP[3]
S04PD	SD0_D2/GP[4]	SD0_D2	GP[4]	GP[4]
S05PD	SD0_D3/GP[5]	SD0_D3	GP[5]	GP[5]

(1) The pin names with PDINHIBR1 register bit field references can have the pulldown register enabled or disabled through this register.

6.8 Debugging Considerations

6.8.1 Pullup and Pulldown Resistors

Proper board design should ensure that input pins to the device DSP always be at a valid logic level and not floating. This may be achieved through pullup and pulldown resistors. The DSP features IPU and IPD resistors on many pins, including all GPIO pins, to eliminate the need, unless otherwise noted, for external pullup and pulldown resistors.

An external pullup and pulldown resistor may need to be used in the following situations:

- Configuration Pins: An external pullup and pulldown resistor is recommended to set the desired value or state (see the configuration pins listed in Table 6-5). Some configuration pins must be connected directly to ground or to a specific supply voltage.
- Other Input Pins: If the IPU and IPD does not match the desired value or state, use an external pullup and pulldown resistor to pull the signal to the opposite rail.

For the configuration pins (listed in Table 6-5), if they are both routed out and high-impedance state (not driven), TI recommends implementing an external pullup and pulldown resistor. In addition, applying external pullup and pulldown resistors on the configuration pins adds convenience to the user in debugging and flexibility in switching operating modes.

When an external pullup or pulldown resistor is used on a pin, the IPU and IPD resistor of the pin must be disabled through the Pullup and Pulldown Inhibit Registers (PDINHIBR1, 2, and 3) [1C17h, 1C18h, and 1C19h, respectively] to minimize power consumption.

Tips for choosing an external pullup and pulldown resistor:

- Consider the total amount of current that may pass through the pullup or pulldown resistor. Include the leakage currents of all the devices connected to the net, as well as any IPU and IPD resistors.
- Decide a target value for the net. For a pulldown resistor, this should be below the lowest V_{IL} level of all inputs connected to the net. For a pullup resistor, this should be preceding the highest V_{IH} level of all inputs on the net. A reasonable choice would be to target the V_{OL} or V_{OH} levels for the logic family of the limiting device; which, by definition, have margin to the V_{IL} and V_{IH} levels.
- Select a pullup and pulldown resistor with the largest possible value that can ensure the net will reach the target pulled value when maximum current from all devices on the net is flowing through the resistor. The current to be considered includes leakage current and any other internal and external pullup and pulldown resistors on the net.
- For bidirectional nets, an additional consideration exists that sets a lower limit on the resistance value of the external resistor. Verify that the resistance is small enough that the weakest output buffer can drive the net to the opposite logic level (including margin).
- Remember to include tolerances when selecting the resistor value.
- For pullup resistors, also remember to include tolerances on the DV_{DDIO} rail.

For most systems, a 1-kΩ resistor can be used to oppose the IPU and IPD while meeting the preceding criteria. Confirm this resistor value is correct for each specific application.

For most systems, a 20-kΩ resistor can be used to compliment the IPU and IPD on the configuration pins while meeting the above criteria. Confirm this resistor value is correct for each specific application.

For more detailed information on input current (I_I), and the low- and high-level input voltages (V_{IL} and V_{IH}) for the device DSP, see Section 5.5, *Electrical Characteristics Over Recommended Ranges of Supply Voltage and Operating Temperature*.

For the IPU and IPD resistors for all device pins, see the peripheral and system-specific terminal functions table in this document.

6.8.2 Bus-Holders

The device has special I/O bus-holder structures to ensure pins are not left floating when CV_{DD} power is removed while I/O power is applied. When CV_{DD} is ON, the bus-holders are disabled and the internal pullups or pulldowns, if applicable, function normally. But when CV_{DD} is OFF and the I/O supply is ON, the bus-holders become enabled and any applicable internal pullups and pulldowns are disabled.

The bus-holders are weak drivers on the pin and, for as long as CV_{DD} is OFF and I/O power is ON, they hold the last state on the pin. If an external device is strongly driving the device I/O pin to the opposite state then the bus-holder will flip state to match the external driver and DC current will stop.

This bus-holder feature prevents unnecessary power consumption when CV_{DD} is OFF and I/O supply is ON. For example, current caused by undriven pins (input buffer oscillation) or DC current flowing through pullups or pulldowns.

If external pullup or pulldown resistors are implemented, then care must be taken that those pullup and pulldown resistors can exceed the maximum current of the internal bus-holder and thereby cause the bus-holder to flip state to match the state of the external pullup or pulldown. Otherwise, DC current will flow unnecessarily. When CV_{DD} power is applied, the bus-holders are disabled (for further details on bus-holders, see Section 5.6.5.2, *Digital I/O Behavior When Core Power (CV_{DD}) is Down*).

6.8.3 CLKOUT Pin

For debug purposes only, the DSP includes a CLKOUT pin which can be used to tap different clocks within the clock generator. The SRC bits of the CLKOUT Control Source Register (CCSSR) can be used to specify the source for the CLKOUT pin.

Note: The bootloader disables the CLKOUT pin through CLKOFF bit in the ST3_55 CPU register.

7 Device and Documentation Support

7.1 Device Nomenclature

To designate the stages in the product development cycle, TI assigns prefixes to the part numbers of all DSP devices and support tools. Each DSP commercial family member has one of three prefixes: TMX, TMP, or TMS (for example, TMS320C5545AZQW10). Texas Instruments recommends two of three possible prefix designators for its support tools: TMDX and TMDS. These prefixes represent evolutionary stages of product development from engineering prototypes (TMX and TMDX) through fully qualified production devices and tools (TMS and TMDS).

Device development evolutionary flow:

TMX Experimental device that is not necessarily representative of the final device's electrical specifications.

TMP Final silicon die that conforms to the device's electrical specifications but has not completed quality and reliability verification.

TMS Fully-qualified production device.

Support tool development evolutionary flow:

TMDX Development-support product that has not yet completed Texas Instruments internal qualification testing.

TMDS Fully qualified development-support product.

TMX and TMP devices and TMDX development-support tools are shipped against the following disclaimer:

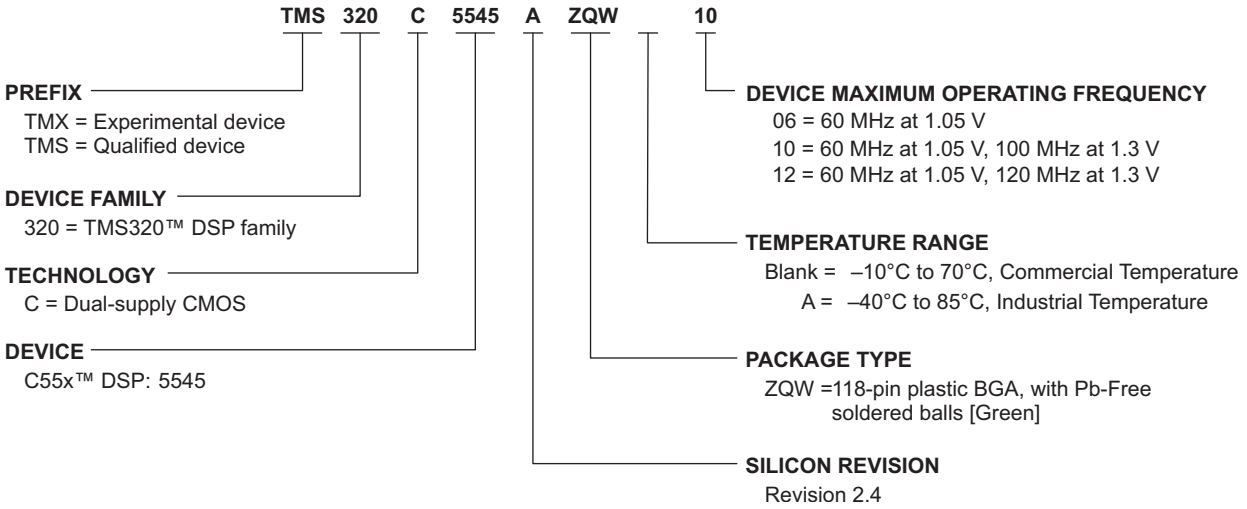
"Developmental product is intended for internal evaluation purposes."

TMS devices and TMDS development-support tools have been characterized fully, and the quality and reliability of the device have been demonstrated fully. TI's standard warranty applies.

Predictions show that prototype devices (TMX or TMP) have a greater failure rate than the standard production devices. Texas Instruments recommends that these devices not be used in any production system because their expected end-use failure rate still is undefined. Only qualified production devices are to be used.

TI device nomenclature also includes a suffix with the device family name. This suffix indicates the package type (for example, ZQW), and the temperature range (for example, "Blank" is the commercial temperature range).

Figure 7-1 provides a legend for reading the complete device name for any DSP platform member.



A. For actual device part numbers (P/Ns) and ordering information, see the TI website (http://www.ti.com)

Figure 7-1. Device Nomenclature

7.2 Tools and Software

TI offers an extensive line of development tools for the TMS320C55x DSP platform, including tools to evaluate the performance of the processors, generate code, develop algorithm implementations, and fully integrate and debug software and hardware modules. The tool's support documentation is electronically available within the Code Composer Studio™ Integrated Development Environment (IDE).

The following products support development of TMS320C55x fixed-point DSP-based applications:

Software Development Tools:

Code Composer Studio Integrated Development Environment (IDE): Associate device as TMS320C5545.

C/C++/Assembly Code Generation, and Debug plus additional development tools

Scalable, Real-Time Foundation Software (DSP/BIOS Version 5.33 or later), which provides the basic run-time target software needed to support any DSP application.

Hardware Development Tools:

Extended Development System (XDS™) Emulator

For a complete listing of development-support tools for the TMS320C55x DSP platform, visit the Texas Instruments web site on the Worldwide Web at http://www.ti.com. For information on pricing and availability, contact the nearest TI field sales office or authorized distributor.

7.3 Documentation Support

To receive notification of documentation updates, navigate to the device product folder on ti.com (**TMS320C5545**). In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

The current documentation that describes the DSP, related peripherals, and other technical collateral is listed below.

Errata

TMS320C5545A Fixed-Point Digital Signal Processor Silicon Revision 2.4 Silicon Errata Describes the known exceptions to the functional specifications for this device.

Application Reports

Using the TMS320C5545/35/34/33/32 Bootloader Describes features of the on-chip ROM for this device, as well as descriptions of how to interface with possible boot devices and generating a boot image to store on an external device.

Power Estimation and Power Consumption Summary for TMS320C5504/05/14/15/32/33/34/35/45 This application report assists in estimating the power consumption for the TMS320C55xx devices (DSPs), using a power estimation spreadsheet.

Migrating From TMS320C5535 to TMS320C5545 This application report provides a summary of the similarities and differences between the TMS320C5535 and TMS320C5545 devices to minimize changes required to migrate from TMS320C5535 to TMS320CC5545.

Validating High Speed and Full Speed USB on the TMS320C5545 Device This application report describes the process to validate electrical requirements of high and full speed USB operations on the TMS320C5545 device.

C5000 DSP-Based Low-Power System Design This application report focuses on the Texas Instruments' C5000 DSP family. Low-power related features are highlighted on the architecture level and keynotes are presented for the C5000-based system design.

User's Guides

TMS320C55x DSP v3.x CPU Reference Guide Describes more detailed information on the C55x CPU.

Technical Reference Manuals

Ultra-Low Power DSP Technical Reference Manual Collection of documents providing detailed information on the device including system control, FFT implementation, and memory access. Detailed information on the device as well as a functional description of the peripherals supported is also included.

7.4 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community The TI engineer-ro-engineer (E2E) community was created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

TI Embedded Processors Wiki Established to help developers get started with Embedded Processors from Texas Instruments and to foster innovation and growth of general knowledge about the hardware and software surrounding these devices.

7.5 Trademarks

C5000, eXpressDSP, Code Composer Studio, DSP/BIOS, RTDX, XDS510, XDS560, MicroStar JUNIOR BGA, E2E are trademarks of Texas Instruments.
All other trademarks are the property of their respective owners.

7.6 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

7.7 Glossary

TI Glossary This glossary lists and explains terms, acronyms, and definitions.

8 Mechanical, Packaging, and Orderable Information

8.1 Packaging Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TMS320C5545AZQW10	LIFEBUY	BGA MICROSTAR JUNIOR	ZQW	118	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-3-260C-168 HR	0 to 0	TMS320C55 45AZQW10	
TMS320C5545AZQW10R	LIFEBUY	BGA MICROSTAR JUNIOR	ZQW	118	2500	Green (RoHS & no Sb/Br)	SNAGCU	Level-3-260C-168 HR	0 to 0	TMS320C55 45AZQW10	
TMS320C5545AZQW12	LIFEBUY	BGA MICROSTAR JUNIOR	ZQW	118	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-3-260C-168 HR	0 to 0	TMS320C55 45AZQW12	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) RoHS: TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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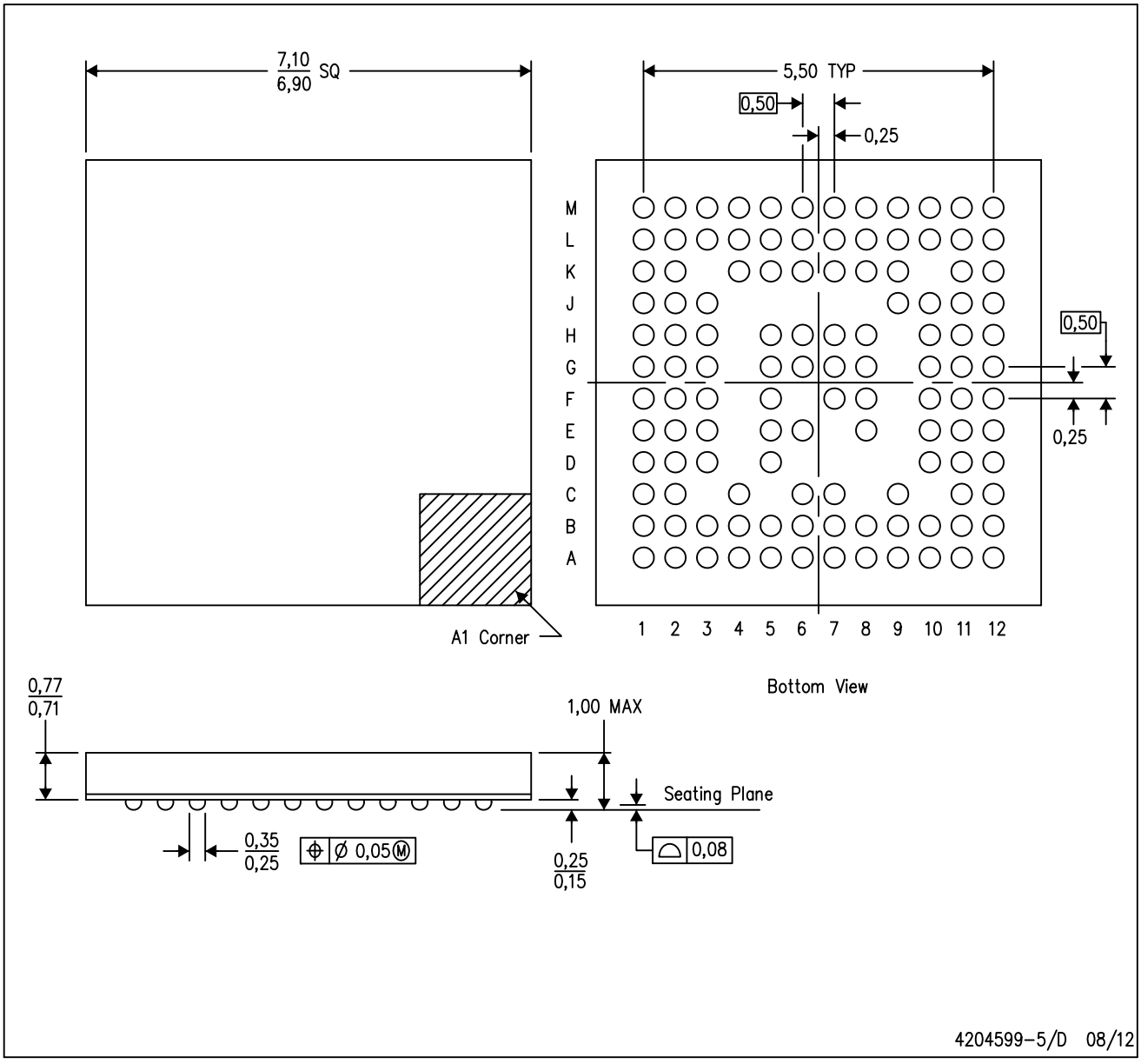
ZQW (S–PBGA–N118) PLASTIC BALL GRID ARRAY



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Falls within JEDEC MO–225
D. This is a Pb–free solder ball design.

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