2-W STEREO AUDIO POWER AMPLIFIER WITH ADVANCED DC VOLUME CONTROL

FEATURES
- 2 W Into 4-Ω Speakers With External Heatsink
- DC Volume Control With 2-dB Steps from -40 dB to 20 dB
  - Fade Mode
  - -85-dB Mute Mode
- Differential Inputs
- 1-μA Shutdown Current (Typical)
- Headphone Mode

APPLICATIONS
- LCD Monitors

DESCRIPTION
The TPA6021A4 is a stereo audio power amplifier that drives 2 W/channel of continuous RMS power into a 4-Ω load when utilizing a heat sink. Advanced dc volume control minimizes external components and allows BTL (speaker) volume control and SE (headphone) volume control.

The 20-pin DIP package allows for the use of a heatsink which provides higher output power.

To ensure a smooth transition between active and shutdown modes, a fade mode ramps the volume up and down.

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.
These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

**AVAILABLE OPTIONS**

<table>
<thead>
<tr>
<th>T_A</th>
<th>PACKAGE</th>
</tr>
</thead>
<tbody>
<tr>
<td>−40°C to 85°C</td>
<td>TPA6021A4N</td>
</tr>
</tbody>
</table>

**ABSOLUTE MAXIMUM RATINGS**

over operating free-air temperature range (unless otherwise noted)\(^{(1)}\)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>V_{SS} Supply voltage, V_{DD}, P_{VDD}</td>
<td>−0.3 V to 6 V</td>
</tr>
<tr>
<td>V_I Input voltage, R_{IN+}, R_{IN−}, L_{IN+}, L_{IN−}</td>
<td>−0.3 V to V_{DD}+0.3 V</td>
</tr>
<tr>
<td>Continuous total power dissipation</td>
<td>See Dissipation Rating Table</td>
</tr>
<tr>
<td>T_A Operating free-air temperature range</td>
<td>−40°C to 85°C</td>
</tr>
<tr>
<td>T_J Operating junction temperature range</td>
<td>−40°C to 150°C</td>
</tr>
<tr>
<td>T_{stg} Storage temperature range</td>
<td>−65°C to 85°C</td>
</tr>
<tr>
<td>Lead temperature 1.6 mm (1/16 inch) from case for 10 seconds</td>
<td>260°C</td>
</tr>
</tbody>
</table>

\(^{(1)}\) Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

**DISSIPATION RATING TABLE\(^{(1)}\)**

<table>
<thead>
<tr>
<th>PACKAGE</th>
<th>T_A = 25°C POWER RATING</th>
<th>DERATING FACTOR ABOVE T_A = 25°C</th>
<th>T_A = 70°C POWER RATING</th>
<th>T_A = 85°C POWER RATING</th>
</tr>
</thead>
<tbody>
<tr>
<td>N</td>
<td>1.8 W</td>
<td>14.5 mW/°C</td>
<td>1.16 W</td>
<td>0.94 W</td>
</tr>
</tbody>
</table>

\(^{(1)}\) All characterization is done using an external heatsink with \(\theta_{SA} = 25°C/W\). The resulting derating factor is 22.2 mW/°C.
### RECOMMENDED OPERATING CONDITIONS

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>MIN</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>(V_{SS})</td>
<td>Supply voltage, (V_{DD}, PV_{DD})</td>
<td>4</td>
<td>5.5</td>
</tr>
<tr>
<td>(V_{IH})</td>
<td>High-level input voltage</td>
<td>(0.8 \times V_{DD})</td>
<td>V</td>
</tr>
<tr>
<td>(V_{IL})</td>
<td>Low-level input voltage</td>
<td>(0.6 \times V_{DD})</td>
<td>V</td>
</tr>
<tr>
<td>(T_{A})</td>
<td>Operating free-air temperature</td>
<td>–40</td>
<td>85</td>
</tr>
</tbody>
</table>

### ELECTRICAL CHARACTERISTICS

\(T_{A} = 25^\circ C, \ V_{DD} = PV_{DD} = 5.5\ V\) (unless otherwise noted)

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>(V_{DD} = 5.5\ V, \ \text{Gain} = 0\ dB, \ \text{SE/BTL} = 0\ V)</td>
<td>30</td>
<td>mV</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>(V_{DD} = 5.5\ V, \ \text{Gain} = 20\ dB, \ \text{SE/BTL} = 0\ V)</td>
<td>50</td>
<td>mV</td>
<td></td>
<td></td>
</tr>
<tr>
<td>PSRR</td>
<td>Power supply rejection ratio</td>
<td>(V_{DD} = PV_{DD} = 4\ V) to 5.5 V</td>
<td>–42</td>
<td>–70</td>
<td>dB</td>
</tr>
<tr>
<td>(I_{IH})</td>
<td>High-level input current (SE/BTL, FADE, SHUTDOWN, VOLUME)</td>
<td>(V_{DD} = PV_{DD} = 5.5\ V), (V_{I} = V_{DD} = PV_{DD})</td>
<td>1</td>
<td>µA</td>
<td></td>
</tr>
<tr>
<td>(I_{IL})</td>
<td>Low-level input current (SE/BTL, FADE, SHUTDOWN, VOLUME)</td>
<td>(V_{DD} = PV_{DD} = 5.5\ V, V_{I} = 0\ V)</td>
<td>1</td>
<td>µA</td>
<td></td>
</tr>
<tr>
<td>(I_{DD})</td>
<td>Supply current, no load</td>
<td>(V_{DD} = PV_{DD} = 5.5\ V, SE/BTL = 0\ V, SHUTDOWN = 2\ V)</td>
<td>6</td>
<td>7.5</td>
<td>9</td>
</tr>
<tr>
<td></td>
<td>(V_{DD} = PV_{DD} = 5.5\ V, SE/BTL = 5.5\ V, SHUTDOWN = 2\ V)</td>
<td>3</td>
<td>5</td>
<td>6</td>
<td>mA</td>
</tr>
<tr>
<td>(I_{DD(SD)})</td>
<td>Supply current, shutdown mode</td>
<td>(SHUTDOWN = 0\ V)</td>
<td>1</td>
<td>20</td>
<td>µA</td>
</tr>
</tbody>
</table>

### OPERATING CHARACTERISTICS

\(T_{A} = 25^\circ C, \ V_{DD} = PV_{DD} = 5\ V, R_{L} = 4\ \Omega\), Gain = 20 dB, Stereo, External Heatsink (unless otherwise noted)

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>(P_{O})</td>
<td>Output power</td>
<td>THD = 1%, \ f = 1\ kHz</td>
<td>1.5(1)</td>
<td>W</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>THD = 10%, \ f = 1 kHz, (V_{DD} = 5\ V)</td>
<td>2(1)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>(THD+N)</td>
<td>Total harmonic distortion + noise</td>
<td>(P_{O} = 1\ W, R_{L} = 8\ \Omega, f = 20\ Hz) to 20 kHz</td>
<td>&lt;0.8%</td>
<td></td>
<td></td>
</tr>
<tr>
<td>(V_{OH})</td>
<td>High-level output voltage</td>
<td>(R_{L} = 8\ \Omega), Measured between output and (V_{DD} = 5.5\ V)</td>
<td>700</td>
<td>mV</td>
<td></td>
</tr>
<tr>
<td>(V_{OL})</td>
<td>Low-level output voltage</td>
<td>(R_{L} = 8\ \Omega), Measured between output and GND, (V_{DD} = 5.5\ V)</td>
<td>400</td>
<td>mV</td>
<td></td>
</tr>
<tr>
<td>(V_{(bypass)})</td>
<td>Bypass voltage (Nominally (V_{DD}/2))</td>
<td>Measured at pin 16, No load, (V_{DD} = 5.5\ V)</td>
<td>2.65</td>
<td>2.75</td>
<td>2.85</td>
</tr>
<tr>
<td></td>
<td>Supply ripple rejection ratio</td>
<td>(f = 1\ kHz, \ \text{Gain} = 0\ dB, C_{(BYP)} = 0.47\ \mu F)</td>
<td>BTL</td>
<td>–82</td>
<td>dB</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>SE</td>
<td>–57</td>
<td>dB</td>
</tr>
<tr>
<td></td>
<td>Noise output voltage</td>
<td>(f = 20\ Hz) to 20 kHz, (\text{Gain} = 0\ dB, C_{(BYP)} = 0.47\ \mu F)</td>
<td>BTL</td>
<td>36</td>
<td>μV RMS</td>
</tr>
<tr>
<td>(Z_{I})</td>
<td>Input impedance (see Figure 18)</td>
<td>(VOLUME = 5\ V)</td>
<td>14</td>
<td>kΩ</td>
<td></td>
</tr>
</tbody>
</table>

(1) Requires an external heatsink with \(θ_{SA} ≤ 25^\circ C/W\).
### Terminal Functions

<table>
<thead>
<tr>
<th>TERMINAL NAME</th>
<th>NO.</th>
<th>I/O</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>BYPASS</td>
<td>16</td>
<td>I</td>
<td>Tap to voltage divider for internal mid-supply bias generator used for analog reference.</td>
</tr>
<tr>
<td>FADE</td>
<td>15</td>
<td>I</td>
<td>Places the amplifier in fade mode if a logic low is placed on this terminal; normal operation if a logic high is placed on this terminal.</td>
</tr>
<tr>
<td>AGND</td>
<td>17</td>
<td>-</td>
<td>Analog power supply ground.</td>
</tr>
<tr>
<td>LIN-</td>
<td>7</td>
<td>I</td>
<td>Left channel negative input for fully differential input.</td>
</tr>
<tr>
<td>LIN+</td>
<td>8</td>
<td>I</td>
<td>Left channel positive input for fully differential input.</td>
</tr>
<tr>
<td>LOUT–</td>
<td>10</td>
<td>O</td>
<td>Left channel negative audio output.</td>
</tr>
<tr>
<td>LOUT+</td>
<td>12</td>
<td>O</td>
<td>Left channel positive audio output.</td>
</tr>
<tr>
<td>NC</td>
<td>13</td>
<td>-</td>
<td>No connection.</td>
</tr>
<tr>
<td>PGND</td>
<td>1, 11</td>
<td>-</td>
<td>Power ground.</td>
</tr>
<tr>
<td>PVDD</td>
<td>3, 9</td>
<td>-</td>
<td>Supply voltage terminal for power stage.</td>
</tr>
<tr>
<td>RIN-</td>
<td>5</td>
<td>I</td>
<td>Right channel negative input for fully differential input.</td>
</tr>
<tr>
<td>RIN+</td>
<td>4</td>
<td>I</td>
<td>Right channel positive input for fully differential input.</td>
</tr>
<tr>
<td>ROUT–</td>
<td>2</td>
<td>O</td>
<td>Right channel negative audio output.</td>
</tr>
<tr>
<td>ROUT+</td>
<td>20</td>
<td>O</td>
<td>Right channel positive audio output.</td>
</tr>
<tr>
<td>SE/BTL</td>
<td>19</td>
<td>I</td>
<td>Output control. When this terminal is high, SE outputs are selected. When this terminal is low, BTL outputs are selected.</td>
</tr>
<tr>
<td>SHUTDOWN</td>
<td>14</td>
<td>I</td>
<td>Places the amplifier in shutdown mode if a TTL logic low is placed on this terminal.</td>
</tr>
<tr>
<td>VDD</td>
<td>6</td>
<td>-</td>
<td>Supply voltage terminal.</td>
</tr>
<tr>
<td>VOLUME</td>
<td>18</td>
<td>I</td>
<td>Terminal for dc volume control. DC voltage range is 0 to V_{DD}.</td>
</tr>
</tbody>
</table>
NOTE: All resistor wipers are adjusted with 32 step volume control.
TYPICAL CHARACTERISTICS

Table of Graphs\(^{(1)}\)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Description</th>
<th>Figure</th>
</tr>
</thead>
<tbody>
<tr>
<td>THD+N</td>
<td>Total harmonic distortion plus noise (BTL)</td>
<td>1, 2</td>
</tr>
<tr>
<td>THD+N</td>
<td>Total harmonic distortion plus noise (SE)</td>
<td>3, 4</td>
</tr>
<tr>
<td>Closed loop response</td>
<td></td>
<td>5, 6</td>
</tr>
<tr>
<td>PD</td>
<td>Power Dissipation</td>
<td>7</td>
</tr>
<tr>
<td>PO</td>
<td>Output power</td>
<td>8</td>
</tr>
<tr>
<td>Crosstalk</td>
<td>vs Frequency</td>
<td>9, 10</td>
</tr>
<tr>
<td>PSRR</td>
<td>Power supply ripple rejection (BTL)</td>
<td>11, 12</td>
</tr>
<tr>
<td>PSRR</td>
<td>Power supply ripple rejection (SE)</td>
<td>13</td>
</tr>
<tr>
<td>Z</td>
<td>Input impedance</td>
<td>14, 15</td>
</tr>
</tbody>
</table>

\(^{(1)}\) All graphs were taken using an external heatsink with \(\theta_{SA} = 25^\circ C/W.\)
Figure 3.

TOTAL HARMONIC DISTORTION + NOISE (SE) vs FREQUENCY

- $V_{DD} = 5 \text{ V}$
- $R_L = 32 \Omega$
- Gain = 14 dB
- $C_i = 0.47 \mu\text{F}$
- $C_o = 330 \mu\text{F}$
- SE Stereo
- $P_0 = 75 \mu\text{W}$

Figure 4.

TOTAL HARMONIC DISTORTION + NOISE (SE) vs FREQUENCY

- $V_{DD} = 5 \text{ V}$
- $R_L = 10 \text{ k}\Omega$
- Gain = 14 dB
- $C_i = 0.47 \mu\text{F}$
- $C_o = 330 \mu\text{F}$
- SE Stereo
- $V_O = 1 V_{RMS}$

Figure 5.

TOTAL HARMONIC DISTORTION + NOISE (BTL) vs OUTPUT POWER

- $V_{DD} = 5 \text{ V}$
- $R_L = 4 \Omega$
- Gain = 20 dB
- $C_i = 0.47 \mu\text{F}$
- BTL Stereo
- 20 kHz
- 20 Hz
- 20 kHz

Figure 6.

TOTAL HARMONIC DISTORTION + NOISE (BTL) vs OUTPUT POWER

- $V_{DD} = 5 \text{ V}$
- $R_L = 8 \Omega$
- Gain = 20 dB
- $C_i = 0.47 \mu\text{F}$
- BTL Stereo
- 20 kHz
- 1 kHz
- 20 Hz
TOTAL HARMONIC DISTORTION + NOISE (SE) vs OUTPUT POWER

V<sub>DD</sub> = 5 V
R<sub>L</sub> = 32 Ω
Gain = 14 dB
C<sub>i</sub> = 0.47 μF
C<sub>O</sub> = 330 μF
SE Stereo

20 Hz
20 kHz
1 kHz

Figure 7.

TOTAL HARMONIC DISTORTION + NOISE (SE) vs OUTPUT VOLTAGE

V<sub>DD</sub> = 5 V
R<sub>L</sub> = 10 kΩ
Gain = 14 dB
C<sub>i</sub> = 0.47 μF
C<sub>O</sub> = 330 μF
SE Stereo

20 kHz
1 kHz

Figure 8.

CLOSED LOOP RESPONSE

V<sub>DD</sub> = 5 V
R<sub>L</sub> = 8 Ω
Gain = 0 dB
Mode = BTL

Figure 9.

CLOSED LOOP RESPONSE

V<sub>DD</sub> = 5 V
R<sub>L</sub> = 8 Ω
Gain = 20 dB
Mode = BTL

Figure 10.
Figure 11. POWER DISSIPATION (PER CHANNEL) vs OUTPUT POWER
VDD = 5 V
BTL
8 Ω
4 Ω

Figure 12. POWER DISSIPATION (PER CHANNEL) vs OUTPUT POWER
VDD = 5 V
SE
8 Ω
16 Ω
32 Ω

Figure 13. OUTPUT POWER vs LOAD RESISTANCE
VDD = 5 V
Gain = 20 dB
BTL Stereo
THD+N = 10%
THD+N = 1%

Figure 14. CROSSTALK vs FREQUENCY
VDD = 5 V
P0 = 1 W
RL = 8 Ω
Gain = 0 dB
BTL
Left to Right
Right to Left

V = 5 V
Gain = 20 dB
BTL Stereo
THD+N = 10%
THD+N = 1%

V = 5 V
Gain = 0 dB
BTL
Figure 15.

CROSSTALK vs FREQUENCY

-40 -60 -80 -100 -120 -140
20 100 200 1 k 2 k 10 k 20 k

V_DD = 5 V
P_O = 1 W
R_L = 8 Ω
Gain = 20 dB
BTL

Left to Right
Right to Left

Figure 16.

POWER SUPPLY REJECTION RATIO (BTL) vs FREQUENCY

0 -20 -40 -60 -80 -100
20 100 200 1 k 2 k 10 k 20 k

V_DD = 5 V
R_L = 8 Ω
C_(BYP) = 0.47 μF
C_I = 0.47 μF
BTL

Gain = 20 dB
Gain = 0 dB

Figure 17.

POWER SUPPLY REJECTION RATIO (SE) vs FREQUENCY

0 -10 -20 -30 -40 -50 -60 -70 -80 -90
20 100 200 1 k 2 k 10 k 20 k

V_DD = 5 V
R_L = 32 Ω
C_(BYP) = 0.47 μF
C_I = 0.47 μF
C_O = 330 μF
SE

Gain = 0 dB
Gain = 14 dB

Figure 18.

INPUT IMPEDANCE vs BTL GAIN

0 10 20 30 40 50 60 70 80 90

-40 -30 -20 -10 0 10 20

BTL Gain – dB

Z_I – Input Impedance – kΩ
APPLICATION INFORMATION

SELECTION OF COMPONENTS

Figure 19 and Figure 20 are schematic diagrams of typical LCD monitor application circuits.

![Schematic Diagram]

A. A 0.47-µF ceramic capacitor should be placed as close as possible to the IC. For filtering lower-frequency noise signals, a larger electrolytic capacitor of 10 µF or greater should be placed near the audio power amplifier.

Figure 19. Typical TPA6021A4 Application Circuit Using Single-Ended Inputs and Input MUX
**APPLICATION INFORMATION (continued)**

**A.** A 0.47-µF ceramic capacitor should be placed as close as possible to the IC. For filtering lower-frequency noise signals, a larger electrolytic capacitor of 10 µF or greater should be placed near the audio power amplifier.

**Figure 20. Typical TPA6021A4 Application Circuit Using Differential Inputs**

**SE/BTL OPERATION**

The ability of the TPA6021A4 to easily switch between BTL and SE modes is one of its most important cost saving features. This feature eliminates the requirement for an additional headphone amplifier in applications where internal stereo speakers are driven in BTL mode but external headphone or speakers must be accommodated. Internal to the TPA6021A4, two separate amplifiers drive OUT+ and OUT−. The SE/BTL input controls the operation of the follower amplifier that drives LOUT− and ROUT−. When SE/BTL is held low, the amplifier is on and the TPA6021A4 is in the BTL mode. When SE/BTL is held high, the OUT− amplifiers are in a high output impedance state, which configures the TPA6021A4 as an SE driver from LOUT+ and ROUT+. IDD is reduced by approximately one-third in SE mode. Control of the SE/BTL input can be from a logic-level CMOS source or, more typically, from a resistor divider network as shown in Figure 21. The trip level for the SE/BTL input can be found in the recommended operating conditions table.
APPLICATION INFORMATION (continued)

Figure 21. TPA6021A4 Resistor Divider Network Circuit

Using a 1/8-in. (3,5 mm) stereo headphone jack, the control switch is closed when no plug is inserted. When closed the 100-kΩ/1-kΩ divider pulls the SE/BTL input low. When a plug is inserted, the 1-kΩ resistor is disconnected and the SE/BTL input is pulled high. When the input goes high, the OUT− amplifier is shut down causing the speaker to mute (open-circuits the speaker). The OUT+ amplifier then drives through the output capacitor (CO) into the headphone jack.

SHUTDOWN MODES

The TPA6021A4 employs a shutdown mode of operation designed to reduce supply current (IDD) to the absolute minimum level during periods of nonuse for power conservation. The SHUTDOWN input terminal should be held high during normal operation when the amplifier is in use. Pulling SHUTDOWN low causes the outputs to mute and the amplifier to enter a low-current state, IDD = 20 µA. SHUTDOWN should never be left unconnected because amplifier operation would be unpredictable.

Table 1. SE/BTL and Shutdown Functions

<table>
<thead>
<tr>
<th>INPUTS(1)</th>
<th>AMPLIFIER STATE</th>
</tr>
</thead>
<tbody>
<tr>
<td>SE/BTL</td>
<td>SHUTDOWN</td>
</tr>
<tr>
<td>X</td>
<td>Low</td>
</tr>
<tr>
<td>Low</td>
<td>High</td>
</tr>
<tr>
<td>High</td>
<td>High</td>
</tr>
<tr>
<td></td>
<td>Mute</td>
</tr>
<tr>
<td></td>
<td>BTL</td>
</tr>
<tr>
<td></td>
<td>SE</td>
</tr>
</tbody>
</table>

(1) Inputs should never be left unconnected.

FADE OPERATION

For design flexibility, a fade mode is provided to slowly ramp up the amplifier gain when coming out of shutdown mode and conversely ramp the gain down when going into shutdown. This mode provides a smooth transition between the active and shutdown states and virtually eliminates any pops or clicks on the outputs.
When the FADE input is a logic low, the device is placed into fade-on mode. A logic high on this pin places the amplifier in the fade-off mode. The voltage trip levels for a logic low (VLL) or logic high (VHH) can be found in the recommended operating conditions table.

When a logic low is applied to the FADE pin and a logic low is then applied on the SHUTDOWN pin, the channel gain steps down from gain step to gain step at a rate of two clock cycles per step. With a nominal internal clock frequency of 58 Hz, this equates to 34 ms (1/29 Hz) per step. The gain steps down until the lowest gain step is reached. The time it takes to reach this step depends on the gain setting prior to placing the device in shutdown. For example, if the amplifier is in the highest gain mode of 20 dB, the time it takes to ramp down the channel gain is 1.05 seconds. This number is calculated by taking the number of steps to reach the lowest gain from the highest gain, or 31 steps, and multiplying by the time per step, or 34 ms.

After the channel gain is stepped down to the lowest gain, the amplifier begins discharging the bypass capacitor from the nominal voltage of VDD/2 to ground. This time is dependent on the value of the bypass capacitor. For a 0.47-µF capacitor that is used in the application diagram in Figure 19, the time is approximately 500 ms. This time scales linearly with the value of bypass capacitor. For example, if a 1-µF capacitor is used for bypass, the time period to discharge the capacitor to ground is twice that of the 0.47-µF capacitor, or 1 second. Figure 22 below is a waveform captured at the output during the shutdown sequence when the part is in fade-on mode. The gain is set to the highest level and the output is at VDD when the amplifier is shut down.

When a logic high is placed on the SHUTDOWN pin and the FADE pin is still held low, the device begins the start-up process. The bypass capacitor will begin charging. Once the bypass voltage reaches the final value of VDD/2, the gain increases in 2-dB steps from the lowest gain level to the gain level set by the dc voltage applied to the VOLUME pin.

In the fade-off mode, the output of the amplifier immediately drops to VDD/2 and the bypass capacitor begins a smooth discharge to ground. When shutdown is released, the bypass capacitor charges up to VDD/2 and the channel gain returns immediately to the value on the VOLUME terminal. Figure 23 below is a waveform captured at the output during the shutdown sequence when the part is in the fade-off mode. The gain is set to the highest level, and the output is at VDD when the amplifier is shut down.

The power-up sequence is different from the shutdown sequence and the voltage on the FADE pin does not change the power-up sequence. Upon a power-up condition, the TPA6021A4 begins in the lowest gain setting and steps up 2 dB every 2 clock cycles until the final value is reached as determined by the dc voltage applied to the VOLUME pin.
VOLUME OPERATION

The VOLUME pin controls the BTL volume when driving speakers, and the SE volume when driving headphones. This pin is controlled with a dc voltage, which should not exceed \( V_{DD} \).

The output volume increases in discrete steps as the dc voltage increases and decreases in discrete steps as the dc voltage decreases. There are a total of 32 discrete gain steps of the amplifier and range from -85 dB to 20 dB for BTL operation and -85 dB to 14 dB for SE operation.

A pictorial representation of the typical volume control can be found in Figure 24.

![Figure 24. Typical DC Volume Control Operation](image-url)
INPUT RESISTANCE

Each gain setting is achieved by varying the input resistance of the amplifier, which can range from its smallest value to over six times that value. As a result, if a single capacitor is used in the input high-pass filter, the –3 dB or cutoff frequency also changes by over six times.

The input resistance at each gain setting is given in Figure 18.

The –3-dB frequency can be calculated using Equation 1.

\[ f_{-3\,\text{dB}} = \frac{1}{2\pi CR_i} \]  

(1)

INPUT CAPACITOR, \( C_i \)

In the typical application an input capacitor (\( C_i \)) is required to allow the amplifier to bias the input signal to the proper dc level for optimum operation. In this case, \( C_i \) and the input impedance of the amplifier (\( R_i \)) form a high-pass filter with the corner frequency determined in Equation 2.

\[ f_{c(\text{highpass})} = \frac{1}{2\pi R_i C_i} \]  

(2)

The value of \( C_i \) is important to consider as it directly affects the bass (low frequency) performance of the circuit. Consider the example where \( R_i \) is 70 kΩ and the specification calls for a flat-bass response down to 40 Hz. Equation 2 is reconfigured as Equation 3.

\[ C_i = \frac{1}{2\pi R_i f_c} \]  

(3)

In this example, \( C_i \) is 56.8 nF, so one would likely choose a value in the range of 56 nF to 1 µF. A further consideration for this capacitor is the leakage path from the input source through the input network (\( C_i \)) and the feedback network to the load. This leakage current creates a dc offset voltage at the input to the amplifier that reduces useful headroom, especially in high gain applications. For this reason, a low-leakage tantalum or ceramic capacitor is the best choice. When polarized capacitors are used, the positive side of the capacitor should face the amplifier input in most applications as the dc level there is held at \( V_{\text{DD}}/2 \), which is likely higher than the source dc level. Note that it is important to confirm the capacitor polarity in the application.
POWER SUPPLY DECOUPLING, $C_{(S)}$

The TPA6021A4 is a high-performance CMOS audio amplifier that requires adequate power supply decoupling to ensure the output total harmonic distortion (THD) is as low as possible. Power supply decoupling also prevents oscillations for long lead lengths between the amplifier and the speaker. The optimum decoupling is achieved by using two capacitors of different types that target different types of noise on the power supply leads. For higher frequency transients, spikes, or digital hash on the line, a good low equivalent-series-resistance (ESR) ceramic capacitor, typically 0.1 µF placed as close as possible to the device $V_{DD}$ lead, works best. For filtering lower-frequency noise signals, a larger aluminum electrolytic capacitor of 10 µF or greater placed near the audio power amplifier is recommended.

MIDRAIL BYPASS CAPACITOR, $C_{(BYP)}$

The midrail bypass capacitor $(C_{(BYP)})$ is the most critical capacitor and serves several important functions. During start-up or recovery from shutdown mode, $C_{(BYP)}$ determines the rate at which the amplifier starts up. The second function is to reduce noise produced by the power supply caused by coupling into the output drive signal. This noise is from the midrail generation circuit internal to the amplifier, which appears as degraded PSRR and THD+N.

Bypass capacitor $(C_{(BYP)})$ values of 0.47-µF to 1-µF ceramic or tantalum low-ESR capacitors are recommended for the best THD and noise performance. For the best pop performance, choose a value for $C_{(BYP)}$ that is equal to or greater than the value chosen for $C_i$. This ensures that the input capacitors are charged up to the midrail voltage before $C_{(BYP)}$ is fully charged to the midrail voltage.

OUTPUT COUPLING CAPACITOR, $C_{(C)}$

In the typical single-supply SE configuration, an output coupling capacitor $(C_{(C)})$ is required to block the dc bias at the output of the amplifier, thus preventing dc currents in the load. As with the input coupling capacitor, the output coupling capacitor and impedance of the load form a high-pass filter governed by Equation 4.

$$f_{c\text{(high)}} = \frac{1}{2\pi R_L C_{(C)}}$$

(4)

The main disadvantage, from a performance standpoint, is the load impedances are typically small, which drives the low-frequency corner higher, degrading the bass response. Large values of $C_{(C)}$ are required to pass low frequencies into the load. Consider the example where a $C_{(C)}$ of 330 µF is chosen and loads vary from 4 Ω, 8 Ω, 32 Ω, 10 kΩ, and 47 kΩ. Table 2 summarizes the frequency response characteristics of each configuration.

<table>
<thead>
<tr>
<th>$R_L$</th>
<th>$C_{(C)}$</th>
<th>LOWEST FREQUENCY</th>
</tr>
</thead>
<tbody>
<tr>
<td>4 Ω</td>
<td>330 µF</td>
<td>120 Hz</td>
</tr>
<tr>
<td>8 Ω</td>
<td>330 µF</td>
<td>60 Hz</td>
</tr>
<tr>
<td>32 Ω</td>
<td>330 µF</td>
<td>15 Hz</td>
</tr>
<tr>
<td>10,000 Ω</td>
<td>330 µF</td>
<td>0.05 Hz</td>
</tr>
<tr>
<td>47,000 Ω</td>
<td>330 µF</td>
<td>0.01 Hz</td>
</tr>
</tbody>
</table>
As Table 2 indicates, most of the bass response is attenuated into a 4-Ω load, an 8-Ω load is adequate, headphone response is good, and drive into line level inputs (a home stereo for example) is exceptional.

**USING LOW-ESR CAPACITORS**

Low-ESR capacitors are recommended throughout this applications section. A real (as opposed to ideal) capacitor can be modeled simply as a resistor in series with an ideal capacitor. The voltage drop across this resistor minimizes the beneficial effects of the capacitor in the circuit. The lower the equivalent value of this resistance, the more the real capacitor behaves like an ideal capacitor.

**BRIDGE-TIED LOAD vs SINGLE-ENDED LOAD**

Figure 26 shows a Class-AB audio power amplifier (APA) in a BTL configuration. The TPA6021A4 BTL amplifier consists of two Class-AB amplifiers driving both ends of the load. There are several potential benefits to this differential drive configuration, but, initially consider power to the load. The differential drive to the speaker means that as one side is slewing up, the other side is slewing down, and vice versa. This in effect doubles the voltage swing on the load as compared to a ground referenced load. Plugging $2 \times V_{O(PP)}$ into the power equation, where voltage is squared, yields 4x the output power from the same supply rail and load impedance (see Equation 5).

$$V_{(rms)} = \frac{V_{O(PP)}}{2^{1/2}}$$

$$\text{Power} = \frac{V_{(rms)}^2}{R_L}$$

(5)

![Figure 26. Bridge-Tied Load Configuration](image-url)
In a typical computer sound channel operating at 5 V, bridging raises the power into an 8-Ω speaker from a single-ended (SE, ground reference) limit of 250 mW to 1 W. In sound power that is a 6-dB improvement, which is loudness that can be heard. In addition to increased power there are frequency response concerns. Consider the single-supply SE configuration shown in Figure 27. A coupling capacitor is required to block the dc offset voltage from reaching the load. These capacitors can be quite large (approximately 33 µF to 1000 µF), so they tend to be expensive, heavy, occupy valuable PCB area, and have the additional drawback of limiting low-frequency performance of the system. This frequency limiting effect is due to the high-pass filter network created with the speaker impedance and the coupling capacitance and is calculated with Equation 6.

\[ f_c = \frac{1}{2\pi R_L C_C} \]  

(6)

For example, a 68-µF capacitor with an 8-Ω speaker would attenuate low frequencies below 293 Hz. The BTL configuration cancels the dc offsets, which eliminates the need for the blocking capacitors. Low-frequency performance is then limited only by the input network and speaker response. Cost and PCB space are also minimized by eliminating the bulky coupling capacitor.

![Figure 27. Single-Ended Configuration and Frequency Response](image)

Increasing power to the load does carry a penalty of increased internal power dissipation. The increased dissipation is understandable considering that the BTL configuration produces 4x the output power of the SE configuration. Internal dissipation versus output power is discussed further in the crest factor and thermal considerations section.

SINGLE-ENDED OPERATION

In SE mode (see Figure 27), the load is driven from the primary amplifier output for each channel (OUT+).

The amplifier switches single-ended operation when the SE/BTL terminal is held high. This puts the negative outputs in a high-impedance state, and effectively reduces the amplifier’s gain by 6 dB.

BTL AMPLIFIER EFFICIENCY

Class-AB amplifiers are inefficient. The primary cause of these inefficiencies is voltage drop across the output stage transistors. There are two components of the internal voltage drop. One is the headroom or dc voltage drop that varies inversely to output power. The second component is due to the sinewave nature of the output. The total voltage drop can be calculated by subtracting the RMS value of the output voltage from \( V_{DD} \). The internal voltage drop multiplied by the RMS value of the supply current (\( I_{DD \text{rms}} \)) determines the internal power dissipation of the amplifier.

An easy-to-use equation to calculate efficiency starts out as being equal to the ratio of power from the power supply to the power delivered to the load. To accurately calculate the RMS and average values of power in the load and in the amplifier, the current and voltage waveform shapes must first be understood (see Figure 28).
Figure 28. Voltage and Current Waveforms for BTL Amplifiers

Although the voltages and currents for SE and BTL are sinusoidal in the load, currents from the supply are very different between SE and BTL configurations. In an SE application the current waveform is a half-wave rectified shape, whereas in BTL it is a full-wave rectified waveform. This means RMS conversion factors are different. Keep in mind that for most of the waveform both the push and pull transistors are not on at the same time, which supports the fact that each amplifier in the BTL device only draws current from the supply for half the waveform. The following equations are the basis for calculating amplifier efficiency.

Efficiency of a BTL amplifier = \( \frac{P_L}{P_{SUP}} \)

Where:
\[ P_L = \frac{V_L \text{rms}^2}{R_L}, \quad \text{and} \quad V_{LRMS} = \frac{V_P}{\sqrt{2}}, \quad \text{therefore,} \quad P_L = \frac{V_P^2}{2R_L} \]

and \( P_{SUP} = V_{DD}I_{DDavg} \) and \( I_{DDavg} = \frac{1}{\pi} \int_0^\pi \frac{V_P}{R_L} \sin(t) \, dt = \frac{1}{\pi} \cdot \frac{V_P}{R_L} \left[ \cos(t) \right]_0^\pi = \frac{2V_P}{\pi R_L} \)

Therefore, \( P_{SUP} = \frac{2V_{DD}V_P}{\pi R_L} \)

substituting PL and PSUP into Equation 7,

Efficiency of a BTL amplifier = \( \frac{V_P^2}{2V_{DD}V_P} \cdot \frac{2R_L}{\pi R_L} = \frac{\pi V_P}{4V_{DD}} \)

Where:
\[ V_P = \sqrt{2P_LR_L} \]

Therefore, \( \eta_{BTL} = \frac{\pi \sqrt{2P_LR_L}}{4V_{DD}} \)

Table 3 employs Equation 8 to calculate efficiencies for four different output power levels. Note that the efficiency of the amplifier is quite low for lower power levels and rises sharply as power to the load is increased resulting in a nearly flat internal power dissipation over the normal operating range. Note that the internal dissipation at full output power is less than in the half power range. Calculating the efficiency for a specific system is the key to proper power supply design. For a stereo 1-W audio system with 8-Ω loads and a 5-V supply, we get an efficiency of 0.628. Total output power is 2-W. Thus the maximum draw on the power supply is almost 3.25 W.
Table 3. Efficiency vs Output Power in 5-V, 8-Ω BTL Systems

<table>
<thead>
<tr>
<th>OUTPUT POWER (W)</th>
<th>EFFICIENCY (%)</th>
<th>PEAK VOLTAGE (V)</th>
<th>INTERNAL DISSIPATION (W)</th>
</tr>
</thead>
<tbody>
<tr>
<td>0.25</td>
<td>31.4</td>
<td>2.00</td>
<td>0.55</td>
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<tr>
<td>0.50</td>
<td>44.4</td>
<td>2.83</td>
<td>0.62</td>
</tr>
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<td>1.00</td>
<td>62.8</td>
<td>4.00</td>
<td>0.59</td>
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<tr>
<td>1.25</td>
<td>70.2</td>
<td>4.47 (1)</td>
<td>0.53</td>
</tr>
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</table>

(1) High peak voltages cause the THD to increase.

A final point to remember about Class-AB amplifiers (either SE or BTL) is how to manipulate the terms in the efficiency equation to utmost advantage when possible. Note that in equation 8, $V_{DD}$ is in the denominator. This indicates that as $V_{DD}$ goes down, efficiency goes up.

**CREST FACTOR AND THERMAL CONSIDERATIONS**

Class-AB power amplifiers dissipate a significant amount of heat in the package under normal operating conditions. A typical music CD requires 12 dB to 15 dB of dynamic range, or headroom above the average power output, to pass the loudest portions of the signal without distortion. In other words, music typically has a crest factor between 12 dB and 15 dB. When determining the optimal ambient operating temperature, the internal dissipated power at the average output power level must be used. From the data sheet graph (Figure 5.), one can see that when the TPA6021A4 is operating from a 5-V supply into a 4-Ω speaker at 1% THD, that output power is 1.5-W so maximum instantaneous output power is 3-W. Use equation 9 to convert watts to dB.

$$P_{dB} = 10 \log \frac{P_W}{P_{ref}} = 10 \log \frac{3 W}{1 W} = 5 \text{ dB}$$

(9)

Subtracting the headroom restriction to obtain the average listening level without distortion yields:

- 5 dB - 15 dB = −10 dB (15-dB crest factor)
- 5 dB - 12 dB = −7 dB (12-dB crest factor)
- 5 dB - 9 dB = −4 dB (9-dB crest factor)
- 5 dB - 6 dB = −1 dB (6-dB crest factor)
- 5 dB - 3 dB = 2 dB (3-dB crest factor)

To convert dB back into watts use equation 10.

$$P_W = 10^{\frac{P_{dB}}{10}} \times P_{ref}$$

(10)

- 48 mW (18-dB crest factor)
- 95 mW (15-dB crest factor)
- 190 mW (12-dB crest factor)
- 380 mW (9-dB crest factor)
- 750 mW (6-dB crest factor)
- 1500 mW (3-dB crest factor)

This is valuable information to consider when attempting to estimate the heat dissipation requirements for the amplifier system. Comparing the worst case, which is 1.5 W of continuous power output with a 3-dB crest factor, against 12-dB and 15-dB applications significantly affects maximum ambient temperature ratings for the system. Using the power dissipation curves for a 5-V, 4-Ω system, the internal dissipation in the TPA6021A4 and maximum ambient temperatures is shown in Table 4.
The maximum dissipated power ($P_{D(max)}$) is reached at a much lower output power level for an 8-$\Omega$ load than for a 4-$\Omega$ load. As a result, this simple formula for calculating $P_{D(max)}$ may be used for an 8-$\Omega$ application.

$$P_{D(max)} = \frac{2V_D^2}{\pi^2 R_L}$$  \hspace{1cm} (11)

However, in the case of a 4-$\Omega$ load, the $P_{D(max)}$ occurs at a point well above the normal operating power level. The amplifier may therefore be operated at a higher ambient temperature than required by the $P_{D(max)}$ formula for a 4-$\Omega$ load.

The maximum ambient temperature depends on the heat-sinking ability of the PCB system. The derating factor for the N package with an external heatsink is shown in the dissipation rating table. Use Equation 12 to convert this to $\theta_{JA}$.

$$\theta_{JA} = \frac{1}{\text{Derating Factor}} = \frac{1}{0.0222} = 45^\circ\text{C/W}$$  \hspace{1cm} (12)

To calculate maximum ambient temperatures, first consider that the numbers from the dissipation graphs are per channel, so the dissipated power needs to be doubled for two channel operation. Given $\theta_{JA}$, the maximum allowable junction temperature, and the total internal dissipation, the maximum ambient temperature can be calculated using Equation 13. The maximum recommended junction temperature for the TPA6021A4 is 150°C. The internal dissipation figures are taken from the Power Dissipation vs Output Power graphs.

$$T_{A Max} = T_J Max - \theta_{JA} P_D$$

$$= 150 - 45 (0.6 \times 2) = 96^\circ\text{C}(15\text{-dB crest factor})$$  \hspace{1cm} (13)

**NOTE:**

Internal dissipation of 0.6 W is estimated for a 2-W system with 15-dB crest factor per channel.

Table 4 and Table 5 show that some applications require no airflow to keep junction temperatures in the specified range. The TPA6021A4 is designed with thermal protection that turns the device off when the junction temperature surpasses 150°C to prevent damage to the IC. Table 4 and Table 5 were calculated for maximum listening volume without distortion. When the output level is reduced the numbers in the table change significantly. Also, using 8-$\Omega$ speakers increases the thermal performance by increasing amplifier efficiency.
### Packaging Information

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<th>Package Drawing</th>
<th>Pins</th>
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(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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