1 Features

- AEC-Q101 Qualified
  - Device HBM Classification Level H3B
  - Device CDM Classification Level C5
  - Device Temperature Range: –40°C to +125°C
- IEC 61000-4-2 Level 4 ESD Protection
  (See the ESD Ratings—IEC Specification Table)
  - ±12-kV Contact Discharge
  - ±15-kV Air Gap Discharge
- IEC 61000-4-4 EFT Protection
  - 80 A (5/50 ns)
- IEC 61000-4-5 Surge Protection
  - 2.5 A (8/20 μs)
- I/O Capacitance 0.42 pF to 0.5 pF (Typical)
- DC Breakdown Voltage 6.4 V (Minimum)
- Ultra Low Leakage Current 10 nA (Maximum)
- Low ESD Clamping Voltage (14 V at 5-A TLP)
- Easy Flow-Through Routing Packages

2 Applications

- End Equipment
  - Head Unit
  - Rear Seat Entertainment
  - Telematics
  - USB Hub
  - Navigation Module
  - Media Interface

- Interfaces
  - USB 2.0
  - USB 3.0
  - HDMI 1.4/2.0
  - LVDS
  - DisplayPort
  - SIM Card

3 Description

The TPDxE05U06-Q1 is a family of unidirectional Transient Voltage Suppressor (TVS) Electrostatic Discharge (ESD) protection diodes with ultra-low capacitance. They are rated to dissipate ESD strikes above the maximum level specified in the IEC 61000-4-2 level 4 international standard. The ultra-low loading capacitance makes these devices ideal for protecting any high-speed signal applications up to 6 Gbps.

These devices are also available without automotive qualification: TPDxE05U06.

Device Information

<table>
<thead>
<tr>
<th>PART NUMBER</th>
<th>PACKAGE</th>
<th>BODY SIZE (NOM)</th>
</tr>
</thead>
<tbody>
<tr>
<td>TPD4E05U06-Q1</td>
<td>USON (10)</td>
<td>2.50 mm × 1.00 mm</td>
</tr>
<tr>
<td>TPD1E05U06-Q1</td>
<td>X1SON (2)</td>
<td>0.60 mm × 1.00 mm</td>
</tr>
</tbody>
</table>

(1) For all available packages, see the orderable addendum at the end of the datasheet.
4 Revision History

Changes from Revision A (August 2014) to Revision B

- Added 1-channel (TPD1E05U06-Q1) package ................................................................. 1
- Added DPY package information in Thermal Information table ........................................ 4
- Added DPY package Dynamic resistance in Electrical Characteristics table .................. 5
- Added DPY package Line capacitance in Electrical Characteristics table ......................... 5

Changes from Revision B (August 2016) to Revision C

- Changed DPY Package pin configuration in the Pin Configuration and Functions section ...... 1

Changes from Original (August 2014) to Revision A

- Added (See the ESD Ratings—IEC Specification Table) to Feature: IEC 61000-4-2 Level 4 ESD Protection .......................... 1
5 Pin Configuration and Functions

**DPY Package**
2-Pin X1SON
Top View

**DQA Package**
10-Pin USON
Top View

---

**Pin Functions TPD1E05U06-Q1 DPY**

<table>
<thead>
<tr>
<th>PIN NO.</th>
<th>TYPE</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>I/O</td>
<td>I/O ESD Protected Channel(1)</td>
</tr>
<tr>
<td>2</td>
<td>GND</td>
<td>Ground; Connect to ground</td>
</tr>
</tbody>
</table>

(1) Place as close to the connector as possible.

**Pin Functions TPD4E05U06-Q1 DQA**

<table>
<thead>
<tr>
<th>PIN NO.</th>
<th>TYPE</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>D1+</td>
<td>I/O ESD Protected Channel(1)</td>
</tr>
<tr>
<td>2</td>
<td>D1−</td>
<td>I/O ESD Protected Channel(1)</td>
</tr>
<tr>
<td>4</td>
<td>D2+</td>
<td>I/O ESD Protected Channel(1)</td>
</tr>
<tr>
<td>5</td>
<td>D2−</td>
<td>I/O ESD Protected Channel(1)</td>
</tr>
<tr>
<td>6, 7, 9, 10</td>
<td>NC</td>
<td>Not Connected; Used for optional straight-through routing. Can be left floating or grounded</td>
</tr>
<tr>
<td>3, 8</td>
<td>GND</td>
<td>Ground; Connect to ground</td>
</tr>
</tbody>
</table>

(1) Place as close to the connector as possible.
6 Specifications

6.1 Absolute Maximum Ratings
over operating free-air temperature range (unless otherwise noted)\(^{(1)(2)}\)

<table>
<thead>
<tr>
<th>Specification</th>
<th>MIN</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>Electrical fast transient</td>
<td></td>
<td>80</td>
<td>A</td>
</tr>
<tr>
<td>IEC 61000-4-4 (5/50 ns)</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Peak pulse</td>
<td>2.5</td>
<td>40</td>
<td>W</td>
</tr>
<tr>
<td>IEC 61000-4-5 Current (tp – 8/20 µs)</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>IEC 61000-4-5 Power (tp – 8/20 µs) - TPD4E05U06-Q1 (^{(3)})</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>T(_A) Operating temperature</td>
<td>–40</td>
<td>125</td>
<td>°C</td>
</tr>
<tr>
<td>T(_{stg}) Storage temperature</td>
<td>–65</td>
<td>150</td>
<td>°C</td>
</tr>
</tbody>
</table>

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) Voltages are with respect to GND unless otherwise noted.

(3) Measured at 25°C

6.2 ESD Ratings—AEC Specification

<table>
<thead>
<tr>
<th>ESD Model</th>
<th>VALUE</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>Human-body model (HBM), per AEC Q100-002 (^{(2)})</td>
<td>±8000</td>
<td>V</td>
</tr>
<tr>
<td>Charged-device model (CDM), per AEC Q100-011</td>
<td>±1000</td>
<td>V</td>
</tr>
</tbody>
</table>

(1) Electrostatic discharge (ESD) to measure device sensitivity and immunity to damage caused by assembly line electrostatic discharges into the device.

(2) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 ESD Ratings—IEC Specification

<table>
<thead>
<tr>
<th>ESD Model</th>
<th>VALUE</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>IEC 61000-4-2 contact discharge - TPD4E05U06-Q1 (^{(1)})</td>
<td>±12000</td>
<td>V</td>
</tr>
<tr>
<td>IEC 61000-4-2 contact discharge - TPD1E05U06-Q1</td>
<td>±12000</td>
<td>V</td>
</tr>
<tr>
<td>IEC 61000-4-2 air-gap discharge</td>
<td>±15000</td>
<td>V</td>
</tr>
</tbody>
</table>

(1) Measured at 25°C, per IEC 61000.4.2 Ed. 2.0 Section 7.2.4.

6.4 Recommended Operating Conditions
over operating free-air temperature range (unless otherwise noted)

<table>
<thead>
<tr>
<th>Specification</th>
<th>MIN</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>V(_I)</td>
<td>0</td>
<td>5.5</td>
<td>V</td>
</tr>
<tr>
<td>T(_A)</td>
<td>–40</td>
<td>125</td>
<td>°C</td>
</tr>
</tbody>
</table>

6.5 Thermal Information

<table>
<thead>
<tr>
<th>Thermal Metric(^{(1)})</th>
<th>TPD1E05U06-Q1 DPA (X1SON)</th>
<th>TPD4E05U06-Q1 DQA (USON)</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>R(_\text{JA})</td>
<td>697.3</td>
<td>327</td>
<td>°C/W</td>
</tr>
<tr>
<td>R(_\text{JC(top)})</td>
<td>471</td>
<td>189.5</td>
<td>°C/W</td>
</tr>
<tr>
<td>R(_\text{JB})</td>
<td>575.9</td>
<td>257.7</td>
<td>°C/W</td>
</tr>
<tr>
<td>(\psi-current)</td>
<td>175.7</td>
<td>60.9</td>
<td>°C/W</td>
</tr>
<tr>
<td>(\psi-board)</td>
<td>575.1</td>
<td>257</td>
<td>°C/W</td>
</tr>
</tbody>
</table>

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.
6.6 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>INPUT – OUTPUT RESISTANCE</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$V_{RWM}$ Reverse stand-off voltage</td>
<td>$I_O &lt; 10 \mu A$</td>
<td></td>
<td></td>
<td>5.5</td>
<td>V</td>
</tr>
<tr>
<td>$V_{BR}$ Break-down voltage</td>
<td>$I_O = 1 \ mA$</td>
<td></td>
<td></td>
<td>6.4</td>
<td>V</td>
</tr>
<tr>
<td>$V_{CLAMP}$ Clamp voltage</td>
<td>$I_{PP} = 1 \ A$, TLP, from I/O to GND (1)</td>
<td></td>
<td></td>
<td>10</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td>$I_{PP} = 5 \ A$, TLP, from I/O to GND (1)</td>
<td></td>
<td></td>
<td>14</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td>$I_{PP} = 1 \ A$, TLP, from GND to I/O (1)</td>
<td></td>
<td></td>
<td>3</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td>$I_{PP} = 5 \ A$, TLP, from GND to I/O (1)</td>
<td></td>
<td></td>
<td>7.5</td>
<td>V</td>
</tr>
<tr>
<td>$I_{LEAK}$ Leakage current</td>
<td>$V_{IO} = 2.5 \ V$</td>
<td></td>
<td></td>
<td>1</td>
<td>nA</td>
</tr>
<tr>
<td>$R_{DYN}$ Dynamic resistance</td>
<td>DPY package</td>
<td>I/O to GND (2)</td>
<td></td>
<td>0.8</td>
<td>Ω</td>
</tr>
<tr>
<td></td>
<td></td>
<td>GND to I/O (2)</td>
<td></td>
<td>0.7</td>
<td>Ω</td>
</tr>
<tr>
<td></td>
<td>DQA package</td>
<td>I/O to GND (2)</td>
<td></td>
<td>0.96</td>
<td>Ω</td>
</tr>
<tr>
<td></td>
<td></td>
<td>GND to I/O (2)</td>
<td></td>
<td>0.9</td>
<td>Ω</td>
</tr>
<tr>
<td>CAPACITANCE</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$C_L$ Line capacitance</td>
<td>$V_{IO} = 2.5 \ V$, $f = 1 \ MHz$, I/O to GND</td>
<td></td>
<td></td>
<td>TPD1E05U06-Q1 DPY package</td>
<td>0.42</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>TPD4E05U06-Q1 DQA package</td>
<td>0.5</td>
</tr>
<tr>
<td>$\Delta C_{IO-TO-GND}$ Variation of input capacitance</td>
<td>GND Pin $= 0 \ V$, $f = 1 \ MHz$, $V_{BIAS} = 2.5 \ V$, Channel x pin to GND – channel y pin to GND</td>
<td></td>
<td></td>
<td></td>
<td>0.05</td>
</tr>
<tr>
<td>$C_{CROSS}$ Channel to channel input capacitance</td>
<td>GND Pin $= 0 \ V$, $f = 1 \ MHz$, $V_{BIAS} = 2.5 \ V$, between channel pins</td>
<td></td>
<td></td>
<td></td>
<td>0.04</td>
</tr>
</tbody>
</table>

(1) Transition line pulse with 100 ns width, 200 ps rise time.
(2) Extraction of $R_{DYN}$ using least squares fit of TLP characteristics between $I = 5 \ A$ and $I = 10 \ A$. 
6.7 Typical Characteristics

Figure 1. Current vs Voltage
Current vs Voltage DC Voltage Sweep I-V Curve

Figure 2. Current and Power vs Time
Surge Curve (tp = 8/20 µs), Pin I/O to GND

Figure 3. Current vs Voltage
Positive TLP Plot I/O to GND

Figure 4. Current vs Voltage
Negative TLP Plot I/O to GND

Figure 5. Leakage Current vs Temperature

Figure 6. Voltage vs Time 8-kV IEC Waveform
Typical Characteristics (continued)

Figure 7. Voltage vs Time – 8-kV IEC Waveform

Figure 8. Insertion Loss vs Frequency
7 Detailed Description

7.1 Overview
The TPDxE05U06-Q1 is a family of unidirectional TVS ESD protection diode arrays with ultra-low capacitance between 0.42 pF and 0.5 pF. They are rated to dissipate ESD strikes above the maximum level specified in the IEC 61000-4-2 level 4 international standard (12-kV contact, 15-kV air gap). The ultra-low loading capacitance makes them ideal for protecting any high-speed signal applications up to 6 Gbps.

7.2 Functional Block Diagram

![Block Diagram](image)

Figure 9. TPD4E05U06-Q1 Block Diagram

![Block Diagram](image)

Figure 10. TPD1E05U06-Q1 Block Diagram

7.3 Feature Description

7.3.1 AEC-Q101 Qualification
These devices are qualified to AEC-Q101 standards. They pass HBM H3B (±8 kV) and CDM C5 (±1 kV) ESD ratings and are qualified to operate from –40°C to +125°C.

7.3.2 IEC 61000-4-2 Level 4 ESD Protection
The I/O pins can withstand ESD events up to ±12-kV contact and ±15-kV air. An ESD-surge clamp diverts the current to ground.

7.3.3 IEC 61000-4-4 EFT Protection
The I/O pins can withstand an electrical fast transient burst of up to 80 A (5/50 ns waveform, 4 kV with 50-Ω impedance). An ESD-surge clamp diverts the current to ground.
Feature Description (continued)

7.3.4 IEC 61000-4-5 Surge Protection
The I/O pins can withstand surge events up to 2.5 A and 40 W (8/20 µs waveform). An ESD-surge clamp diverts this current to ground.

7.3.5 I/O Capacitance
The capacitance between each I/O pin to ground is 0.5 pF. These capacitances support data rates up to 5 Gbps.

7.3.6 DC Breakdown Voltage
The DC breakdown voltage of each I/O pin is a minimum of 6.4 V. This ensures that sensitive equipment is protected from surges above the reverse standoff voltage of 5 V.

7.3.7 Ultra-Low Leakage Current
The I/O pins feature an ultra-low leakage current of 10 nA (Maximum) with a bias of 2.5 V.

7.3.8 Low ESD Clamping Voltage
The I/O pins feature an ESD clamp that is capable of clamping the voltage to 10 V (\(I_{pp} = 1\) A).

7.3.9 Easy Flow-Through Routing
The layout of this device makes it simple and easy to add protection to an existing layout. The packages offers flow-through routing, requiring minimal modification to an existing layout.

7.4 Device Functional Modes
The TPDxE05U06-Q1 are passive integrated circuits that triggers when voltages are above \(V_{BR}\) or below the lower diodes \(V_f\) (–0.6 V). During ESD events, voltages as high as ±15 kV (air) can be directed to ground via the internal diode network. When the voltages on the protected line fall below the trigger levels of TPDxE05U06-Q1 (usually within 10s of nano-seconds) the devices reverts to passive.
8 Application and Implementation

8.1 Application Information

The TPD4E05U06-Q1 is a diode type TVS which is typically used to provide a path to ground for dissipating ESD events on hi-speed signal lines between a human interface connector and a system. As the current from ESD passes through the TVS, only a small voltage drop is present across the diode. This is the voltage presented to the protected IC. The low $R_{\text{DYN}}$ of the triggered TVS holds this voltage, $V_{\text{CLAMP}}$, to a safe level for the protected IC.

8.2 Typical Application

![HDMI Connector Diagram]

Figure 11. HDMI 1.4 Application

8.2.1 Design Requirements

For this design example, two TPD4E05U06-Q1 devices, and a TPD5S116 are being used in an HDMI 1.4 application. This provides a complete port protection scheme.

Given the HDMI 1.4 application, the parameters in Table 1 are known.

<table>
<thead>
<tr>
<th>DESIGN PARAMETER</th>
<th>VALUE</th>
</tr>
</thead>
<tbody>
<tr>
<td>Signal range on pins 1, 2, 4, or 5</td>
<td>0 V to 5 V</td>
</tr>
<tr>
<td>Operating frequency</td>
<td>1.7 GHz</td>
</tr>
</tbody>
</table>

8.2.2 Detailed Design Procedure

To begin the design process, some parameters must be decided upon; the designer needs to know the following:

- Signal range on all the protected lines
- Operating frequency
8.2.2.1 Signal Range on Pin 1, 2, 4, or 5

The TPD4E05U06-Q1 has 4 identical protection channels for signal lines. The symmetry of the device provides flexibility when selecting which of the 4 I/O channels protect which signal lines. Any I/O will support a signal range of 0 to 5.5 V.

8.2.2.2 Operating Frequency

The TPD4E05U06-Q1 has a capacitance of 0.5 pF (Typical), supporting HDMI 1.4 data rates.

8.2.3 Application Curve

![Figure 12. 3.4 Gbps HDMI Eye Diagram](image-url)
9 Layout

9.1 Layout Guidelines

- The optimum placement is as close to the connector as possible.
  - EMI during an ESD event can couple from the trace being struck to other nearby unprotected traces, resulting in early system failures.
  - The PCB designer needs to minimize the possibility of EMI coupling by keeping any unprotected traces away from the protected traces which are between the TVS and the connector.
- Route the protected traces as straight as possible.
- Eliminate any sharp corners on the protected traces between the TVS and the connector by using rounded corners with the largest radii possible.
  - Electric fields tend to build up on corners, increasing EMI coupling.

9.2 Layout Example

This application is typical of an HDMI 1.4 layout.

![VIA to GND Plane](image)

Figure 13. TPD4E05U06-Q1 Layout
10 Device and Documentation Support

10.1 Documentation Support

10.1.1 Related Documentation
For related documentation see the following:
• TPD1E05U06-Q1 Evaluation Module User's Guide
• Reading and Understanding an ESD Protection Datasheet
• ESD Layout Guide
• TPD4E05U06DQA EVM User's Guide

10.2 Receiving Notification of Documentation Updates
To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on Alert me to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

10.3 Related Links
The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

<table>
<thead>
<tr>
<th>PARTS</th>
<th>PRODUCT FOLDER</th>
<th>SAMPLE &amp; BUY</th>
<th>TECHNICAL DOCUMENTS</th>
<th>TOOLS &amp; SOFTWARE</th>
<th>SUPPORT &amp; COMMUNITY</th>
</tr>
</thead>
<tbody>
<tr>
<td>TPD4E05U06-Q1</td>
<td>Click here</td>
<td>Click here</td>
<td>Click here</td>
<td>Click here</td>
<td>Click here</td>
</tr>
<tr>
<td>TPD1E05U06-Q1</td>
<td>Click here</td>
<td>Click here</td>
<td>Click here</td>
<td>Click here</td>
<td>Click here</td>
</tr>
</tbody>
</table>

10.4 Community Resources
The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community TI's Engineer-to-Engineer (E2E) Community. Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support TI's Design Support Quickly find helpful E2E forums along with design support tools and contact information for technical support.

10.5 Trademarks
E2E is a trademark of Texas Instruments. All other trademarks are the property of their respective owners.

10.6 Electrostatic Discharge Caution
This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

10.7 Glossary
SLYZ022 — TI Glossary.
This glossary lists and explains terms, acronyms, and definitions.
11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.
## PACKAGING INFORMATION

<table>
<thead>
<tr>
<th>Orderable Device</th>
<th>Status (1)</th>
<th>Package Type</th>
<th>Package Drawing</th>
<th>Pins</th>
<th>Package Qty</th>
<th>Eco Plan (2)</th>
<th>Lead/Ball Finish</th>
<th>MSL Peak Temp</th>
<th>Op Temp (°C)</th>
<th>Device Marking (4/5)</th>
<th>Samples</th>
</tr>
</thead>
<tbody>
<tr>
<td>TPD1E05U06QDPYRQ1</td>
<td>ACTIVE</td>
<td>X1SON</td>
<td>DPY</td>
<td>2</td>
<td>10000</td>
<td>Green (RoHS &amp; no Sb/Br)</td>
<td>NIPDAU</td>
<td>Level-1-260C-UNLIM</td>
<td>-40 to 125</td>
<td>4O</td>
<td>Samples</td>
</tr>
<tr>
<td>TPD4E05U06QDQARQ1</td>
<td>ACTIVE</td>
<td>USON</td>
<td>DQA</td>
<td>10</td>
<td>3000</td>
<td>Green (RoHS &amp; no Sb/Br)</td>
<td>NIPDAU</td>
<td>NIPDAUAG</td>
<td>Level-2-260C-1 YEAR</td>
<td>-40 to 125</td>
<td>(BRH, CQ1)</td>
</tr>
</tbody>
</table>

---

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) **MSL, Peak Temp:** The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) **Lead/Ball Finish -** Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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OTHER QUALIFIED VERSIONS OF TPD1E05U06-Q1, TPD4E05U06-Q1:

- Catalog: TPD1E05U06, TPD4E05U06

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
TAPE AND REEL INFORMATION

<table>
<thead>
<tr>
<th>Device</th>
<th>Package Type</th>
<th>Package Drawing</th>
<th>Pins</th>
<th>SPQ</th>
<th>Reel Diameter (mm)</th>
<th>Reel Width W1 (mm)</th>
<th>A0 (mm)</th>
<th>B0 (mm)</th>
<th>K0 (mm)</th>
<th>P1 (mm)</th>
<th>W (mm)</th>
<th>Pin1 Quadrant</th>
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<td>DPY</td>
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<td>DQA</td>
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*All dimensions are nominal.*
### TAPE AND REEL BOX DIMENSIONS

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<th>SPQ</th>
<th>Length (mm)</th>
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*All dimensions are nominal*
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
NOTES: (continued)

3. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5–1994.
B. This drawing is subject to change without notice.
C. SON (Small Outline No-Lead) package configuration.
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