1 Features
- IEEE 1394 Live Insertion Detection
- ESD Protection Exceeds IEC61000-4-2 (Level 4)
  - ±15-kV Human-Body Model (HBM)
  - ±6-kV IEC 61000-4-2 Contact Discharge
- 4-Channel Matching ESD Clamps for High-Speed Differential Lines
- Available in an 8-Pin X2SON (DQL) package

2 Applications
Firewire Interface

3 Description
The TPD4S1394 provides robust system level ESD solution for the IEEE 1394 port, along with a live insertion detection mechanism for high-speed lines interfacing a low-voltage, ESD sensitive core chipset. This device protects and monitors up to two differential input pairs. The optimized line capacitance protects the data lines with data rates in excess of 1.6 GHz without degrading signal integrity.

The TPD4S1394 incorporates a live insertion detection circuit whose output state changes when improper voltage levels are present on the input data lines. The FWPWR_EN signal controls an external FireWire port power switch. During the live insertion event if there is a floating GND or a high level signal at the D+ or D– pins, the internal comparator detects the changes and pull the FWPWR_EN signal to a low state. When FWPWR_EN is driven low, there is an internal delay mechanism preventing it from being driven to the high state regardless of the inputs to the comparator.

Additionally, the TPD4S1394 performs ESD protection on the four inputs pins: D1+, D1–, D2+, and D2–. The TPD4S1394 conforms to the IEC61000-4-2 (Level 4) ESD protection and ±15-kV HBM ESD protection. The TPD4S1394 is characterized for operation over ambient air temperature of −40°C to 85°C.

A 0.1-µF decoupling capacitor is required at VCC.

Device Information (1)

<table>
<thead>
<tr>
<th>PART NUMBER</th>
<th>PACKAGE</th>
<th>BODY SIZE (NOM)</th>
</tr>
</thead>
<tbody>
<tr>
<td>TPD4S1394</td>
<td>X2SON (8)</td>
<td>2.00 mm × 1.40 mm</td>
</tr>
</tbody>
</table>

(1) For all available packages, see the orderable addendum at the end of the data sheet.
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4 Revision History
NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (March 2013) to Revision B Page

- Added Device Information table, Pin Configuration and Functions section, Specifications section, ESD Ratings table, Switching Characteristics table, Detailed Description section, Application and Implementation section, Power Supply Recommendations section, Layout section, Device and Documentation Support section, and Mechanical, Packaging, and Orderable Information section ......................................................... 1
- Added Thermal Information table ................................................................. 4

Changes from Original (November 2009) to Revision A Page

- Removed hard coded ordering information table. Information contained in Package Orderable Addendum .................. 1
5 Pin Configuration and Functions

DQL Package
6-Pin X2SON
(Top View)

VCC  1  8  D1+
GND  2  7  D1–
VCMLP  3  6  D2+
FWPWR_EN  4  5  D2–

Pin Functions

<table>
<thead>
<tr>
<th>PIN</th>
<th>TYPE</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>NAME</td>
<td>NO.</td>
<td>D1+</td>
</tr>
<tr>
<td></td>
<td></td>
<td>8  Input</td>
</tr>
<tr>
<td></td>
<td></td>
<td>High-speed ESD clamp input</td>
</tr>
<tr>
<td>D1–</td>
<td>7</td>
<td>Input</td>
</tr>
<tr>
<td></td>
<td></td>
<td>High-speed ESD clamp input</td>
</tr>
<tr>
<td>D2+</td>
<td>6</td>
<td>Input</td>
</tr>
<tr>
<td></td>
<td></td>
<td>High-speed ESD clamp input</td>
</tr>
<tr>
<td>D2–</td>
<td>5</td>
<td>Input</td>
</tr>
<tr>
<td></td>
<td></td>
<td>High-speed ESD clamp input</td>
</tr>
<tr>
<td>FWPWR_EN</td>
<td>4</td>
<td>Output</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Control output</td>
</tr>
<tr>
<td>GND</td>
<td>2</td>
<td>Ground</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Ground</td>
</tr>
<tr>
<td>VCC</td>
<td>1</td>
<td>Power</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Power supply</td>
</tr>
<tr>
<td>VCMLP</td>
<td>3</td>
<td>Output</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Comparator trip reference</td>
</tr>
</tbody>
</table>

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)\(^{(1)}\)

<table>
<thead>
<tr>
<th>NAME</th>
<th>Type</th>
<th>MIN</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>VCC</td>
<td>Supply voltage</td>
<td>−0.5</td>
<td>4.6</td>
<td>V</td>
</tr>
<tr>
<td>VIO</td>
<td>IO voltage at D+, D–, VCLMP</td>
<td>0</td>
<td>4</td>
<td>V</td>
</tr>
<tr>
<td>FWPWR_EN</td>
<td>Switch output</td>
<td>−0.5</td>
<td>4.6</td>
<td>V</td>
</tr>
<tr>
<td>TA</td>
<td>Operating free-air temperature</td>
<td>−40</td>
<td>85</td>
<td>ºC</td>
</tr>
<tr>
<td>T_stg</td>
<td>Storage temperature</td>
<td>−65</td>
<td>150</td>
<td>ºC</td>
</tr>
</tbody>
</table>

\(^{(1)}\) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

<table>
<thead>
<tr>
<th>NAME</th>
<th>Type</th>
<th>MIN</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>(V_{(ESD)})</td>
<td>Electrostatic discharge</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(^{(1)})</td>
<td>All pins except 5, 6, 7, and 8</td>
<td>±2500</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>Charged-device model (CDM), per JEDEC specification JESD22-C101(^{(2)})</td>
<td>Pins 5, 6, 7, and 8</td>
<td>±15000</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>IEC 61000-4-2 contact discharge</td>
<td>All pins except 5, 6, 7, and 8</td>
<td>±1000</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>IEC 61000-4-2 air-gap discharge</td>
<td>Pins 5, 6, 7, and 8 (interface side)</td>
<td>±6000</td>
<td></td>
<td>V</td>
</tr>
</tbody>
</table>

\(^{(1)}\) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

\(^{(2)}\) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.
6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>MIN</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>V(_{DC})</td>
<td>3</td>
<td>3.6</td>
<td>V</td>
</tr>
</tbody>
</table>

6.4 Thermal Information

<table>
<thead>
<tr>
<th>THERMAL METRIC(^{(1)})</th>
<th>TPD4S1394 DQL (X2SON)</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>(R_{JUA}) Junction-to-ambient thermal resistance</td>
<td>167.5</td>
<td>°C/W</td>
</tr>
<tr>
<td>(R_{JUC(top)}) Junction-to-case (top) thermal resistance</td>
<td>56.8</td>
<td>°C/W</td>
</tr>
<tr>
<td>(R_{JUB}) Junction-to-board thermal resistance</td>
<td>82.3</td>
<td>°C/W</td>
</tr>
<tr>
<td>(\psi_{JT}) Junction-to-top characterization parameter</td>
<td>1.5</td>
<td>°C/W</td>
</tr>
<tr>
<td>(\psi_{JB}) Junction-to-board characterization parameter</td>
<td>82</td>
<td>°C/W</td>
</tr>
</tbody>
</table>

\(^{(1)}\) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

6.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)\(^{(1)}\)

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>(V_{DX}) FWPWR_EN trip voltage</td>
<td>High-to-low</td>
<td>2.9</td>
<td>3.4</td>
<td>4</td>
<td>V</td>
</tr>
<tr>
<td>() (D+ and D– pins)</td>
<td>Low-to-high</td>
<td>2.7</td>
<td>3.2</td>
<td>3.8</td>
<td>V</td>
</tr>
<tr>
<td>(V_{CLMP}) Value on pin</td>
<td>No connection</td>
<td>2.45</td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>(V_{BR}) Breakdown voltage at (V_{CLAMP})</td>
<td>(I = 1) mA</td>
<td>4.2</td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>(V_{D}) Diode forward voltage for lower clamp</td>
<td>(I_{D} = 8) mA lower clamp diode</td>
<td>–0.6</td>
<td>–0.8</td>
<td>–0.95</td>
<td>V</td>
</tr>
<tr>
<td>FWPWR_EN Switch output</td>
<td>(V_{CC})</td>
<td></td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>(R_{DYN}) Dynamic resistance (in and out clamp) of D+, D–</td>
<td>(I = 1) A</td>
<td>1</td>
<td></td>
<td></td>
<td>Ω</td>
</tr>
<tr>
<td>(C_{IO}) I/O capacitance of D+, D–</td>
<td>(V_{IO} = 2.5) V</td>
<td>1.5</td>
<td>2</td>
<td></td>
<td>pF</td>
</tr>
<tr>
<td>(I_{CC}) Current consumption</td>
<td>(V_{CC} = 3.3) V, FWPWR_EN = high</td>
<td>130</td>
<td>200</td>
<td></td>
<td>µA</td>
</tr>
</tbody>
</table>

\(^{(1)}\) A 0.1-µF decoupling capacitor is required at VCC.

6.6 Switching Characteristics

over operating free-air temperature range (unless otherwise noted)

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>(t_{TRIP})</td>
<td>Delay time for FWPWR_EN to go low</td>
<td>0.5</td>
<td>2</td>
<td>5</td>
<td>µs</td>
</tr>
<tr>
<td>(t_{RESET})</td>
<td>Delay time for FWPWR_EN to go high after trip</td>
<td>300</td>
<td>450</td>
<td>600</td>
<td>ms</td>
</tr>
</tbody>
</table>
6.7 Typical Characteristics

![Figure 1. I/O Capacitance vs I/O Voltage](image)

![Figure 2. Insertion Loss (S21)](image)

-3.0 dB Frequency = 2.4 GHz
7 Detailed Description

7.1 Overview
TPD4S1394 is a FireWire interface part that complies to the IEEE 1394 standard. The device has ESD protection for four high-speed data lines that pass 6-kV IEC61000-4-2 standard. Each dataline's I/O capacitance associated with the ESD cell is minimal and supports high data rate. There is a live insertion detection circuit integrated in TPD4S1394. During the live insertion event if there is a floating GND or a high-level signal at D+ or D–, the FWPWR_EN is driven low, disabling the external FireWire power switch.

7.2 Functional Block Diagram

7.3 Feature Description
TPD4S1394’s high-speed ESD cells on the data lines protect the pins from up to ±6-kV IEC 61000-4-2 contact discharge. The live insertion protection circuit detects improper voltages on the data lines and turn off the FireWire port power switch during an abnormal condition.

7.4 Device Functional Modes
The TPD4S1394’s D1+, D1–, D2+, and D2– pins are a passive-integrated circuit that activates when voltages exceed the forward voltage plus $V_{CMLP}$ or fall below the lower diodes forward voltage (~0.6 V). $V_{CC}$ must be within recommended voltage range for live insertion detection circuit to work correctly.
8 Application and Implementation

NOTE
Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information
TPD4S1394 has both high-speed ESD cells to protect the D1+, D1–, D2+, and D2– lines and live insertion detection circuit to identify improper status during insertion and to control the external power switch.

8.2 Typical Application

![Typical Application Schematic](image)

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**Figure 3. Typical Application Schematic**

8.2.1 Design Requirements
For this design example, a TPD4S1394 is used to protect the FireWire connector and detect live insertion. 

Table 1 shows the design parameters:

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>EXAMPLE VALUE</th>
</tr>
</thead>
<tbody>
<tr>
<td>Power supply, V&lt;sub&gt;CC&lt;/sub&gt;</td>
<td>3.3 V</td>
</tr>
<tr>
<td>Data line operating frequency</td>
<td>400 MHz (800 Mbps)</td>
</tr>
</tbody>
</table>
8.2.2 Detailed Design Procedure
The data transfer rate of 800 Mbps is well below the bandwidth of the data pins of TPD4S1394. So the parasitics associated with the ESD cells on these lines do not degrade the signal integrity. 3.3-V power supplies are commonly available from the board and can be used to power the live insertion detection circuit.

8.2.3 Application Curves

![Graphs showing I/O Capacitance vs I/O Voltage and Insertion Loss (S21)](image)

9 Power Supply Recommendations
TI recommends a power supply for $V_{CC}$ is from 3 V to 3.6 V.

10 Layout

10.1 Layout Guidelines
- The optimum placement is as close to the connector as possible.
  - EMI during an ESD event can couple from the trace being struck to other nearby unprotected traces, resulting in early system failures.
  - The PCB designer must minimize the possibility of EMI coupling by keeping any unprotected traces away from the protected traces which are between the TVS and the connector.
- Route the protected traces as straight as possible.
- Eliminate any sharp corners on the protected traces between the TVS and the connector by using rounded corners with the largest radii possible.
  - Electric fields tend to build up on corners, increasing EMI coupling.
10.2 Layout Example

![Diagram of TPD4S1394 layout example]

Figure 6. TPD4S1394 Layout Example
11 Device and Documentation Support

11.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on Alert me to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

**TI E2E™ Online Community** *TI's Engineer-to-Engineer (E2E) Community*. Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

**Design Support** *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.3 Trademarks

E2E is a trademark of Texas Instruments. All other trademarks are the property of their respective owners.

11.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.5 Glossary

**SLYZ022 — TI Glossary.**

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.
## PACKAGING INFORMATION

<table>
<thead>
<tr>
<th>Orderable Device</th>
<th>Status (1)</th>
<th>Package Type</th>
<th>Package Drawing</th>
<th>PIns</th>
<th>Package Qty</th>
<th>Eco Plan (2)</th>
<th>Lead/Ball Finish (6)</th>
<th>MSL Peak Temp</th>
<th>Op Temp (°C)</th>
<th>Device Marking (4/5)</th>
<th>Samples</th>
</tr>
</thead>
<tbody>
<tr>
<td>TPD4S1394DQLR</td>
<td>ACTIVE</td>
<td>X2SON</td>
<td>DQL</td>
<td>8</td>
<td>3000</td>
<td>Green (RoHS &amp; no Sb/Br)</td>
<td>CU NIPDAU</td>
<td>Level-1-260C-UNLIM</td>
<td>-40 to 85</td>
<td>(5J7 ~ 5JR)</td>
<td></td>
</tr>
</tbody>
</table>

(1) The marketing status values are defined as follows:
- **ACTIVE**: Product device recommended for new designs.
- **LIFEBUY**: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
- **NRND**: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
- **PREVIEW**: Device has been announced but is not in production. Samples may or may not be available.
- **OBSOLETE**: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check [http://www.ti.com/productcontent](http://www.ti.com/productcontent) for the latest availability information and additional product content details.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

**Important Information and Disclaimer:** The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.
## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

**TAPE DIMENSIONS**

<table>
<thead>
<tr>
<th>Dimension</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>A0</td>
<td>Dimension designed to accommodate the component width</td>
</tr>
<tr>
<td>B0</td>
<td>Dimension designed to accommodate the component length</td>
</tr>
<tr>
<td>K0</td>
<td>Dimension designed to accommodate the component thickness</td>
</tr>
<tr>
<td>W</td>
<td>Overall width of the carrier tape</td>
</tr>
<tr>
<td>P1</td>
<td>Pitch between successive cavity centers</td>
</tr>
</tbody>
</table>

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**

*All dimensions are nominal.

<table>
<thead>
<tr>
<th>Device</th>
<th>Package Type</th>
<th>Package Drawing</th>
<th>Pins</th>
<th>SPQ</th>
<th>Reel Diameter (mm)</th>
<th>Reel Width W1 (mm)</th>
<th>A0 (mm)</th>
<th>B0 (mm)</th>
<th>K0 (mm)</th>
<th>P1 (mm)</th>
<th>W (mm)</th>
<th>Pin1 Quadrant</th>
</tr>
</thead>
<tbody>
<tr>
<td>TPD4S1394DQLR</td>
<td>X2SON</td>
<td>DQL</td>
<td>8</td>
<td>3000</td>
<td>3000</td>
<td>180.0</td>
<td>9.5</td>
<td>1.6</td>
<td>2.3</td>
<td>0.5</td>
<td>4.0</td>
<td>8.0</td>
</tr>
</tbody>
</table>

Pack Materials-Page 1
## TAPE AND REEL BOX DIMENSIONS

<table>
<thead>
<tr>
<th>Device</th>
<th>Package Type</th>
<th>Package Drawing</th>
<th>Pins</th>
<th>SPQ</th>
<th>Length (mm)</th>
<th>Width (mm)</th>
<th>Height (mm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>TPD4S1394DQLR</td>
<td>X2SON</td>
<td>DQL</td>
<td>8</td>
<td>3000</td>
<td>184.0</td>
<td>184.0</td>
<td>19.0</td>
</tr>
</tbody>
</table>

*All dimensions are nominal*
DQL (R-PX2SON-N8)  PLASTIC SMALL OUTLINE NO-LEAD

Pin 1 Index Area

0.40
0.34

0.05 C

0.05 C

0.05
0.00
Seating Height

0.10 Nominal Lead Frame

Seating Plane

1.80

1.50

0.50

8X 0.40
0.30

8X 0.25
0.15

0.10 C A B
0.05 C

Pin 1 Identifier
0.10 X 45°

8
7
6
5
1 2 3 4

2.05
1.95

1.45
1.35

Bottom View

NOTES:  A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. SON (Small Outline No-Lead) package configuration.

4210271/A  06/09
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC-7351 is recommended for alternate designs.
D. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.
E. Maximum stencil thickness 0.127 mm (5 mils). All linear dimensions are in millimeters.
F. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
G. Side aperture dimensions over-print land for acceptable area ratio > 0.66. Customer may reduce side aperture dimensions if stencil manufacturing process allows for sufficient release at smaller opening.
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