TPIC6595
POWER LOGIC 8-BIT SHIFT REGISTER

- Low rDS(on) . . . 1.3 Ω Typical
- Avalanche Energy . . . 75 mJ
- Eight Power DMOS Transistor Outputs of 250-mA Continuous Current
- 1.5-A Pulsed Current Per Output
- Output Clamp Voltage at 45 V
- Devices Are Cascadeable
- Low Power Consumption

description

The TPIC6595 is a monolithic, high-voltage, high-current power 8-bit shift register designed for use in systems that require relatively high load power. The device contains a built-in voltage clamp on the outputs for inductive transient protection. Power driver applications include relays, solenoids, and other medium-current or high-voltage loads.

This device contains an 8-bit serial-in, parallel-out shift register that feeds an 8-bit D-type storage register. Data transfers through both the shift and storage registers on the rising edge of the shift-register clock (SRCK) and the register clock (RCK) respectively. The storage register transfers data to the output buffer when shift-register clear (SRCLR) is high. When SRCLR is low, the input shift register is cleared. When output enable (G) is held high, all data in the output buffers is held low and all drain outputs are off. When G is held low, data from the storage register is transparent to the output buffers. The serial output (SER OUT) allows for cascading of the data from the shift register to additional devices.

Outputs are low-side, open-drain DMOS transistors with output ratings of 45 V and 250-mA continuous sink current capability. When data in the output buffers is low, the DMOS-transistor outputs are off. When data is high, the DMOS-transistor outputs have sink current capability.

Separate power and logic level ground pins are provided to facilitate maximum system flexibility. Pins 1, 10, 11, and 20 are internally connected, and each pin must be externally connected to the power system ground in order to minimize parasitic inductance. A single-point connection between pin 19, logic ground (LGND), and pins 1, 10, 11, and 20, power grounds (PGND), must be externally made in a manner that reduces crosstalk between the logic and load circuits.

The TPIC6595 is characterized for operation over the operating case temperature range of −40°C to 125°C.
logic diagram (positive logic)

G

RCK

SRCLR

SRCK

SER IN

DRAIN0

DRAIN1

DRAIN2

DRAIN3

DRAIN4

DRAIN5

DRAIN6

DRAIN7

PGND

1, 10, 11, 20

18

SER OUT

Logic diagram of the TPIC6595 Power Logic 8-Bit Shift Register.
absolute maximum ratings over recommended operating case temperature range (unless otherwise noted)†

Logic supply voltage, \( V_{CC} \) (see Note 1) ............................ 7 V  
Logic input voltage range, \( V_I \) ........................................... −0.3 V to 7 V  
Power DMOS drain-to-source voltage, \( V_{DS} \) (see Note 2) ......................... 45 V  
Continuous source-drain diode anode current ........................................... 1 A  
Pulsed source-drain diode anode current ........................................... 2 A  
Pulsed drain current, each output, all outputs on, \( I_{Dn}, T_A = 25^\circ C \) (see Note 3) ......................... 750 mA  
Continuous drain current, each output, all outputs on, \( I_{Dn}, T_A = 25^\circ C \) ......................... 250 mA  
Peak drain current single output, \( I_{DM}, T_A = 25^\circ C \) (see Note 3) ......................... 2 A  
Single-pulse avalanche energy, \( E_{AS} \) (see Note 4) ................................. 75 mJ  
Avalanche current, \( I_{AS} \) (see Note 4) ........................................... 1 A  
Continuous total power dissipation ................................. See Dissipation Rating Table  
Operating virtual junction temperature range, \( T_J \) ........................................... −40°C to 150°C  
Storage temperature range, \( T_{stg} \) ........................................... −65°C to 150°C  
Lead temperature 1.6 mm (1/16 inch) from case for 10 seconds ......................... 260°C  

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values are with respect to LGND and PGND.  
2. Each power DMOS source is internally connected to PGND.  
3. Pulse duration ≤ 100 µs, duty cycle ≤ 2 %  
4. DRAIN supply voltage = 15 V, starting junction temperature (\( T_{JS} \)) = 25°C, \( L = 100 \, \text{mH}, I_{AS} = 1 \, \text{A} \) (see Figure 4).
## recommended operating conditions over recommended operating temperature range (unless otherwise noted)

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<th>PARAMETER</th>
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<td>Logic supply voltage, V_{CC}</td>
<td>4.5</td>
<td>5.5</td>
<td>V</td>
</tr>
<tr>
<td>High-level input voltage, V_{IH}</td>
<td>0.85 V_{CC}</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>Low-level input voltage, V_{IL}</td>
<td>0.15 V_{CC}</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>Pulsed drain output current, T_C = 25°C, V_{CC} = 5 V (see Notes 3 and 5)</td>
<td>−1.8</td>
<td>1.5</td>
<td>A</td>
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<tr>
<td>Setup time, SER IN high before SRCK^, t_{SU} (see Figure 2)</td>
<td>10</td>
<td></td>
<td>ns</td>
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<tr>
<td>Hold time, SER IN high after SRCK^, t_{H} (see Figure 2)</td>
<td>10</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>Pulse duration, t_w (see Figure 2)</td>
<td>20</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>Operating case temperature, T_C</td>
<td>−40</td>
<td>125°C</td>
<td>°C</td>
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## electrical characteristics, V_{CC} = 5 V, T_C = 25°C (unless otherwise noted)

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<th>PARAMETER</th>
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<th>MAX</th>
<th>UNIT</th>
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<tbody>
<tr>
<td>V_{(BR)DSX} Drain-source breakdown voltage</td>
<td>I_D = 1 mA, V_{DS(on)} = 0.5 V</td>
<td>45</td>
<td></td>
<td></td>
<td>V</td>
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<tr>
<td>V_{SD} Source-drain diode forward voltage</td>
<td>I_F = 250 mA, V_{CC} = 4.5 V</td>
<td>0.85</td>
<td>1</td>
<td>V</td>
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<td>V_{OH} High-level output voltage, SER OUT</td>
<td>I_{OH} = −20 mA, V_{CC} = 4.5 V</td>
<td>4.4</td>
<td>4.49</td>
<td>V</td>
<td></td>
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<tr>
<td></td>
<td>I_{OH} = −4 mA, V_{CC} = 4.5 V</td>
<td>4.1</td>
<td>4.3</td>
<td>V</td>
<td></td>
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<td>V_{OL} Low-level output voltage, SER OUT</td>
<td>I_{OH} = 20 mA, V_{CC} = 4.5 V</td>
<td>0.002</td>
<td>0.1</td>
<td>V</td>
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</tr>
<tr>
<td></td>
<td>I_{OH} = 4 mA, V_{CC} = 4.5 V</td>
<td>0.2</td>
<td>0.4</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>V_{(hys)} Input hysteresis</td>
<td>V_{DS} = 15 V</td>
<td>1.3</td>
<td></td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>I_{IH} High-level input current</td>
<td>V_{CC} = 5.5 V, V_{I} = V_{CC}</td>
<td>1</td>
<td>µA</td>
<td></td>
<td></td>
</tr>
<tr>
<td>I_{IL} Low-level input current</td>
<td>V_{CC} = 5.5 V, V_{I} = 0</td>
<td>−1</td>
<td>µA</td>
<td></td>
<td></td>
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<tr>
<td>I_{CCL} Logic supply current</td>
<td>I_O = 0, I_O = 0, V_{DS(on)} = 0.5 V, C_L = 30 pF, C_L = 30 pF, f_{SRCK} = 5 MHz, I_O = 0, f_{SRCK} = 5 MHz, I_O = 0</td>
<td>15</td>
<td>100</td>
<td>µA</td>
<td></td>
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<tr>
<td>I_{CC(FRQ)} Logic supply current frequency</td>
<td>I_{SRCK} = 5 MHz, I_O = 0, I_O = 0</td>
<td>0.6</td>
<td>5</td>
<td>mA</td>
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<tr>
<td>I_{N} Nominal current</td>
<td>V_{DS(on)} = 0.5 V, I_N = I_D, V_{DS(on)} = 0.5 V, I_N = I_D, T_C = 85°C</td>
<td>250</td>
<td></td>
<td>mA</td>
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<tr>
<td>I_{DSX} Off-state drain current</td>
<td>V_{DS} = 40 V</td>
<td>0.05</td>
<td>1</td>
<td>µA</td>
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<tr>
<td></td>
<td>V_{DS} = 40 V, T_C = 125°C</td>
<td>0.15</td>
<td>5</td>
<td>µA</td>
<td></td>
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<tr>
<td>f_{DS(on)} Static drain-source on-state resistance</td>
<td>I_D = 250 mA, V_{CC} = 4.5 V</td>
<td>1.3</td>
<td>2</td>
<td>Ω</td>
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<tr>
<td></td>
<td>I_D = 250 mA, V_{CC} = 4.5 V</td>
<td>2</td>
<td>3.2</td>
<td>Ω</td>
<td></td>
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<tr>
<td></td>
<td>I_D = 500 mA, V_{CC} = 4.5 V</td>
<td>1.3</td>
<td>2</td>
<td>Ω</td>
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</table>

## switching characteristics, V_{CC} = 5 V, T_C = 25°C

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<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
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</thead>
<tbody>
<tr>
<td>t_{PLH} Propagation delay time, low-to-high-level output from G</td>
<td>C_L = 30 pF, I_D = 250 mA, V_{DS(on)} = 0.5 V, I_N = I_D, T_C = 85°C</td>
<td>650</td>
<td>ns</td>
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<tr>
<td>t_{PHL} Propagation delay time, high-to-low-level output from G</td>
<td>I_{SRCK} = 5 MHz, I_O = 0, C_L = 30 pF, f_{SRCK} = 5 MHz, I_O = 0</td>
<td>150</td>
<td>ns</td>
<td>ns</td>
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<td>t_r Rise time, drain output</td>
<td></td>
<td>750</td>
<td>ns</td>
<td>ns</td>
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<td>t_{f} Fall time, drain output</td>
<td></td>
<td>425</td>
<td>ns</td>
<td>ns</td>
<td></td>
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<tr>
<td>t_{a} Reverse-recovery-current rise time</td>
<td></td>
<td>100</td>
<td>ns</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>t_{r} Reverse-recovery-time</td>
<td></td>
<td>300</td>
<td>ns</td>
<td>ns</td>
<td></td>
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</table>

NOTES:  
1. Pulse duration ≤ 100 µs, duty cycle ≤ 2%
5. Technique should limit T_J − T_C to 10°C maximum.
2. These parameters are measured with voltage-sensing contacts separate from the current-carrying contacts.
3. Nominal current is defined for a consistent comparison between devices from different sources. It is the current that produces a voltage drop of 0.5 V at T_C = 85°C.

Texas Instruments
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265
thermal resistance

<table>
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<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>MIN</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>$R_{JA}$ Thermal resistance, junction-to-ambient</td>
<td>DW package All 8 outputs with equal power</td>
<td>111</td>
<td>108</td>
<td>°C/W</td>
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PARAMETER MEASUREMENT INFORMATION

![Test Circuit Diagram]

**Figure 1. Resistive Load Operation**

![Voltage Waveforms Diagram]

**Figure 2. Test Circuit, Switching Times, and Voltage Waveforms**

**NOTES:**
A. Outputs DRAIN 1, 2, 5, and 6 low (PGND), all other DRAIN outputs are at 24 V. The word generator has the following characteristics:
- $t_r \leq 10$ ns, $t_f \leq 10$ ns, $t_w = 300$ ns,
- pulsed repetition rate (PRR) = 5 kHz, $Z_O = 50$ Ω.
B. $C_L$ includes probe and jig capacitance.
PARAMETER MEASUREMENT INFORMATION

NOTES:  
A. The $V_{GG}$ amplitude and $R_G$ are adjusted for $di/dt = 20 \text{ A/µs}$. A $V_{GG}$ double-pulse train is used to set $I_F = 0.25 \text{ A}$, where $t_1 = 10 \mu s$, $t_2 = 7 \mu s$, and $t_3 = 3 \mu s$.

B. The DRAIN terminal under test is connected to the TP K test point. All other terminals are connected together and connected to the TP A test point.

Figure 3. Reverse-Recovery-Current Test Circuit and Waveforms of Source-Drain Diode

NOTES:  
A. The word generator has the following characteristics: $t_r \leq 10 \text{ ns}$, $t_f \leq 10 \text{ ns}$, $Z_O = 50 \Omega$.

B. Input pulse duration, $t_w$, is increased until peak current $I_{AS} = 1 \text{ A}$.

Energy test level is defined as $E_{AS} = I_{AS} \times V(\text{BR})_{DSX} \times t_{av}/2 = 75 \text{ mJ}$, where $t_{av}$ = avalanche time.

Figure 4. Single-Pulse Avalanche Energy Test Circuit and Waveforms
TYPICAL CHARACTERISTICS

PEAK AVALANCHE CURRENT

\[ I_{\text{AS}} \text{ vs } t_{\text{av}} \]

\[ T_{JS} = 25^\circ \text{C} \]

\[ V_{CC} = 5 \text{ V} \]

\[ T_{JS} = -40^\circ \text{C} \text{ to } 125^\circ \text{C} \]

**Figure 5**

SUPPLY CURRENT

\[ I_{\text{CC}} \text{ vs } f \]

\[ V_{CC} = 5 \text{ V} \]

\[ T_{JS} = -40^\circ \text{C} \text{ to } 125^\circ \text{C} \]

**Figure 6**

MAXIMUM CONTINUOUS DRAIN CURRENT OF EACH OUTPUT

\[ I_{\text{D}} \text{ vs } N \]

\[ V_{CC} = 5 \text{ V} \]

\[ T_{A} = 25^\circ \text{C} \]

\[ T_{A} = 100^\circ \text{C} \]

\[ T_{A} = 125^\circ \text{C} \]

**Figure 7**

MAXIMUM PEAK DRAIN CURRENT OF EACH OUTPUT

\[ I_{\text{D}} \text{ vs } N \]

\[ V_{CC} = 5 \text{ V} \]

\[ T_{A} = 25^\circ \text{C} \]

\[ d = \frac{t_{W}}{t_{\text{period}}} = 1 \text{ ms/t_{period}} \]

\[ d = 5\% \]

\[ d = 10\% \]

\[ d = 50\% \]

\[ d = 80\% \]

**Figure 8**
TYPICAL CHARACTERISTICS

**STATIC DRAIN-SOURCE ON-STATE RESISTANCE vs DRAIN CURRENT**

![Graph showing static drain-source on-state resistance vs drain current for different temperatures.](image)

**VCC = 5 V**

See Note A

- $T_C = 125°C$
- $T_C = 25°C$
- $T_C = -40°C$

**ID** - Drain Current - A

<table>
<thead>
<tr>
<th>$V_{CC}$ - Logic Supply Voltage - V</th>
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<td>3</td>
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$T_C = 125°C$

$T_C = 25°C$

$T_C = -40°C$

**SWITCHING TIME vs FREE-AIR TEMPERATURE**

![Graph showing switching time vs free-air temperature.](image)

$t_{PHL}$

$t_{PLH}$

- $I_D = 250 mA$
- $T_C = 25°C$
- $T_C = -40°C$

**NOTE A:** Technique should limit $T_J - T_C$ to 10°C maximum.
# Revision History

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<td>5/18/05</td>
<td>B</td>
<td>5</td>
<td>Figure 1</td>
<td>Changed SRCLR timing diagram</td>
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<tr>
<td>4/1992</td>
<td></td>
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## PACKAGING INFORMATION

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<td>Green (RoHS &amp; no Sb/Br)</td>
<td>CU NIPDAU</td>
<td>Level-1-260C-UNLIM</td>
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<td>Pb-Free (RoHS)</td>
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(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check [http://www.ti.com/productcontent](http://www.ti.com/productcontent) for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. – The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

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### TAPE AND REEL INFORMATION

*All dimensions are nominal*

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<th>Package Drawing</th>
<th>Pins</th>
<th>SPQ</th>
<th>Reel Diameter (mm)</th>
<th>Reel Width W1 (mm)</th>
<th>A0 (mm)</th>
<th>B0 (mm)</th>
<th>K0 (mm)</th>
<th>P1 (mm)</th>
<th>W (mm)</th>
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</table>

**Notes:**

- **A0**: Dimension designed to accommodate the component width
- **B0**: Dimension designed to accommodate the component length
- **K0**: Dimension designed to accommodate the component thickness
- **W**: Overall width of the carrier tape
- **P1**: Pitch between successive cavity centers
# TAPE AND REEL BOX DIMENSIONS

<table>
<thead>
<tr>
<th>Device</th>
<th>Package Type</th>
<th>Package Drawing</th>
<th>Pins</th>
<th>SPQ</th>
<th>Length (mm)</th>
<th>Width (mm)</th>
<th>Height (mm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>TPIC6595DWR</td>
<td>SOIC</td>
<td>DW</td>
<td>20</td>
<td>2000</td>
<td>350.0</td>
<td>350.0</td>
<td>43.0</td>
</tr>
<tr>
<td>TPIC6595DWRG4</td>
<td>SOIC</td>
<td>DW</td>
<td>20</td>
<td>2000</td>
<td>350.0</td>
<td>350.0</td>
<td>43.0</td>
</tr>
</tbody>
</table>

*All dimensions are nominal*
### N (R–PDIP–T**) PLASTIC DUAL–IN–LINE PACKAGE

#### MECHANICAL DATA

**16 PINS SHOWN**

**DIMENSIONS:**

<table>
<thead>
<tr>
<th>PINS **</th>
<th>14</th>
<th>16</th>
<th>18</th>
<th>20</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>A MAX</strong></td>
<td>0.775 (19.69)</td>
<td>0.775 (19.69)</td>
<td>0.920 (23.37)</td>
<td>1.060 (26.92)</td>
</tr>
<tr>
<td><strong>A MIN</strong></td>
<td>0.745 (18.92)</td>
<td>0.745 (18.92)</td>
<td>0.850 (21.59)</td>
<td>0.940 (23.88)</td>
</tr>
</tbody>
</table>

**VARIATION:**

| MS–001 | AA | BB | AC | AD |

**NOTES:**

A. All linear dimensions are in inches (millimeters).

B. This drawing is subject to change without notice.

⚠️ Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).

⚠️ The 20 pin end lead shoulder width is a vendor option, either half or full width.

**Dimensions (inches):**

- **A:** 0.045 (1.14) 0.030 (0.76) 0.020 (0.51) MIN
- **B:** 0.100 (2.54)
- **0.325 (8.26) MIN**
- **0.430 (10.92) MAX**
- **0.010 (0.25) NOM**

**Gauge Plane:**

- **0.015 (0.38)**

**Seating Plane:**

- **0.200 (5.08) MAX**

**14/18 Pin Only:**

- **0.010 (0.25) MAX**
NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
5. Reference JEDEC registration MS-013.
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

9. Board assembly site may have different recommendations for stencil design.
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