TPS22916xx 1-V – 5.5-V, 2-A, 60-mΩ Ultra-Low Leakage Load Switch

1 Features

- Input Operating Voltage Range (V_{IN}): 1 V–5.5 V
- Maximum Continuous Current (I_{MAX}): 2 A
- ON-Resistance (R_{ON}):
  - 5 V_{IN} = 60 mΩ (typ), 100 mΩ (85°C max)
  - 1.8 V_{IN} = 100 mΩ (typ), 150 mΩ (85°C max)
  - 1 V_{IN} = 200 mΩ (typ), 325 mΩ (85°C max)
- Ultra-Low Power Consumption:
  - ON State (I_Q): 0.5 µA (typ), 1 µA (max)
  - OFF State (I_{SD}): 10 nA (typ), 100 nA (max)
  - TPS22916CL (I_{SD}): 100 nA (typ), 300 nA (max)
- Smart ON Pin Pull Down (R_{PD}):
  - ON ≥ V_{IH} (I_{ON}): 10 nA (max)
  - ON ≤ V_{IL} (R_{PD}): 750 kΩ (typ)
- Slow Timing in C Version Limits Inrush Current:
  - 5-V Turnon time (t_{ON}): 1400 µs at 5 mV/µs
  - 1.8-V Turnon time (t_{ON}): 3000 µs at 1 mV/µs
  - 1-V Turnon time (t_{ON}): 6500 µs at 0.3 mV/µs
- Fast Timing in B Version Reduces Wait Time:
  - 5-V Turnon time (t_{ON}): 115 µs at 57 mV/µs
  - 1.8-V Turnon time (t_{ON}): 250 µs at 12 mV/µs
  - 1-V Turnon time (t_{ON}): 510 µs at 3.3 mV/µs
- Always-ON True Reverse Current Blocking (RCB):
  - Activation Current (I_{RCB}): –500 mA (typ)
  - Reverse Leakage ($I_{IN,RCB}$): –300 nA (max)
- Quick Output Discharge (QOD): 150 Ω (typ) (N version has no QOD)
- Active Low Enable Option (L Version)

2 Applications

- Wearables
- Smartphones
- Tablets
- Portable Speakers

3 Description

The TPS22916xx is a small, single channel load switch using a low leakage P-Channel MOSFET for minimum power loss. Advanced gate control design supports operating voltages as low as 1 V with minimal increase in ON-Resistance and power loss.

Multiple timing options are available to support various system loading conditions. For heavy capacitive loads, the slow turnon timing in the C version minimizes the inrush current. In cases with light capacitive loads, the fast timing in the B version reduces required wait time.

The switch ON state is controlled by a digital input that is capable of interfacing directly with low-voltage control signals. Both Active High and Active Low (L) versions are available. When power is first applied, a Smart Pull Down is used to keep the ON pin from floating until system sequencing is complete. Once the ON pin is deliberately driven high (≥V_{IH}), the Smart Pull Down is disconnected to prevent unnecessary power loss.

The TPS22916xx is available in a small, space saving 0.74-mm × 0.74-mm, 0.4-mm pitch, 0.5-mm height 4-pin Wafer-Chip-Scale (WCSP) package (YFP). The device is characterized for operation over a temperature range of –40°C to +85°C.

Device Information(1)

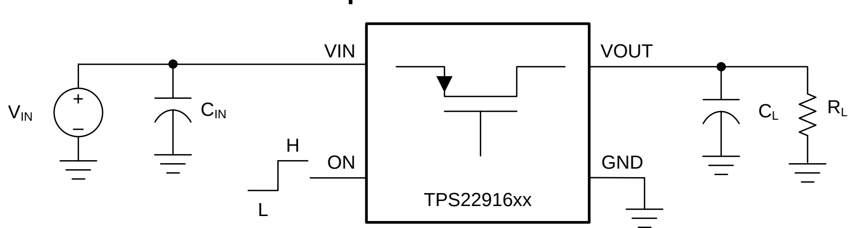
PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPS22916xx	WCSP (4)	0.74 mm × 0.74 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Device Comparison Table

VERSION	TIMING	QOD	ENABLE (ON)
TPS22916B	Fast	Yes	Active High
TPS22916C	Slow	Yes	Active High
TPS22916CN	Slow	No	Active High
TPS22916CL	Slow	Yes	Active Low

Simplified Schematic



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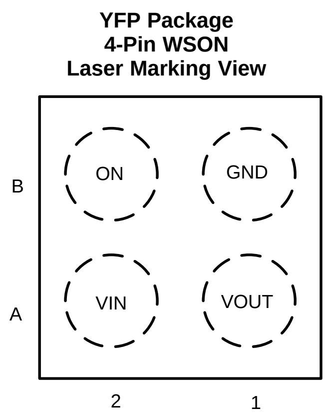
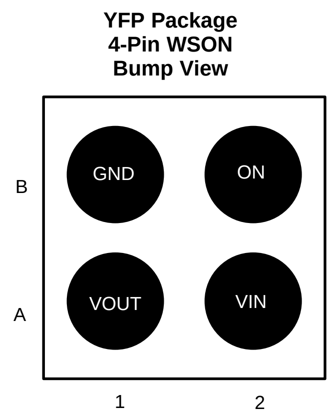
• Changed Package Drawing Dimensions	21

Changes from Revision A (September 2017) to Revision B	Page
• Changed Pinout drawing labeled Laser Marking	1

Changes from Original (July 2017) to Revision A	Page
• Changed device document from Advanced Info to Production Data	1

5 Pin Configuration and Functions





TPS22916xx Pin Functions

PIN		TYPE	DESCRIPTION
NO.	NAME		
A1	VOUT	Power	Switch output
A2	VIN	Power	Switch input
B1	GND	Ground	Device ground
B2	ON	Digital input	Device enable

6 Specifications

6.1 Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
V_{IN}	Input voltage	–0.3	6	V
V_{OUT}	Output voltage	–0.3	6	V
V_{ON}	Enable voltage	–0.3	6	V
I_{MAX}	Maximum continuous switch current		2	A
I_{PLS}	Maximum pulsed switch current, pulse < 300-µs, 2% duty cycle		2.5	A
$T_{J,MAX}$	Maximum junction temperature		125	°C
T_{STG}	Storage temperature	–65	150	°C
T_{LEAD}	Maximum Lead temperature (10-s soldering time)		300	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 500-V HBM is possible with the necessary precautions. Pins listed as ±2000 V may actually have higher performance.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 250-V CDM is possible with the necessary precautions. Pins listed as ±500 V may actually have higher performance.

6.3 Recommended Operating Conditions

Over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_{IN}	Input voltage	1	5.5	V
V_{OUT}	Output voltage	0	5.5	V
V_{IH}	High-level input voltage, ON	1	5.5	V
V_{IL}	Low-level input voltage, ON	0	0.35	V
T_A	Operating free-air temperature	–40	85	°C

6.4 Thermal Information

Thermal Parameters(1)		TPS22916xx YFP (WCSP) 4 PINS	UNIT
θ_{JA}	Junction-to-ambient thermal resistance	193	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance	2.3	°C/W
θ_{JB}	Junction-to-board thermal resistance	36	°C/W
ψ_{JT}	Junction-to-top characterization parameter	12	°C/W
ψ_{JB}	Junction-to-board characterization parameter	36	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Electrical Characteristics

Unless otherwise noted, the specification in the following table applies for all variants over the entire recommended power supply voltage range of 1 V to 5.5 V unless noted otherwise. Typical Values are at 25°C.

PARAMETER		TEST CONDITIONS		T_J	MIN	TYP	MAX	UNIT
INPUT SUPPLY (VIN)								
$I_{Q,VIN}$	V_{IN} Quiescent current	Enabled, V_{OUT} = Open		–40°C to +85°C		0.5	1.0	µA
$I_{SD,VIN}$	V_{IN} Shutdown current	Disabled, V_{OUT} = GND (TPS22916B/C/CN)		–40°C to +85°C		10	100	nA
		Disabled, V_{OUT} = GND (TPS22916CL)		–40°C to +85°C		100	300	nA
ON-RESISTANCE (R_{ON})								
R_{ON}	ON-Resistance	I_{OUT} = 200 mA	V_{IN} = 5 V	25°C		60	80	mΩ
				–40°C to +85°C			100	
				–40°C to +105°C			120	
			V_{IN} = 3.6 V	25°C		70	90	
				–40°C to +85°C			120	
				–40°C to +105°C			140	
			V_{IN} = 1.8 V	25°C		100	125	
				–40°C to +85°C			150	
				–40°C to +105°C			175	
			V_{IN} = 1.2 V	25°C		150	200	
				–40°C to +85°C			250	
				–40°C to +105°C			300	
			V_{IN} = 1 V	25°C		200	275	
				–40°C to +85°C			325	
				–40°C to +105°C			375	
ENABLE PIN (ON)								
I_{ON}	ON Pin leakage	Enabled		–40°C to +85°C	–10		10	nA
R_{PD}	Smart Pull Down Resistance	Disabled		–40°C to +85°C		750		kΩ
REVERSE CURRENT BLOCKING (RCB)								
I_{RCB}	RCB Activation Current	Enabled, V_{OUT} > V_{IN}		–40°C to +85°C		-500		mA
t_{RCB}	RCB Activation time	Enabled, V_{OUT} > V_{IN} + 200mV		–40°C to +85°C		10		µs
V_{RCB}	RCB Release Voltage	Enabled, V_{OUT} > V_{IN}		–40°C to +85°C		25		mV
$I_{IN,RCB}$	VIN Reverse Leakage Current	0 V ≤ V_{IN} + V_{RCB} ≤ V_{OUT} ≤ 5.5 V		–40°C to +85°C	–300			nA
QUICK OUTPUT DISCHARGE (QOD)								
QOD (1)	Output discharge resistance	Disabled (Not in TPS22916CN)		–40°C to +85°C		150		Ω

(1) For more information on which devices include quick output discharge, see the *Device Functional Modes* section.

6.6 Switching Characteristics

Unless otherwise noted, the typical characteristics in the following table applies over the entire recommended power supply voltage range of 1 V to 5.5 V at 25°C with a load of C_L = 0.1µF, R_L = 10Ω.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
TPS22916B						
t_{ON}	Turn On Time	V_{IN} = 5 V		115		µs
		V_{IN} = 3.6 V		140		
		V_{IN} = 1.8 V		250		
		V_{IN} = 1.2 V		350		
		V_{IN} = 1 V		510		
t_{RISE}	Rise Time	V_{IN} = 5 V		70		µs
		V_{IN} = 3.6 V		80		
		V_{IN} = 1.8 V		130		
		V_{IN} = 1.2 V		190		
		V_{IN} = 1 V		240		
SR_{ON}	Slew Rate	V_{IN} = 5 V		57		mV/µs
		V_{IN} = 3.6 V		36		
		V_{IN} = 1.8 V		12		
		V_{IN} = 1.2 V		5.1		
		V_{IN} = 1 V		3.3		
t_{OFF}	Turn Off Time	V_{IN} = 5 V		5		µs
		V_{IN} = 3.6 V		5		
		V_{IN} = 1.8 V		10		
		V_{IN} = 1.2 V		15		
		V_{IN} = 1 V		25		
t_{FALL}	Fall Time	C_L = 0.1 µF, R_L = 10 Ω (1)		2.3		µs
		C_L = 1µF, R_L = Open (1)		315		

(1) See the *Fall Time (t_{FALL}) and Quick Output Discharge (QOD)* section for information on how R_L and C_L affect Fall Time.

Switching Characteristics (continued)

Unless otherwise noted, the typical characteristics in the following table applies over the entire recommended power supply voltage range of 1 V to 5.5 V at 25°C with a load of C_L = 0.1µF, R_L = 10Ω.

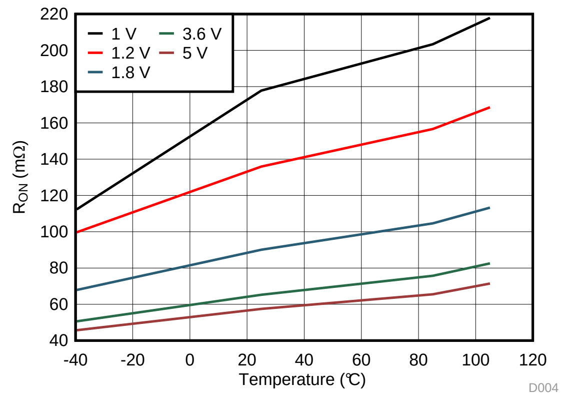
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
TPS22916C, TPS22916CN, TPS22916CL						
t_{ON}	Turn On Time	V_{IN} = 5 V		1400		µs
		V_{IN} = 3.6 V		1700		
		V_{IN} = 1.8 V		3000		
		V_{IN} = 1.2 V		5000		
		V_{IN} = 1 V		6500		
t_{RISE}	Rise Time	V_{IN} = 5 V		800		µs
		V_{IN} = 3.6 V		900		
		V_{IN} = 1.8 V		1400		
		V_{IN} = 1.2 V		2300		
		V_{IN} = 1 V		3000		
SR_{ON}	Slew Rate	V_{IN} = 5 V		5		mV/µs
		V_{IN} = 3.6 V		3.2		
		V_{IN} = 1.8 V		1		
		V_{IN} = 1.2 V		0.4		
		V_{IN} = 1 V		0.3		
t_{OFF}	Turn Off Time	V_{IN} = 5 V		5		µs
		V_{IN} = 3.6 V		5		
		V_{IN} = 1.8 V		10		
		V_{IN} = 1.2 V		15		
		V_{IN} = 1 V		25		
t_{FALL}	Fall Time (2)	C_L = 0.1 µF, R_L = 10 Ω (1)		2.3		µs
		CL = 10µF, RL = Open (1)		3150		

(2) Devices without Quick Output Discharge (QOD) may not discharge completely.

6.7 Typical Characteristics

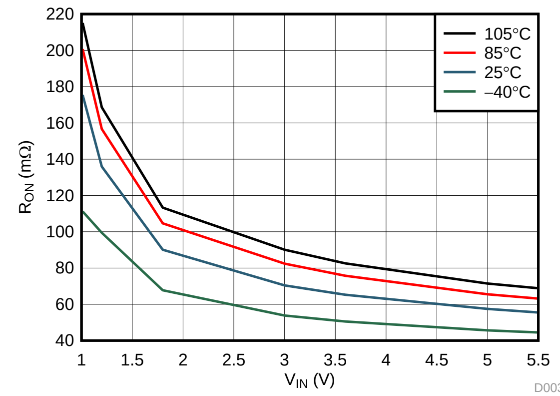
6.7.1 Typical Electrical Characteristics

The typical characteristics curves in this section apply to all devices unless otherwise noted.



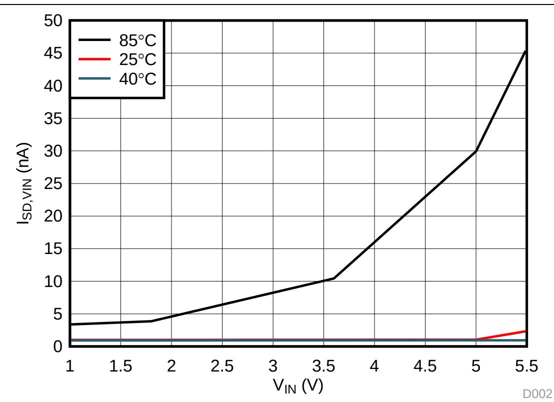
Enabled

Figure 1. ON-Resistance vs Temperature



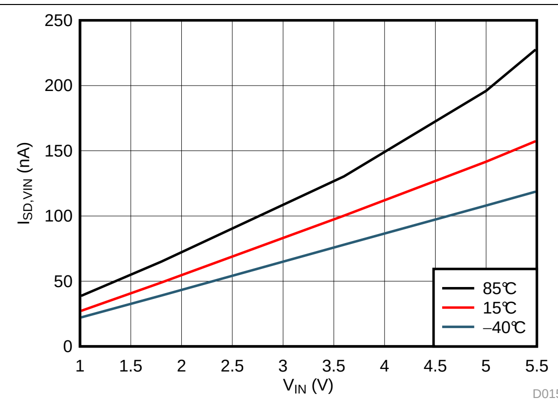
Enabled

Figure 2. ON-Resistance vs Input voltage



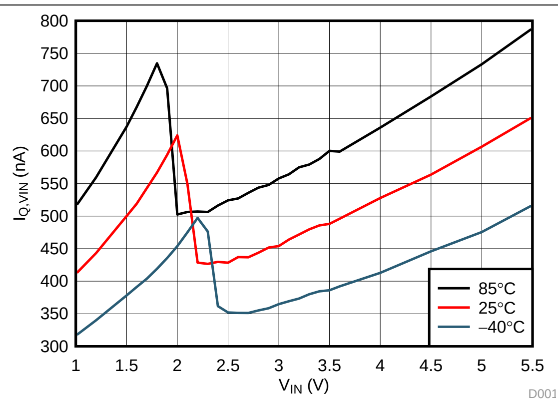
TPS22916C, TPS22916CN, TPS22916B $V_{ON} \leq V_{IL}$

Figure 3. Shutdown Current



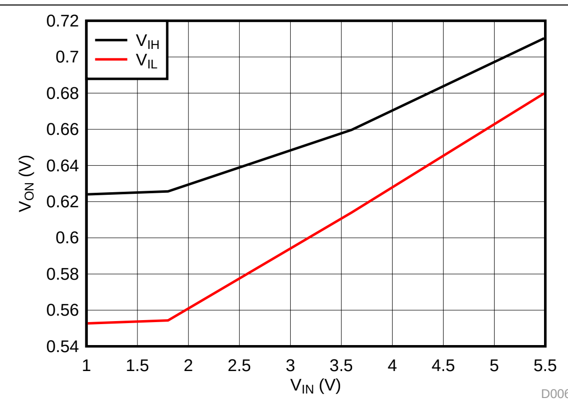
TPS22916CL $V_{ON} \geq V_{IH}$

Figure 4. Shutdown Current (Active Low)



Enabled

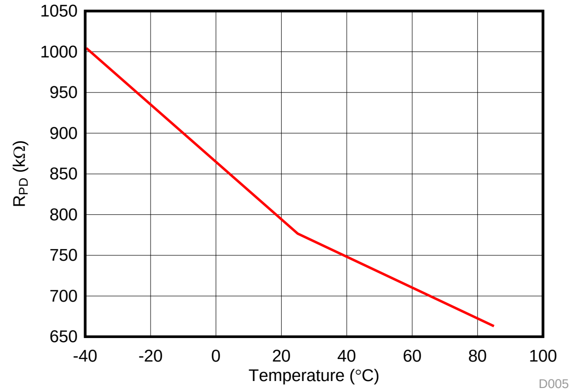
Figure 5. Quiescent Current



–40°C to +85°C

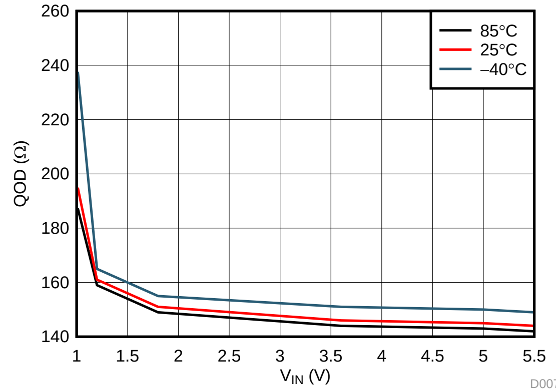
Figure 6. ON Pin Threshold

Typical Electrical Characteristics (continued)



$V_{ON} \leq V_{IL}$

Figure 7. ON Pin Smart Pull Down

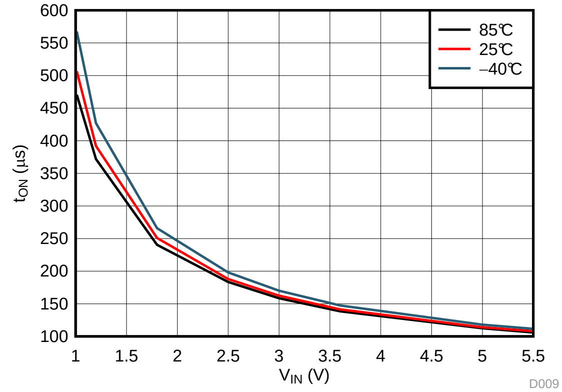


TPS22916C TPS22916CL TPS22916B

Figure 8. Quick Output Discharge

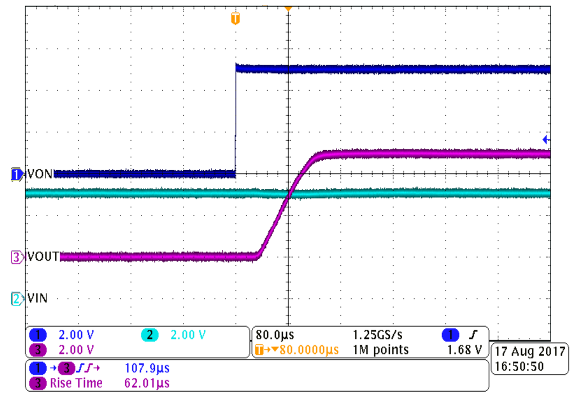
6.7.2 Typical Switching Characteristics

The typical data in this section apply to all devices at 25°C unless otherwise noted.



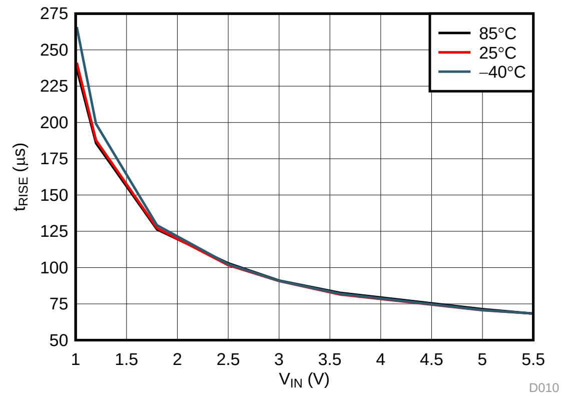
C_L = 0.1 µF R_L = 10 Ω

Figure 9. Fast Turn On Time



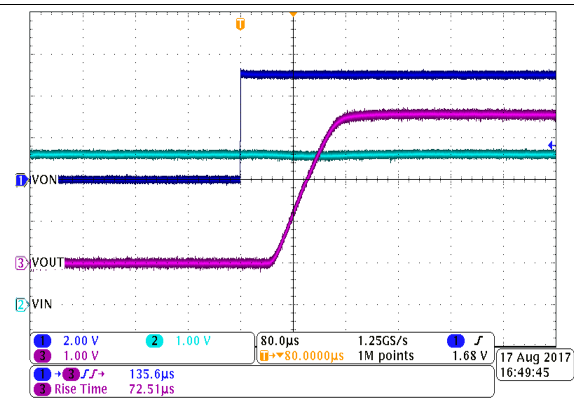
TPS22916B V_{IN} = 5 V C_L = 0.1 µF R_L = 10 Ω

Figure 10. Fast Turn On at 5 V



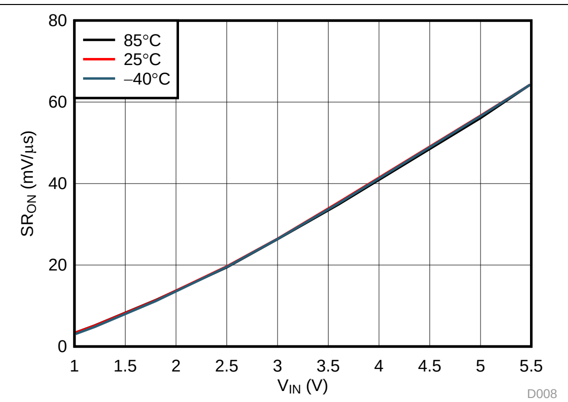
C_L = 0.1 µF R_L = 10 Ω

Figure 11. Fast Rise Time



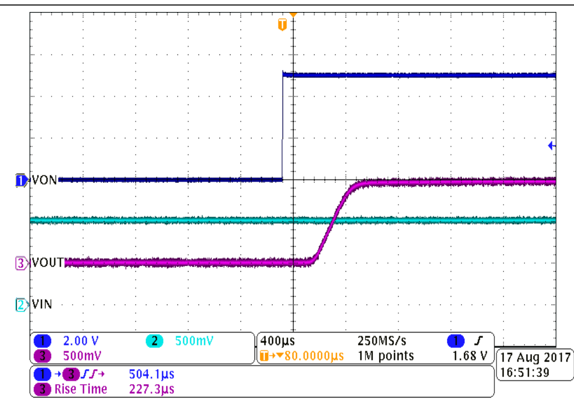
TPS22916B V_{IN} = 3.6 V C_L = 0.1 µF R_L = 10 Ω

Figure 12. Fast Turn On at 3.6 V



C_L = 0.1 µF R_L = 10 Ω

Figure 13. Fast Slew Rate

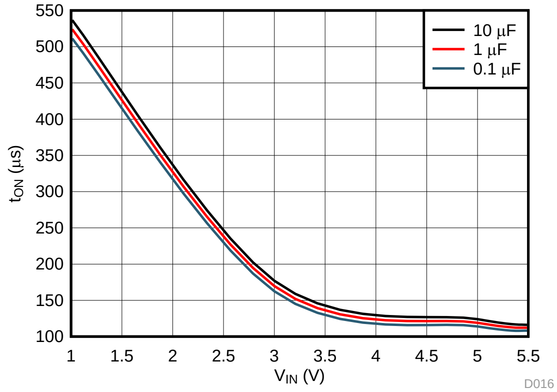


TPS22916B V_{IN} = 1 V C_L = 0.1 µF R_L = 10 Ω

Figure 14. Fast Turn on at 1 V

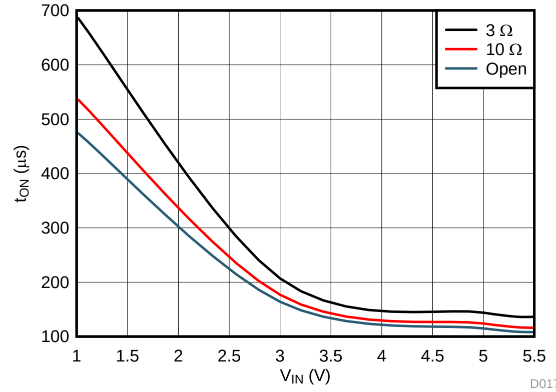
Typical Switching Characteristics (continued)

The typical data in this section apply to all devices at 25°C unless otherwise noted.



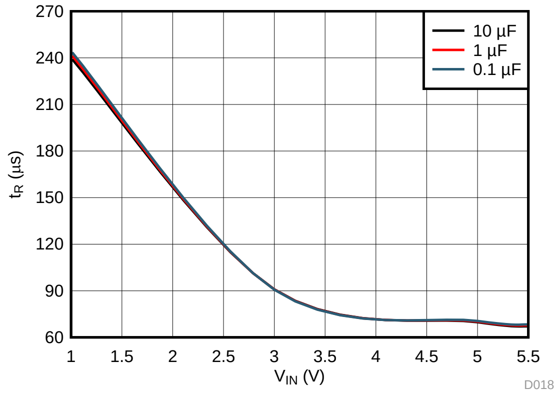
R_L = 10 Ω TPS22916B

Figure 15. Fast Turn On vs Load Capacitance



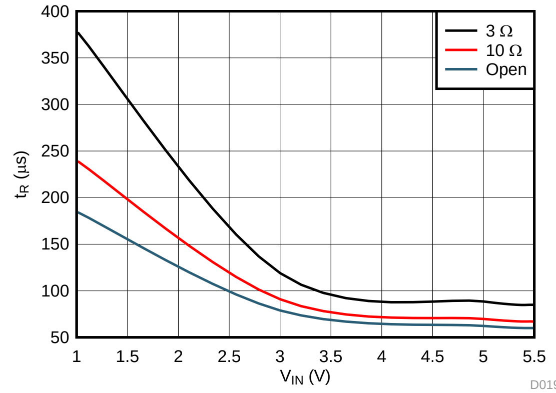
C_L = 10 µF TPS22916B

Figure 16. Fast Turn On vs Load Resistance



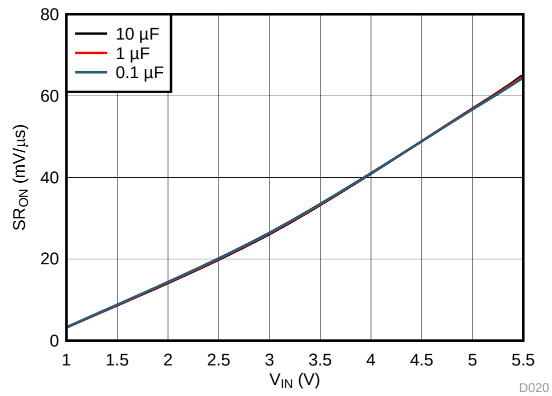
R_L = 10 Ω TPS22916B

Figure 17. Fast Rise Time vs Load Capacitance



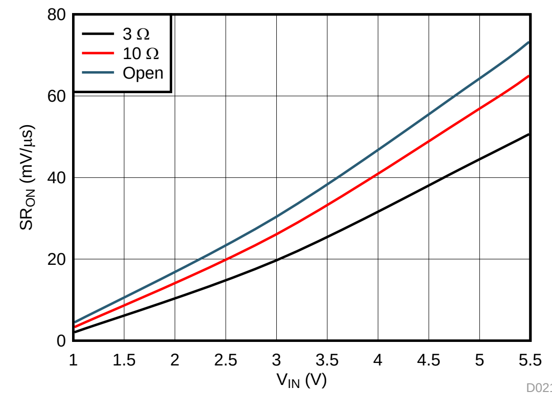
C_L = 10 µF TPS22916B

Figure 18. Fast Rise Time vs Load Resistance



R_L = 10 Ω TPS22916B

Figure 19. Fast Slew Rate vs Load Capacitance

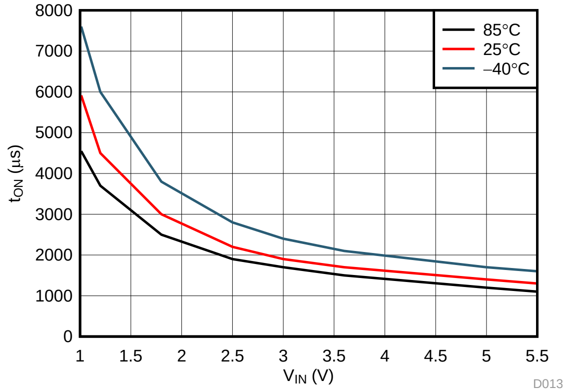


C_L = 10 µF TPS22916B

Figure 20. Fast Slew Rate vs Load Resistance

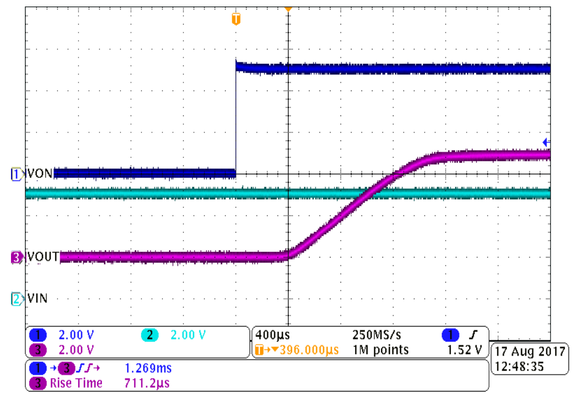
Typical Switching Characteristics (continued)

The typical data in this section apply to all devices at 25°C unless otherwise noted.



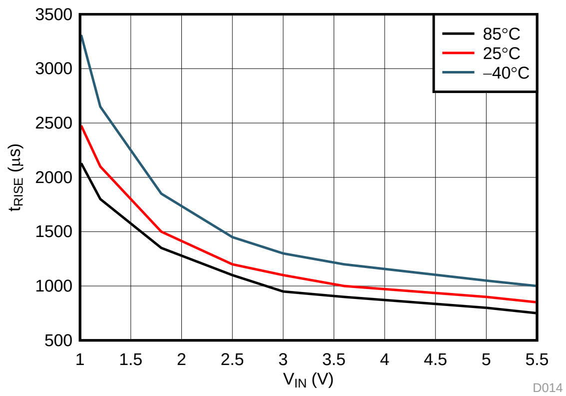
C_L = 0.1 µF R_L = 10 Ω

Figure 21. Slow Turn on Time



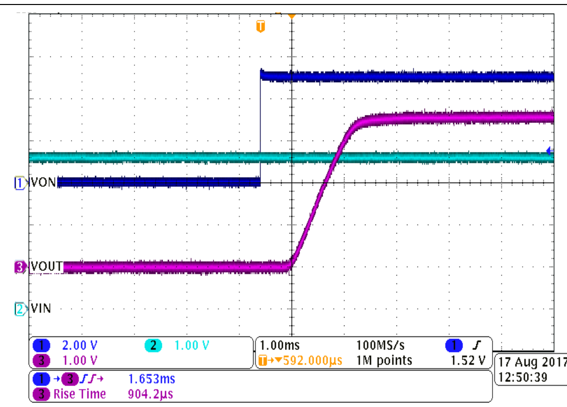
TPS22916C V_{IN} = 5 V C_L = 0.1 µF R_L = 10 Ω

Figure 22. Slow Turn on at 5 V



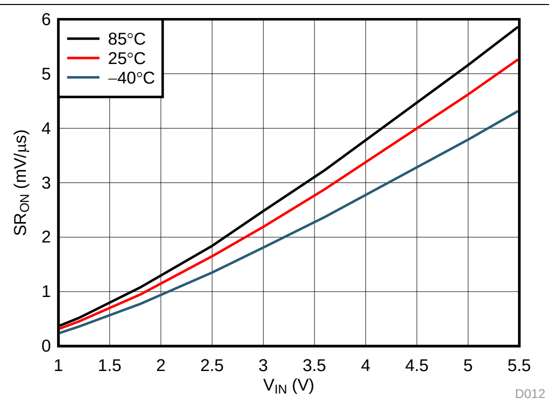
C_L = 0.1 µF R_L = 10 Ω

Figure 23. Slow Rise Time



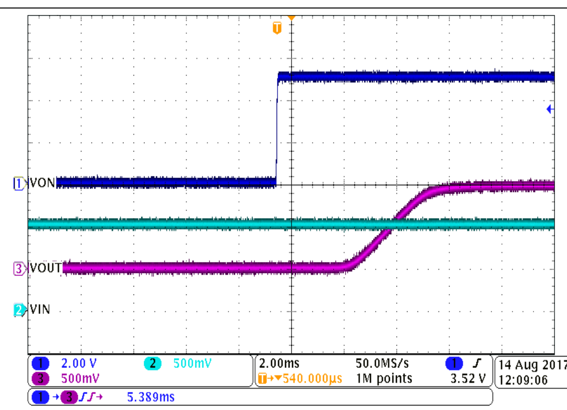
TPS22916C V_{IN} = 3.6 V C_L = 0.1 µF R_L = 10 Ω

Figure 24. Slow Turn On at 3.6 V



C_L = 0.1 µF R_L = 10 Ω

Figure 25. Slow Slew Rate

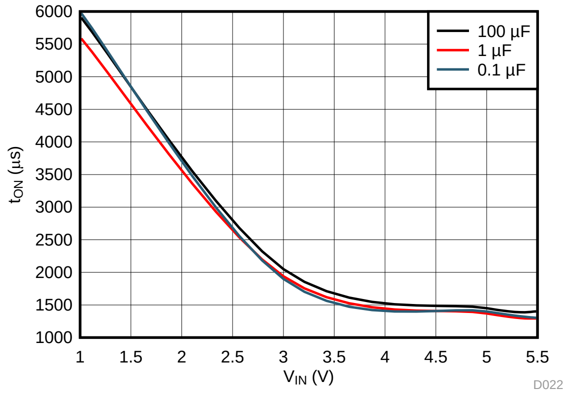


TPS22916C V_{IN} = 1 V C_L = 0.1 µF R_L = 10 Ω

Figure 26. Slow Turn On at 1 V

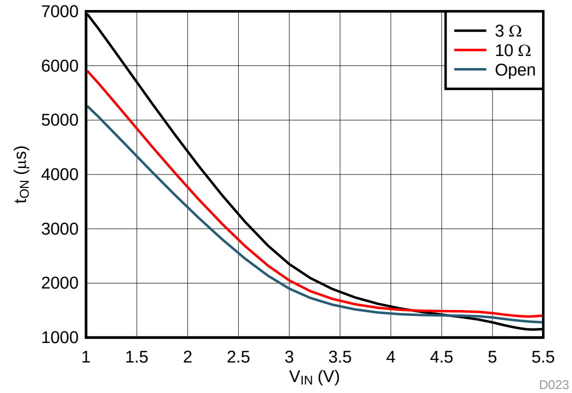
Typical Switching Characteristics (continued)

The typical data in this section apply to all devices at 25°C unless otherwise noted.



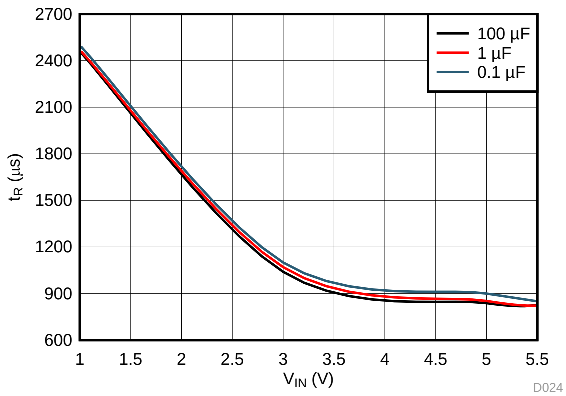
R_L = 10 Ω TPS22916C TPS22916CN TPS22916CL

Figure 27. Slow Turn On vs Load Capacitance



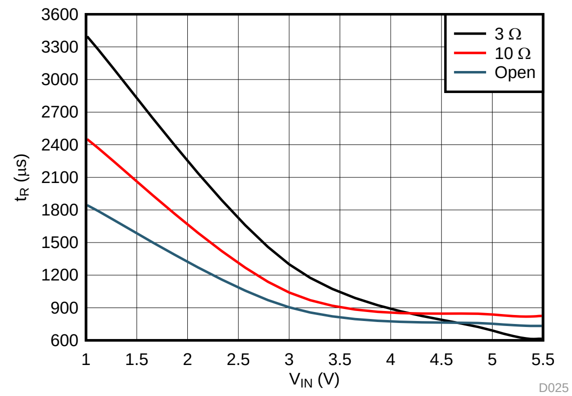
C_L = 100 µF TPS22916C TPS22916CN TPS22916CL

Figure 28. Slow Turn On vs Load Resistance



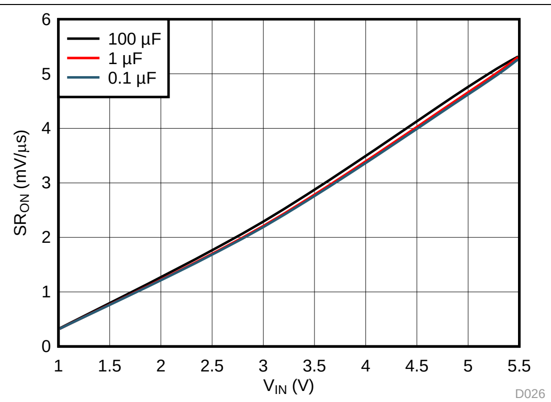
R_L = 10 Ω TPS22916C TPS22916CN TPS22916CL

Figure 29. Slow Rise Time vs Load Capacitance



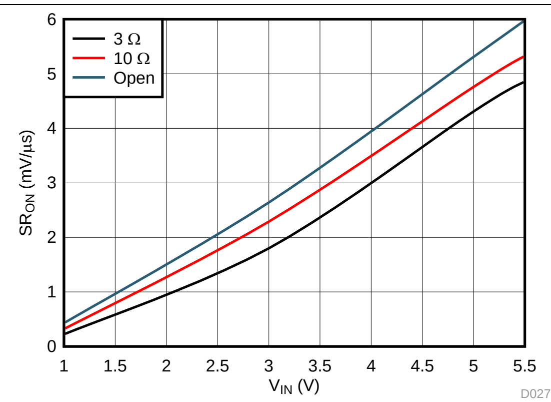
C_L = 100 µF TPS22916C TPS22916CN TPS22916CL

Figure 30. Slow Rise Time vs Load Resistance



R_L = 10 Ω TPS22916C TPS22916CN TPS22916CL

Figure 31. Slow Slew Rate vs Load Capacitance



C_L = 100 µF TPS22916C TPS22916CN TPS22916CL

Figure 32. Slow Slew Rate vs Load Resistance

Typical Switching Characteristics (continued)

The typical data in this section apply to all devices at 25°C unless otherwise noted.

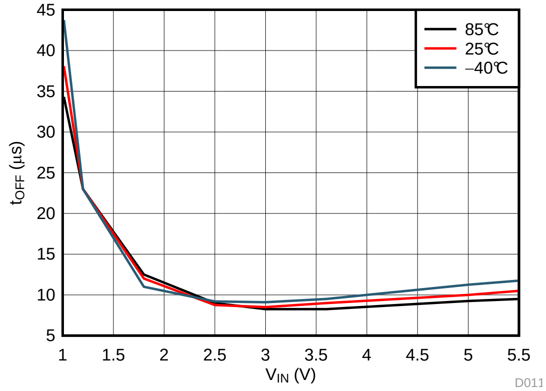
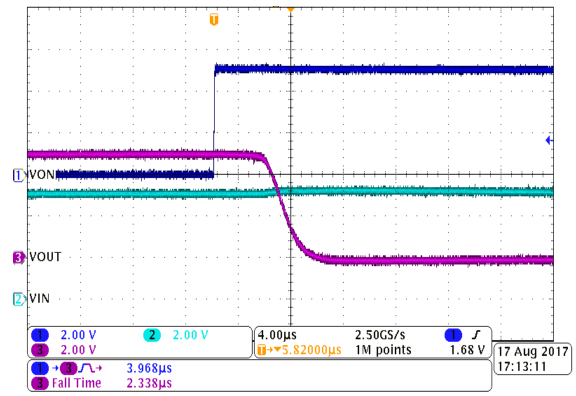
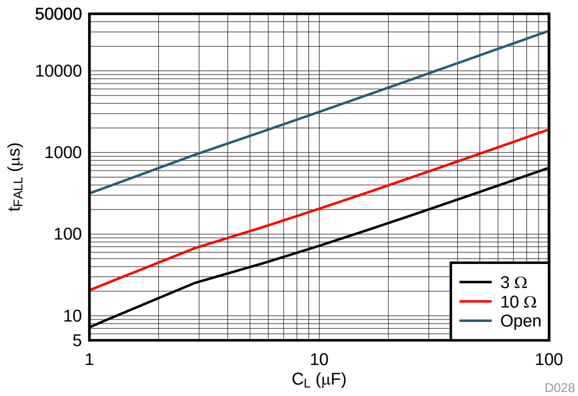


Figure 33. Turn Off Time



TPS22916CL V_{IN} = 5 V C_L = 0.1 µF R_L = 10 Ω

Figure 34. Turn Off at 5 V (Active Low)



V_{IN} = 1 V to 5.5 V TPS22916C TPS22916CL TPS22916B

Figure 35. Fall Time

7 Parameter Measurement Information

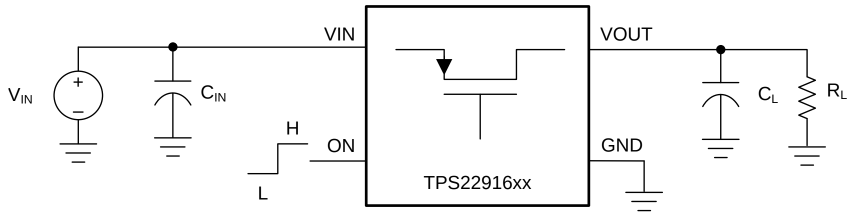


Figure 36. TPS22916 Test Circuit

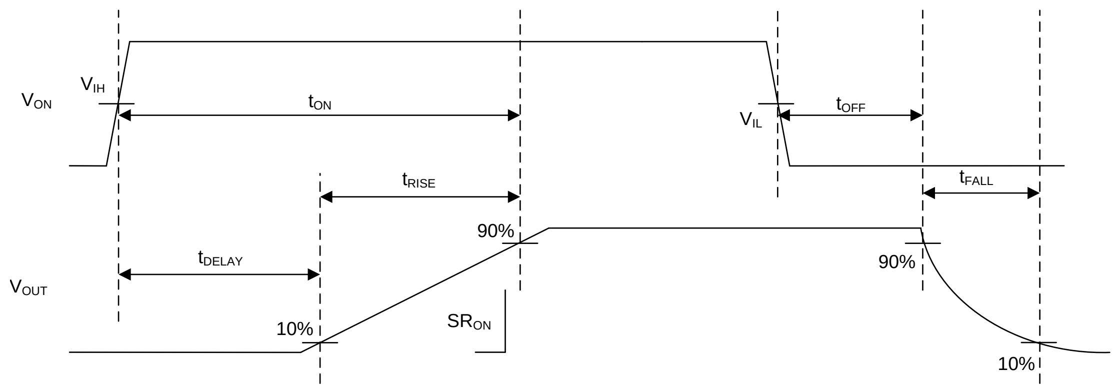


Figure 37. TPS22916 Timing Waveform

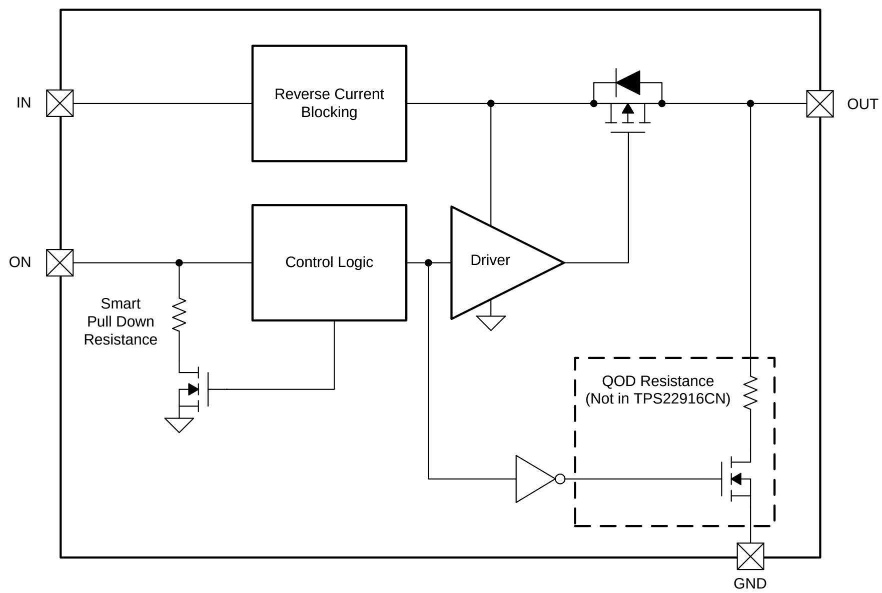
8 Detailed Description

8.1 Overview

This family of devices are single channel, 2-A load switches in ultra-small, space saving 4-pin WCSP package. These devices implement a low resistance P-channel MOSFET with a controlled rise time for applications that need to limit inrush current.

These devices are designed to have very low leakage current during off state. This prevents downstream circuits from pulling high standby current from the supply. Integrated control logic, driver, power supply, and output discharge FET eliminates the need for additional external components, which reduces solution size and BOM count.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 On and Off Control

The ON pin controls the state of the switch. The ON pin is compatible with standard GPIO logic threshold. It can be used with any microcontroller with 1.2-V, 1.8-V, 2.5-V, 3.3-V, or 5.5-V GPIO.

8.3.2 Fall Time (t_{FALL}) and Quick Output Discharge (QOD)

The TPS22916B/C/CL include a Quick Output Discharge feature. When the switch is disabled, a discharge resistor is connected between VOUT and GND. This resistor has a typical value of QOD and prevents the output from floating while the switch is disabled.

As load capacitance and load resistance increase: t_{FALL} increases. The larger the load resistance or load capacitance is, the longer it takes to discharge the capacitor, resulting in a longer fall time.

Feature Description (continued)

The output fall time is determined by how quickly the load capacitance is discharged and can be found using Equation 1 .

$$t_{FALL} = -(R_{DIS}) \times C_L \times \ln(V_{10\%}/V_{90\%})$$

Where

- $V_{10\%}$ is 10% of the initial output voltage
- $V_{90\%}$ is 90% of the initial output voltage
- R_{DIS} is the result of the QOD resistance in parallel with the Load Resistance R_L
- C_L is the load capacitance (1)

With the Quick Output Discharge feature, the QOD resistance is in parallel with R_L. This provides a lower total load resistance as seen from the load capacitance which discharges the capacitance faster resulting in a smaller t_{FALL}.

8.3.3 Full-Time Reverse Current Blocking

In a scenario where the device is enabled and V_{OUT} is greater than V_{IN} there is potential for reverse current to flow through the pass FET or the body diode. When the reverse current threshold (I_{RCB}) is exceeded, the switch is disabled within t_{RCB}. The Switch will remain off and block reverse current as long as the reverse voltage condition exists. Once V_{OUT} has dropped below the V_{RCB} release threshold the TPS22916xx will turn back on with slew rate control.

8.4 Device Functional Modes

Table 1 describes the state for each variant as determined by the ON pin

Table 1. Device Function Table

ON	TPS22916B	TPS22916C	TPS22916CN	TPS22916CL
≤ V_{IL}	Disabled	Disabled	Disabled	Enabled
≥ V_{IH}	Enabled	Enabled	Enabled	Disabled

Table 2 shows when QOD is active for each variant.

Table 2. QOD Function Table

Device	TPS22916B	TPS22916C	TPS22916CN	TPS22916CL
Enabled	No	No	No	No
Disabled	Yes	Yes	No	Yes

Table 3 shows when the ON Pin Smart Pull Down is active.

Table 3. Smart-ON Pull Down

V_{ON}	Pull Down
≤ V_{IL}	Connected
≥ V_{IH}	Disconnected

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

This section highlights some of the design considerations when implementing this device in various applications. A PSPICE model for this device is also available in the product page of this device.

9.1.1 Typical Application

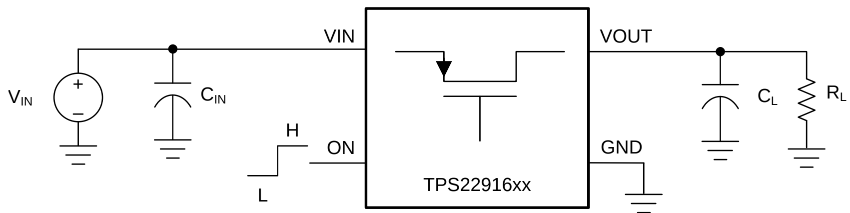


Figure 38. Typical Application

9.1.1.1 Design Requirements

For this design example, below, use the input parameters shown in Table 4.

Table 4. Design Parameters

Design Parameter	Example Value
Input Voltage (V_{IN})	3.6 V
Load Capacitance (C_L)	47 µF
Maximum Inrush Current (I_{RUSH})	300 mA

9.1.1.2 Detailed Design Procedure

9.1.1.2.1 Maximum Inrush Current

When the switch is enabled, the output capacitors must be charged up from 0-V to VIN voltage. This charge arrives in the form of inrush current. Inrush current can be calculated using the following equation:

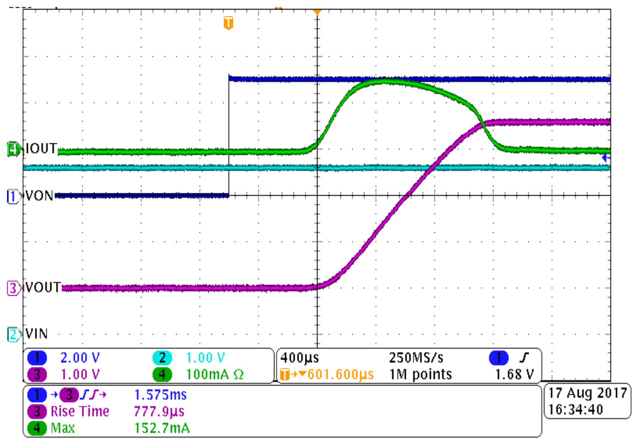
$$I_{RUSH} = C_L \times SR_{ON} \quad (2)$$

$$I_{RUSH} = 47\mu F \times 3.2 mV/\mu s \quad (3)$$

$$I_{RUSH} = 150mA \quad (4)$$

The TPS22916x offers multiple rise time options to control the inrush current during turn-on. The appropriate device can be selected based upon the maximum acceptable slew rate which can be calculated using the design requirements and the inrush current equation. In this case, the TPS22916C provides a slew rate slow enough to limit the inrush current to the desired amount.

9.1.1.3 Application Curve



V_{IN} = 3.6 V C_L = 47µF R_L = Open
TPS22916C T_A = 25°C

Figure 39. Inrush Current

10 Power Supply Recommendations

The device is designed to operate with a VIN range of 1 V to 5.5 V. The VIN power supply must be well regulated and placed as close to the device terminal as possible. The power supply must be able to withstand all transient load current steps. In most situations, using an input capacitance (C_{IN}) of 1 µF is sufficient to prevent the supply voltage from dipping when the switch is turned on. In cases where the power supply is slow to respond to a large transient current or large load current step, additional bulk capacitance may be required on the input.

11 Layout

11.1 Layout Guidelines

For best performance, all traces must be as short as possible. To be most effective, the input and output capacitors must be placed close to the device to minimize the effects that parasitic trace inductances may have on normal operation. Using wide traces for VIN, VOUT, and GND helps minimize the parasitic electrical effects.

11.2 Layout Example

Equation 3 shows an example for these devices. Notice the connection to system ground between the V_{OUT} Bypass Capacitor ground and the GND pin of the load switch, this creates a ground barrier which helps to reduce the ground noise seen by the device.

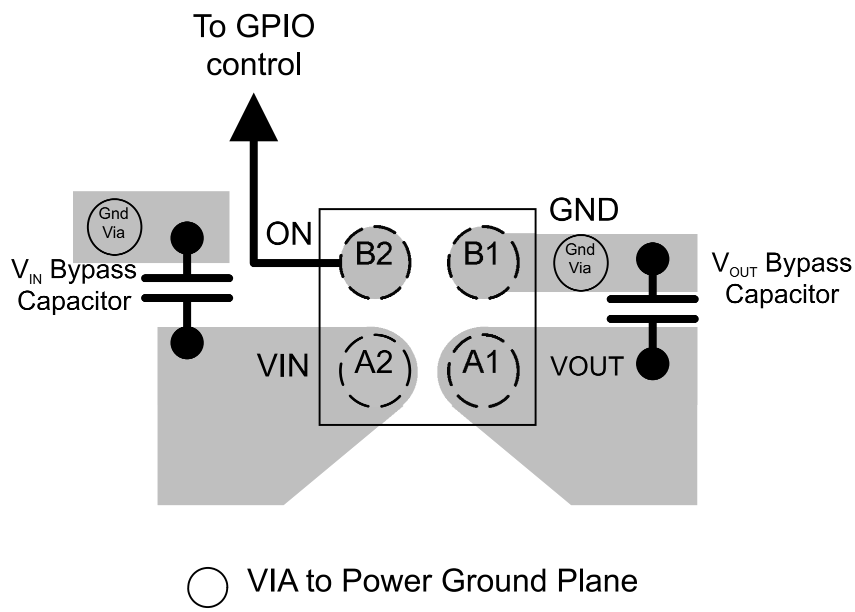


Figure 40. TPS22916xx Layout

11.3 Thermal Considerations

The maximum IC junction temperature must be restricted to 125°C under normal operating conditions. To calculate the maximum allowable dissipation, $P_{D(max)}$ for a given output current and ambient temperature, use Equation 5 as a guideline:

$$P_{D(MAX)} = \frac{T_{J(MAX)} - T_A}{R_{\theta JA}} \tag{5}$$

Where,

$P_{D(max)}$ = maximum allowable power dissipation
$T_{J(max)}$ = maximum allowable junction temperature
T_A = ambient temperature for the device
θ_{JA} = junction to air thermal impedance. See the *Thermal Information* section.

12 Device and Documentation Support

12.1 Documentation Support

12.1.1 Related Documentation

For related documentation see the following:

TPS22916 Load Switch Evaluation Module

12.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.4 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

12.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

13.1 Package Option Addendum

13.1.1 Packaging Information

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish(3)	MSL Peak Temp (4)	Op Temp (°C)	Device Marking(5)(6)
TPS22916BYFPR	Active	DSBGA	YFP	4	3000	Green (RoHS & no Sb/Br)	SAC396	Level-1-260C-UNLIM	-40 to 85	BA
TPS22916BYFPT	Active	DSBGA	YFP	4	250	Green (RoHS & no Sb/Br)	SAC396	Level-1-260C-UNLIM	-40 to 85	BA
TPS22916CLYFPR	Active	DSBGA	YFP	4	3000	Green (RoHS & no Sb/Br)	Call TI	Level-1-260C-UNLIM	-40 to 85	B9
TPS22916CLYFPT	Active	DSBGA	YFP	4	250	Green (RoHS & no Sb/Br)	Call TI	Level-1-260C-UNLIM	-40 to 85	B9

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PRE_PROD Unannounced device, not in production, not available for mass market, nor on the web, samples not available.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

(4) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(5) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device

(6) Multiple Device markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

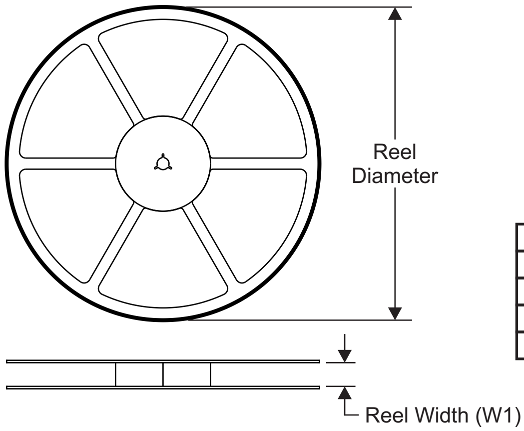
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

Package Option Addendum (continued)

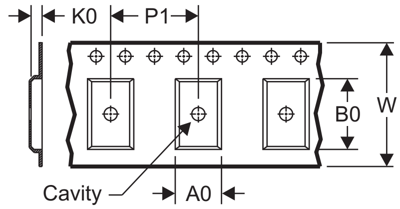
Orderable Device	Status [1]	Package Type	Package Drawing	Pins	Package Qty	Eco Plan [2]	Lead/Ball Finish[3]	MSL Peak Temp [4]	Op Temp (°C)	Device Marking[5][6]
TPS22916CNYFPR	Active	DSBGA	YFP	4	3000	Green (RoHS & no Sb/Br)	SAC396	Level-1-260C-UNLIM	-40 to 85	B8
TPS22916CNYFPT	Active	DSBGA	YFP	4	250	Green (RoHS & no Sb/Br)	SAC396	Level-1-260C-UNLIM	-40 to 85	B8
TPS22916CYFPR	Active	DSBGA	YFP	4	3000	Green (RoHS & no Sb/Br)	SAC396	Level-1-260C-UNLIM	-40 to 85	B7
TPS22916CYFPT	Active	DSBGA	YFP	4	250	Green (RoHS & no Sb/Br)	SAC396	Level-1-260C-UNLIM	-40 to 85	B7

13.1.2 Tape and Reel Information

REEL DIMENSIONS

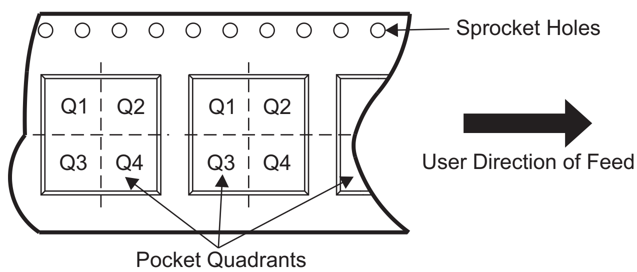


TAPE DIMENSIONS



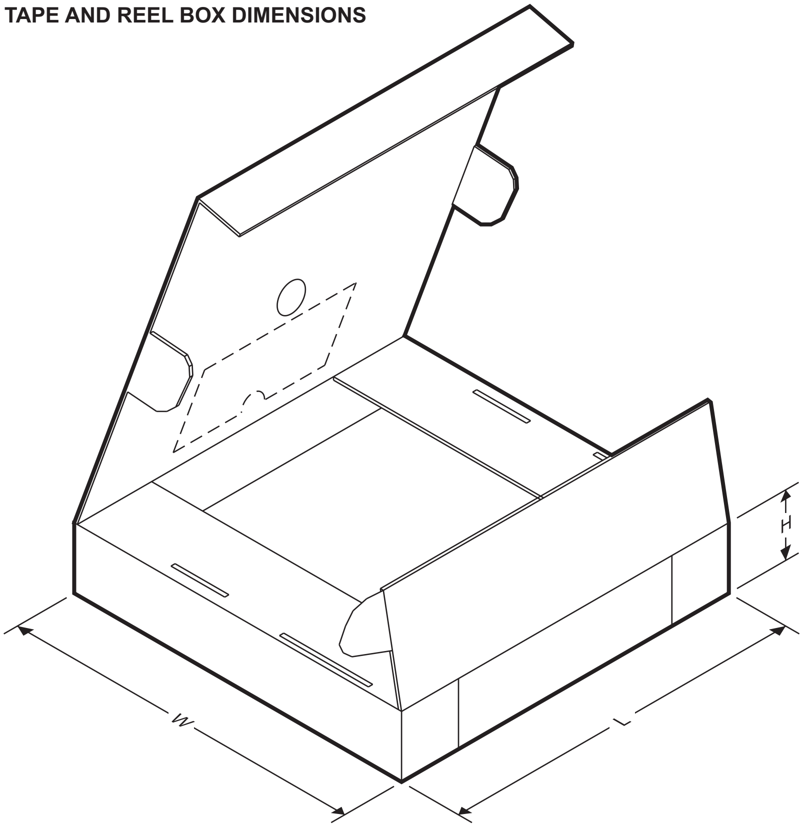
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS22916BYFPR	DSBGA	YFP	4	3000	180.0	8.4	0.86	0.86	0.59	4.0	8.0	Q1
TPS22916BYFPT	DSBGA	YFP	4	250	180.0	8.4	0.86	0.86	0.59	4.0	8.0	Q1
TPS22916CLYFPR	DSBGA	YFP	4	3000	180.0	8.4	0.86	0.86	0.59	4.0	8.0	Q1
TPS22916CLYFPT	DSBGA	YFP	4	250	180.0	8.4	0.86	0.86	0.59	4.0	8.0	Q1
TPS22916CNYFPR	DSBGA	YFP	4	3000	180.0	8.4	0.86	0.86	0.59	4.0	8.0	Q1
TPS22916CNYFPT	DSBGA	YFP	4	250	180.0	8.4	0.86	0.86	0.59	4.0	8.0	Q1
TPS22916CYFPR	DSBGA	YFP	4	3000	180.0	8.4	0.86	0.86	0.59	4.0	8.0	Q1
TPS22916CYFPT	DSBGA	YFP	4	250	180.0	8.4	0.86	0.86	0.59	4.0	8.0	Q1

TAPE AND REEL BOX DIMENSIONS



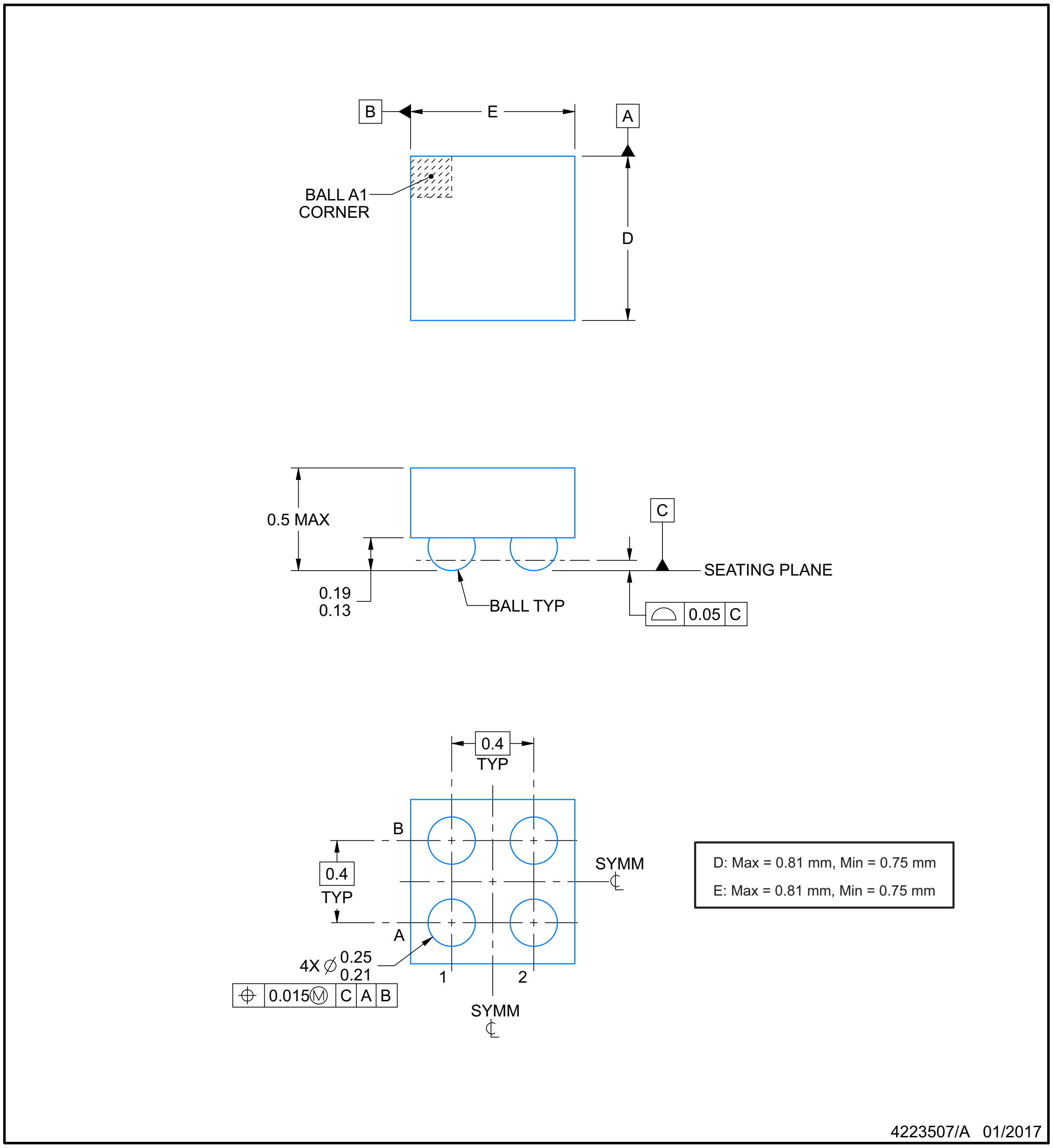
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS22916BYFPR	DSBGA	YFP	4	3000	182.0	182.0	20.0
TPS22916BYFPT	DSBGA	YFP	4	250	182.0	182.0	20.0
TPS22916CLYFPR	DSBGA	YFP	4	3000	182.0	182.0	20.0
TPS22916CLYFPT	DSBGA	YFP	4	250	182.0	182.0	20.0
TPS22916CNYFPR	DSBGA	YFP	4	3000	182.0	182.0	20.0
TPS22916CNYFPT	DSBGA	YFP	4	250	182.0	182.0	20.0
TPS22916CYFPR	DSBGA	YFP	4	3000	182.0	182.0	20.0
TPS22916CYFPT	DSBGA	YFP	4	250	182.0	182.0	20.0

PACKAGE OUTLINE

YFP0004

DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY



NOTES:

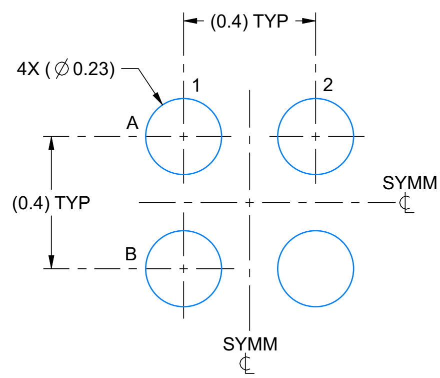
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

EXAMPLE BOARD LAYOUT

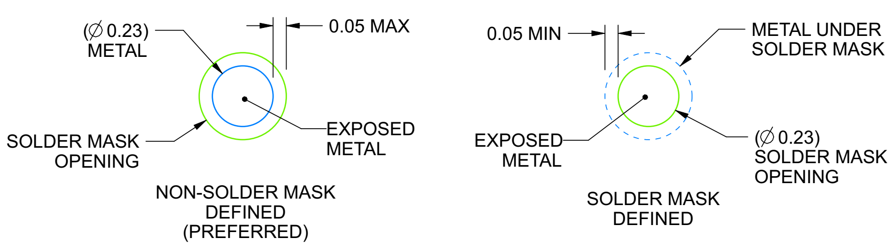
YFP0004

DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:50X



SOLDER MASK DETAILS
NOT TO SCALE

4223507/A 01/2017

NOTES: (continued)

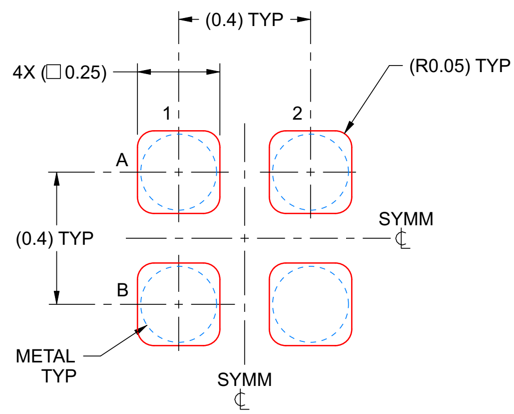
3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. For more information, see Texas Instruments literature number SNVA009 (www.ti.com/lit/snva009).

EXAMPLE STENCIL DESIGN

YFP0004

DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:50X

4223507/A 01/2017

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS22916BYFPR	ACTIVE	DSBGA	YFP	4	3000	Green (RoHS & no Sb/Br)	SAC396	Level-1-260C-UNLIM	-40 to 85	BA	Samples
TPS22916BYFPT	ACTIVE	DSBGA	YFP	4	250	Green (RoHS & no Sb/Br)	SAC396	Level-1-260C-UNLIM	-40 to 85	BA	Samples
TPS22916CLYFPR	ACTIVE	DSBGA	YFP	4	3000	Green (RoHS & no Sb/Br)	SAC396	Level-1-260C-UNLIM	-40 to 85	B9	Samples
TPS22916CLYFPT	ACTIVE	DSBGA	YFP	4	250	Green (RoHS & no Sb/Br)	SAC396	Level-1-260C-UNLIM	-40 to 85	B9	Samples
TPS22916CNYFPR	ACTIVE	DSBGA	YFP	4	3000	Green (RoHS & no Sb/Br)	SAC396	Level-1-260C-UNLIM	-40 to 85	B8	Samples
TPS22916CNYFPT	ACTIVE	DSBGA	YFP	4	250	Green (RoHS & no Sb/Br)	SAC396	Level-1-260C-UNLIM	-40 to 85	B8	Samples
TPS22916CYFPR	ACTIVE	DSBGA	YFP	4	3000	Green (RoHS & no Sb/Br)	SAC396	Level-1-260C-UNLIM	-40 to 85	B7	Samples
TPS22916CYFPT	ACTIVE	DSBGA	YFP	4	250	Green (RoHS & no Sb/Br)	SAC396	Level-1-260C-UNLIM	-40 to 85	B7	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

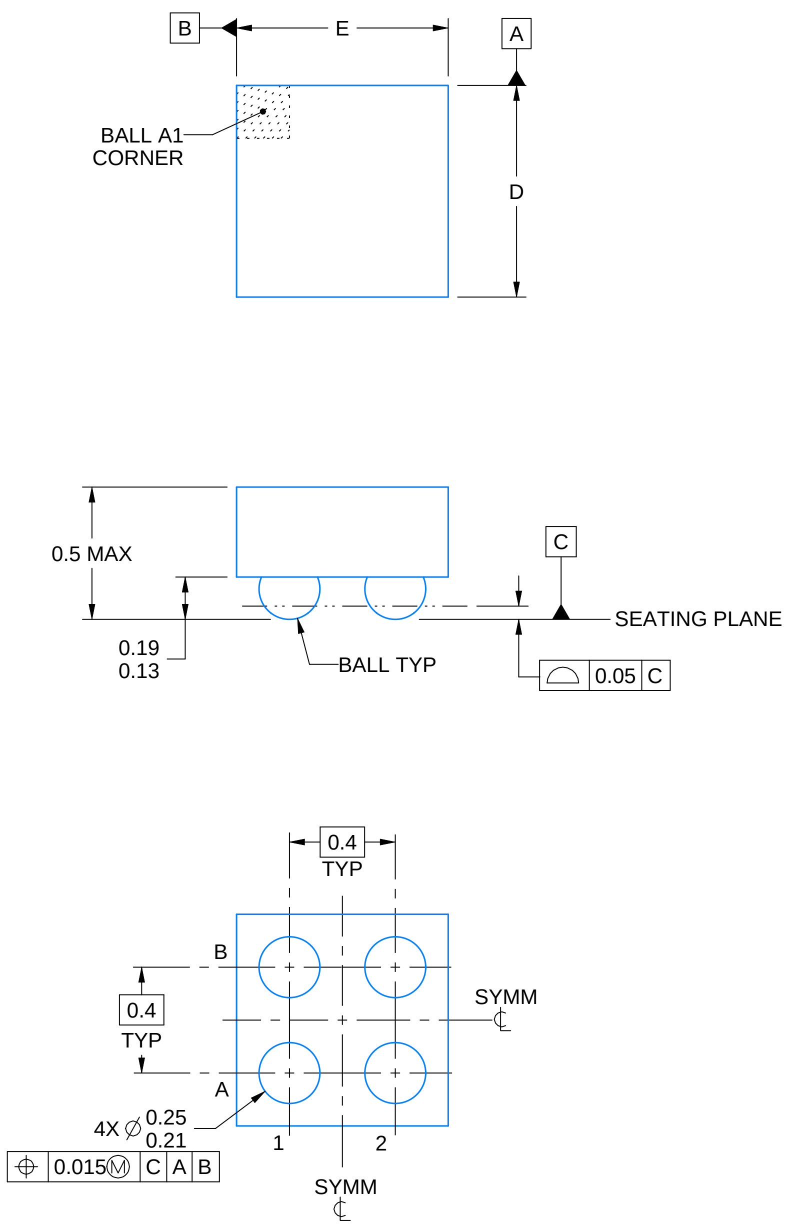
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.



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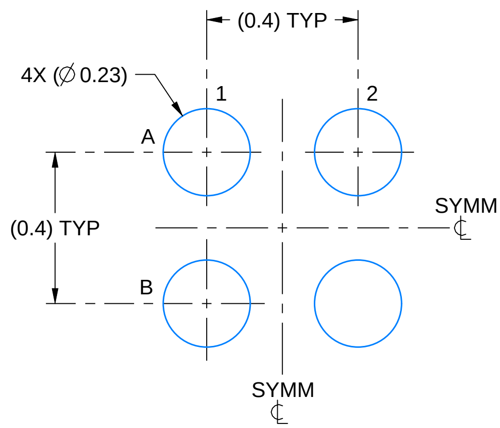
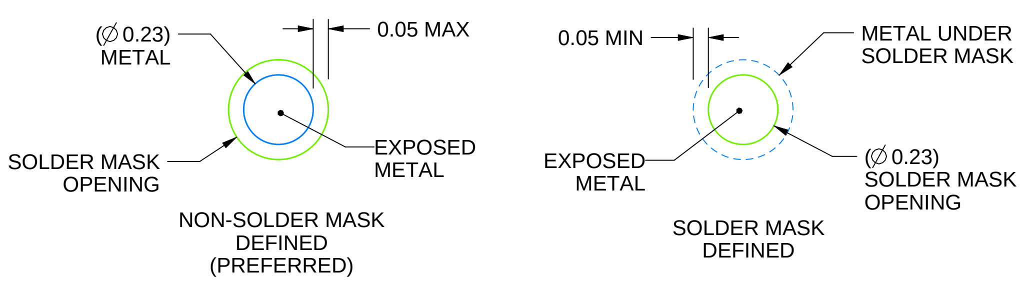
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:50X



SOLDER MASK DETAILS
NOT TO SCALE

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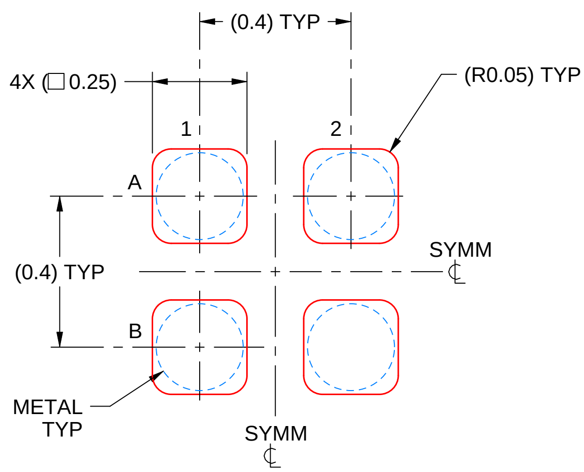
NOTES: (continued)

3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. For more information, see Texas Instruments literature number SNVA009 (www.ti.com/lit/snva009).



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:50X

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NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

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