

## TPS2400 Overvoltage Protection Controller

### 1 Features

- Up to 100-V Overvoltage Protection
- 6.9-V Overvoltage Shutdown Threshold
- 3-V Undervoltage Shutdown Threshold
- Overvoltage Turnoff Time Less than 1  $\mu$ s
- External N-Channel MOSFET Driven by Internal Charge Pump
- 1-mA Maximum Static Supply Current
- 5-Pin SOT-23 Package
- -40°C to 85°C Ambient Temperature Range
- 2.5-kV Human-Body-Model, 500-V CDM Electrostatic Discharge Protection

### 2 Applications

- Cellular Phones
- PDAs
- Portable PCs
- Media Players
- Digital Cameras
- GPS

### 3 Description

The TPS2400 overvoltage protection controller is used with an external N-channel MOSFET to isolate sensitive electronics from destructive voltage spikes and surges. It is specifically designed to prevent large voltage transients associated with automotive environments (load dump) from damaging sensitive circuitry. When potentially damaging voltage levels are detected by the TPS2400 the supply is disconnected from the load before any damage can occur.

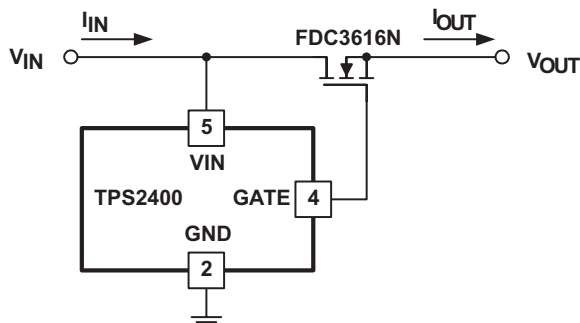
Internal circuitry includes a trimmed band-gap reference, oscillator, Zener diode, charge pump, comparator, and control logic. The TPS2400 device is designed for use with an external N-channel MOSFET, which are readily available in a wide variety of voltages.

#### Device Information<sup>(1)</sup>

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPS2400	SOT-23 (5)	2.90 mm x 1.60 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

#### Application Diagram



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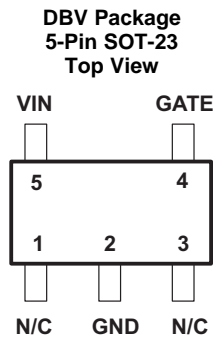
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## 4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

<b>Changes from Revision A (August 2008) to Revision B</b>	<b>Page</b>
<ul style="list-style-type: none"> <li>Added <i>ESD Ratings</i> table, <i>Feature Description</i> section, <i>Device Functional Modes</i>, <i>Application and Implementation</i> section, <i>Power Supply Recommendations</i> section, <i>Layout</i> section, <i>Device and Documentation Support</i> section, and <i>Mechanical, Packaging, and Orderable Information</i> section .....</li> </ul>	<b>1</b>

## 5 Pin Configuration and Functions



### Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
GATE	4	O	Output gate drive for an external N-channel MOSFET
GND	2	—	Ground
NC	1, 3	—	No internal connection
VIN	5	I	Input voltage

## 6 Specifications

### 6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) <sup>(1)</sup>

			MIN	MAX	UNIT
V <sub>VIN</sub>	Input voltage	VIN	-0.3	110	V
V <sub>OUT</sub>	Output voltage	GATE (continuous)	-0.3	22	V
		GATE (transient, < 10 μs, Duty Cycle < 0.1%)	-0.3	25	
Continuous total power dissipation			See <a href="#">Thermal Information</a>		
T <sub>J</sub>	Operating junction temperature		-40	125	°C
T <sub>A</sub>	Operating free-air temperature		-40	85	°C
T <sub>stg</sub>	Storage temperature		-65	150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

### 6.2 ESD Ratings

			VALUE	UNIT
V <sub>(ESD)</sub>	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins <sup>(1)</sup>	±2500	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins <sup>(2)</sup>	±500	

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

### 6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
Supply voltage at V <sub>IN</sub>			3.1		6.8	V
Operating junction temperature			-40		125	°C

### 6.4 Thermal Information

THERMAL METRIC <sup>(1)</sup>		TPS2400	UNIT
		DBV (SOT-23)	
		5 PINS	
R <sub>θJA</sub>	Junction-to-ambient thermal resistance	219.6	°C/W
R <sub>θJC(top)</sub>	Junction-to-case (top) thermal resistance	126.2	°C/W
R <sub>θJB</sub>	Junction-to-board thermal resistance	51.2	°C/W
Ψ <sub>JT</sub>	Junction-to-top characterization parameter	15.9	°C/W
Ψ <sub>JB</sub>	Junction-to-board characterization parameter	50.1	°C/W
R <sub>θJC(bot)</sub>	Junction-to-case (bottom) thermal resistance	N/A	°C/W

- (1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, [SPRA953](#).

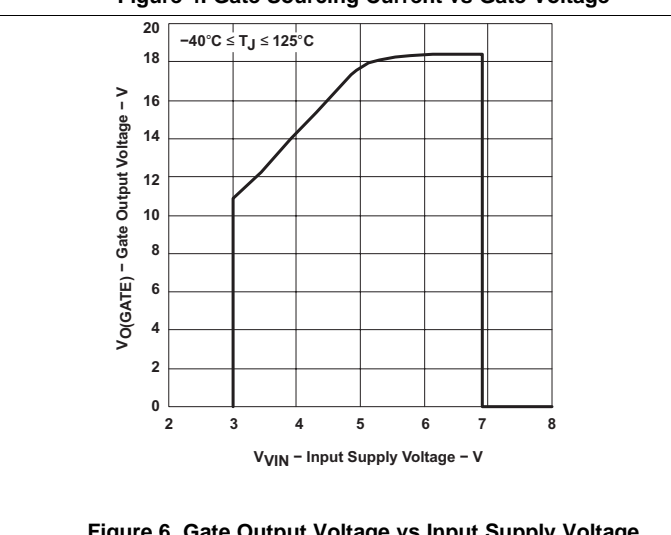
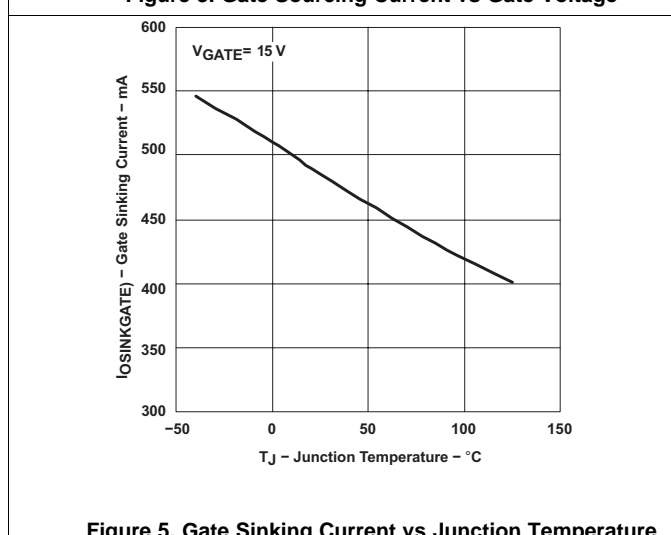
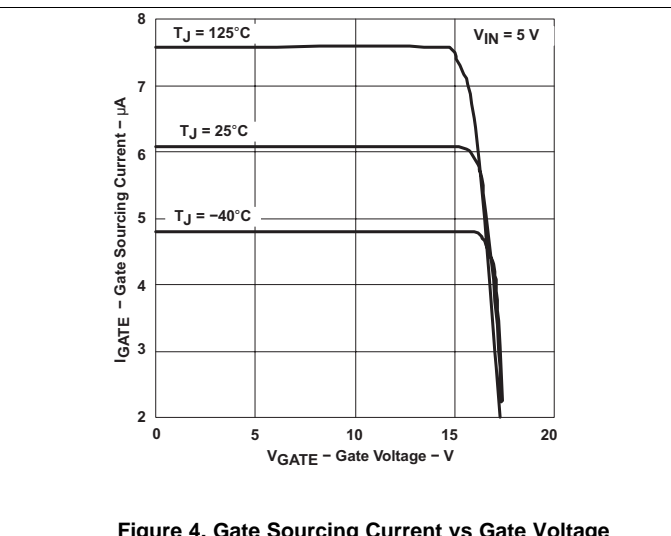
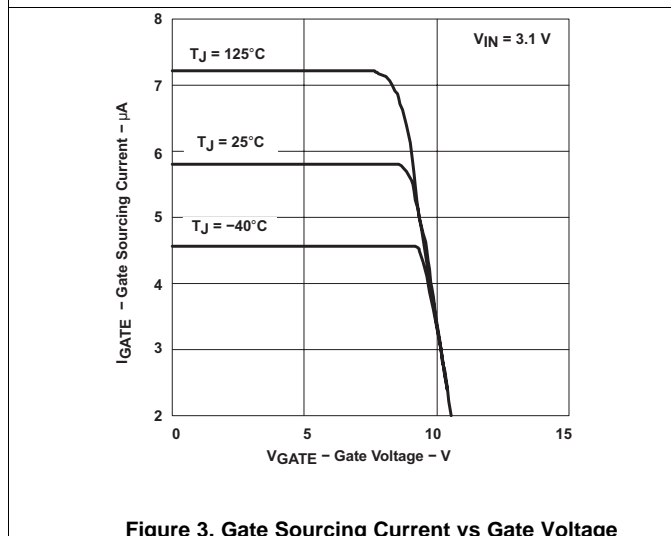
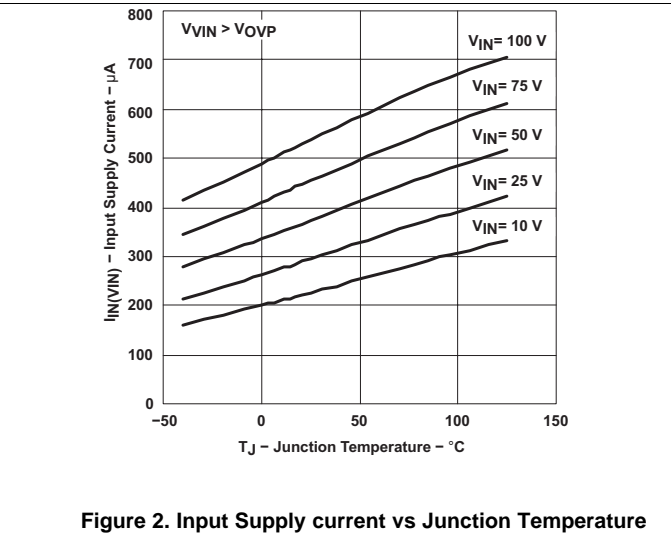
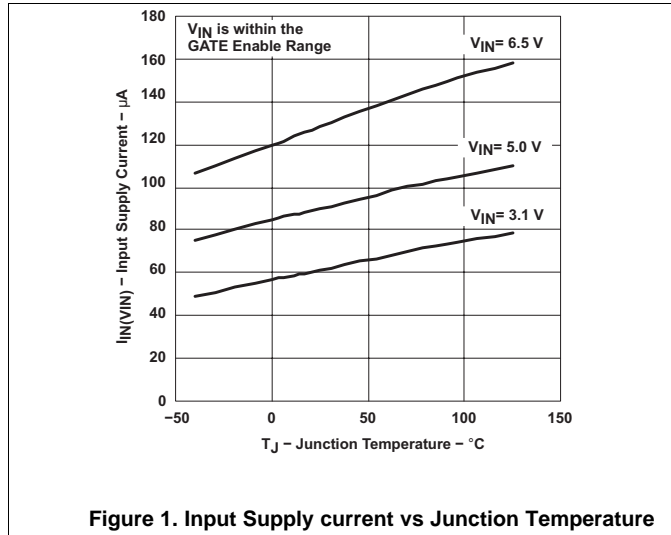
## 6.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT	
<b>INPUT</b>							
$I_{I(VIN)}$	Input supply current, $V_{IN}$	$V_{I(VIN)} = 3.1\text{ V}$		65	110	$\mu\text{A}$	
		$V_{I(VIN)} = 5\text{ V}$		95	180		
		$V_{I(VIN)} = 6.5\text{ V}$		135	220		
		$V_{I(VIN)} = 100\text{ V}$		550	1000		
$UVLO_{(upper)}$	Undervoltage lockout upper threshold	$V_{I(VIN)}$ rising	2.9	3	3.1	V	
$UVLO_{(hyst)}$	Undervoltage lockout hysteresis		85	100	115	mV	
$OVP_{(upper)}$	Overvoltage protection upper threshold	$V_{I(VIN)}$ rising	6.7	6.9	7.1	V	
$OVP_{(hyst)}$	Overvoltage protection hysteresis		135	150	165	mV	
<b>GATE DRIVE</b>							
$I_{OSOURCE(gate)}$	Gate sourcing current	$V_{I(VIN)} = 3.1\text{ V}, V_{O(gate)} = 7\text{ V}$		3		10	$\mu\text{A}$
		$V_{I(VIN)} = 5\text{ V}, V_{O(gate)} = 10\text{ V}$		3		10	
$I_{OSINK(gate)}$	Gate sinking current <sup>(1)</sup>	$V_{I(VIN)} = 7.2\text{ V}, V_{O(gate)} = 15\text{ V}$		350	485	600	mA
$V_{OH(gate)}$	Gate output high voltage	$V_{I(VIN)} = 3.1\text{ V}, I_{OSOURCE(gate)} = 1\text{ }\mu\text{A}$		10		12	V
		$V_{I(VIN)} = 5\text{ V}, I_{OSOURCE(gate)} = 1.5\text{ }\mu\text{A}$		16		19	
		$V_{I(VIN)} = 6.5\text{ V}, I_{OSOURCE(gate)} = 1.5\text{ }\mu\text{A}$		16		20	
$V_{OHMAX(gate)}$	Gate output high maximum voltage	$I_{OSOURCE(gate)} = 0\text{ }\mu\text{A}$				20	V
$V_{OL(gate)}$	Gate output low voltage	$V_{I(VIN)} = 7.2\text{ V}, I_{OSINK(gate)} = 50\text{ mA}$				1	V
$T_{ON(prop)}$	Gate turnon propagation delay, (50% $V_{I(vin)}$ to $V_{O(gate)} = 1\text{ V}$ , $R_{LOAD} = 10\text{ M}\Omega$ )	$V_{I(VIN)}$ stepped from 0 V to 5 V, $C_{LOAD} = 1\text{ nF}$		0.1		0.6	ms
		$C_{LOAD} = 10\text{ nF}$		0.9		3	
$T_{ON(rise)}$	Gate turnon rise time, ( $V_{O(gate)} = 1\text{ V}$ to 90% $V_{O(gate)}$ , $R_{LOAD} = 10\text{ M}\Omega$ )	$V_{I(VIN)}$ stepped from 0 V to 5 V, $C_{LOAD} = 1\text{ nF}$		1.5		6	ms
		$C_{LOAD} = 10\text{ nF}$		15		55	
$T_{OFF}$	Turnoff time, (50% $V_{I(VIN)}$ step to $V_{O(GATE)} = 6.9\text{ V}$ , $R_{LOAD} = 10\text{ M}\Omega$ )	$V_{I(VIN)}$ stepped from 6 V to 8 V, $C_{LOAD} = 1\text{ nF}$		5		0.25	$\mu\text{s}$
		$C_{LOAD} = 10\text{ nF}$		5		0.5	

(1) Pulse-testing techniques maintain junction temperature close to ambient temperature; thermal effects must be taken into account separately.

## 6.6 Typical Characteristics



Typical Characteristics (continued)

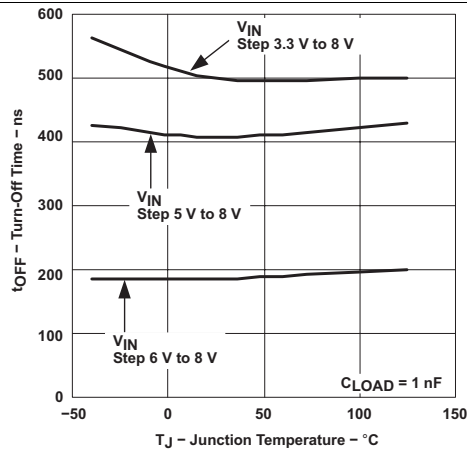


Figure 7. Turnoff Time to V<sub>GATE</sub> = 6.9 V vs Junction Temperature

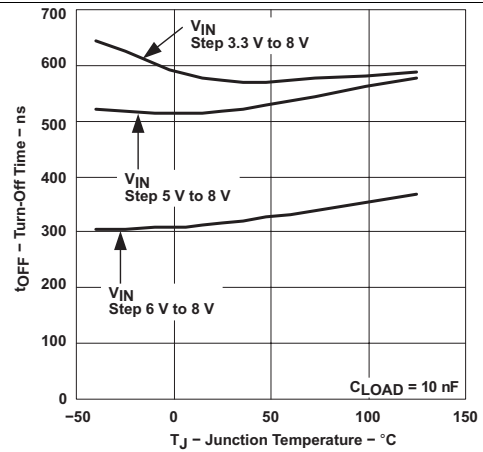


Figure 8. Turnoff Time to V<sub>GATE</sub> = 6.9 V vs Junction Temperature

## 7 Parameter Measurement Information

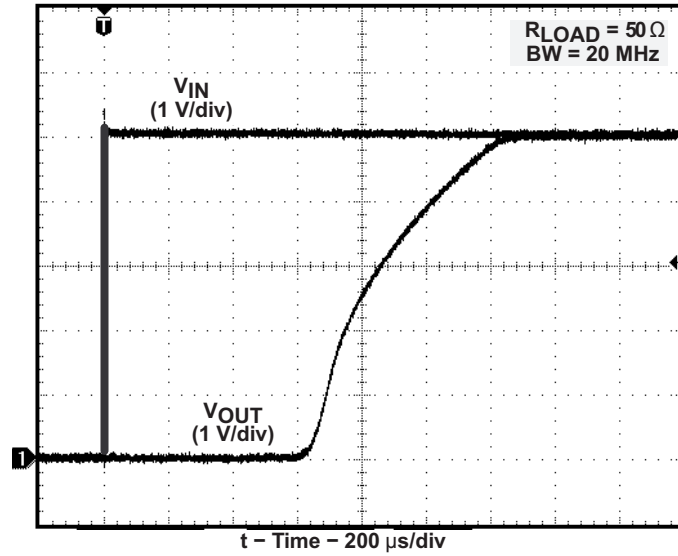


Figure 9. Output Turnon Response

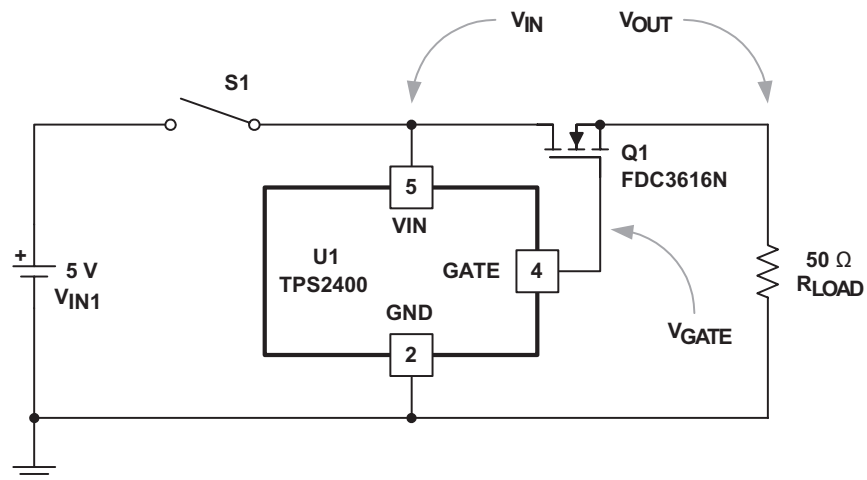


Figure 10. Output Turnon Response Test Circuit



Parameter Measurement Information (continued)

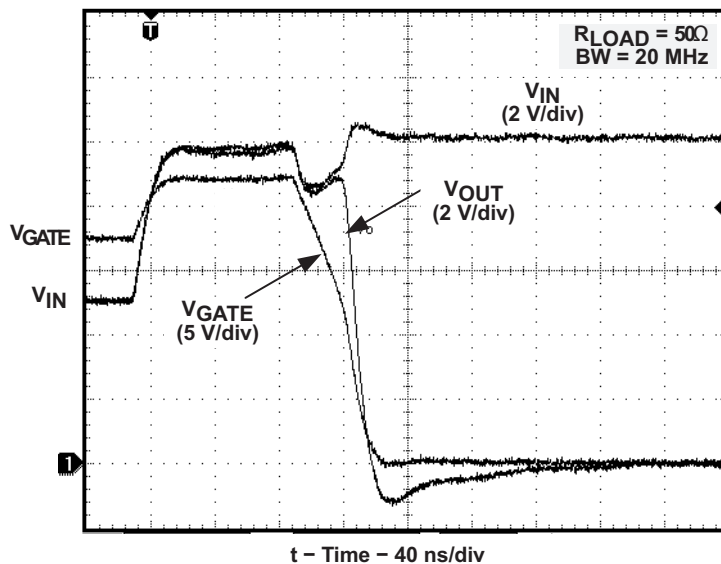


Figure 11. Output Turnoff Response

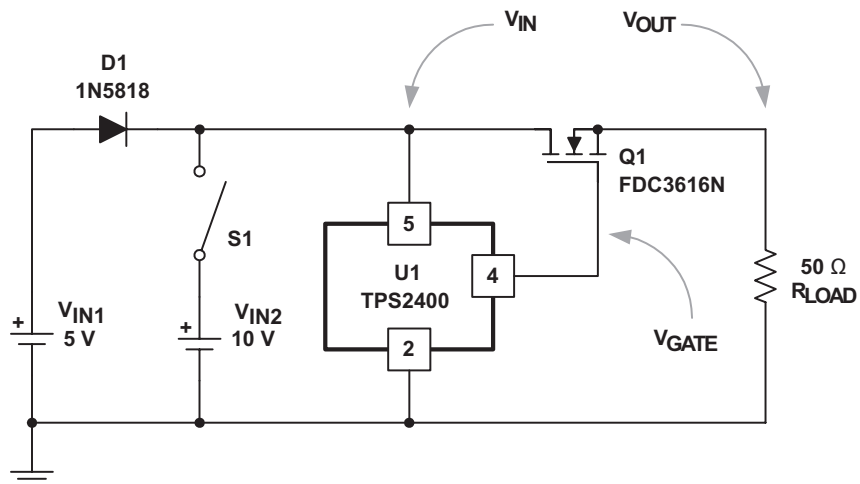


Figure 12. Output Turnoff Response Test Circuit



## Feature Description (continued)

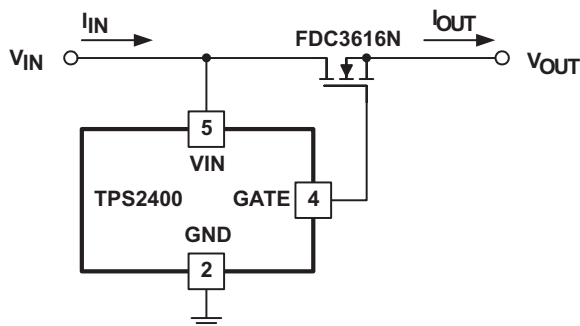


Figure 13. Application Diagram

## 8.4 Device Functional Modes

### 8.4.1 Overvoltage Protection

An overvoltage condition is commonly created in these situations:

- Unplugging a wall adapter from an AC outlet. Energy stored in the transformer magnetizing inductance is released and spikes the output voltage.
- Powering an appliance with the wrong voltage adapter (user error).
- Automotive load dump due to ignition, power windows, or starter motor (for example).
- An AC power-line transient.
- Power switch contact bounce (causes power supply/distribution inductive kick), (See [Figure 14](#)).

Many electronic appliances use a transient voltage suppressor (TVS) for overvoltage protection as shown in [Figure 14](#). The TVS is typically a metal-oxide varistor (MOV) or Transzorb. The former is a nonlinear resistor with a soft turnon characteristic whereas the latter is a large junction Zener diode with a very sharp turnon characteristic. These devices have high pulse-power capability and pico-second response time. A TVS clamps the load voltage to a safe level so the load operates uninterrupted in the presence of power supply output-voltage spikes. But in the event of a voltage surge, fuse F2 blows and must be replaced to restore operation.

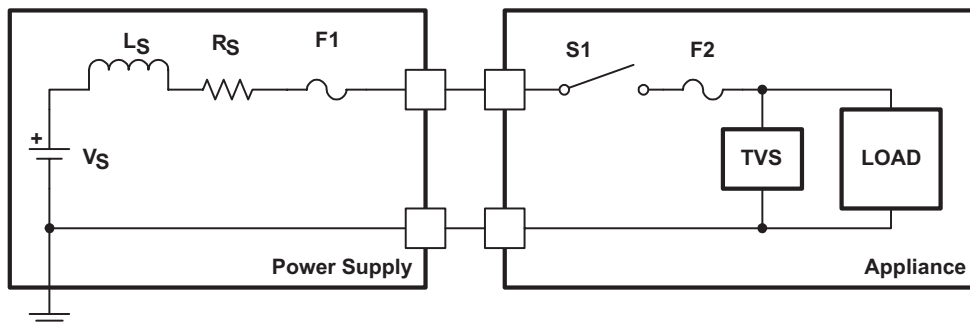


Figure 14. Load Protection Using Transient Voltage Suppressor Clamps

The TPS2400 circuit in [Figure 15](#) protects the load from an overvoltage, not by clamping the load voltage like a TVS, but by disconnecting the load from the power supply. The circuit responds to an overvoltage in less than 1  $\mu$ s and rides out a voltage surge without blowing fuse F2. The voltage surge can be of indefinite duration.

The load can see a voltage spike of up to 1  $\mu$ s, the amount of time it takes the TPS2400 to disconnect the load from the power supply. A low-power Zener diode D2 can be used to clamp the load voltage to a safe level. In most cases, diode D2 is not necessary because the load bypass capacitor (not shown) forms a low-pass filter with resistor  $R_S$  and inductor  $L_S$  to significantly attenuate the spike.

## 9 Application and Implementation

### NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

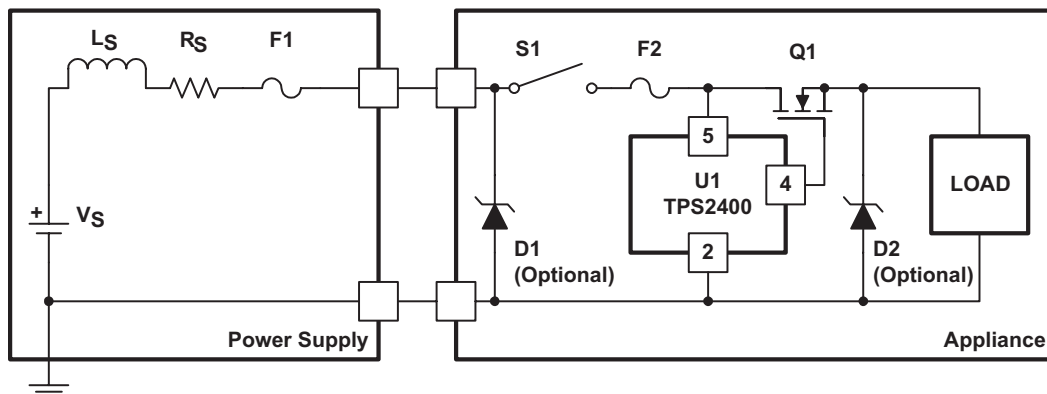
### 9.1 Application Information

The TPS2400 device provides application flexibility and can be used in many types of systems for load protection.

### 9.2 Typical Applications

#### 9.2.1 TPS2400 Application

When the TPS2400 disconnects the load from the power supply, the power-supply output-voltage spikes as the stored energy in inductor  $L_S$  is released. A Zener diode D1 or a small ceramic capacitor can be used to keep the voltage spike at a safe level.



**Figure 15. TPS2400 Application Block Diagram**

#### 9.2.1.1 Design Requirements

Table 1 shows the parameters for this design example.

**Table 1. Design Parameters**

DESIGN PARAMETERS	EXAMPLE VALUE
MOSFET Input Capacitance, $C_G$	2 nF
Load Capacitance, $C_L$	100 $\mu$ F

#### 9.2.1.2 Detailed Design Procedure

##### 9.2.1.2.1 Controlling the Load Inrush-Current

Figure 16 is a simplified representation of an appliance with a plug-in power supply (for example, wall adapter). When power is first applied to the load in Figure 16, the large filter capacitor  $C_{LOAD}$  acts like a short circuit, producing an immediate inrush-current that is limited by the power-supply output resistance and inductance,  $R_S$  and  $L_S$ , respectively. This current can be several orders of magnitude greater than the steady-state load current. The large inrush current can damage power connectors P1 and J1 and power switch S1, and stress components. Increasing the power-supply output resistance and inductance lowers the inrush current. However, the former increases system power-dissipation and the latter decreases connector and switch reliability by encouraging the contacts to arc when they bounce.

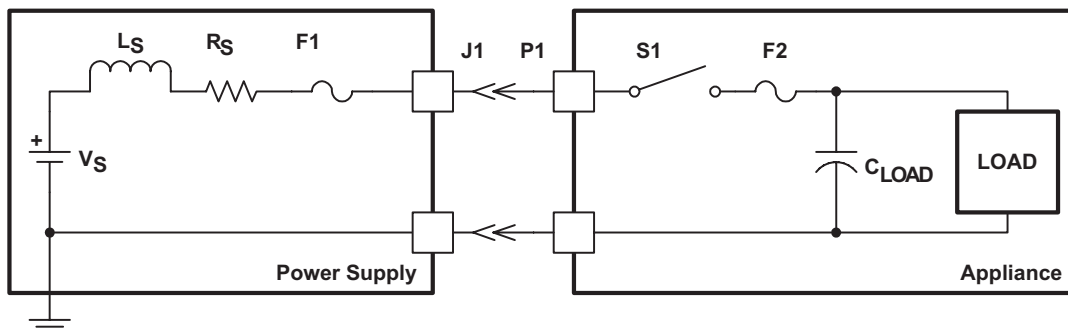


Figure 16. Power-Supply Output Resistance and Inductance Circuit Model

The TPS2400 circuit in Figure 17 limits the inrush current without these drawbacks. The TPS2400 device charges the transistor Q1 gate capacitance  $C_G$  with a  $5\text{-}\mu\text{A}$  source when Q1 is commanded to turn on. Transistor Q1 is wired as a source follower so the gate-voltage slew rate and the load-voltage slew rate are identical and equal to

$$\frac{\partial V_L}{\partial t} = \frac{5\ \mu\text{A}}{C_G} \tag{1}$$

The corresponding inrush current is:

$$I_{\text{INRUSH}} \approx C_L \times \frac{\partial V_L}{\partial t} = \left( \frac{C_L}{C_G} \right) \times 5\ \mu\text{A} \tag{2}$$

When solving Equation 1 using  $C_G = 2\ \text{nF}$ , we get  $2500\ \text{V/s}$ . Then we can use Equation 2 to approximate the inrush current of  $250\ \text{mA}$ .

An external capacitor and a series  $1\text{-k}\Omega$  resistor can be connected to the gate of Q1 and ground to reduce inrush current further. In this case, the parameter  $C_G$  in Equation 1 and Equation 2 is the sum of the internal and external FET gate capacitance. The  $1\text{-k}\Omega$  resistor decouples the external gate capacitor, so the TPS2400 device can rapidly turn off transistor Q1 in response to an overvoltage condition.

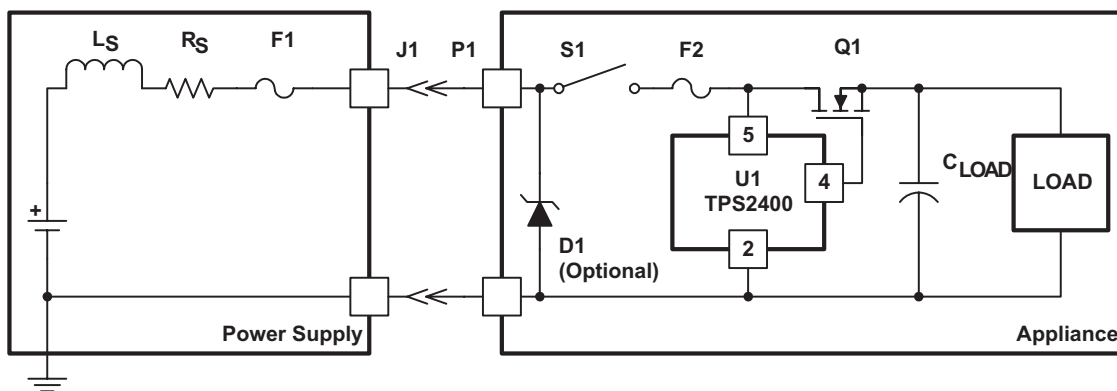


Figure 17. Turnon Voltage Slew Rate Control Using the TPS2400

### 9.2.1.3 Application Curve

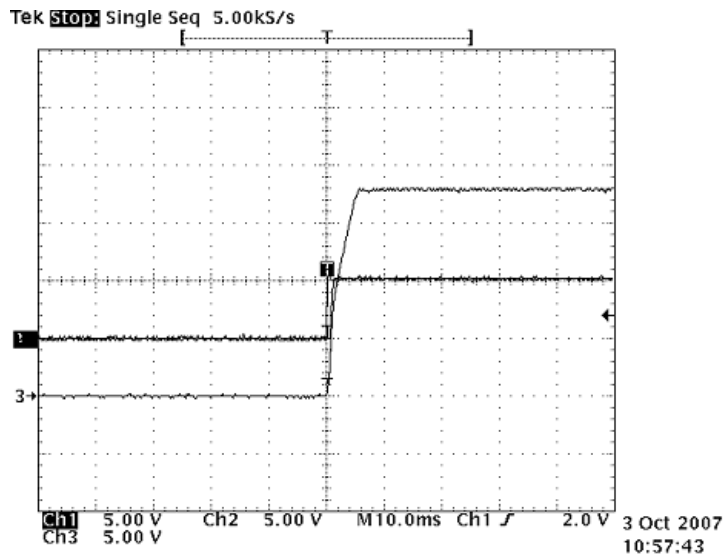


Figure 18. Circuit Start-Up With VIN = 5 V

### 9.2.2 High-Side Switch Overvoltage Protector That Can Drive a 12-V Load

Detailed information for the circuit shown in Figure 19 can be found in the application note, *Overvoltage Protector for High-Loads (SLVA163)*.

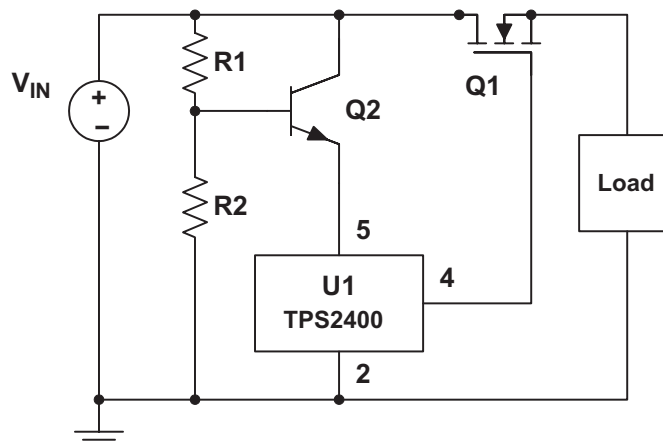


Figure 19. High-Side Switch Overvoltage Protector That Can Drive a 12-V Load

### 9.2.3 Low-Side Switch Overvoltage Protector That Can Drive a 12-V Load

Detailed information for the circuit shown in Figure 20 can be found in the application note, *Overvoltage Protector for High-Loads (SLVA163)*.

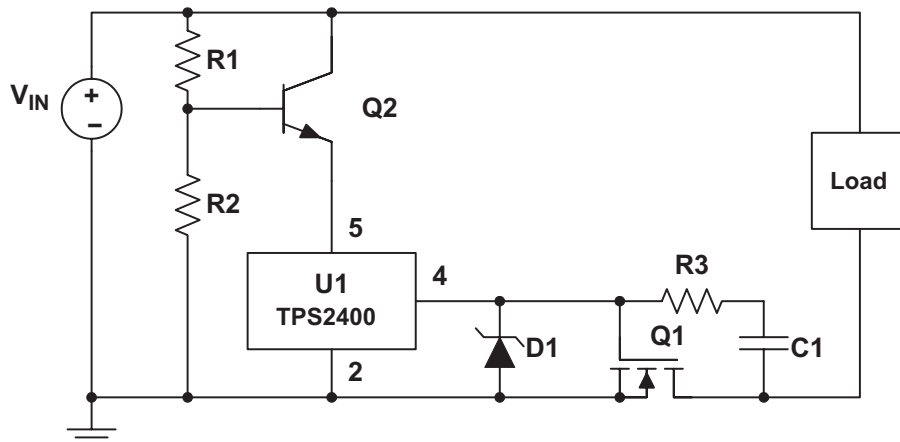


Figure 20. Low-Side Switch Overvoltage Protector That Can Drive a 12-V Load

## 10 Power Supply Recommendations

The TPS2400 device is designed to operate from 3.3-V to 5-V input supplies.  $V_{IN}$  is 100-V tolerant, but keep within the recommended steady-state operating range of 3.1 V to 6.8 V.

## 11 Layout

### 11.1 Layout Guidelines

Parts placement must be driven by power flow in a point-to-point manner from input to output. Avoid leakage paths from GATE to GND, which might load down the small GATE output current.

### 11.2 Layout Example

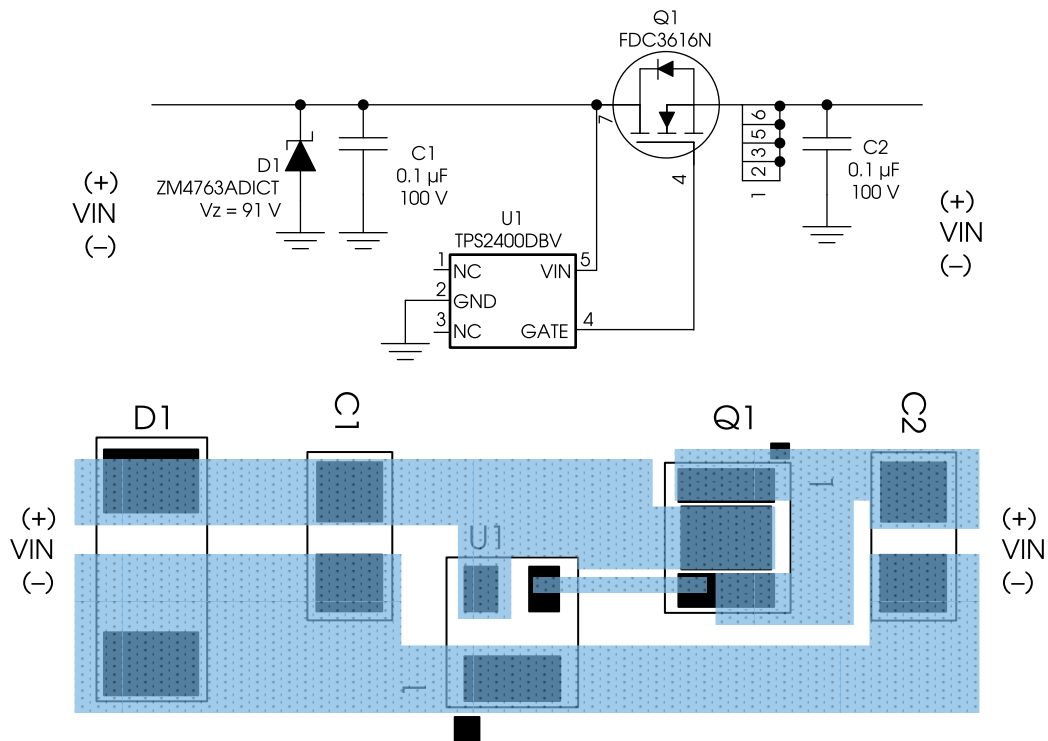


Figure 21. Suggested Layout



## 12 Device and Documentation Support

### 12.1 Documentation Support

#### 12.1.1 Related Documentation

For related documentation see the following:

*Overvoltage Protector for High-Voltage Loads*, [SLVA163](#).

### 12.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

**TI E2E™ Online Community** *TI's Engineer-to-Engineer (E2E) Community*. Created to foster collaboration among engineers. At [e2e.ti.com](#), you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

**Design Support** *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

### 12.3 Trademarks

E2E is a trademark of Texas Instruments.  
All other trademarks are the property of their respective owners.

### 12.4 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

### 12.5 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

## 13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS2400DBVR	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	BIJ	<a href="#">Samples</a>
TPS2400DBVRG4	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	BIJ	<a href="#">Samples</a>
TPS2400DBVT	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	BIJ	<a href="#">Samples</a>
TPS2400DBVTG4	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	BIJ	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSELETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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## TAPE AND REEL INFORMATION



### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS2400DBVR	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS2400DBVT	SOT-23	DBV	5	250	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS2400DBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
TPS2400DBVT	SOT-23	DBV	5	250	180.0	180.0	18.0



DBV (R-PDSO-G5)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
  - D. Publication IPC-7351 is recommended for alternate designs.
  - E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.

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