TPS27082L 1.2-V to 8-V, 3-A PFET Load Switch With Configurable Slew Rate, Fast Transient Isolation and Hysteretic Control

1 Features

- Low ON-Resistance, High Current PFET
  - $R_{ON} = 32 \, \text{m}\Omega$ (Typical) at $V_{GS} = –4.5 \, \text{V}$
  - $R_{ON} = 44 \, \text{m}\Omega$ (Typical) at $V_{GS} = –3.0 \, \text{V}$
  - $R_{ON} = 85 \, \text{m}\Omega$ (Typical) at $V_{GS} = –1.8 \, \text{V}$
  - $R_{ON} = 97 \, \text{m}\Omega$ (Typical) at $V_{GS} = –1.5 \, \text{V}$
  - $R_{ON} = 155 \, \text{m}\Omega$ (Typical) at $V_{GS} = –1.2 \, \text{V}$
- Configurable Turn-ON and Turn-OFF Slew Rate
  - 10-µs Default Minimum Output Rise Time at $\text{VIN}=5 \, \text{V}$
- Configurable Turnon and Turnoff Slew Rate
- Supports a Wide Range of VIN 1.2 V Up to 8 V
- Excellent OFF Isolation Even Under Fast Input Transients
- 1.0V up to 8V NMOS Control Logic Interface With Configurable Hysteresis
- Fully Protected Against ESD (All Pins)
  - HBM 2000 V, CDM 500 V
- Very Low ON-state Quiescent Current (Down to 1.2 µA)
- Very Low OFF-state Leakage Current (Typical 100 nA)
- Available in 2.9 mm × 1.6 mm x 0.75mm SOT-23 (DDC) Package

2 Applications

- High-Side Load Switches
- Inrush-current Controls
- Power Sequencing and Controls
- Stand-by Power Isolation
- Portable Power Switches

3 Description

The TPS27082L IC is a high-side load switch that integrates a Power PFET and a control circuit in a tiny TSOT-23 package. TPS27082L requires very low ON-state quiescent current and offers very low OFF-state leakage thus optimizing system power efficiency.

TPS27082L ON/OFF logic interface features hysteresis, thus providing a robust logic interface even under very noisy operating conditions. TPS27082L ON/OFF interface supports direct interfacing to low voltage GPIOs down to 1 V. The TPS27082L level shifts ON/OFF logic signal to VIN levels without requiring an external level shifter.

TPS27082L features a novel OFF isolation circuit that prevents PMOS from turning ON in applications that may have fast transients, at the VIN pin when the load switch is in the OFF-state.

Device Information

<table>
<thead>
<tr>
<th>PART NUMBER</th>
<th>PACKAGE</th>
<th>BODY SIZE (NOM)</th>
</tr>
</thead>
<tbody>
<tr>
<td>TPS27082DDC</td>
<td>SOT (6)</td>
<td>2.90 mm × 1.60 mm</td>
</tr>
</tbody>
</table>

(1) For all available packages, see the orderable addendum at the end of the data sheet.
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4 Revision History
NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision B (September 2013) to Revision C Page

• Added Pin Configuration and Functions section, Storage Conditions table, ESD Ratings table, Feature Description section, Device Functional Modes, Application and Implementation section, Power Supply Recommendations section, Layout section, Device and Documentation Support section, and Mechanical, Packaging, and Orderable Information section ................................................................. 1

Changes from Revision A (April 2013) to Revision B Page

• Removed Ordering Information table. ................................................ 1
• Fixed UNIT typo for ON/OFF input logic hysteresis PARAMETER.................................................................................. 5

Changes from Original (December 2012) to Revision A Page

• Updated wording in the document.................................................. 1
5 Pin Configuration and Functions

Pin Functions

<table>
<thead>
<tr>
<th>PIN</th>
<th>I/O</th>
<th>NAME</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>GND</td>
<td>I</td>
<td>1</td>
<td>Connect to the system GND</td>
</tr>
<tr>
<td>VOUT</td>
<td>O</td>
<td>2</td>
<td>Drain Terminal of Power PFET (Q1) – If required, connect a slew control capacitor between pins VOUT and R1/C</td>
</tr>
<tr>
<td></td>
<td>I</td>
<td>3</td>
<td>Source Terminal of Power PFET (Q1) – connect a pull-up resistor between the pins VIN and R1/C</td>
</tr>
<tr>
<td>VIN</td>
<td>I</td>
<td>4</td>
<td>Active high enable – when driven with a high impedance driver, connect an external pull down resistor to GND</td>
</tr>
<tr>
<td>ON/OFF</td>
<td>I</td>
<td>5</td>
<td>Gate Terminal of Power PFET (Q1)</td>
</tr>
<tr>
<td>R1/C1</td>
<td>I</td>
<td>6</td>
<td></td>
</tr>
</tbody>
</table>

DDC Package
6-Pin SOT
Top View
6 Specifications

6.1 Absolute Maximum Ratings
Specified at $T_J = -40\,^\circ C$ to 125$^\circ C$ (unless otherwise noted)

<table>
<thead>
<tr>
<th>Specification</th>
<th>MIN</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{IN_{\text{max}}}$, $V_{OUT_{\text{max}}}$</td>
<td>$-0.1$</td>
<td>$8$</td>
<td>V</td>
</tr>
<tr>
<td>$V_{\text{ON/OFF}}$</td>
<td>$-0.3$</td>
<td>$8$</td>
<td>V</td>
</tr>
<tr>
<td>$I_{Q1-\text{ON}}$</td>
<td>$3$</td>
<td></td>
<td>A</td>
</tr>
<tr>
<td>$I_{Q1-\text{pul}}$</td>
<td></td>
<td>$9.5$</td>
<td></td>
</tr>
<tr>
<td>$P_D$</td>
<td>$1190$</td>
<td></td>
<td>mW</td>
</tr>
<tr>
<td>$T_A$</td>
<td>$-40$</td>
<td>$125$</td>
<td>$^\circ C$</td>
</tr>
<tr>
<td>$T_{J_{\text{max}}}$</td>
<td></td>
<td>$150$</td>
<td>$^\circ C$</td>
</tr>
<tr>
<td>$T_{stg}$</td>
<td>$-65$</td>
<td>$150$</td>
<td>$^\circ C$</td>
</tr>
</tbody>
</table>

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) Operating at the absolute $T_{J_{\text{max}}}$ of 150$^\circ C$ can affect reliability – for higher reliability it is recommended to ensure $T_J < 125^\circ C$

(3) Refer to TI's design support web page at www.ti.com/thermal for improving device thermal performance.

(4) Pulse Width < 300µs, Duty Cycle < 2%

(5) $T_{J_{\text{max}}}$ limits and other related conditions apply. Refer to SOA charts, Figure 8 through Figure 13

6.2 ESD Ratings

<table>
<thead>
<tr>
<th>ESD</th>
<th>VALUE</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{\text{ESD}}$</td>
<td>±2000</td>
<td>V</td>
</tr>
<tr>
<td>$V_{\text{CH}}$</td>
<td>±500</td>
<td>V</td>
</tr>
</tbody>
</table>

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

<table>
<thead>
<tr>
<th>Specification</th>
<th>MIN</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{IN}$</td>
<td>$1$</td>
<td>$8$</td>
<td>V</td>
</tr>
<tr>
<td>$T_A$</td>
<td>$-40$</td>
<td>$85$</td>
<td>$^\circ C$</td>
</tr>
<tr>
<td>$T_J$</td>
<td>$-40$</td>
<td>$105$</td>
<td>$^\circ C$</td>
</tr>
</tbody>
</table>

6.4 Thermal Information

<table>
<thead>
<tr>
<th>THERMAL METRIC$^{(1)}$</th>
<th>TPS27082L</th>
</tr>
</thead>
<tbody>
<tr>
<td>$R_{JUA}$</td>
<td>Junction-to-ambient thermal resistance</td>
</tr>
<tr>
<td>$R_{JUC(top)}$</td>
<td>Junction-to-case (top) thermal resistance</td>
</tr>
<tr>
<td>$R_{JUB}$</td>
<td>Junction-to-board thermal resistance</td>
</tr>
<tr>
<td>$\Psi_{JT}$</td>
<td>Junction-to-top characterization parameter</td>
</tr>
<tr>
<td>$\Psi_{JB}$</td>
<td>Junction-to-board characterization parameter</td>
</tr>
<tr>
<td>$R_{JUC(bot)}$</td>
<td>Junction-to-case (bottom) thermal resistance</td>
</tr>
</tbody>
</table>

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report, SPRA953.
### 6.5 Electrical Characteristics

Full temperature range spans \( T_J = -40^\circ C \) to 125°C (unless otherwise noted)

#### OFF CHARACTERISTICS

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>( T_A = T_J = 25^\circ C )</th>
<th>FULL TEMP RANGE(^{(1)})</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>( V_{ON/OFF} )</td>
<td>( V_{ON/OFF} = 0 ) V, ( VGS(Q1) = 0 ) V, ( ID(Q1) = 250 ) µA</td>
<td>(-8)</td>
<td>( -8 )</td>
<td>V</td>
</tr>
<tr>
<td>( I_{FN} )</td>
<td>( V_{ON/OFF} = 0 ) V, ( RL = 2.5 ) Ω</td>
<td>( 0.15 )</td>
<td>( 30 )</td>
<td>µA</td>
</tr>
<tr>
<td></td>
<td>( V_{ON/OFF} = 0 ) V, ( RL = 2.5 ) Ω</td>
<td>( 0.04 )</td>
<td>( 12 )</td>
<td></td>
</tr>
</tbody>
</table>

#### ON CHARACTERISTICS\(^{(3)}\)

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>( T_A = T_J = 25^\circ C )</th>
<th>FULL TEMP RANGE(^{(1)})</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>( V_{T+} ) Positive going ON/OFF threshold voltage(^{(4)})</td>
<td>( VIN = 5.0 ) V, ( R1 = 125 ) kΩ, ( RL = 2.5 ) Ω</td>
<td>( 1.0 )</td>
<td>( 730 )</td>
<td>mV</td>
</tr>
<tr>
<td>( V_{T–} ) Negative going ON/OFF threshold voltage(^{(4)})</td>
<td>( VIN = 5.0 ) V, ( ID(Q1) &lt; 175 ) µA, ( R1 = 125 ) kΩ(^{(1)})</td>
<td>( 400 )</td>
<td>( 270 )</td>
<td>mV</td>
</tr>
<tr>
<td>( \Delta V_T ) ON/OFF input logic hysteresis(^{(4)})</td>
<td>( VIN = 5.0 ) V, ( R1 = 1 ) MΩ</td>
<td>( 600 )</td>
<td>( 300 )</td>
<td>mV</td>
</tr>
</tbody>
</table>

#### Q1 Channel ON resistance\(^{(5)}\)

<table>
<thead>
<tr>
<th>( R_{Q1(ON)} )</th>
<th>Q1 Channel ON resistance ( R_{Q1(ON)} )</th>
<th>( VGS_{Q1} = -4.5V, ID = 3.0 ) A</th>
<th>( 32 )</th>
<th>( 64 )</th>
<th>mΩ</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>( VGS_{Q1} = -3.0V, ID = -2.5 ) A</td>
<td>( 44 )</td>
<td>( 84 )</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>( VGS_{Q1} = -2.5V, ID = 2.5 ) A</td>
<td>( 50 )</td>
<td>( 76 )</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>( VGS_{Q1} = -1.8V, ID = 2.0 ) A</td>
<td>( 82 )</td>
<td>( 113 )</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>( VGS_{Q1} = -1.5V, ID = 1.0 ) A</td>
<td>( 97 )</td>
<td>( 150 )</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>( VGS_{Q1} = -1.2V, ID = 0.50 ) A</td>
<td>( 155 )</td>
<td>( 250 )</td>
<td></td>
</tr>
</tbody>
</table>

#### Q1 DRAIN-SOURCE DIODE PARAMETERS\(^{(1)}\)(\(^{(3)}\))(\(^{(6)}\))

<table>
<thead>
<tr>
<th>IFSD</th>
<th>Source-drain diode peak forward current</th>
<th>( V_{SD(Q1)} = 0.8V ), ( VON/OFF = 0 ) V</th>
<th>( 1 )</th>
<th>A</th>
</tr>
</thead>
<tbody>
<tr>
<td>VFS</td>
<td>Source-drain forward voltage</td>
<td>( IFSD(Q1) = -0.6A ), ( VON/OFF = 0 ) V</td>
<td>( 1.0 )</td>
<td>V</td>
</tr>
</tbody>
</table>

(1) Specified by design only
(2) Refer to \( I_{VFIN} \) plots for more information
(3) Pulse width < 300µs, Duty cycle < 2%
(4) Refer to charts for more information on \( V_{T+}/V_{T–} \) thresholds
(5) Refer to SOA charts for operating current information
(6) Not rated for continuous current operation

### 6.6 Dissipation Ratings

See \(^{(1)}\)(\(^{(2)}\)(\(^{(3)}\)).

<table>
<thead>
<tr>
<th>BOARD</th>
<th>PACKAGE</th>
<th>( R_{JC} )</th>
<th>( R_{JA} )((^{(4)}))</th>
<th>( T_A &lt; 25^\circ C )</th>
<th>( T_A = 70^\circ C )</th>
<th>( T_A = 85^\circ C )</th>
<th>( T_A = 105^\circ C )</th>
<th>DERATING FACTOR ( ABOVE T_A = 25^\circ C )</th>
</tr>
</thead>
<tbody>
<tr>
<td>High-K</td>
<td>6-Pin TSOT</td>
<td>43°C/W</td>
<td>105°C/W</td>
<td>1190 mW</td>
<td>760 mW</td>
<td>619 mW</td>
<td>428 mW</td>
<td>9.55 mW/°C</td>
</tr>
</tbody>
</table>

(1) Maximum dissipation values for retaining a maximum allowable device junction temperature of 150°C
(2) Refer to TI’s design support web page at www.ti.com/thermal for improving device thermal performance
(3) Package thermal data based on a 76x114x1.6mm, 4-layer board with 2-oz Copper on outer layers
(4) Operating at the absolute \( T_J \) max of 150°C can affect reliability; \( T_J \leq 125^\circ C \) is recommended
6.7 Typical Characteristics

Figure 1. Vdrop vs IL; VGS_Q1 = –1.2 V

Figure 2. Vdrop vs IL; VGS_Q1 = –1.8 V

Figure 3. Vdrop vs IL; VGS_Q1 = –2.5 V

Figure 4. Vdrop vs IL; VGS_Q1 = –3.3 V

Figure 5. Vdrop vs IL; VGS_Q1 = –4.5 V

Figure 6. Vdrop vs IL; VGS_Q1 = –5.5 V
Typical Characteristics (continued)

6.7.1 PFET Q1 Minimum Safe Operating Area (SOA)
(Refer to Dissipation Ratings for PCB details)

Figure 7. Vdrop vs IL; VGS_Q1 = -7 V

Figure 8. Q1 SOA at VGS_Q1=-4.5V

Figure 9. Q1 SOA at VGS_Q1=-3.0V

Figure 10. Q1 SOA at VGS_Q1=-2.5V

Figure 11. Q1 SOA at VGS_Q1=-1.8V
PFET Q1 Minimum Safe Operating Area (SOA) (continued)

(Refer to Dissipation Ratings for PCB details)

Figure 12. Q1 SOA at VGS_Q1=-1.5V

Figure 13. Q1 SOA at VGS_Q1=-1.2V

Figure 14. ON/OFF Positive and Negative Going Threshold Voltage
7 Detailed Description

7.1 Overview
The TPS27082L IC is a high side load switch that integrates a Power PFET and its control circuit in a tiny TSOT-23 package. TPS27082L supports up to 8V supply input and up to 3A of load current. The TPS27082L can be used in a variety of applications. The device has a programmable slew rate which helps reduce or eliminate power supply droop due to large inrush currents. During shutdown, the device has very low leakage currents.

7.2 Functional Block Diagram

7.3 Feature Description
TPS27082L uses a low-voltage power PMOS transistor used as the pass element or switch between the supply and load. It also integrates an NMOS transistor to turn the PMOS on and off by interfacing with a wide range of GPIO voltages. Asserting an input voltage higher than Vih (1V) enables the PMOS switch by turning the NMOS and the NMOS driving the PMOS gate towards ground. Series resistance of 12.5 kΩ connected at the source of NPN is integrated for TPS27082L. To control output rise time is programmed by connecting external capacitor at pin 6 of the device to design a delay time for PMOS to turn on.

7.4 Device Functional Modes

7.4.1 ON/OFF
When Vin > about 1 V and V(ON/OFF) > 1 V, the switch will turn on and Vout ≈ Vin.
When Vin > about 1 V and V(ON/OFF) < 1 V, the switch will turn off and Vout ≠ Vin.

7.4.2 Fastest Output Rise Time
Whenever it is desired to achieve the fastest output rise time, do not put a capacitor between Vout (Pins 2 and 3) and R1/C1 (pin 6).

7.4.3 Controlled Output Rise Time
Whenever it is desired to control the output rise time, tie pin 1 (R2) to a resistance (R2) and put a capacitor (C1) between Vout (Pins 2 and 3) and R1/C1 (pin 6).
8 Application and Implementation

NOTE
Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI’s customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information
The TPS27082L IC is a high side load switch that integrates a Power PFET and a Control NMOS in a tiny package. The TPS27082L internal components are rated for up to 8V supply and support up to 3A of load current.

8.2 Typical Application
The TPS27082L can be used in a variety applications. Figure 15 shows a general application of TPS27082L to control the load inrush current. This section will highlight some of the design considerations when implementing this device in various applications.

8.2.1 Design Requirements
Add an external pullup resistor R1 between VIN and R1/C1 to control the ON-resistance of the load switch. Guidelines for sizing R1 can be found in Configuring Q1 ON-Resistance. In addition, TI recommends an output capacitor at VOUT to minimize the impact of inrush current from instantaneous switching. See Configuring Turnon Slew Rate for details regarding capacitor sizing.

8.2.2 Detailed Design Procedure
8.2.2.1 Configuring Q1 ON-Resistance
\[ V_{GS-Q1} = -V_{IN} \times \frac{R1}{R1 + 12.5 \, k\Omega} \] (1)
For example, R1 = 125 k\(\Omega\), VIN = 5 V sets \(V_{GS-Q1} = -4.5 V\)
Typical Application (continued)

NOTE
It is recommended to keep \( R1 \geq 125 \, \text{kΩ} \). Higher value resistor \( R1 \) reduces ON-state quiescent current, increases turn-OFF delay, while reducing ON/OFF negative going threshold voltage \( V_{T-} \).

8.2.2.2 Configuring Turnon Slew Rate

Switching a large capacitive load \( CL \) instantaneously results in a load inrush current given by the following equation:

\[
I_{\text{inrush}} = C_{\text{load}} \times \frac{dV}{dt} = C_{\text{load}} \times \frac{V_{\text{OUTfinal}} - V_{\text{OUTinitial}}}{\text{Vout Slew Rate}}
\]

An uncontrolled fast rising ON/OFF logic input may result in a high slew rate \((dV/dt)\) at the output thus leading to a higher load inrush current. To control the inrush current connect a capacitor \( C1 \) as shown in the Figure 15. Use the following approximate empirical equation to configure the TPS27082L slew rate to a specific value.

\[
t_{\text{rise}} = \frac{50 \times 10^3 \times C1}{\text{VIN}^{2/3}} \text{ sec}
\]

where

- \( t_{\text{rise}} \) is the time delta starting from the ON/OFF signal’s rising edge to charge up the load capacitor \( CL \) from 10% to 90% of \( \text{VIN} \) voltage

Table 1. Capacitor C1 Selection for Standard Output Rise Time

<table>
<thead>
<tr>
<th>( t_{\text{rise}} ) (µSec) (Typical)</th>
<th>C1 (F) ( R1 = 125 , \text{kΩ} )</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>VIN=7V</td>
</tr>
<tr>
<td>5</td>
<td>0</td>
</tr>
<tr>
<td>50</td>
<td>3.46n</td>
</tr>
<tr>
<td>100</td>
<td>6.91n</td>
</tr>
<tr>
<td>250</td>
<td>17.3n</td>
</tr>
<tr>
<td>470</td>
<td>32.5n</td>
</tr>
<tr>
<td>1000</td>
<td>69.1n</td>
</tr>
</tbody>
</table>

NOTE
The \( t_{\text{rise}} \) equation and the capacitor \( C1 \) values recommended in the table above are under typical conditions and are accurate to within ±20%. Ensure \( R1 > 125kΩ \); and select a closest standard valued capacitor \( C1 \).

8.2.2.3 Configuring Turnoff Delay

TPS27082L PMOS turnoff delay from the falling edge of ON/OFF logic signal depends upon the component values of resistor \( R1 \) and capacitor \( C1 \). Lower values of resistor \( R1 \) ensures quicker turnoff.

\[
t_{\text{off}} > (R1 \times C1 \text{ sec})
\]

8.2.2.4 OFF Isolation Under VIN Transients

TPS27082L architecture helps isolate fast transients at the VIN when PFET is in the OFF state. Best transient isolation is achieved when an external capacitor \( C1 \) is not connected across VOUT and R1/C1 pins. When a capacitor \( C1 \) is present the VIN to VOUT coupling is capacitive and is set by the \( C1 \) to \( CL \) capacitance ratio. TPS27082L architecture prevents direct conduction through PFET.
8.2.2.5 Low Voltage ON/OFF Interface

To turn on the load switch apply a voltage > 1.0 V at the ON/OFF pin. The TPS27082L features hysteresis at its ON/OFF input. The turnon and turnoff thresholds are dependent upon the value of resistor R1. Refer to the Electrical Characteristics table and Figure 14 for details on the positive and negative going ON/OFF thresholds.

In applications where ON/OFF signal is not available connect ON/OFF pin to the VIN pin. The TPS27082L will turn ON and OFF in sync with the input supply connected to VIN.

8.2.2.6 On-Chip Power Dissipation

Use below approximate equation to calculate TPS27082L’s on-chip power dissipation $P_D$:

$$ P_D = I_{DQ1}^2 \times R_{Q1(ON)} $$

where

- $I_{DQ1}$ is the DC current flowing through the transistor Q1

Refer to Electrical Characteristics table and the Figure 1 through Figure 7 to estimate $R_{Q1(ON)}$ for various values of VGSQ1.

Note: MOS switches can get extremely hot when operated in saturation region. As a general guideline, to avoid transistors Q1 going into saturation region set $VGS > VDS + 1.0$ V. E.g. $VGS > 1.5$ V and $VDS < 200mV$ ensures switching region.

8.2.3 Application Curve

![Figure 16. VIN Pin Leakage Current](image-url)
8.3 System Examples

8.3.1 TFT LCD Module Inrush Current Control

LCD panels require inrush current control to prevent permanent system damages during turn-ON and turn-OFF events.

8.3.2 Standby Power Isolation

Many applications have some always ON modules to support various core functions. However, some modules are selectively powered ON or OFF to save power and multiplexing of various on board resources. Such modules that are selectively turned ON or OFF require standby power generation. In such applications TPS27082L requires only a single pull-up resistor. In this configuration the VOUT voltage rise time is approximately 250ns when VIN = 5V.

8.3.3 Boost Regulator With True Shutdown

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System Examples (continued)

The most common boost regulator topology provides a current leakage path through inductor and diode into the feedback resistor even when the regulator is shut down. Adding a TPS27082L in the input side power path prevents this leakage current and thus providing a true shutdown.

8.3.4 Single Module Multiple Power Supply Sequencing

![Diagram of a single module multiple power supply sequencing](image)

Figure 20. Power Sequencing Using TPS27082L, Example 1

Most modern SOCs and CPUs require multiple voltage inputs for its Analog, Digital cores and IO interfaces. These ICs require that these supplies be applied simultaneously or in a certain sequence. TPS27082L when configured, as shown in Figure 20, with the VOUT1 rise time adjusted appropriately through resistor R2 and capacitor C1, will delay the early arriving LDO output to match up with late arriving DC-DC output and thus achieving power sequencing.

8.3.5 Multiple Modules Interdependent Power Supply Sequencing

![Diagram of multiple modules interdependent power supply sequencing](image)

Figure 21. Power Sequencing Using TPS27082L, Example 2

For system integrity reasons a certain power sequencing may be required among various modules. As shown in Figure 21, Module 2 will power up only after Module 1 is powered up and the Module 1 GPIO output is enabled to turn ON Module 2. TPS27082L when used as shown in Figure 21 will not only sequence the Module 2 power, but also it will help prevent inrush current into the power path of Module 1 and 2.
System Examples (continued)

8.3.6 Multiple Modules Interdependent Supply Sequencing Without a GPIO Input

When a GPIO signal is not available connecting the ON/OFF pin of TPS27082 connected to Module 2 will power up Module 2 after Module 1, when resistor R4 and capacitor C1 are chosen appropriately. The two TPS27082L in this configuration will also control load inrush current.
9 Power Supply Recommendations

The device is designed to operate from a VIN range of 1.0 V to 8.0 V. This supply must be well regulated and placed as close to the device terminal as possible with the recommended 1-μF bypass capacitor. If the supply is located more than a few inches from the device terminals, additional bulk capacitance may be required in addition to the ceramic bypass capacitors. If additional bulk capacitance is required, an electrolytic, tantalum, or ceramic capacitor of 1 μF may be sufficient.

10 Layout

10.1 Layout Guidelines

For best operational performance of the device, use good PCB layout practices, including:

- VIN and VOUT traces should be as short and wide as possible to accommodate for high current.
- The VIN pin should be bypassed to ground with low ESR ceramic bypass capacitors. The typical recommended bypass capacitance is 1-μF ceramic with X5R or X7R dielectric. This capacitor should be placed as close to the device pins as possible.
- The VOUT pin should be bypassed to ground with low ESR ceramic bypass capacitors. The typical recommended bypass capacitance is one-tenth of the VIN bypass capacitor of X5R or X7R dielectric rating. This capacitor should be placed as close to the device pins as possible.

10.2 Layout Example

![Layout Diagram](image-url)
10.3 Thermal Considerations

For higher reliability it is recommended to limit TPS27082L IC’s die junction temperature to less than 125°C. The IC junction temperature is directly proportional to the on-chip power dissipation. Use the following equation to calculate maximum on-chip power dissipation to restrict the die junction temperature target to safe limits:

\[
PD_{(MAX)} = \frac{T_{J(MAX)} - T_A}{\theta_{JA}}
\]

where

- \(T_{J(MAX)}\) is the target maximum junction temperature,
- \(T_A\) is the operating ambient temperature,
- and \(R_{θJA}\) is the package junction to ambient thermal resistance. (6)

10.3.1 Improving Package Thermal Performance

The package \(R_{θJA}\) value under standard conditions on a High-K board is available in Dissipation Ratings. \(R_{θJA}\) value depends upon the PCB layout. An external heat sink and/or a cooling mechanism like a cold air fan can help reduce \(R_{θJA}\) and thus improving device thermal capability. Refer to TI’s design support web page at www.ti.com/thermal for a general guidance on improving device thermal performance.
11 Device and Documentation Support

11.1 Community Resources
The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

**TI E2E™ Online Community** *TI's Engineer-to-Engineer (E2E) Community.* Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

**Design Support** *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.2 Trademarks
E2E is a trademark of Texas Instruments. All other trademarks are the property of their respective owners.

11.3 Electrostatic Discharge Caution

![Electrostatic Discharge Icon]

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.4 Glossary

**SLYZ022 — Ti Glossary.**

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.
## PACKAGING INFORMATION

<table>
<thead>
<tr>
<th>Orderable Device</th>
<th>Status (1)</th>
<th>Package Type</th>
<th>Package Drawing</th>
<th>PIns</th>
<th>Package Qty</th>
<th>Eco Plan (2)</th>
<th>Lead/Ball Finish (6)</th>
<th>MSL Peak Temp (3)</th>
<th>Op Temp (°C)</th>
<th>Device Marking (4/5)</th>
<th>Samples</th>
</tr>
</thead>
<tbody>
<tr>
<td>TPS27082LDDCR</td>
<td>NRND</td>
<td>SOT-23-THIN</td>
<td>DDC</td>
<td>6</td>
<td>3000</td>
<td>Green (RoHS &amp; no Sb/Br)</td>
<td>CU SN</td>
<td>Level-1-260C-UNLIM</td>
<td>-40 to 125</td>
<td>BUA</td>
<td></td>
</tr>
</tbody>
</table>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) **MSL, Peak Temp.** - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "--" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) **Lead/Ball Finish** - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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## TAPE AND REEL INFORMATION

### TAPE DIMENSIONS

<table>
<thead>
<tr>
<th>A0</th>
<th>Dimension designed to accommodate the component width</th>
</tr>
</thead>
<tbody>
<tr>
<td>B0</td>
<td>Dimension designed to accommodate the component length</td>
</tr>
<tr>
<td>K0</td>
<td>Dimension designed to accommodate the component thickness</td>
</tr>
<tr>
<td>W</td>
<td>Overall width of the carrier tape</td>
</tr>
<tr>
<td>P1</td>
<td>Pitch between successive cavity centers</td>
</tr>
</tbody>
</table>

### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

```
  Q1  Q2
  Q3  Q4
  S1  S2
  .   .
```

*All dimensions are nominal*

<table>
<thead>
<tr>
<th>Device</th>
<th>Package Type</th>
<th>Package Drawing</th>
<th>Pins</th>
<th>SPQ</th>
<th>Reel Diameter</th>
<th>Reel Width W1</th>
<th>A0</th>
<th>B0</th>
<th>K0</th>
<th>P1</th>
<th>W</th>
<th>Pin1 Quadrant</th>
</tr>
</thead>
<tbody>
<tr>
<td>TPS27082LDDCR</td>
<td>SOT-23-THIN</td>
<td>DDC</td>
<td>6</td>
<td>3000</td>
<td>180.0</td>
<td>9.5</td>
<td>3.17</td>
<td>1.1</td>
<td>4.0</td>
<td>8.0</td>
<td>Q3</td>
<td></td>
</tr>
</tbody>
</table>
**TAPE AND REEL BOX DIMENSIONS**

<table>
<thead>
<tr>
<th>Device</th>
<th>Package Type</th>
<th>Package Drawing</th>
<th>Pins</th>
<th>SPQ</th>
<th>Length (mm)</th>
<th>Width (mm)</th>
<th>Height (mm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>TPS27082LDDCR</td>
<td>SOT-23-THIN</td>
<td>DDC</td>
<td>6</td>
<td>3000</td>
<td>184.0</td>
<td>184.0</td>
<td>19.0</td>
</tr>
</tbody>
</table>

*All dimensions are nominal*
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
NOTES: (continued)

4. Publication IPC-7351 may have alternate designs.
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
7. Board assembly site may have different recommendations for stencil design.
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