TPS779-Q1, TPS780-Q1

TPS37xx-Q1

Dual-Channel, Low-Power, High-Accuracy Voltage Detectors

1 Features
- Qualified for Automotive Applications
- AEC-Q100 Qualified With the Following Results:
  - Device Temperature Grade 1: –40°C to 125°C
  - Ambient Operating Temperature Range
  - Device HBM ESD Classification Level H2
  - Device CDM ESD Classification Level C4B
- Two-Channel Detectors in Small Packages
- High-Accuracy Threshold and Hysteresis: 1.0%
- Low Quiescent Current: 2 µA (typ)
- Adjustable Detection Voltage Down to 1.2 V
- 5% and 10% Hysteresis Options
- Temperature Range: –40°C to +125°C
- Push-Pull (TPS3779-Q1) and Open-Drain (TPS3780-Q1) Output Options
- Available in an SOT-23 Package

2 Applications
- DSPs, Microcontrollers, and Microprocessors
- Advanced Driver Assistance Systems (ADAS)
- Infotainment and Clusters
- Power-Supply Sequencing Applications

3 Description
The TPS3779-Q1 and TPS3780-Q1 are a family of high-accuracy, two-channel voltage detectors featuring low power and small solution size. The SENSE1 and SENSE2 inputs include hysteresis to reject brief glitches, thus ensuring stable output operation without false triggering. This device family offers different factory-set hysteresis options of 5% or 10%.

The TPS3779-Q1 and TPS3780-Q1 have adjustable SENSEx inputs that can be configured by an external resistor divider. When the voltage at the SENSE1 or SENSE2 input goes below the falling threshold, OUT1 or OUT2 is driven low, respectively. When SENSE1 or SENSE2 rises above the rising threshold, OUT1 or OUT2 goes high, respectively.

The devices have a very low quiescent current of 2 µA (typical) and provide a precise, space-conscious solution for voltage detection suitable for low-power, system-monitoring, and portable applications. The TPS3779-Q1 and TPS3780-Q1 operate from 1.5 V to 5.5 V, over the –40°C to +125°C temperature range.

Device Information(1)

<table>
<thead>
<tr>
<th>PART NUMBER</th>
<th>PACKAGE</th>
<th>BODY SIZE (NOM)</th>
</tr>
</thead>
<tbody>
<tr>
<td>TPS37xx-Q1</td>
<td>SOT-23 (6)</td>
<td>2.90 mm × 1.60 mm</td>
</tr>
</tbody>
</table>

(1) For all available packages, see the orderable addendum at the end of the datasheet.

Sense Threshold (VT+) Deviation versus Temperature

Typical Schematic

An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.
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4 Revision History
NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (June 2016) to Revision A

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<tr>
<th>Page</th>
</tr>
</thead>
<tbody>
<tr>
<td>3</td>
</tr>
<tr>
<td>5</td>
</tr>
</tbody>
</table>

- Added TPS3780A-Q1 row to Device Comparison Table .................. 3
- Added TPS37xxA-Q1 row to \( V_{IT} \) parameter in Electrical Characteristics table .......................... 5
5 Device Comparison Table

<table>
<thead>
<tr>
<th>PRODUCT</th>
<th>HYSTERESIS (%)</th>
<th>OUTPUT</th>
</tr>
</thead>
<tbody>
<tr>
<td>TPS3779B-Q1</td>
<td>5</td>
<td>Push-pull</td>
</tr>
<tr>
<td>TPS3779C-Q1</td>
<td>10</td>
<td>Push-pull</td>
</tr>
<tr>
<td>TPS3780A-Q1</td>
<td>0.5</td>
<td>Open-drain</td>
</tr>
<tr>
<td>TPS3780B-Q1</td>
<td>5</td>
<td>Open-drain</td>
</tr>
<tr>
<td>TPS3780C-Q1</td>
<td>10</td>
<td>Open-drain</td>
</tr>
</tbody>
</table>

6 Pin Configuration and Functions

**Pin Functions**

<table>
<thead>
<tr>
<th>NAME</th>
<th>NO.</th>
<th>I/O</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>GND</td>
<td>5</td>
<td>—</td>
<td>Ground</td>
</tr>
<tr>
<td>OUT1</td>
<td>2</td>
<td>O</td>
<td>OUT1 is the output for SENSE1. OUT1 is asserted (driven low) when the voltage at SENSE1 falls below (V_{IT-}). OUT1 is deasserted (goes high) after SENSE1 rises higher than (V_{IT+}). OUT1 is a push-pull output for the TPS3779-Q1 and an open-drain output for the TPS3780-Q1. The open-drain device (TPS3780-Q1) can be pulled up to 5.5 V independent of VDD; a pullup resistor is required for this device.</td>
</tr>
<tr>
<td>OUT2</td>
<td>3</td>
<td>O</td>
<td>OUT2 is the output for SENSE2. OUT2 is asserted (driven low) when the voltage at SENSE2 falls below (V_{IT-}). OUT2 is deasserted (goes high) after SENSE2 rises higher than (V_{IT+}). OUT2 is a push-pull output for the TPS3779-Q1 and an open-drain output for the TPS3780-Q1. The open-drain device (TPS3780-Q1) can be pulled up to 5.5 V independent of VDD; a pullup resistor is required for this device.</td>
</tr>
<tr>
<td>SENSE1</td>
<td>6</td>
<td>I</td>
<td>This pin is connected to the voltage to be monitored with the use of an external resistor divider. When the voltage at this pin drops below the threshold voltage (V_{IT+}), OUT1 is asserted.</td>
</tr>
<tr>
<td>SENSE2</td>
<td>4</td>
<td>I</td>
<td>This pin is connected to the voltage to be monitored with the use of an external resistor divider. When the voltage at this pin drops below the threshold voltage (V_{IT+}), OUT2 is asserted.</td>
</tr>
<tr>
<td>VDD</td>
<td>1</td>
<td>I</td>
<td>Supply voltage input. Connect a 1.5-V to 5.5-V supply to VDD in order to power the device. Good analog design practice is to place a 0.1-(\mu)F ceramic capacitor close to this pin (required for VDD &lt; 1.5 V).</td>
</tr>
</tbody>
</table>
7 Specifications

7.1 Absolute Maximum Ratings
over operating junction temperature range (unless otherwise noted)\(^{(1)}\)

<table>
<thead>
<tr>
<th></th>
<th>MIN</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>Voltage</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>VDD</td>
<td>–0.3</td>
<td>7</td>
<td>V</td>
</tr>
<tr>
<td>OUT1, OUT2 (TPS3779-Q1 only)</td>
<td>–0.3</td>
<td>VDD + 0.3</td>
<td></td>
</tr>
<tr>
<td>OUT1, OUT2 (TPS3780-Q1 only)</td>
<td>–0.3</td>
<td>7</td>
<td></td>
</tr>
<tr>
<td>SENSE1, SENSE2</td>
<td>–0.3</td>
<td>7</td>
<td></td>
</tr>
<tr>
<td>Current</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>OUT1, OUT2</td>
<td>±20</td>
<td></td>
<td>mA</td>
</tr>
<tr>
<td>Temperature</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Operating junction, (T_J)(^{(2)})</td>
<td>–40</td>
<td>125</td>
<td>°C</td>
</tr>
<tr>
<td>Storage, (T_{STG})</td>
<td>–65</td>
<td>150</td>
<td></td>
</tr>
</tbody>
</table>

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) For low-power devices, the junction temperature rise above the ambient temperature is negligible; therefore, the junction temperature is considered equal to the ambient temperature (\(T_J = T_A\)).

7.2 ESD Ratings

<table>
<thead>
<tr>
<th>Electrostatic discharge</th>
<th>VALUE</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>Human-body model (HBM), per AEC Q100-002(^{(1)})</td>
<td>±2000</td>
<td>V</td>
</tr>
<tr>
<td>Charged-device model (CDM), per AEC Q100-011</td>
<td>±500</td>
<td></td>
</tr>
</tbody>
</table>

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

7.3 Recommended Operating Conditions
over operating junction temperature range (unless otherwise noted)

<table>
<thead>
<tr>
<th></th>
<th>MIN</th>
<th>NOM</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>Power-supply voltage</td>
<td>1.5</td>
<td>5.5</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>Sense voltage</td>
<td>0</td>
<td>5.5</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>Output voltage (TPS3779-Q1 only)</td>
<td>0</td>
<td>VDD + 0.3</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Output voltage (TPS3780-Q1 only)</td>
<td>0</td>
<td>5.5</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>(R_{PU}) Pullup resistor (TPS3780-Q1 only)</td>
<td>1.5</td>
<td>10,000</td>
<td>kΩ</td>
<td></td>
</tr>
<tr>
<td>Current</td>
<td>–5</td>
<td></td>
<td>mA</td>
<td></td>
</tr>
<tr>
<td>(C_{IN}) Input capacitor</td>
<td>0.1</td>
<td></td>
<td>µF</td>
<td></td>
</tr>
<tr>
<td>(T_J) Junction temperature</td>
<td>–40</td>
<td>25</td>
<td>125</td>
<td>°C</td>
</tr>
</tbody>
</table>

7.4 Thermal Information

<table>
<thead>
<tr>
<th>THERMAL METRIC(^{(1)})</th>
<th>TPS3779-Q1, TPS3780-Q1</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>(R_{JA}) Junction-to-ambient thermal resistance</td>
<td>193.9</td>
<td>°C/W</td>
</tr>
<tr>
<td>(R_{JCTOP}) Junction-to-case (top) thermal resistance</td>
<td>134.5</td>
<td>°C/W</td>
</tr>
<tr>
<td>(R_{JCB}) Junction-to-board thermal resistance</td>
<td>39.0</td>
<td>°C/W</td>
</tr>
<tr>
<td>(\psi_{JT}) Junction-to-top characterization parameter</td>
<td>30.4</td>
<td>°C/W</td>
</tr>
<tr>
<td>(\psi_{JB}) Junction-to-board characterization parameter</td>
<td>38.5</td>
<td>°C/W</td>
</tr>
<tr>
<td>(R_{JCBOT}) Junction-to-case (bottom) thermal resistance</td>
<td>N/A</td>
<td>°C/W</td>
</tr>
</tbody>
</table>

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.
7.5 Electrical Characteristics

all specifications are over the operating temperature range of $-40^\circ C < T_J < +125^\circ C$ and $1.5 \text{ V} \leq \text{VDD} \leq 5.5 \text{ V}$ (unless otherwise noted); typical values are at $T_J = 25^\circ C$ and VDD = 3.3 V

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>VDD Input supply range</td>
<td></td>
<td>1.5</td>
<td>5.5</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>$V_{(POR)}$ Power-on-reset voltage(^{(1)})</td>
<td>$V_{OL}$ (max) = 0.2 V, $I_{OL}$ = 15 $\mu$A</td>
<td>0.8</td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>$I_{DD}$ Supply current (into VDD pin)</td>
<td>VDD = 3.3 V, no load</td>
<td>2.09</td>
<td>5.80</td>
<td></td>
<td>$\mu$A</td>
</tr>
<tr>
<td></td>
<td>VDD = 5.5 V, no load</td>
<td>2.29</td>
<td>6.50</td>
<td></td>
<td>$\mu$A</td>
</tr>
<tr>
<td>$V_{IT+}$ Positive-going input threshold voltage</td>
<td>$V_{(SENSEX)}$ rising</td>
<td>1.194</td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>$V_{IT-}$ Negative-going input threshold voltage</td>
<td>$V_{(SENSEX)}$ falling</td>
<td>1.188</td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td></td>
<td>TPS37xxA-Q1 (0.5% hysteresis)</td>
<td></td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td></td>
<td>TPS37xxB-Q1 (5% hysteresis)</td>
<td>1.134</td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td></td>
<td>TPS37xxC-Q1 (10% hysteresis)</td>
<td>1.074</td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>$I_{(SENSEX)}$ Input current</td>
<td>$V_{(SENSEX)}$ = 0 V or VDD</td>
<td>-15</td>
<td>15</td>
<td></td>
<td>nA</td>
</tr>
<tr>
<td>$V_{OL}$ Low-level output voltage</td>
<td>VDD $\geq$ 1.5 V, $I_{SINK}$ = 0.4 mA</td>
<td>0.25</td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td></td>
<td>VDD $\geq$ 2.7 V, $I_{SINK}$ = 2 mA</td>
<td>0.25</td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td></td>
<td>VDD $\geq$ 4.5 V, $I_{SINK}$ = 3.2 mA</td>
<td>0.30</td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>$V_{OH}$ High-level output voltage (TPS3779-Q1 only)</td>
<td>VDD $\geq$ 1.5 V, $I_{SOURCE}$ = 0.4 mA</td>
<td>0.8 VDD</td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td></td>
<td>VDD $\geq$ 2.7 V, $I_{SOURCE}$ = 1 mA</td>
<td>0.8 VDD</td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td></td>
<td>VDD $\geq$ 4.5 V, $I_{SOURCE}$ = 2.5 mA</td>
<td>0.8 VDD</td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>$I_{(ODE)}$ Open-drain output leakage current (TPS3780-Q1 only)</td>
<td>High impedance, $V_{(SENSEX)} = V_{(OUTx)} = 5.5$ V</td>
<td>-250</td>
<td>250</td>
<td></td>
<td>nA</td>
</tr>
</tbody>
</table>

\(^{(1)}\) Outputs are undetermined below $V_{(POR)}$. 

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Product Folder Links: TPS3779-Q1 TPS3780-Q1
7.6 Timing Requirements

typical values are at $T_J = 25^\circ C$ and VDD = 3.3 V; SENSEx transitions between 0 V and 1.3 V

<table>
<thead>
<tr>
<th></th>
<th>MIN</th>
<th>NOM</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>$t_{PD(r)}$</td>
<td></td>
<td>5.5</td>
<td></td>
<td>µs</td>
</tr>
<tr>
<td>$t_{PD(f)}$</td>
<td></td>
<td>10</td>
<td></td>
<td>µs</td>
</tr>
<tr>
<td>$t_{SD}$</td>
<td></td>
<td>570</td>
<td></td>
<td>µs</td>
</tr>
</tbody>
</table>

(1) During power-on or when a VDD transient is below VDD(min), the outputs reflect the input conditions 570 µs after VDD transitions through VDD(min).

Figure 1. Timing Diagram
7.7 Typical Characteristics

at $T_J = 25^\circ C$ with a 0.1-µF capacitor close to VDD (unless otherwise noted)
Typical Characteristics (continued)

at \( T_J = 25°C \) with a 0.1-\( \mu \)F capacitor close to VDD (unless otherwise noted)

Figure 8. Output Voltage Low vs Output Current
(VDD = 3.3 V)

Figure 9. Output Voltage Low vs Output Current
(VDD = 5.5 V)

Figure 10. Output Voltage High vs Output Current
(VDD = 1.5 V)

Figure 11. Output Voltage High vs Output Current
(VDD = 3.3 V)

Figure 12. Output Voltage High vs Output Current
(VDD = 5.5 V)

Figure 13. Propagation Delay from SENSEx High to Output High
Typical Characteristics (continued)

at $T_J = 25^\circ C$ with a 0.1-µF capacitor close to VDD (unless otherwise noted)

**Figure 14. Propagation Delay from SENSEx Low to Output Low**

**Figure 15. Startup Delay**

**Figure 16. Minimum Transient Duration vs Overdrive**

(VDD = 1.5 V)

High-to-low transition occurs above the curve

**Figure 17. Minimum Transient Duration vs Overdrive**

(VDD = 5.5 V)

High-to-low transition occurs above the curve

**Figure 18. Minimum Transient Duration vs Overdrive**

(VDD = 1.5 V)

Low-to-high transition occurs above the curve

**Figure 19. Minimum Transient Duration vs Overdrive**

(VDD = 5.5 V)

Low-to-high transition occurs above the curve
8 Detailed Description

8.1 Overview
The TPS3779-Q1 and TPS3780-Q1 are small, low quiescent current ($I_{DD}$), dual-channel voltage detectors. These devices have high-accuracy rising and falling input thresholds, and assert the output as shown in Table 1. The output (OUTx pin) goes low when the SENSEx pin is less than $V_{IT-}$ and goes high when the pin is greater than $V_{IT+}$. The TPS3779-Q1 and TPS3780-Q1 offer two hysteresis options (5% and 10%) for use in a wide variety of applications. These devices have two independent voltage-detection channels that can be used in systems where multiple voltage rails are required to be monitored, or where one channel can be used as an early warning signal and the other channel can be used as the system reset signal.

Table 1. TPS3779-Q1, TPS3780-Q1 Truth Table

<table>
<thead>
<tr>
<th>CONDITIONS</th>
<th>OUTPUT</th>
</tr>
</thead>
<tbody>
<tr>
<td>SENSE1 &lt; $V_{IT-}$</td>
<td>OUT1 = low</td>
</tr>
<tr>
<td>SENSE2 &lt; $V_{IT-}$</td>
<td>OUT2 = low</td>
</tr>
<tr>
<td>SENSE1 &gt; $V_{IT+}$</td>
<td>OUT1 = high</td>
</tr>
<tr>
<td>SENSE2 &gt; $V_{IT+}$</td>
<td>OUT2 = high</td>
</tr>
</tbody>
</table>

8.2 Functional Block Diagrams

Figure 20. TPS3779-Q1 Block Diagram

Figure 21. TPS3780-Q1 Block Diagram
8.3 Feature Description

8.3.1 Inputs (SENSE1, SENSE2)

The TPS3779-Q1 and TPS3780-Q1 each have two comparators for voltage detection. Each comparator has one external input; the other input is connected to the internal reference. The comparator rising threshold is designed and trimmed to be equal to \( V_{IT^+} \), and the falling threshold is trimmed to be equal to \( V_{IT^-} \). The built-in falling hysteresis options make the devices immune to supply rail noise and ensure stable operation.

The comparator inputs can swing from ground to 5.5 V, regardless of the device supply voltage used. Although not required in most cases, for extremely noisy applications, good analog design practice is to place a 1-nF to 10-nF bypass capacitor at the comparator input in order to reduce sensitivity to transients and layout parasitic.

For each SENSEEx input, the corresponding output (OUTx) is driven to logic low when the input voltage drops below \( V_{IT^+} \). When the voltage exceeds \( V_{IT^+} \), the output (OUTx) is driven high; see Figure 1.

8.3.2 Outputs (OUT1, OUT2)

In a typical device application, the outputs are connected to a reset or enable input of another device, such as a digital signal processor (DSP), central processing unit (CPU), field-programmable gate array (FPGA), or application-specific integrated circuit (ASIC); or the outputs are connected to the enable input of a voltage regulator, such as a dc-dc or low-dropout (LDO) regulator.

The TPS3779-Q1 provides two push-pull outputs. The logic high level of the outputs is determined by the VDD pin voltage. Pullup resistors are not required with this configuration, thus saving board space. However, all interface logic levels must be examined. All OUTx connections must be compatible with the VDD pin logic level.

The TPS3780-Q1 provides two open-drain outputs (OUT1 and OUT2); pullup resistors must be used to hold these lines high when the output goes to a high-impedance condition (not asserted). By connecting pullup resistors to the proper voltage rails, the outputs can be connected to other devices at correct interface voltage levels. The outputs can be pulled up to 5.5 V, independent of the device supply voltage. To ensure proper voltage levels, make sure to choose the correct pullup resistor values. The pullup resistor value is determined by \( V_{OL} \), the sink current capability, and the output leakage current (\( I_{LKG(OD)} \)). These values are specified in the Electrical Characteristics table. By using wired-AND logic, OUT1 and OUT2 can be combined into one logic signal. The Inputs (SENSE1, SENSE2) section describes how the outputs are asserted or deasserted. See Figure 1 for a description of the relationship between threshold voltages and the respective output.

8.4 Device Functional Modes

8.4.1 Normal Operation (VDD ≥ VDD(min))

When the voltage on VDD is greater than VDD(min) for \( t_{SD} \), the output signals react to the present state of the corresponding SENSEEx pins.

8.4.2 Power-On-Reset (VDD < \( V_{(POR)} \))

When the voltage on VDD is lower than the required voltage to internally pull the logic low output to GND (\( V_{(POR)} \)), both outputs are undefined and are not to be relied upon for proper system function.
9 Application and Implementation

NOTE
Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information
The TPS3779-Q1 and TPS3780-Q1 are used as precision, dual-voltage detectors. The monitored voltage, VDD voltage, and output pullup voltage (TPS3780-Q1 only) can be independent voltages or connected in any configuration.

9.1.1 Threshold Overdrive
Threshold overdrive is how much \( V_{\text{SENSE1,2}} \) exceeds the specified threshold, and is important to know because a smaller overdrive results in a slower OUTx response. Threshold overdrive is calculated as a percent of the threshold in question, as shown in Equation 1:

\[
\text{Overdrive} = \left| \frac{V_{\text{SENSE1,2}}}{V_{\text{IT}}} - 1 \right| \times 100\%
\]

where
- \( V_{\text{IT}} \) is either \( V_{\text{IT–}} \) or \( V_{\text{IT+}} \), depending on whether calculating the overdrive for the negative-going threshold or the positive-going threshold, respectively
- \( V_{\text{SENSE1,2}} \) is the voltage at the SENSE1 or SENSE2 input

Equation 1

Figure 16 illustrates the minimum detectable pulse on the SENSEx inputs versus overdrive, and is used to visualize the relationship that overdrive has on \( t_{PD(f)} \) for negative-going events.

9.1.2 Sense Resistor Divider
The resistor divider values and target threshold voltage can be calculated by using Equation 2 and Equation 3 to determine \( V_{\text{MON(UV)}} \) and \( V_{\text{MON(PG)}} \), respectively.

\[
V_{\text{MON(UV)}} = \left( 1 + \frac{R1}{R2} \right) \times V_{\text{IT–}}
\]

(2)

\[
V_{\text{MON(PG)}} = \left( 1 + \frac{R1}{R2} \right) \times V_{\text{IT+}}
\]

(3)

where
- \( R1 \) and \( R2 \) are the resistor values for the resistor divider on the SENSEx pins
- \( V_{\text{MON(UV)}} \) is the target voltage at which an undervoltage condition is detected
- \( V_{\text{MON(PG)}} \) is the target voltage at which the output goes high when \( V_{\text{MONx}} \) rises

Choose \( R_{\text{TOTAL}} \) (equal to \( R1 + R2 \)) so that the current through the divider is approximately 100 times higher than the input current at the SENSEx pins. The resistors can have high values to minimize current consumption as a result of low input bias current without adding significant error to the resistive divider. For details on sizing input resisters, see the Optimizing Resistor Dividers at a Comparator Input application report (SLVA450), available for download from www.ti.com.
9.2 Typical Applications

9.2.1 Monitoring Two Separate Rails

Figure 22. Monitoring Two Separate Rails Schematic

9.2.1.1 Design Requirements

Table 2. Design Parameters

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>DESIGN REQUIREMENT</th>
<th>DESIGN RESULT</th>
</tr>
</thead>
<tbody>
<tr>
<td>VDD</td>
<td>5 V</td>
<td>5 V</td>
</tr>
<tr>
<td>Hysteresis</td>
<td>10%</td>
<td>10%</td>
</tr>
<tr>
<td>Monitored voltage 1</td>
<td>3.3 V nominal, ( V_{\text{MON(PG)}} = 2.9 ) V, ( V_{\text{MON(UV)}} = 2.6 ) V</td>
<td>( V_{\text{MON(PG)}} = 2.908 ) V, ( V_{\text{MON(UV)}} = 2.618 ) V</td>
</tr>
<tr>
<td>Monitored voltage 2</td>
<td>3 V nominal, ( V_{\text{MON(PG)}} = 2.6 ) V, ( V_{\text{MON(UV)}} = 2.4 ) V</td>
<td>( V_{\text{MON(PG)}} = 2.606 ) V, ( V_{\text{MON(UV)}} = 2.371 ) V</td>
</tr>
<tr>
<td>Output logic voltage</td>
<td>3.3-V CMOS</td>
<td>3.3-V CMOS</td>
</tr>
</tbody>
</table>

9.2.1.2 Detailed Design Procedure

1. Select the TPS3780C-Q1. The C version is selected to satisfy the hysteresis requirement. The TPS3780-Q1 is selected for the output logic requirement. An open-drain output allows for the output to be pulled up to a voltage other than VDD.

2. The resistor divider values are calculated by using Equation 2 and Equation 3. For SENSE1, \( R_1 = 1.13 \) M\( \Omega \) and \( R_2 = 787 \) k\( \Omega \). For SENSE2, \( R_3 (R_1) = 681 \) k\( \Omega \) and \( R_4 (R_2) = 576 \) k\( \Omega \).

9.2.1.3 Application Curve

Figure 23. Monitoring Two Separate Rails Curve
9.2.2 Early Warning Detection

![Early Warning Detection Schematic](image)

**Figure 24. Early Warning Detection Schematic**

9.2.2.1 Design Requirements

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>DESIGN REQUIREMENT</th>
<th>DESIGN RESULT</th>
</tr>
</thead>
<tbody>
<tr>
<td>VDD</td>
<td>V&lt;sub&gt;MON&lt;/sub&gt;</td>
<td>V&lt;sub&gt;MON&lt;/sub&gt;</td>
</tr>
<tr>
<td>Hysteresis</td>
<td>10%</td>
<td>10%</td>
</tr>
<tr>
<td>Monitored voltage 1</td>
<td>V&lt;sub&gt;MON(PG)&lt;/sub&gt; = 3.3 V, V&lt;sub&gt;MON(UV)&lt;/sub&gt; = 3 V</td>
<td>V&lt;sub&gt;MON(PG)&lt;/sub&gt; = 3.330 V, V&lt;sub&gt;MON(UV)&lt;/sub&gt; = 2.997 V</td>
</tr>
<tr>
<td>Monitored voltage 2</td>
<td>V&lt;sub&gt;MON(PG)&lt;/sub&gt; = 3.9 V, V&lt;sub&gt;MON(UV)&lt;/sub&gt; = 3.5 V</td>
<td>V&lt;sub&gt;MON(PG)&lt;/sub&gt; = 3.921 V, V&lt;sub&gt;MON(UV)&lt;/sub&gt; = 3.529 V</td>
</tr>
</tbody>
</table>

9.2.2.2 Detailed Design Procedure

1. Select the TPS3779C-Q1. The C version is selected to satisfy the hysteresis requirement. The TPS3779-Q1 is selected to save on component count and board space.

2. Use Equation 4 to calculate the total resistance for the resistor divider. Determine the minimum total resistance of the resistor network necessary to achieve the current consumption specification. For this example, the current flow through the resistor network is chosen to be 1.41 µA. Use the key transition point for V<sub>MON2</sub>. For this example, the low-to-high transition, V<sub>MON(PG)</sub>, is considered more important.

\[
R_{\text{TOTAL}} = \frac{V_{\text{MON(PG2)}}}{I} = \frac{3.9 \text{ V}}{1.41 \mu\text{A}} = 2.78 \text{ MΩ}
\]

where
- V<sub>MON(PG2)</sub> is the target voltage at which OUT2 goes high when V<sub>MON</sub> rises
- I is the current flowing through the resistor network

3. After \( R_{\text{TOTAL}} \) is determined, R3 can be calculated using Equation 5. Select the nearest 1% resistor value for R3. In this case, 845 kΩ is the closest value.

\[
R_3 = \frac{V_{\text{IT+}}}{I} = \frac{1.194 \text{ V}}{1.41 \mu\text{A}} = 846 \text{ kΩ}
\]

4. Use Equation 6 to calculate R2. Select the nearest 1% resistor value for R2. In this case, 150 kΩ is the closest value. Use the key transition point for V<sub>MON1</sub>. For this example, the high-to-low transition, V<sub>MON(UV)</sub>, is considered more important.

\[
R_2 = \frac{R_{\text{TOTAL}}}{V_{\text{MON(UV1)}}} \cdot V_{\text{IT−}} - R_3 = \frac{2.78 \text{ MΩ}}{3 \text{ V}} \cdot 1.074 \text{ V} - 845 \text{ kΩ} = 149 \text{ kΩ}
\]

where
- V<sub>MON(UV1)</sub> is the target voltage at which OUT1 goes low when V<sub>MON</sub> falls
5. Use Equation 7 to calculate R1. Select the nearest 1% resistor value for R1. In this case, 1.78 MΩ is a 1% resistor.

\[
R1 = R_{\text{TOTAL}} - R2 - R3 = 2.78 \text{ MΩ} - 150 \text{ kΩ} - 845 \text{ kΩ} = 1.78 \text{ MΩ}
\]  

(7)

### 9.2.2.3 Application Curve

![Application Curve](image)

**Figure 25. Early Warning Detection Curve**

### 10 Power-Supply Recommendations

The TPS3779-Q1 and TPS3780-Q1 are designed to operate from an input voltage supply range between 1.5 V and 5.5 V. An input supply capacitor is not required for this device; however, good analog practice is to place a 0.1-µF or greater capacitor between the VDD pin and the GND pin. This device has a 7-V absolute maximum rating on the VDD pin. If the voltage supply providing power to VDD is susceptible to any large voltage transient that can exceed 7 V, additional precautions must be taken.

For applications where SENSEx is greater than 0 V before VDD, and is subject to a startup slew rate of less than 200 mV per 1 ms, the output can be driven to logic high in error. To correct the output, cycle the SENSEx lines below \( V_{IT^-} \) or sequence SENSEx after VDD.

### 11 Layout

#### 11.1 Layout Guidelines

Place the VDD decoupling capacitor close to the device.

Avoid using long traces for the VDD supply node. The VDD capacitor, along with parasitic inductance from the supply to the capacitor, can form an LC tank circuit that creates ringing with peak voltages above the maximum VDD voltage.

#### 11.2 Layout Example

![Layout Example](image)

**Figure 26. Example SOT-23 Layout**
12 Device and Documentation Support

12.1 Device Support

12.1.1 Development Support

12.1.1.1 Evaluation Modules

An evaluation module (EVM) is available to assist in the initial circuit performance evaluation using the TPS3779-Q1 and TPS3780-Q1. The TPS3780EVM-154 Evaluation Module details the design kits and evaluation modules for the TPS3780EVM-154.

The EVM can be requested at Texas Instruments through the TPS3779-Q1 and TPS3780-Q1 product folders, or purchased directly from the TI eStore.

12.1.1.2 Spice Models

Computer simulation of circuit performance using SPICE is often useful when analyzing the performance of analog circuits and systems. A SPICE model for the TPS3779-Q1 and TPS3780-Q1 is available through the respective device product folders under Simulation Models.

12.1.2 Device Nomenclature

The TPS3779xQyyyzQ1 and TPS3780xQyyyzQ1 are the generic naming conventions for these devices. The TPS3779-Q1 and TPS3780-Q1 represent the family of these devices; x is used to display the hysteresis version, yyy is reserved for the package designator, and z is the package quantity.

• Example: TPS3780CDBVRQ1
  • Family: TPS3780-Q1 (open-drain)
  • Hysteresis: 10%
  • DBV package: 6-pin SOT-23
  • Package quantity: R is for 3000 pieces

12.2 Documentation Support

12.2.1 Related Documentation

For related documentation see the following:

• TPS3780EVM-154 Evaluation Module (SLVU796)
• Optimizing Resistor Dividers at a Comparator Input Application Report (SLVA450)

12.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on Alert me to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.4 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

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<tr>
<th>PARTS</th>
<th>PRODUCT FOLDER</th>
<th>SAMPLE &amp; BUY</th>
<th>TECHNICAL DOCUMENTS</th>
<th>TOOLS &amp; SOFTWARE</th>
<th>SUPPORT &amp; COMMUNITY</th>
</tr>
</thead>
<tbody>
<tr>
<td>TPS3779-Q1</td>
<td>Click here</td>
<td>Click here</td>
<td>Click here</td>
<td>Click here</td>
<td>Click here</td>
</tr>
<tr>
<td>TPS3780-Q1</td>
<td>Click here</td>
<td>Click here</td>
<td>Click here</td>
<td>Click here</td>
<td>Click here</td>
</tr>
</tbody>
</table>
12.5 Community Resources
The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

**TI E2E™ Online Community**  *TI's Engineer-to-Engineer (E2E) Community.* Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

**Design Support**  *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.6 Trademarks
E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

12.7 Electrostatic Discharge Caution
This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.8 Glossary
**SLYZ022 — TI Glossary.**
This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information
The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.
PACKAGING INFORMATION

<table>
<thead>
<tr>
<th>Orderable Device</th>
<th>Status (1)</th>
<th>Package Type</th>
<th>Package Drawing</th>
<th>Pins</th>
<th>Package Qty</th>
<th>Eco Plan (2)</th>
<th>Lead/Ball Finish</th>
<th>MSL Peak Temp</th>
<th>Op Temp (°C)</th>
<th>Device Marking (4/5)</th>
<th>Samples</th>
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<td>CU NIPDAU</td>
<td>Level-2-260C-1 YEAR</td>
<td>-40 to 125</td>
<td>12OE</td>
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<td>3000</td>
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<td>6</td>
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<td>Green (RoHS &amp; no Sb/Br)</td>
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<td>Level-2-260C-1 YEAR</td>
<td>-40 to 125</td>
<td>12HE</td>
<td></td>
</tr>
</tbody>
</table>

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBsolete: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.
Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI’s liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF TPS3779-Q1, TPS3780-Q1:

- Catalog: TPS3779, TPS3780

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
## TAPE AND REEL INFORMATION

### TAPE DIMENSIONS

- **A0**: Dimension designed to accommodate the component width
- **B0**: Dimension designed to accommodate the component length
- **K0**: Dimension designed to accommodate the component thickness
- **W**: Overall width of the carrier tape
- **P1**: Pitch between successive cavity centers

### TAPE AND REEL INFORMATION

### PACKAGE MATERIALS INFORMATION

*All dimensions are nominal.

<table>
<thead>
<tr>
<th>Device</th>
<th>Package Type</th>
<th>Package Drawing</th>
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<th>Reel Diameter (mm)</th>
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<th>A0 (mm)</th>
<th>B0 (mm)</th>
<th>K0 (mm)</th>
<th>P1 (mm)</th>
<th>W (mm)</th>
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</table>
**TAPE AND REEL BOX DIMENSIONS**

*All dimensions are nominal*

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<tr>
<th>Device</th>
<th>Package Type</th>
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<th>Length (mm)</th>
<th>Width (mm)</th>
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<td>3000</td>
<td>180.0</td>
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NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
4. Leads 1, 2, 3 may be wider than leads 4, 5, 6 for package orientation.
5. Reference JEDEC MO-178.
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.
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