MIDRANGE INPUT SYNCHRONOUS BUCK CONTROLLER
WITH VOLTAGE FEED-FORWARD

FEATURES
• Operation Over 4.5-V to 28-V Input Range
• Fixed-Frequency Voltage-Mode Controller
• Integrated Unity Gain Amplifier for Remote Output Sensing
• Predictive Gate Drive™ Generation II for Improved Efficiency
• <1% Internal 700-mV Reference
• Input Voltage Feed Forward Control
• Prebiased Output Compatible
• Internal Gate Drive Outputs for High-Side and Synchronous N-Channel MOSFETs
• Switching Frequency Programmable to 1 MHz
• 20-Pin QFN Package
• Thermal Shutdown Protection
• Software Design Tool and EVM Available

APPLICATIONS
• Power Modules
• Networking/Telecom
• Industrial
• Servers

DESCRIPTION
The TPS40074 is a mid voltage, wide input (4.5-V to 28-V), synchronous, step-down controller, offering design flexibility for a variety of user programmable functions, including; soft start, UVLO, operating frequency, voltage feed-forward and high-side FET sensed short circuit protection.

The TPS40074 incorporates MOSFET gate drivers for external N-channel high side and synchronous rectifier (SR) MOSFETs. The gate drive logic incorporates second generation predictive anti-cross conduction circuitry to prevent simultaneous high side and synchronous rectifier conduction, while minimizing to eliminating current flow in the body diode of the SR FET. The TPS40074 allows for starting into pre-biased outputs by not allowing the synchronous rectifier FET to turn on until the commanded voltage during soft start is greater than the existing pre-bias voltage.

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

Predictive Gate Drive is a trademark of Texas Instruments.
TPS40074

ORDERING INFORMATION

<table>
<thead>
<tr>
<th>$T_A$</th>
<th>PACKAGE</th>
<th>PART NUMBER</th>
</tr>
</thead>
<tbody>
<tr>
<td>40°C to 85°C</td>
<td>Plastic QFN (RHL)</td>
<td>TPS40074RHLT(1)</td>
</tr>
<tr>
<td></td>
<td></td>
<td>TPS40074RHLR(2)</td>
</tr>
</tbody>
</table>

(1) The TPS40074 is available taped and reeled only. Add an T suffix (i.e. TPS40074RHLT) to the orderable part number for quantities of 250 units per small reel.

(2) Add an R suffix (i.e. TPS40074RHLR) to the orderable part number for quantities of 3,000 units per small reel.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range unless otherwise noted(1)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>TPS40074</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{DD}$</td>
<td>Input voltage range</td>
<td>VDD, ILIM</td>
</tr>
<tr>
<td>$V_{DD}$</td>
<td>Input voltage range</td>
<td>FB, KFF, PGD, SYNC</td>
</tr>
<tr>
<td>$V_{DD}$</td>
<td>Input voltage range</td>
<td>SW</td>
</tr>
<tr>
<td>$V_{DD}$</td>
<td>Input voltage range</td>
<td>SA+, SA-</td>
</tr>
<tr>
<td>$V_{DD}$</td>
<td>Input voltage range</td>
<td>SW, transient &lt; 50 ns</td>
</tr>
<tr>
<td>$V_{OUT}$</td>
<td>Output voltage range</td>
<td>COMP, RT, SS</td>
</tr>
<tr>
<td>$V_{OUT}$</td>
<td>Output voltage range</td>
<td>BOOST, HDRV</td>
</tr>
<tr>
<td>$V_{OUT}$</td>
<td>Output voltage range</td>
<td>DBP, SAO, LDRV</td>
</tr>
<tr>
<td>$V_{OUT}$</td>
<td>Output voltage range</td>
<td>LVBP</td>
</tr>
<tr>
<td>$I_{OUT}$</td>
<td>Output current source</td>
<td>LDRV, HDRV</td>
</tr>
<tr>
<td>$I_{OUT}$</td>
<td>Output current sink</td>
<td>LDRV, HDRV</td>
</tr>
<tr>
<td>$I_{OUT}$</td>
<td>Output current sink</td>
<td>KFF</td>
</tr>
<tr>
<td>$I_{OUT}$</td>
<td>Output current sink</td>
<td>RT</td>
</tr>
<tr>
<td>$I_{OUT}$</td>
<td>Output current sink</td>
<td>LVBP</td>
</tr>
<tr>
<td>$T_J$</td>
<td>Operating junction temperature range</td>
<td>–40 to 125</td>
</tr>
<tr>
<td>$T_{stg}$</td>
<td>Storage temperature</td>
<td>–55 to 150</td>
</tr>
</tbody>
</table>

(1) Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

<table>
<thead>
<tr>
<th>Parameter</th>
<th>MIN</th>
<th>NOM</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{DD}$</td>
<td>4.5</td>
<td>28</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>$T_A$</td>
<td>–40</td>
<td>85</td>
<td></td>
<td>°C</td>
</tr>
</tbody>
</table>
### ELECTRICAL CHARACTERISTICS

$T_A = -40^\circ\text{C} \text{ to } 85^\circ\text{C}$, $V_{IN} = 12\, V_{\text{DC}}$, $R_T = 90.9\, \text{k}\Omega$, $I_{KFF} = 300\, \mu\text{A}$, $f_{SW} = 500\, \text{kHz}$, all parameters at zero power dissipation (unless otherwise noted).

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>INPUT SUPPLY</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$V_{DD}$</td>
<td>Input voltage range, VIN</td>
<td>4.5</td>
<td>28</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td><strong>OPERATING CURRENT</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$I_{DD}$</td>
<td>Quiescent current</td>
<td>Output drivers not switching</td>
<td>2.5</td>
<td>3.5</td>
<td>mA</td>
</tr>
<tr>
<td><strong>LVBP</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$V_{LVBP}$</td>
<td>Output voltage</td>
<td>$T_A = T_J = 25^\circ\text{C}$</td>
<td>3.9</td>
<td>4.2</td>
<td>4.5</td>
</tr>
<tr>
<td><strong>OSCILLATOR/RAMP GENERATOR</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$f_{OSC}$</td>
<td>Accuracy</td>
<td></td>
<td></td>
<td></td>
<td>kHz</td>
</tr>
<tr>
<td>$V_{RT}$</td>
<td>RT voltage</td>
<td></td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>$t_{ON(min)}$</td>
<td>Minimum output pulse time&lt;sup&gt;(1)&lt;/sup&gt;</td>
<td>$C_{HDRV} = 0, \text{nF}$</td>
<td></td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>$V_{IH}$</td>
<td>High-level input voltage, SYNC</td>
<td></td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>$V_{IL}$</td>
<td>Low-level input voltage, SYNC</td>
<td></td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>$I_{SYNC}$</td>
<td>Input current, SYNC</td>
<td></td>
<td></td>
<td></td>
<td>µA</td>
</tr>
<tr>
<td></td>
<td>Maximum duty cycle</td>
<td>$V_{FB} = 0, V$, $100, \text{kHz} \leq f_{SW} \leq 500, \text{kHz}$</td>
<td>84%</td>
<td>95%</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>$V_{FB} = 0, V$, $f_{SW} = 1, \text{MHz}$</td>
<td>76%</td>
<td>93%</td>
<td></td>
</tr>
<tr>
<td>$V_{KFF}$</td>
<td>Feed-forward voltage</td>
<td></td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>$I_{KFF}$</td>
<td>Feed-forward current operating range&lt;sup&gt;(1)&lt;/sup&gt;</td>
<td></td>
<td></td>
<td></td>
<td>µA</td>
</tr>
<tr>
<td><strong>SOFT START</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$I_{SS}$</td>
<td>Charge current</td>
<td></td>
<td></td>
<td></td>
<td>µA</td>
</tr>
<tr>
<td>$t_{OSSCH}$</td>
<td>Discharge time</td>
<td>$C_{SS} = 3.9, \text{nF}$</td>
<td></td>
<td></td>
<td>µs</td>
</tr>
<tr>
<td>$t_{SS}$</td>
<td>Soft-start time</td>
<td>$C_{SS} = 3.9, \text{nF}$, $V_{SS}$ rising from 0.7 V to 1.6 V</td>
<td>210</td>
<td>290</td>
<td>500</td>
</tr>
<tr>
<td></td>
<td>Command zero output voltage&lt;sup&gt;(2)(1)&lt;/sup&gt;</td>
<td></td>
<td></td>
<td></td>
<td>mV</td>
</tr>
<tr>
<td><strong>DBP</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$V_{DBP}$</td>
<td>Output voltage</td>
<td>$V_{DD} &gt; 10, V$</td>
<td>7</td>
<td>8</td>
<td>9</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>$V_{VDD} = 4.5, V$, $I_{OUT} = 25, mA$</td>
<td>4.0</td>
<td>4.3</td>
</tr>
<tr>
<td><strong>ERROR AMPLIFIER</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$V_{FB}$</td>
<td>Feedback regulation voltage total variation</td>
<td>$T_A = T_J = 25^\circ\text{C}$</td>
<td>0.698</td>
<td>0.700</td>
<td>0.704</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$0^\circ\text{C} \leq T_A = T_J \leq 85^\circ\text{C}$</td>
<td>0.690</td>
<td>0.700</td>
<td>0.707</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$-40^\circ\text{C} \leq T_A = T_J \leq 85^\circ\text{C}$</td>
<td>0.690</td>
<td>0.700</td>
<td>0.715</td>
</tr>
<tr>
<td>$V_{SS(Offset)}$</td>
<td>Soft-start offset from VSS&lt;sup&gt;(1)&lt;/sup&gt;</td>
<td>Offset from VSS to error amplifier</td>
<td></td>
<td></td>
<td>1</td>
</tr>
<tr>
<td>$A_{GBWP}$</td>
<td>Gain bandwidth&lt;sup&gt;(1)&lt;/sup&gt;</td>
<td></td>
<td></td>
<td></td>
<td>MHz</td>
</tr>
<tr>
<td>$A_{VOL}$</td>
<td>Open loop gain</td>
<td></td>
<td></td>
<td></td>
<td>dB</td>
</tr>
<tr>
<td>$I_{SRC}$</td>
<td>Output source current</td>
<td></td>
<td></td>
<td></td>
<td>mA</td>
</tr>
<tr>
<td>$I_{SINK}$</td>
<td>Output sink current</td>
<td></td>
<td></td>
<td></td>
<td>mA</td>
</tr>
<tr>
<td>$I_{IAS}$</td>
<td>Input bias current</td>
<td>$V_{FB} = 0.7, V$</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>SHORT CIRCUIT CURRENT PROTECTION</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$I_{ILIM}$</td>
<td>Current sink into ILIM pin</td>
<td></td>
<td></td>
<td></td>
<td>µA</td>
</tr>
<tr>
<td>$V_{ILIM(Off)}$</td>
<td>Current limit offset voltage</td>
<td>$V_{ILIM} = 11.5, V$, $(V_{SW} - V_{ILIM})$, $V_{VDD} = 12, V$</td>
<td>-50</td>
<td>-30</td>
<td>-10</td>
</tr>
<tr>
<td>$t_{ILIM}$</td>
<td>Minimum HDRV pulse width</td>
<td>During short circuit</td>
<td>135</td>
<td>225</td>
<td>ns</td>
</tr>
<tr>
<td>Propagation delay to output&lt;sup&gt;(1)&lt;/sup&gt;</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>$t_{BLANK}$</td>
<td>Blanking time&lt;sup&gt;(1)&lt;/sup&gt;</td>
<td></td>
<td></td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>$t_{OFF}$</td>
<td>Off time during a fault (SS cycle times)</td>
<td></td>
<td></td>
<td></td>
<td>cycles</td>
</tr>
</tbody>
</table>

<sup>(1)</sup> Ensured by design. Not production tested.

<sup>(2)</sup> For zero output voltage only. Does not assure lack of activity on HDRV or LDRV.
### ELECTRICAL CHARACTERISTICS (continued)

$T_A = -40^\circ\text{C}$ to $85^\circ\text{C}$, $V_{IN} = 12\text{ V}_{dc}$, $R_T = 90.9\ \text{k}\Omega$, $I_{KFF} = 300\ \mu\text{A}$, $f_{SW} = 500\ \text{kHz}$, all parameters at zero power dissipation (unless otherwise noted)

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{SW}$</td>
<td>Switching level to end precondition (3)</td>
<td>$V_{VDD} - V_{SW}$</td>
<td>2</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>$I_{FC}$</td>
<td>Precondition time (3)</td>
<td>100</td>
<td>ns</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$V_{ILM(pre)}$</td>
<td>Current limit precondition voltage threshold (3)</td>
<td>6.8</td>
<td>V</td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>OUTPUT DRIVERS</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$I_{HFA}$</td>
<td>High-side driver fall time (3)</td>
<td>$C_{HDRV} = 2200\ \text{pF}$, (HDRV - SW)</td>
<td>36</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>$I_{HRI}$</td>
<td>High-side driver rise time (3)</td>
<td>$C_{HDRV} = 2200\ \text{pF}$, (HDRV - SW)</td>
<td>48</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>$I_{HFA}$</td>
<td>High-side driver fall time (3)</td>
<td>$C_{HDRV} = 2200\ \text{pF}$, (HDRV - SW)</td>
<td>72</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>$I_{HRI}$</td>
<td>High-side driver rise time (3)</td>
<td>$C_{HDRV} = 2200\ \text{pF}$, (HDRV - SW)</td>
<td>96</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>$I_{LFA}$</td>
<td>Low-side driver fall time (3)</td>
<td>$C_{LDRV} = 2200\ \text{pF}$, (LDRV - SW)</td>
<td>24</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>$I_{LRI}$</td>
<td>Low-side driver rise time (3)</td>
<td>$C_{LDRV} = 2200\ \text{pF}$, (LDRV - SW)</td>
<td>48</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>$I_{LFA}$</td>
<td>Low-side driver fall time (3)</td>
<td>$C_{LDRV} = 2200\ \text{pF}$, (LDRV - SW)</td>
<td>48</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>$I_{LRI}$</td>
<td>Low-side driver rise time (3)</td>
<td>$C_{LDRV} = 2200\ \text{pF}$, (LDRV - SW)</td>
<td>96</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>$V_{OH}$</td>
<td>High-level output voltage, HDRV</td>
<td>$I_{HDRV} = 0.01\ \text{A}$, (VBOOST - HDRV)</td>
<td>0.7</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>$V_{OL}$</td>
<td>Low-level output voltage, HDRV</td>
<td>$I_{HDRV} = 0.01\ \text{A}$, (VBOOST - HDRV)</td>
<td>0.95</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>$V_{OH}$</td>
<td>High-level output voltage, LDRV</td>
<td>$I_{LDRV} = 0.01\ \text{A}$, (VBOOST - LDRV)</td>
<td>0.06</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>$V_{OL}$</td>
<td>Low-level output voltage, LDRV</td>
<td>$I_{LDRV} = 0.01\ \text{A}$, (VBOOST - LDRV)</td>
<td>1.35</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td><strong>BOOST REGULATOR</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$V_{BOOST}$</td>
<td>Output voltage</td>
<td>$V_{VDD} = 12\ \text{V}$</td>
<td>15.2</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td><strong>UVLO</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$V_{UVLO}$</td>
<td>Programmable UVLO threshold voltage</td>
<td>$R_{KFF} = 90.9\ \text{k}\Omega$, turn-on, $V_{VDD}$ rising</td>
<td>6.2</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Programmable UVLO hysteresis</td>
<td>$R_{KFF} = 90.9\ \text{k}\Omega$</td>
<td>1.10</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Fixed UVLO threshold voltage</td>
<td>$V_{VDD}$ rising</td>
<td>4.30</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Fixed UVLO hysteresis</td>
<td></td>
<td>275</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td><strong>POWER GOOD</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$V_{PGD}$</td>
<td>Powergood voltage</td>
<td>$I_{PGD} = 1\ \text{mA}$</td>
<td>370</td>
<td>550</td>
<td></td>
</tr>
<tr>
<td>$V_{FBH}$</td>
<td>High-level output voltage, FB</td>
<td></td>
<td>770</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>$V_{FBL}$</td>
<td>Low-level output voltage, FB</td>
<td></td>
<td>630</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td><strong>SENSE AMPLIFIER</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$V_{IO}$</td>
<td>Input offset voltage</td>
<td>$V_{SA+} = V_{SA-} = 1.25\ \text{V}$, Offset referenced to SA+ and SA-</td>
<td>-.9</td>
<td>mV</td>
<td></td>
</tr>
<tr>
<td>$A_{ODI}$</td>
<td>Differential gain</td>
<td>$V_{SA+} - V_{SA-} = 4.5\ \text{V}$</td>
<td>0.995</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>$V_{ICM}$</td>
<td>Input common mode range (4)</td>
<td>$V_{SA+} - V_{SA-} = 4.5\ \text{V}$</td>
<td>1000</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>$R_{S}$</td>
<td>Internal resistance for setting gain</td>
<td></td>
<td>14</td>
<td>26</td>
<td></td>
</tr>
<tr>
<td>$I_{OH}$</td>
<td>Output source current</td>
<td></td>
<td>20</td>
<td>15</td>
<td></td>
</tr>
<tr>
<td>$I_{OL}$</td>
<td>Output sink current</td>
<td></td>
<td>25</td>
<td>35</td>
<td></td>
</tr>
<tr>
<td><strong>GBWP</strong></td>
<td>Gain bandwidth (3)</td>
<td></td>
<td>2</td>
<td>MHz</td>
<td></td>
</tr>
<tr>
<td><strong>TERMAL SHUTDOWN</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Shutdown temperature threshold (3)</td>
<td></td>
<td>165</td>
<td>°C</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Hysteresis (3)</td>
<td></td>
<td>15</td>
<td>°C</td>
<td></td>
</tr>
</tbody>
</table>

(3) Ensured by design. Not production tested.
(4) 3 V at internal amplifier terminals, 6 V at SA+ and SA- pins.
### Table 1. TERMINAL FUNCTIONS

<table>
<thead>
<tr>
<th>TERMINAL NAME NO.</th>
<th>I/O</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>BOOM 11</td>
<td>I</td>
<td>The BOOST voltage is 8-V greater than the input voltage. The peak voltage on BOOST is equal to the SW node voltage plus the voltage present at DBP less the bootstrap diode drop. This drop can be 1.4 V for the internal bootstrap diode or 300 mV for an external schottkey diode. The voltage differential between this pin and SW is the available drive voltage for the high-side FET.</td>
</tr>
<tr>
<td>COMP 6</td>
<td>O</td>
<td>Output of the error amplifier, input to the PWM comparator. A feedback network is connected from this pin to the FB pin to compensate the overall loop. This pin is internally clamped to a 3.4-V maximum output drive capability for quicker recovery from a saturated feedback loop situation.</td>
</tr>
<tr>
<td>DBP 9</td>
<td>O</td>
<td>8-V regulator output used for the gate drive of the N-channel synchronous rectifier and as the supply for charging the bootstrap capacitor. This pin should be bypassed to ground with a 1.0-µF ceramic capacitor.</td>
</tr>
<tr>
<td>FB 5</td>
<td>I</td>
<td>Inverting input to the error amplifier. In normal operation the voltage on this pin is equal to the internal reference voltage, 0.7 V.</td>
</tr>
<tr>
<td>GND 3</td>
<td>-</td>
<td>Ground reference for the device.</td>
</tr>
<tr>
<td>HDRV 12</td>
<td>O</td>
<td>Floating gate drive for the high-side N-channel MOSFET. This pin switches from BOOST (MOSFET on) to SW (MOSFET off).</td>
</tr>
<tr>
<td>ILIM 14</td>
<td>I</td>
<td>Short circuit protection programming pin. This pin is used to set the overcurrent threshold. An internal current sink from this pin to ground sets a voltage drop across an external resistor connected from this pin to VDD. The voltage on this pin is compared to the voltage drop (V(<em>{\text{DD}}) - V(</em>{\text{SW}})) across the high side N-channel MOSFET during conduction. Just prior to the beginning of a switching cycle this pin is pulled to approximately V(_{\text{DD}})/2 and released when SW is within 2 V of VDD or after a timeout (the precondition time) - whichever occurs first. Placing a capacitor across the resistor from ILIM to VDD allows the ILIM threshold to decrease during the switch on time, effectively programming the ILIM blanking time. See Applications Information section.</td>
</tr>
<tr>
<td>KFF 15</td>
<td>I</td>
<td>A resistor is connected from this pin to VDD programs the amount of input voltage feed-forward. The current fed into this pin is used to control the slope of the PWM ramp and program undervoltage lockout. Nominal voltage at this pin is maintained at 400 mV.</td>
</tr>
<tr>
<td>LDRV 8</td>
<td>O</td>
<td>Gate drive for the N-channel synchronous rectifier. This pin switches from DBP (MOSFET on) to PGND (MOSFET off). For proper operation, the total gate charge of the MOSFET connected to LDRV should be less than 50nC.</td>
</tr>
<tr>
<td>LVBP 17</td>
<td>O</td>
<td>4.2-V reference used for internal device logic and analog functions. This pin should be bypassed to GND with a 0.1-µF ceramic capacitor. External loads less than 1 mA and electrically quiet may be applied.</td>
</tr>
<tr>
<td>PGD 18</td>
<td>O</td>
<td>This is an open drain output that pulls to ground when soft start is active, or when the FB pin is outside a ±10% band around the 700 mV reference voltage.</td>
</tr>
<tr>
<td>PGND 7</td>
<td>O</td>
<td>Power ground reference for the device. There should be a low-impedance path from this pin to the source(s) of the lower MOSFET(s).</td>
</tr>
<tr>
<td>RT 16</td>
<td>I</td>
<td>A resistor is connected from this pin to GND to set the switching frequency.</td>
</tr>
<tr>
<td>SA+ 20</td>
<td>I</td>
<td>Noninverting input of the remote voltage sense amplifier.</td>
</tr>
<tr>
<td>SA- 1</td>
<td>I</td>
<td>Inverting input of the remote voltage sense amplifier.</td>
</tr>
<tr>
<td>SAO 2</td>
<td>O</td>
<td>Output of the remote voltage sense amplifier.</td>
</tr>
<tr>
<td>SS 4</td>
<td>I</td>
<td>Soft-start programming pin. A capacitor connected from this pin to GND programs the soft-start time. The capacitor is charged with an internal current source of 12 µA. The resulting voltage ramp on the SS pin is used as a second non-inverting input to the error amplifier. The voltage at this error amplifier input is approximately 1 V less that on the SS pin. Output voltage regulation is controlled by the SS voltage ramp until the voltage on the SS pin reaches the internal offset voltage of 1 V plus the internal reference voltage of 700 mV. If SS is below the internal offset voltage of 1 V (300 mV minimum ensured), the resulting output voltage is zero. Also provides timing for fault recovery attempts. Maximum recommended capacitor is 22nF.</td>
</tr>
<tr>
<td>SW 10</td>
<td>I</td>
<td>This pin is connected to the switched node of the converter and used for overcurrent sensing as well as gate drive timing. This pin is also the return pin from the high-side FET for the floating high-side FET driver. A 1.5-Ω resistor is required in series with this pin to protect against substrate current issues.</td>
</tr>
<tr>
<td>SYNC 19</td>
<td>I</td>
<td>Logic input for pulse train to synchronize oscillator.</td>
</tr>
<tr>
<td>VDD 13</td>
<td>I</td>
<td>Supply voltage for the device.</td>
</tr>
</tbody>
</table>
APPLICATION INFORMATION

The TPS40074 allows the user to construct synchronous voltage mode buck converters with inputs ranging from 4.5 V to 28 V and outputs as low as 700 mV. Predictive gate drive circuitry optimizes switching delays for increased efficiency and improved converter output power capability. Voltage feed-forward is employed to ease loop compensation for wide input range designs and provide better line transient response.

An on-board unity gain differential amplifier is provided for remote sensing in applications that require the tightest load regulation. The TPS40074 incorporates circuitry to allow startup into a pre-existing output voltage without sinking current from the source of the pre-existing output voltage. This avoids damaging sensitive loads at startup. The controller can be synchronized to an external clock source or can free run at a user programmable frequency. An integrated power good indicator is available for logic (open drain) output of the condition of the output of the converter.

MINIMUM PULSE WIDTH

The TPS40074 has limitations on the minimum pulse width that can be used to design a converter. Reliable operation is guaranteed for nominal pulse widths of 150 ns and above. This places some restrictions on the conversion ratio that can be achieved at a given switching frequency. Figure 2 shows minimum output voltage for a given input voltage and frequency.

SLEW RATE LIMIT ON VDD

The regulator that supplies power for the drivers on the TPS40074 requires a limited rising slew rate on VDD for proper operation if the input voltage is above 10 V. If the slew rate is too great, this regulator can over shoot and damage to the part can occur. To ensure that the part operates properly, limit the slew rate to no more than 0.12 V/μs as the voltage at VDD crosses 8 V. If necessary, an R-C filter can be used on the VDD pin of the device. Connect the resistor from the VDD pin to the input supply of the converter. Connect the capacitor from the VDD pin to PGND. There should not be excessive (more than a 200-mV) voltage drop across the resistor in normal operation. This places some constraints on the R-C values that can be used. Figure 1 is a schematic fragment that shows the connection of the R-C slew rate limit circuit. Equation 1 and Equation 2 give values for R and C that limits the slew rate in the worst case condition.

![Diagram of TPS40074](UDG-05058)

Figure 1. Limiting the Slew Rate

Submit Documentation Feedback
APPLICATION INFORMATION (continued)

\[
R < \frac{0.2 \text{ V}}{f_{SW} \times Q_{g(TOT)} + I_{DD}} \tag{1}
\]

\[
C > \frac{V_{\text{VIN}} - 8 \text{ V}}{R \times SR} \tag{2}
\]

where

- \( V_{\text{VIN}} \) is the final value of the input voltage ramp
- \( f_{SW} \) is the switching frequency
- \( Q_{g(TOT)} \) is the combined total gate charge for both upper and lower MOSFETs (from MOSFET data sheet)
- \( I_{DD} \) is the TPS40074 input current (3.5 mA maximum)
- \( SR \) is the maximum allowed slew rate \( [12 \times 10^4] \) (V/s)

SETTING THE SWITCHING FREQUENCY (PROGRAMMING THE CLOCK OSCILLATOR)

The TPS40074 has independent clock oscillator and PWM ramp generator circuits. The clock oscillator serves as the master clock to the ramp generator circuit. Connecting a single resistor from \( R_T \) to ground sets the switching frequency of the clock oscillator. The clock frequency is related to \( R_T \) by:

\[
R_T = \left( \frac{1}{f_{SW}(\text{kHz}) \times 17.82 \times 10^{-6} - 23} \right) \text{k}\Omega \tag{3}
\]

![Minimum Output Voltage vs Frequency Graph](image-url)
PROGRAMMING THE RAMP GENERATOR CIRCUIT AND UVLO FUNCTION

The ramp generator circuit provides the actual ramp used by the PWM comparator and provides voltage feed-forward by varying the PWM ramp slope as the line voltage changes. As the input voltage to the converter increases, the slope of the PWM ramp increase by a proportionate amount. The programmable UVLO circuit works by monitoring the level reached by the PWM ramp during a clock cycle. The PWM ramp must reach approximately 1 V in amplitude during a clock cycle, or the converter is not be allowed to start. This programmable UVLO point is set via a single resistor (R_{KFF}) connected from KFF to VDD. R_{KFF}, V_{START} and R_{RT} are related by (approximately)

$$R_{KFF} = 0.131 \times R_T \times V_{UVLO(on)} - 1.61 \times 10^{-3} \times V_{UVLO(on)}^2 + 1.886 \times V_{UVLO} - 1.363 - 0.02 \times R_T - 4.87 \times 10^{-5} \times R_T^2$$

(4)

where
- \( V_{UVLO(on)} \) is in volts
- \( R_{KFF} \) and \( R_T \) are in k\( \Omega \)

This yields typical numbers for the programmed startup voltage. The minimum and maximum values may vary up \( \pm 15\% \) from this number. Figure 5 through Figure 7 show the typical relationship of \( V_{UVLO(on)}, V_{UVLO(off)} \) and \( R_{KFF} \) at three common frequencies.
Figure 5.  $f_{SW} = 300$ kHz

Figure 6.  $f_{SW} = 500$ kHz

Figure 7.  $f_{SW} = 750$ kHz
APPLICATION INFORMATION (continued)

The programmable UVLO circuit incorporates 20% hysteresis from the start voltage to the shutdown voltage. For example, if the startup voltage is programmed to be 10 V, the controller starts when $V_{DD}$ reaches 10 V and shuts down when $V_{DD}$ falls below 8 V. The maximum duty cycle begins to decrease as the input voltage rises to twice the startup voltage. Below this point, the maximum duty cycle is as specified in the electrical table. Note that with this scheme, the theoretical maximum output voltage that the converter can produce is approximately two times the programmed startup voltage. For design, set the programmed startup voltage equal to or greater than the desired output voltage divided by maximum duty cycle (85% for frequencies 500 kHz and below). For example, a 5-V output converter should not have a programmed startup voltage below 5.9 V. Figure 8 shows the theoretical maximum duty cycle (typical) for various programmed startup voltages.

Figure 8.
APPLICATION INFORMATION (continued)

Figure 9 shows the effect of changing input voltage on the duty cycle, and how that change takes place. The pulse width modulator (PWM) ramp input is generated using a current that is proportional to the current into the KFF pin. The TPS40074 holds this pin at a constant 400 mV, so connecting a resistor from KFF to the input power supply causes a current to flow into the KFF pin that is proportional to the input voltage. The slope of the ramp signal to the PWM is therefore proportional to the input voltage. This allows the duty cycle to change with variations in Vin without requiring much response from the error amplifier, resulting in very good line transient response. Another benefit is essentially constant PWM gain over the entire input voltage operating range. This makes the output control loop easier to design for a wide input range converter.

![Figure 9. Voltage Feed-Forward and PWM Duty Cycle Waveforms](VDG-03172)

PROGRAMMING SOFT START

TPS40074 uses a closed-loop approach to ensure a controlled ramp on the output during start-up. Soft-start is programmed by connecting an external capacitor (C_{SS}) from the SS pin to GND. This capacitor is charged by a fixed current, generating a ramp signal. The voltage on SS is level shifted down approximately 1 V and fed into a separate non-inverting input to the error amplifier. The loop is closed on the lower of the level shifted SS voltage or the 700-mV internal reference voltage. Once the level shifted SS voltage rises above the internal reference voltage, output voltage regulation is based on the internal reference. To ensure a controlled ramp-up of the output voltage the soft-start time should be greater than the L-C_{OUT} time constant or:

\[
t_{\text{START}} \geq 2\pi \times \sqrt{\frac{L}{C_{\text{OUT}}}} \quad \text{(seconds)}
\]

where

- L is the value of the filter inductor
- C_{OUT} is the value of the output capacitance
- t_{\text{START}} is the output ramp up-time

For a desired soft-start time, the soft-start capacitance, C_{SS}, can be found from:

\[
C_{\text{SS}} \times t_{\text{SS}} = \frac{i_{\text{SS}}}{V_{FB}}
\]

To ensure correct start up of the converter, the soft-start time is limited and can be calculated using Equation 7.
APPLICATION INFORMATION (continued)

\[ t_{\text{START}} \leq \frac{D_{\text{MIN}}}{f_{\text{SW}} \times 10^{-7}} \text{ ms} \]  

(7)

where
- \( D_{\text{MIN}} \) is the minimum operating duty cycle
- \( f_{\text{SW}} \) is the converter switching frequency

Please note: There is a direct correlation between \( t_{\text{START}} \) and the input current required during start-up. The lower \( t_{\text{START}} \) is, the higher the input current required during start-up since the output capacitance must be charged faster.

PROGRAMMING SHORT CIRCUIT PROTECTION

The TPS40074 uses a two-tier approach to short circuit protection. The first tier is a pulse-by-pulse protection scheme. Short circuit protection is implemented by sensing the voltage drop across the high-side MOSFET while it is turned on. The MOSFET drain to source voltage is compared to the voltage dropped across a resistor (\( R_{\text{ILIM}} \)) connected from VDD to the ILIM pin. The voltage drop across this resistor is produced by a constant current sink. If the voltage drop across the MOSFET exceeds the voltage drop across the ILIM resistor the switching pulse is immediately terminated. The MOSFET remains off until the next switching cycle is initiated.

In addition, just prior to the high-side MOSFET turning on, the ILIM pin is pulled down to approximately half of VDD. The ILIM pin is allowed to return to its nominal value after one of two events occur:
1. The SW node rises to within approximately 2 V of VDD
2. An internal timeout occurs, approximately 125-ns after ILIM is initially pulled down

If the SW node rises to within approximately 2-V of VDD, the device allows ILIM to go back to its nominal value. This is illustrated in Figure 10 A. T1 is the delay time from the internal PWM signal being asserted and the rise of SW. This includes the driver delay of 50 ns typical, and the turn on time of the high-side MOSFET. The MOSFET used should have a turn on time less than 75 ns. T2 is the reaction time of the sensing circuit that allows ILIM to start to return to its nominal value, typically 20ns.

Figure 10. Switching and Current Limit Waveforms and Timing Relationship
The second event that can cause ILIM to return to its nominal value is for an internal timeout to expire. This is illustrated in Figure 10 B as T3. Here SW never rises to VDD-2, for whatever reason, and the internal timer times out. This allows the ILIM pin to start its transition back to its nominal value.

Prior to ILIM starting back to its nominal value, short circuit sensing is not enabled. In normal operation, this insures that the SW node is at a higher voltage than ILIM when short circuit sensing starts, avoiding false trips while allowing for a quicker blanking delay than would ordinarily be possible. Placing a capacitor across RILIM sets an exponential approach to the normal voltage at the ILIM pin. This exponential “decay” of the short circuit threshold can be used to compensate for ringing on the SW node after its rising edge and to help compensate for slower turn-on MOSFETs. Choosing the proper capacitance requires care. If the capacitance is too large, the voltage at ILIM does not approach the desired short circuit level quickly enough, resulting in an apparent shift in short circuit threshold as pulse width changes.

The comparator that looks at ILIM and SW to determine if a short circuit condition exists has a clamp on its SW input. This clamp makes the SW node never appear to fall more than 1.4 V (approximately, could be as much as 2 V at –40°C) below VDD. While ILIM is more than 1.4 V below VDD short circuit sensing is effectively disabled, giving a programmable absolute blanking time. As a general rule, it is best to make the time constant of the R-C at the ILIM pin 20% or less of the nominal pulse width of the converter (See Equation 13)

The second tier protection incorporates a fault counter. The fault counter is incremented on each cycle with an overcurrent pulse and decremented on a clock cycle without an overcurrent pulse. When the counter reaches seven (7) a fault condition is declared by the controller. When this happens, the output drivers turn both MOSFETs off. Seven soft-start cycles are initiated (without activity on the HDRV and LDRV outputs) and the PWM is disabled during this period. The counter is decremented on each soft-start cycle. When the counter is decremented to zero the PWM is re-enabled and the controller attempts to restart. If the fault has been removed the output starts up normally. If the output fault is still present the counter counts seven overcurrent pulses and re-enters the second tier fault mode. Refer to Figure 11 for typical fault protection waveforms.

![Figure 11. Typical Fault Protection Waveforms](vdg-03174)
APPLICATION INFORMATION (continued)

The minimum short circuit limit threshold \( I_{SCP} \) depends on \( t_{\text{START}} \), \( C_{\text{OUT}} \), \( V_{\text{OUT}} \), and the load current at turn-on \( I_{\text{LOAD}} \):

\[
I_{SCP} > \frac{C_{\text{OUT}} \times V_{\text{OUT}}}{t_{\text{START}}} + I_{\text{LOAD}} \text{ (A)}
\]  

(8)

The short circuit limit programming resistor \( R_{\text{ILIM}} \) is calculated from:

\[
R_{\text{ILIM}} = \frac{100 \times \left( R_{\text{DS(onMAX)}} \times I_{\text{SCP}} + V_{\text{ILIM (ofst)}} \right) + 9 \times R_{\text{VDD}} \times I_{\text{RVDD}} + 4.5 \text{ V}}{109 \times I_{\text{ILIM}}} \text{ (Ω)}
\]  

(9)

where

- \( I_{\text{ILIM}} \) is the current into the ILIM pin (135 µA typical)
- \( V_{\text{ILIM (ofst)}} \) is the offset voltage of the ILIM comparator (-30 mV typical)
- \( I_{\text{SCP}} \) is the short-circuit protection current
- \( R_{\text{DS(onMAX)}} \) is the drain-to-source resistance of the high-side MOSFET
- \( R_{\text{VDD}} \) is the slew rate limit resistor if used
- \( I_{\text{RVDD}} \) is the current through \( R_{\text{VDD}} \) and can be calculated using Equation 10.

\[
I_{\text{RVDD}} = f_{\text{SW}} \times Q_{g(TOT)} + I_{\text{DD}} \text{ (A)}
\]  

(10)

where

- \( f_{\text{SW}} \) is the switching frequency
- \( Q_{g(TOT)} \) is the combined total gate charge fro both upper and lower MOSFETs (from MOSFET datasheet)
- \( I_{\text{DD}} \) is the TPS40074 input current (3.5-mA maximum)

To find the range of the short circuit threshold values use the following equations.

\[
I_{\text{SCP(max)}} = \frac{1.09 \times I_{\text{ILIM(max)}} \times R_{\text{ILIM}} - 0.09 \times R_{\text{VDD}} \times I_{\text{RVDD}} - 0.045 + 50 \text{ mV}}{R_{\text{DS(onMIN)}}} \text{ (A)}
\]  

(11)

\[
I_{\text{SCP(min)}} = \frac{1.09 \times I_{\text{ILIM(min)}} \times R_{\text{ILIM}} - 0.09 \times R_{\text{VDD}} \times I_{\text{RVDD}} - 0.045 + 10 \text{ mV}}{R_{\text{DS(onMAX)}}} \text{ (A)}
\]  

(12)

The TPS40074 provides short-circuit protection only. As such, it is recommended that the minimum short circuit protection level be placed at least 20% above the maximum output current required from the converter. The maximum output of the converter should be the steady state maximum output plus any transient specification that may exist.

The ILIM capacitor maximum value can be found from:

\[
C_{\text{ILIM(max)}} = \frac{V_{\text{OUT}} \times 0.2}{V_{\text{IN}} \times R_{\text{ILIM}} \times f_{\text{SW}}} \text{ (Farads)}
\]  

(13)

Note that this is a recommended maximum value. If a smaller value can be used, it should be to improve protection. For most applications, consider using half the maximum value shown in Equation 13.

BOOST AND DBP BYPASS CAPACITANCE

The BOOST capacitance provides a local, low-impedance flying source for the high-side driver. The BOOST capacitor should be a good quality, high-frequency ceramic capacitor. A minimum value of 100-nF is suggested.

The DBP capacitor has to provide energy storage for switching both the synchronous MOSFET and the high-side MOSFET (via the BOOST capacitor). The suggested value for this capacitor is 1-µF ceramic, minimum.
INTERNAL REGULATORS

The internal regulators are linear regulators that provide controlled voltages for the drivers and the internal circuitry to operate from. The low-side driver operates directly from the 8-V regulator supply while the high-side driver bootstrap capacitor is charged from this supply. The actual voltage delivered to the high-side driver is the voltage on the DBP pin less any drop from the bootstrap diode. If the internal bootstrap diode is used, the drop across that diode is nominally 1.4 V at room temperature. This regulator has two modes of operation. At voltages below 8.5 V on VDD, the regulator is in a low dropout mode of operation and tries to provide as little impedance as possible from VDD to DBP. When VDD is above 10 V, the regulator regulates DBP to 8 V. Between these two voltages, the regulator is in whatever state it was in when VDD entered this region. The LVBP pin is connected to a 4.2-V regulator that supplies power for the internal control circuitry. Small amounts of current can be drawn from these pins for other external circuit functions, as long as power dissipation in the controller chip remains at acceptable levels and junction temperature does not exceed 125°C. Any external load connected to LVBP should be electrically quiet to avoid degrading performance of the TPS40074. Typical output voltages for these two regulators are shown in Figure 12 and Figure 13.

DIFFERENTIAL SENSE AMPLIFIER

The TPS40074 has an on board differential amplifier intended for use as a remote sensing amplifier for the output voltage. Use of this amplifier for remote sensing eliminates load regulation issues due to voltage drops that occur between the converter and the actual point of load. The amplifier is powered from the DBP pin and can be used to monitor output voltages up to 6 V with a DBP voltage of 8 V. For lower DBP voltages, the sense amplifier can be used to monitor output voltages up to 2-V below the DBP voltage. The internal resistors used to configure the amplifier for unity gain match each other closely, but their absolute values can vary as much as 30%, so adding external resistance to alter the gain is not accurate in a production environment.
APPLICATION INFORMATION (continued)

SYNCHRONIZATION
The SYNC pin accepts logic level signals and is used to synchronize the TPS40074 to an external clock source. Synchronization occurs on the rising edge of the signal at the SYNC pin. There is a fixed delay of approximately 300 ns from the rising edge of the waveform at SYNC to the HDRV output turning on the high-side FET. The pin may be left floating in this function is not used, or it may be connected to GND. The frequency of the external clock must be greater than the free running frequency of the device as set by the resistor on the RT pin (R_{RT}). This pin requires a totem pole drive, or open collector/drain if pull up resistor to either LVBP or a separate supply between 2.5 V and 5 V is used. Synchronization does not affect the modulator gain due to the voltage feed forward circuitry. The programmable UVLO thresholds are affected by synchronization. The thresholds are shifted by the ratio of the sync frequency to the free running frequency of the converter. For example, synchronizing to a frequency 20% higher than the free running frequency results in the programmable UVLO thresholds shifting up 20% from their calculated free run values. The synchronization frequency should be kept less than 1.5 times the free run frequency for best performance, although higher multipliers can be used.

POWERGOOD OPERATION
The PGD pin is an open drain output that actively pulls to GND if any of the following conditions are met (assuming that the input voltage is above 4.5 V)
- Soft-start is active (V_{VSS} < 3.5 V)
- V_{FB} < 0.63 V
- V_{FB} > 0.77 V
- Programmable UVLO condition not satisfied (V_{IN} below programmed level)
- Overcurrent condition exists
- Die temperature is greater than 165°C

PRE-BIASED OUTPUTS
Some applications require that the converter not sink current during startup if a pre-existing voltage exists at the output. Since synchronous buck converters inherently sink current some method of overcoming this characteristic must be employed. Applications that require this operation are typically power rails for a multi supply processor or ASIC. The method used in this controller, is to not allow the low side or rectifier FET to turn on until there the output voltage commanded by the start up ramp is higher than the pre-existing output voltage. This is detected by monitoring the internal pulse width modulator (PWM) for its first output pulse. Since this controller uses a closed loop startup, the first output pulse from the PWM does not occur until the output voltage is commanded to be higher than the pre-existing voltage. This effectively limits the controller to sourcing current only during the startup sequence.

If the pre-existing voltage is higher that the intended regulation point for the output of the converter, the converter starts and sinks current when the soft-start time has completed

OUTPUT RIPPLE CONSIDERATION
In addition to the typical output ripple associated with switching converters, (which can vary from 5 mV to 150 mV) the TPS40074 exhibits a low-frequency ripple from 5 mV to 50 mV. The ripple, a consequence of the charge pump in the driver supply regulator, is well bounded under changes in line, load, and temperature. The ripple frequency does vary with the converter switching frequency and can vary from 10 kHz to 60 kHz.
APPLICATION INFORMATION (continued)

TPS40074 POWER DISSIPATION

The power dissipation in the TPS40074 is largely dependent on the MOSFET driver currents and the input voltage. The driver current is proportional to the total gate charge, Qg, of the external MOSFETs. Driver power (neglecting external gate resistance) can be calculated from:

\[ P_D = Q_g \times V_{DR} \times f_{SW} \] (Watts/driver)

where

- \( V_{DR} \) is the driver output voltage

The total power dissipation in the TPS40074, assuming the same MOSFET is selected for both the high-side and synchronous rectifier is described in Equation 15.

\[ P_T = \left( \frac{2 \times P_D}{V_{DR}} + I_Q \right) \times V_{IN} \] (Watts)

or

\[ P_T = \left( 2 \times Q_g \times f_{SW} + I_Q \right) \times V_{IN} \] (Watts)

where

- \( I_Q \) is the quiescent operating current (neglecting drivers)

The maximum power capability of the TPS40074 PowerPAD package is dependent on the layout as well as air flow. The thermal impedance from junction to air ambient assuming 2-oz. copper trace and thermal pad with solder and no air flow is \( \theta_{JA} = 60 \, \text{°C/W} \)

The maximum allowable package power dissipation is related to ambient temperature by Equation 17.

\[ P_T = \frac{T_J - T_A}{\theta_{JA}} \] (Watts)

Substituting Equation 17 into Equation 16 and solving for \( f_{SW} \) yields the maximum operating frequency for the TPS4007x. The result is described in Equation 18.

\[ f_{SW} = \left( \frac{\left[ \frac{T_J - T_A}{\theta_{JA}} - I_Q \right]}{2 \times Q_g} \right) \] (Hz)

BOOST DIODE

The TPS40074 has internal diodes to charge the boost capacitor connected from SW to BOOST. The drop across this diode is rather large at 1.4-V nominal at room temperature resulting in the drive voltage to the high-side MOSFET being reduced by this amount from the DBP voltage. If this drop is too large for a particular application, an external diode may be connected from DBP (anode) to BOOST (cathode). This provides significantly improved gate drive for the high-side MOSFET, especially at lower input voltages.

LOW VOLTAGE OPERATION

If the programmable UVLO is set to less than 6.5 V nominal, connect a 330-kΩ resistor across the soft-start capacitor. This eliminates a race condition inside the device that can lead to an output voltage overshoot on power down of the part.
APPLICATION INFORMATION (continued)

GROUNDING AND BOARD LAYOUT

The TPS40074 provides separate signal ground (GND) and power ground (PGND) pins. Care should be given to proper separation of the circuit grounds. Each ground should consist of a plane to minimize its impedance if possible. The high power noisy circuits such as the output, synchronous rectifier, MOSFET driver decoupling capacitor (DBP), and the input capacitor should be connected to PGND plane.

Sensitive nodes such as the FB resistor divider and RT should be connected to the GND plane. The GND plane should only make a single point connection to the PGND plane. It is suggested that the GND pin be tied to the copper area for the PowerPAD underneath the chip. Tie the PGND to the PowerPAD copper area as well and make the connection to the power circuit ground from the PGND pin. Reference the output voltage divider to the GND pin.

Component placement should ensure that bypass capacitors (LVPB and DBP) are located as close as possible to their respective power and ground pins. Also, sensitive circuits such as FB, RT and ILIM should not be located near high dv/dt nodes such as HDRV, LDRV, BOOST, and the switch node (SW). Failure to follow careful layout practices results in sub-optimal operation.

SYNCHRONOUS RECTIFIER CONTROL

Table 2 describes the state of the rectifier MOSFET control under various operating conditions.

<table>
<thead>
<tr>
<th>SOFT-START</th>
<th>NORMAL</th>
<th>FAULT (FAULT RECOVERY IS SAME AS SOFT-START)</th>
<th>OVERVOLTAGE</th>
</tr>
</thead>
<tbody>
<tr>
<td>Off until first high-side pulse is detected, then on when high-side MOSFET is off</td>
<td>Turns off at the start of a new cycle. Turns on when the high-side MOSFET is turned off</td>
<td>OFF</td>
<td>Turns OFF only at start of next cycle ON if duty cycle is &gt; 0</td>
</tr>
</tbody>
</table>

For proper operation, the total gate charge of the MOSFET connected to LDRV should be less than 50nC.
DESIGN EXAMPLE

1. SPECIFICATIONS

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>INPUT CURRENT</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>( V_{IN} ) Input voltage</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>( V_{O} ) Output voltage</td>
<td>( I_{OUT} = 10 , A )</td>
<td>10.8</td>
<td>12.0</td>
<td>13.2</td>
<td>V</td>
</tr>
<tr>
<td>Regulation</td>
<td></td>
<td></td>
<td>1.47</td>
<td></td>
<td></td>
</tr>
<tr>
<td>( V_{RIPPLE} ) Output ripple voltage</td>
<td>( I_{O(max)} = 15 , A )</td>
<td></td>
<td></td>
<td>30</td>
<td>mV</td>
</tr>
<tr>
<td>( V_{OVER} ) Output overshoot</td>
<td>( I_{STEP} = 8 , A )</td>
<td></td>
<td></td>
<td>50</td>
<td></td>
</tr>
<tr>
<td>( V_{UNDER} ) Output undershoot</td>
<td>( I_{STEP} = 8 , A )</td>
<td></td>
<td></td>
<td>50</td>
<td></td>
</tr>
<tr>
<td>( I_{LOAD} ) Output current</td>
<td></td>
<td></td>
<td></td>
<td>0</td>
<td>15</td>
</tr>
<tr>
<td>( I_{SCP} ) Short circuit current trip point</td>
<td></td>
<td></td>
<td>16</td>
<td></td>
<td>30</td>
</tr>
<tr>
<td>( \eta ) Efficiency</td>
<td>( V_{IN} = 12 , V, , I_{LOAD} = 15 , A )</td>
<td></td>
<td></td>
<td>85%</td>
<td></td>
</tr>
<tr>
<td>( f_{SW} ) Switching frequency</td>
<td></td>
<td></td>
<td></td>
<td>400</td>
<td>kHz</td>
</tr>
</tbody>
</table>

2. SCHEMATIC

Figure 14. TPS40074 Reference Design Schematic
3. COMPONENT SELECTION

3.1 Power Train Components
Designers familiar with the buck converter can skip to section 3.2 Component Selection for TPS40074.

3.1.1 Output Inductor, \( L_0 \)
The output inductor is one of the most important components to select. It stores the energy necessary to keep the output regulated when the switch MOSFET is turned off. The value of the output inductor dictates the peak and RMS currents in the converter. These currents are important when selecting other components. Equation 19 can be used to calculate a value for \( L \).

\[
L = \frac{V_O}{V_{IN(max)}} \times \frac{\left( V_{IN(max)} - V_O \right)}{f_{SW} \times \Delta I}
\]  
(19)

\( \Delta I \) is the allowable ripple in the inductor. Selecting \( \Delta I \) also sets the output current when the converter goes into discontinuous mode (DCM) operation. Since this converter utilizes MOSFETs for the rectifier, DCM is not a major concern. Select \( \Delta I \) to be between 20% and 30% of maximum \( I_{LOAD} \). For this design, \( \Delta I \) of 3 A was selected. The calculated \( L \) is 1.1 \( \mu \)H. A standard inductor with value of 1.0 \( \mu \)H was chosen. This increases \( \Delta I \) by about 10% to 3.3 A.

With this \( \Delta I \) value, calculate the RMS and peak current flowing in \( L_0 \). Note this peak current is also seen by the switching MOSFET and synchronous rectifier.

\[
I_{LOAD,RMS} = \sqrt{I_{LOAD}^2 + \frac{\Delta I^2}{12}} = 15.03 \text{ A}
\]  
(20)

\[
I_{PK} = I_{LOAD} + \frac{\Delta I^2}{2} = 16.65 \text{ A}
\]  
(21)

3.1.2 Output Capacitor, \( C_O \), ELCO and MLCC
Several parameters must be considered when selecting the output capacitor. The capacitance value should be selected based on the output overshoot, \( V_{OVER} \), and undershoot, \( V_{UNDER} \), during a transient load, \( I_{STEP} \), on the converter. The equivalent series resistance (ESR) is chosen to allow the converter meet the output ripple specification, \( V_{RIPPLE} \). The voltage rating must be greater than the maximum output voltage. Other parameters to consider are: equivalent series inductance which is important in fast transient load situations. Also size and technology can be factors when choosing the output capacitor. In this design a large capacitance electrolytic type capacitor, \( C_O \), ELCO, is used to meet the overshoot and undershoot specifications. Its ESR is chosen to meet the output ripple specification. While a smaller multiple layer ceramic capacitor, \( C_O \) MLCC, is used to filter high frequency noise.

The minimum required capacitance and maximum ESR can be calculated using the equations below.

\[
C_O > \frac{L \times I_{STEP}^2}{2 \times V_{UNDER} \times D_{MAX} \times (V_{IN} - V_O)}
\]  
(22)

\[
C_O > \frac{L \times I_{STEP}^2}{2 \times V_{OVER} \times V_O}
\]  
(23)

\[
ESR < \frac{V_{RIPPLE}}{\Delta I}
\]  
(24)

Using Equation 22 through Equation 24, the capacitance for \( C_O \) should be greater than 495 \( \mu \)F and its ESR should be less than 9.1m\( \Omega \). The 1000 \( \mu \)F/25 V capacitor from Rubycon’s MBZ or Panasonic’s series EEU-FL was chosen. Its ESR is 19 m\( \Omega \), so two in parallel are used. The slightly higher ESR is offset by the four times increase in capacitance. A 2.2 \( \mu \)F/16 V MLCC is also added in parallel to reduce high frequency noise.
3.1.3. Input Capacitor, C_{in}, ELCO and MLCC

The input capacitor is selected to handle the ripple current of the buck stage. Also a relative large capacitance is used to keep the ripple voltage on the supply line low. This is especially important where the supply line is high impedance. It is recommended that the supply line be kept low impedance. The input capacitor ripple current can be calculated using Equation 25.

\[
I_{\text{CAP(RMS)}} = \sqrt{\left(I_{\text{LOAD(max)}} - I_{\text{IN(avg)}}\right)^2 + \frac{\Delta I^2}{12}} \times D + I_{\text{IN(avg)}}^2 \times (1 - D)
\]  

(25)

where

- \(I_{\text{IN(avg)}}\) is the average input current

This is calculated simply by multiplying the output DC current by the duty cycle. The ripple current in the input capacitor is 5.05 A. A 1206 MLCC using X7R material has a typical dissipation factor of 5%. For a 2.2 µF capacitor at 400 kHz the ESR is approximately 7.2 mΩ. If two capacitors are used in parallel the power dissipation in each capacitor is less than 46 mW.

A 470 µF/16 V electrolytic capacitor is added to maintain the voltage on the input rail.

3.1.4. Switching MOSFET, QSW

The following key parameters must be met by the selected MOSFET.

- Drain source voltage, \(V_{DS}\), must be able to withstand the input voltage plus spikes that may be on the switching node. For this design a \(V_{DS}\) rating of 25 V to 30 V is recommended.
- Drain current, \(I_D\), at 25°C, must be greater than that calculated using Equation 26. For this design, \(I_D\) should be greater than 5 A.

\[
I_D = \sqrt{\frac{V_O}{V_{\text{IN(min)}}} \times \left(I_{\text{LOAD(max)}}^2 + \frac{\Delta I^2}{12}\right)}
\]  

(26)

- Gate source voltage, \(V_{GS}\) must be able to withstand the gate voltage from the control device. For the TPS40074 this is 9 V.

Once the above boundary parameters are defined the next step in selecting the switching MOSFET is to select the key performance parameters. Efficiency is the performance characteristic which drives the other selection criteria. Target efficiency for this design is 90%. Based on 1.5-V output and 15 A this equates to a power loss in the converter of 2.5 W. Using this figure a target of 0.5 W dissipated in the switching MOSFET was chosen.
Equation 27 through Equation 30 can be used to calculate the power loss, $P_{QSW}$, in the switching MOSFET

$$P_{QSW} = P_{QSW(CON)} + P_{QSW(SW)} + P_{QSW(GATE)}$$

(27)

$$P_{QSW(CON)} = R_{DS(on)} \times I_D^2 = R_{DS(on)} \times \frac{V_O}{V_{IN}} \times \left( \frac{I_{LOAD}^2 + 4 \Delta I^2}{12} \right)$$

(28)

$$P_{QSW(SW)} = V_{IN} \times f_{SW} \times \left[ \left( \frac{I_{LOAD} + 2 \Delta I}{2} \right) \times \frac{Q_{gs1} + Q_{gd}}{I_g} + \frac{Q_{OSS(SW)} + Q_{OSS(SR)}}{2} \right]$$

(29)

$$P_{QSW(GATE)} = Q_{g(TOT)} \times V_g \times F_{SW}$$

(30)

where

- $P_{QSW(CON)}$ = conduction losses
- $P_{QSW(SW)}$ = switching losses
- $P_{QSW(GATE)}$ = gate drive losses
- $Q_{gs}$ = drain source charge or Miller charge
- $Q_{gs1}$ = gate source post threshold charge
- $I_g$ = gate drive current
- $Q_{OSS(SW)}$ = synchronous MOSFET output charge
- $Q_{OSS(SR)}$ = synchronous MOSFET output charge
- $Q_{g(TOT)}$ = total gate charge from zero volts to the gate voltage
- $V_g$ = gate voltage

If the total estimated loss is split evenly between conduction and switching losses, Equation 27 and Equation 28 yields preliminary values for $R_{DS(on)}$ and $(Q_{gs1} + Q_{gd})$. Note output losses due to $Q_{OSS}$ and gate losses have been ignored here. Once a MOSFET is selected these parameters can be added.

The switching MOSFET for this design should have an $R_{DS(on)}$ of less than 9 mΩ. The sum of $Q_{gd}$ and $Q_{gs}$ should be approximately 4 nC.

It is not always possible to get a MOSFET which meets both these criteria so a compromise may have to be made. Also by selecting different MOSFETs close to this criteria and calculating power loss the final selection can be made. It was found that the PH6325L MOSFET from Philips semiconductor gave reasonable results. This device has an $R_{DS(on)}$ of 6.3 mΩ and a $(Q_{gs1} + Q_{gd})$ of 5.9 nC. The estimated conduction losses are 0.178 W and the switching losses are 0.270 W. This gives a total estimated power loss of 0.448 W versus 0.5 W for our initial boundary condition. Note this does not include gate losses of approximately 10 mW and output losses of less than 1 mW.

3.1.5 Rectifier MOSFET, QSR

Similar criteria can be used for the rectifier MOSFET. There is one significant difference. Due to the body diode conducting, the rectifier MOSFET switches with near zero voltage across its drain and source so effectively with near zero switching losses. However, there are some losses in the body diode. These are minimized by reducing the delay time between the transition from the switching MOSFET turn off to rectifier MOSFET turn on and vice versa. The TPS40074 incorporates TI's proprietary predictive gate drive which helps reduce this delay to between 10 ns and 20 ns.
The calculations for the losses in the rectifier MOSFET are show in Equation 31 through Equation 34.

\[ P_{QSR} = P_{QSR(CON)} + P_{DIODE} + P_{QSR(GATE)} \]  

\[ P_{QSR(CON)} = R_{DS(on)} \times \left( 1 - \frac{V_O}{V_{IN}} - (t_1 + t_2) \times f_{SW} \right) \times \left( I_{LOAD}^2 + \frac{\Delta I^2}{12} \right) \]  

\[ P_{DIODE} = V_f \times I_{LOAD} \times (t_1 + t_2) \times f_{SW} \]  

\[ P_{QSR(GATE)} = Q_g(TOTAL) \times V_g \times f_{SW} \]  

where

- \( P_{DIODE} \) = body diode losses
- \( t_1 \) = body diode conduction prior to turn on of channel = 10 ns for predictive gate drive
- \( t_2 \) = body diode conduction after turn off of channel = 10 ns for predictive gate drive
- \( V_f \) = body diode forward voltage

Estimating the body diode losses based on a forward voltage of 1.2 V gives 0.142 W. The gate losses are unknown at this time so assume 0.1 W gate losses. This leaves 0.258 W for conduction losses. Using this figure a target \( R_{DS(on)} \) of 1.1 m\( \Omega \) was calculated. This is an extremely low value. It is not possible to meet this without paralleling multiple MOSFETs. Paralleling MOSFETs increases the gate capacitance and slows down switching speeds. This increases body diode and gate losses.

The PH2625L from Philips was chosen. Using the parameters from its data sheet the actual expected power losses were calculated. Conduction loss is 0.527 W, body diode loss is 0.142 W and the gate loss was 0.174 W. This totals 0.843 W associated with the rectifier MOSFET. This is somewhat greater than the initial allowance. Because of this the converter may not hit its efficiency figure at the maximum load.

Two other criteria should be verified before finalizing on the rectifier MOSFET. One is the requirement to ensure that predictive gate drive functions correctly. The maximum turn off delay of the PH2625L is 67 ns. The minimum turn on delay of the PH6325L is 25 ns. These devices easily meet the 100 ns difference requirement.

Secondly the ratio between \( C_{gs} \) and \( C_{gd} \) should be greater than 1. The \( C_{gs} \) of the PH2625L is 2133 pF and the \( C_{gd} \) is 1622 pF, so the \( C_{gs}:C_{gd} \) ratio is 1.3:1. This helps reduce the risk of \( dv/dt \) induced turn on of the rectifier MOSFET. If this is likely to be a problem a small resistor may be added in series with the boost capacitor, \( C_{BOOST} \).

### 3.2 Component Selection for TPS40074

#### 3.2.1 Timing Resistor, \( R_T \)

The timing resistor is calculated using the following equation.

\[ R_T = \frac{1}{f_{SW} \times 17.82 \times 10^{-6}} - 23 \]  

This gives a resistor value of 117.3 k\( \Omega \). Using the E24 range of resistor values a 118-k\( \Omega \) resistor was selected. The nominal frequency using this resistor is 398 kHz.

#### 3.2.2 Feed Forward and UVLO Resistor, \( R_{KFF} \)

A resistor connected to the KFF pin of the device feeds into the ramp generator. This resistor provides current into the ramp generator proportional to the input voltage. The ramp is then adjusted to compensate for different input voltages. Is provides the voltage feed forward feature of the TPS40074.

The same resistor also sets the under voltage lock out point. The input start voltage should be used to calculate a value for \( R_{KFF} \). For this converter the minimum input voltage is 10.8 V however due to tolerances in the device, a start voltage of 15% less than the minimum input voltage is selected. The start voltage for \( R_{KFF} \) calculation is 9.18 V. Using Equation 36 \( R_{KFF} \) can be selected.

\[ R_{KFF} = 0.131 \times R_T \times V_{UVLO(on)} - 1.61 \times 10^{-3} \times V_{UVLO(on)}^2 + 1.886 \times V_{UVLO} - 1.363 - 0.02 \times R_T - 4.87 \times 10^{-5} \times R_T^2 \]  

where
• \( V_{\text{UVLO(on)}} \) is in volts
• \( R_{\text{EFF}} \) and \( R_T \) are in kΩ

This equation gives a \( R_{\text{EFF}} \) value of 154.7 kΩ. The closest lower standard value should be selected. For this design and using E24 resistor range 154 kΩ was chosen. This yields a typical start voltage of 9.14 V.

### 3.2.3 Soft Start Capacitor

It is good practice to limit the rise time of the output voltage. This helps prevent output overshoot and possible damage to the load. The selection of the soft start time is arbitrary, but it must meet one condition; it should be greater than the time constant of the output filter, \( L \) and \( C_O \). This time is given by Equation 37

\[
t_{\text{START}} \geq 2\pi \times \sqrt{L \times C_O}
\]  
(37)

The soft-start time must be greater than 0.281 ms. A time of 1 ms was chosen, this time also helps keep the initial input current during start up low. The value of \( C_{\text{SS}} \) can be calculated using Equation 38.

\[
C_{\text{SS}} \geq \frac{12 \times 10^{-6}}{0.7} \times t_{\text{START}}
\]  
(38)

\( C_{\text{SS}} \) should be greater than 17 nF, a 22 nF MLCC was chosen. The calculated start time using this capacitor is 1.28 ms.

### 3.2.4 Short Circuit Protection, \( R_{\text{ILIM}} \) and \( C_{\text{ILIM}} \)

Short circuit protection is programmed using the \( R_{\text{ILIM}} \) resistor. Selection of this resistor depends on the \( R_{\text{DS(on)}} \) of the switching MOSFET selected and the required short circuit current trip point, \( I_{\text{SCP}} \). The minimum \( I_{\text{SCP}} \) is limited by the inductor peak current, the output voltage, the output capacitor and the soft start time. Their relationship is given by Equation 39. A short circuit current trip point greater than that calculated by this equation should be used.

\[
I_{\text{SCP}} \geq \frac{C_O \times V_{\text{OUT}}}{t_{\text{START}}} + I_{\text{LOAD}} + \frac{\Delta I}{2}
\]  
(39)

The minimum short circuit current trip point for this design is 16.65 A. This value is used in Equation 40 to calculate the minimum \( R_{\text{ILIM}} \) value.

\[
R_{\text{ILIM}} = \frac{100 \times \left( R_{\text{DS(on)MAX}} \times I_{\text{SCP}} + V_{\text{ILIM(min)}} \right)}{109 \times I_{\text{ILIM(max)}}} + 4.5 \text{ V}
\]  
(40)

\( R_{\text{ILIM}} \) is calculated to be 1.59 kΩ. The closest standard value greater than 1.59 kΩ is chose, this is 1.62 kΩ. To verify that the short circuit current requirements are met the minimum and maximum short circuit current can be calculated using Equation 41 and Equation 42.

\[
I_{\text{SCP(min)}} = \frac{1.09 \times I_{\text{ILIM(min)}} \times R_{\text{ILIM}} - 0.045 \text{ V} - V_{\text{ILIM(max)}}}{R_{\text{DS(on)MAX}}}
\]  
(41)

\[
I_{\text{SCP(max)}} = \frac{1.09 \times I_{\text{ILIM(max)}} \times R_{\text{ILIM}} - 0.045 \text{ V} - V_{\text{ILIM(min)}}}{R_{\text{DS(on)MIN}}}
\]  
(42)

The minimum \( I_{\text{SCP}} \) is 17.05 A and the maximum is 47.04 A.

It is recommended to add a small capacitor, \( C_{\text{ILIM}} \), across \( R_{\text{ILIM}} \). The value of this capacitor should be less than that calculated in Equation 43.

\[
C_{\text{ILIM(max)}} = \frac{V_O \times 0.2}{V_{\text{IN}} \times R_{\text{ILIM}} \times t_{\text{SW}}}
\]  
(43)

This equation yields a maximum \( C_{\text{ILIM}} \) of 38 pF. A value half this is chosen, 22 pF.

### 3.2.5 Voltage Decoupling Capacitors, \( C_{\text{DBP}}, C_{\text{LVBP}} \) and \( C_{\text{VDD}} \)

Several pins on the TPS40074 have DC voltages. It is recommended to add small decoupling capacitors to these pins. Below is a list of the recommended values.
• $C_{DBP} = 1.0 \mu F$
• $C_{LVBP} = 0.1 \mu F$
• $C_{VDD} = 4.7 \mu F$

3.2.6 Boost Voltage, $C_{BOOST}$ and $D_{BOOST}$ (optional)

A capacitor charge pump or boost circuit is required to drive an N-channel MOSFET in the switch location of a buck converter. The TPS40074 contains the elements for this boost circuit. The designer just has to add a capacitor, $C_{BOOST}$, from the switch node of the buck power stage to the BOOST pin of the device. Selection of this capacitor is based on the total gate charge of the switching MOSFET and the allowable ripple on the boost voltage, $\Delta V_{BOOST}$. A ripple of 0.15 V is assumed for this design. Using these two parameters and Equation 44 the minimum value for $C_{BOOST}$ can be calculated.

$$C_{BOOST} > \frac{Q_{g(TOTAL)}}{\Delta V_{BOOST}}$$  \hspace{1cm} (44)

The total gate charge of the switching MOSFET is 13.3 nC. A minimum $C_{BOOST}$ of 0.089 $\mu F$ is required. A 0.1 $\mu F$ capacitor was chosen.

This capacitor must be able to withstand the maximum voltage on DBP (10 V in this instance). A 50 V capacitor is used for expediency.

To reduce losses in the TPS40074 and to increase the available gate voltage for the switching MOSFET an external diode can be added between the DBP pin and the BOOST pin of the device. A small signal schottky should be used here, such as the BAT54.

3.3 Closing the Feedback Loop, $R_{Z1}$, $R_{P1}$, $R_{PZ2}$, $R_{SET1}$, $R_{SET2}$, $C_{Z2}$, $C_{P2}$ and $C_{PZ1}$

A graphical method is used to select the compensation components. This is a standard feedforward buck converter. Its PWM gain is shown in Equation 45.

$$K_{PWM} = \frac{V_{UVLO}}{1 V}$$  \hspace{1cm} (45)

The gain of the output L-C filter is given by Equation 46

$$K_{LC} = \frac{\left(1 + s \times ESR \times C_O\right)}{1 + s \times \left(\frac{L}{R_{LOAD}}\right) + s^2 \times L \times C_O}$$  \hspace{1cm} (46)

The PWM and LC gain is, shown in Equation 47.

$$G_e(s) = K_{PWM} \times K_{LC} = \frac{V_{UVLO}}{1 V} \times \frac{\left(1 + s \times ESR \times C_O\right)}{1 + s \times \left(\frac{L}{R_{LOAD}}\right) + s^2 \times L \times C_O}$$  \hspace{1cm} (47)

To describe this in a Bode plot, the DC gain must be expressed in dB. The DC gain is equal to $K_{PWM}$. To express this in dB we take its LOG and multiple by 20. For this converter the DC gain is shown in Equation 48.

$$DCGAIN = 20 \times \text{LOG} \left(\frac{V_{UVLO}}{1 V}\right) = 20 \times \text{LOG}(9.14) = 19.3 \text{ dB}$$  \hspace{1cm} (48)

The pole and zero frequencies should be calculated, also. A double pole is associated with the L-C and a zero is associated with the ESR of the output capacitor. The frequency at where these occur can be calculated using the following two equations.
\[ f_{LC\_Pole} = \frac{1}{2\pi \sqrt{L \times C_O}} = 3559 \text{ Hz} \]  

(49)

\[ f_{ESR\_Zero} = \frac{1}{2\pi \times ESR \times C_O} = 8377 \text{ Hz} \]  

(50)

The resulting bode plot is shown in Figure 15.

![Figure 15. PWM and LC Filter Gain](image)

The next step is to establish the required compensation gain to achieve the desired overall system response. The target response is to have the crossover frequency between 1/10 to 1/4 times the switching frequency. To have a phase margin greater than 45° and a gain margin greater than 6 dB.

A Type III compensation network, as shown in Figure 16, was used for this design. This network gives the best overall flexibility for compensating the converter.

![Figure 16. Type III Compensation with TPS40074](image)

A typical bode plot to this type of compensation network is shown in Figure 17.
The high frequency gain and the break (pole and zero) frequencies are calculated using the following equations.

\[ V_O = V_{FB} \times \frac{R_{Z1} + R_{SET}}{R_{SET}} \]

\[ R_{SET} = \frac{R_{SET1} \times R_{SET2}}{R_{SET1} + R_{SET2}} \]

\[ \text{GAIN} = \frac{R_{PZ2}}{R_{Z1} \times \left( \frac{R_{P1}}{C_{PZ1}} \right)} \]

\[ f_{P1} = \frac{1}{2\pi \times R_{P1} \times C_{PZ1}} \]

\[ f_{P2} = \frac{1}{2\pi \times R_{PZ2} \times C_{P2} \times C_{Z2}} = \frac{1}{2\pi \times R_{PZ2} \times C_{P2}} \]

\[ f_{Z1} = \frac{1}{2\pi \times R_{Z1} \times C_{PZ1}} \]

\[ f_{Z2} = \frac{1}{2\pi \times \left( R_{PZ2} + R_{P1} \right) \times C_{Z2}} = \frac{1}{2\pi \times R_{PZ2} \times C_{Z2}} \]

Using this PWM and L-C bode plot the following actions ensure stability.

1. Place two zero’s close to the double pole, i.e. \( f_{Z1} = f_{Z2} = 3559 \) Hz
2. Place a pole at one octave below the desired crossover frequency. The crossover frequency was selected as one quarter the switching frequency, \( f_{CO} = 100 \) kHz, \( f_{P1} = 50 \) kHz
3. Place the second pole about an octave above \( f_{CO} \). This ensures that the overall system gain falls off quickly to give good gain margin, \( f_{P2} = 200 \) kHz
4. The high-frequency gain is sufficient to ensure 0 dB at the required crossover frequency, \( \text{GAIN} = -1 \times \text{GAIN of PWM and LC at the crossover frequency, GAIN} = 17.2 \) dB, or 7.24

Desired frequency response and resultant overall system response can be seen in Figure 18.
Using these values and the equations above the resistors and capacitors around the compensation network can be calculated.

1. Set $R_{Z1} = 10$ kΩ.
2. Calculate $R_{SET}$ using Equation 51; $R_{SET} = 8750$ Ω. Two resistors in parallel, $R_{SET1}$ and $R_{SET2}$, are used to make up $R_{SET}$. $R_{SET1} = 9.53$ kΩ, $R_{SET2} = 105$ kΩ.
3. Using Equation 56 and $f_{Z1} = 3559$ Hz, $C_{PZ1}$ can be calculated to be 4.47 nF; $C_{PZ1} = 4.7$ nF.
4. $F_{P1}$ and Equation 54 yields $R_{P1}$ to be 677 Ω, $R_{P1} = 680$ kΩ.
5. The required gain of 17.2 dB (7.24) and Equation 54 sets the value for $R_{PZ1}$. Note actual gain used for this calculation was 20 dB (10), this ensures that the gain of the transfer function is high enough, $R_{PZ1} = 6.2$ kΩ.
6. $C_{Z2}$ is calculated using Equation 57 and the desired frequency for the second zero, $C_{Z2} = 6.8$ nF.
7. $C_{P2}$ is calculated using the second pole frequency and Equation 55, $C_{P2} = 150$ pF.

Using MathCAD the above values were used to draw the actual Bode plot for gain and phase. From these plots the crossover frequency, phase margin and gain margin can be recorded.

### Table 3. Theoretical System Stability Results

<table>
<thead>
<tr>
<th>ESR (Ω)</th>
<th>CROSSOVER FREQUENCY (kHz)</th>
<th>PHASE MARGIN (°)</th>
<th>GAIN MARGIN (dB)</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>23.1</td>
<td>72</td>
<td>&gt; 46</td>
</tr>
<tr>
<td>0.0095</td>
<td>98.6</td>
<td>78.8</td>
<td>&gt; 33</td>
</tr>
</tbody>
</table>
ALTERNATE APPLICATIONS

Some alternative application diagrams are shown in Figure 21 through Figure 23.
Figure 21. 400 kHz, 12 V to 1.2 V Converter with Powergood Indication
Figure 22. 300 kHz Intermediate Bus (5 V to 12 V) to 3.3 V Converter
Figure 23. Sequenced Supplies, Synchronized 180° Out of Phase
## PACKAGING INFORMATION

<table>
<thead>
<tr>
<th>Orderable Device</th>
<th>Status</th>
<th>Package Type</th>
<th>Package Drawing</th>
<th>Pins</th>
<th>Package Qty</th>
<th>Eco Plan</th>
<th>Lead/Ball Finish</th>
<th>MSL Peak Temp</th>
<th>Op Temp (°C)</th>
<th>Device Marking</th>
<th>Samples</th>
</tr>
</thead>
<tbody>
<tr>
<td>TPS40074RHLR</td>
<td>ACTIVE</td>
<td>VQFN</td>
<td>RHL</td>
<td>20</td>
<td>3000</td>
<td>Green (RoHS &amp; no Sb/Br)</td>
<td>CU NIPDAU</td>
<td>Level-2-260C-1 YEAR</td>
<td>-40 to 85</td>
<td>40074</td>
<td></td>
</tr>
</tbody>
</table>

(1) The marketing status values are defined as follows:
- **ACTIVE**: Product device recommended for new designs.
- **LIFEBUY**: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
- **NRND**: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
- **PREVIEW**: Device has been announced but is not in production. Samples may or may not be available.
- **OBSOLETE**: TI has discontinued the production of the device.

(2) **RoHS**: TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt**: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green**: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) **MSL, Peak Temp.**: The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) **Lead/Ball Finish**: Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

**Important Information and Disclaimer**: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.
### TAPE AND REEL INFORMATION

#### TAPE DIMENSIONS

- **A0**: Dimension designed to accommodate the component width
- **B0**: Dimension designed to accommodate the component length
- **K0**: Dimension designed to accommodate the component thickness
- **W**: Overall width of the carrier tape
- **P1**: Pitch between successive cavity centers

#### Reel Dimensions

- **Reel Diameter**
- **Reel Width** (W1)

#### Quadrant Assignments for PIN 1 Orientation in Tape

<table>
<thead>
<tr>
<th>Device</th>
<th>Package Type</th>
<th>Package Drawing</th>
<th>Pins</th>
<th>SPQ</th>
<th>Reel Diameter (mm)</th>
<th>Reel Width W1 (mm)</th>
<th>A0 (mm)</th>
<th>B0 (mm)</th>
<th>K0 (mm)</th>
<th>P1 (mm)</th>
<th>W (mm)</th>
<th>Pin1 Quadrant</th>
</tr>
</thead>
<tbody>
<tr>
<td>TPS40074RHLR</td>
<td>VQFN</td>
<td>RHL</td>
<td>20</td>
<td>3000</td>
<td>330.0</td>
<td>12.4</td>
<td>3.8</td>
<td>4.8</td>
<td>1.6</td>
<td>8.0</td>
<td>12.0</td>
<td>Q1</td>
</tr>
</tbody>
</table>

*All dimensions are nominal.*
## TAPE AND REEL BOX DIMENSIONS

*All dimensions are nominal*

<table>
<thead>
<tr>
<th>Device</th>
<th>Package Type</th>
<th>Package Drawing</th>
<th>Pins</th>
<th>SPQ</th>
<th>Length (mm)</th>
<th>Width (mm)</th>
<th>Height (mm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>TPS40074RHLR</td>
<td>VQFN</td>
<td>RHL</td>
<td>20</td>
<td>3000</td>
<td>367.0</td>
<td>367.0</td>
<td>35.0</td>
</tr>
</tbody>
</table>
Images above are just a representation of the package family, actual package may vary. Refer to the product data sheet for package details.
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
6. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate
design recommendations.
IMPORTANT NOTICE

Texas Instruments Incorporated (TI) reserves the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. TI’s published terms of sale for semiconductor products (http://www.ti.com/sc/docs/stdterms.htm) apply to the sale of packaged integrated circuit products that TI has qualified and released to market. Additional terms may apply to the use or sale of other types of TI products and services.

Reproduction of significant portions of TI information in TI data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such reproduced documentation. Information of third parties may be subject to additional restrictions. Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and/or implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyers and others who are developing systems that incorporate TI products (collectively, “Designers”) understand and agree that Designers remain responsible for using their independent analysis, evaluation and judgment in designing their applications and that Designers have full and exclusive responsibility to assure the safety of Designers’ applications and compliance of their applications (and of all TI products used in or for Designers’ applications) with all applicable regulations, laws and other applicable requirements. Designers agree that, with respect to their applications, Designers have all the necessary expertise to create and implement safeguards that (1) anticipate dangerous consequences of failures, (2) monitor failures and their consequences, and (3) lessen the likelihood of failures that might cause harm and take appropriate actions. Designers agree that prior to using or distributing any applications that include TI products, Designer will thoroughly test such applications and the functionality of such TI products as used in such applications.

TI’s provision of technical, application or other design advice, quality characterization, reliability data or other services or information, including, but not limited to, reference designs and materials relating to evaluation modules, (collectively, “TI Resources”) are intended to assist designers who are developing applications that incorporate TI products; by downloading, accessing or using TI Resources in any way, Designer (individually or, if Designer is acting on behalf of a company, Designer’s company) agrees to use any particular TI Resource solely for this purpose and subject to the terms of this Notice.

TI’s provision of TI Resources does not expand or otherwise alter TI’s applicable published warranties or warranty disclaimers for TI products, and no additional obligations or liabilities arise from TI providing such TI Resources. TI reserves the right to make corrections, enhancements, improvements and other changes to its TI Resources. TI has not conducted any testing other than that specifically described in the published documentation for a particular TI Resource.

Designers are authorized to use, copy and modify any individual TI Resource only in connection with the development of applications that include the TI product(s) identified in such TI Resource. NO OTHER LICENSE, EXPRESS OR IMPLIED, BY ESTOPPEL OR OTHERWISE TO THE PROPERTY RIGHT OF TI OR ANY THIRD PARTY IS GRANTED HEREIN, including but not limited to any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information regarding or referencing third-party products or services does not constitute a license to use such products or services, or a warranty or endorsement thereof. Use of TI Resources may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

TI RESOURCES ARE PROVIDED “AS IS” AND WITH ALL FAULTS. TI DISCLAIMS ALL OTHER WARRANTIES OR REPRESENTATIONS, EXPRESS OR IMPLIED, REGARDING RESOURCES OR USE THEREOF, INCLUDING BUT NOT LIMITED TO ACCURACY OR COMPLETENESS, TITLE, ANY EPIDEMIC FAILURE WARRANTY AND ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, AND NON-INFRINGEMENT OF ANY THIRD PARTY INTELLECTUAL PROPERTY RIGHTS. TI SHALL NOT BE LIABLE FOR AND SHALL NOT DEFEND OR INDEMNIFY DESIGNER AGAINST ANY CLAIM, INCLUDING BUT NOT LIMITED TO ANY INFRINGEMENT CLAIM THAT RELATES TO OR IS BASED ON ANY COMBINATION OF PRODUCTS EVEN IF DESCRIBED IN TI RESOURCES OR OTHERWISE. IN NO EVENT SHALL TI BE LIABLE FOR ANY ACTUAL, DIRECT, SPECIAL, COLLATERAL, INDIRECT, PUNITIVE, INCIDENTAL, CONSEQUENTIAL OR EXEMPLARY DAMAGES IN CONNECTION WITH OR ARISING OUT OF TI RESOURCES OR USE THEREOF, AND REGARDLESS OF WHETHER TI HAS BEEN ADVISED OF THE POSSIBILITY OF SUCH DAMAGES.

Unless TI has explicitly designated an individual product as meeting the requirements of a particular industry standard (e.g., ISO/TS 16949 and ISO 26262), TI is not responsible for any failure to meet such industry standard requirements.

Where TI specifically promotes products as facilitating functional safety or as compliant with industry functional safety standards, such products are intended to help enable customers to design and create their own applications that meet applicable functional safety standards and requirements. Using products in an application does not by itself establish any safety features in the application. Designers must ensure compliance with safety-related requirements and standards applicable to their applications. Designers may not use any TI products in life-critical medical equipment unless authorized officers of the parties have executed a special contract specifically governing such use. Life-critical medical equipment is medical equipment where failure of such equipment would cause serious bodily injury or death (e.g., life support, pacemakers, defibrillators, heart pumps, neurostimulators, and implantables). Such equipment includes, without limitation, all medical devices identified by the U.S. Food and Drug Administration as Class III devices and equivalent classifications outside the U.S.

TI may expressly designate certain products as completing a particular qualification (e.g., Q100, Military Grade, or Enhanced Product). Designers agree that it has the necessary expertise to select the product with the appropriate qualification designation for their applications and that proper product selection is at Designers’ own risk. Designers are solely responsible for compliance with all legal and regulatory requirements in connection with such selection.

Designers will fully indemnify TI and its representatives against any damages, costs, losses, and/or liabilities arising out of Designer’s non-compliance with the terms and provisions of this Notice.