TPS5117 Single Synchronous Step-Down Controller

1 Features

- High Efficiency, Low Power Consumption, 4.5-μA Typical Shutdown Current
- Fixed Frequency Emulated On-Time Control, Adjustable from 100 kHz to 550 kHz
- D-CAP™ Mode With 100-ns Load Step Response
- < 1% Initial Reference Accuracy
- Output Voltage Range: 0.75 V to 5.5 V
- Wide Input Voltage Range: 1.8 V to 28 V
- Selectable Auto-Skip/PWM-Only Operation
- Temperature Compensated (4500 ppm/°C) Low-Side R_{DS(on)} Overcurrent Sensing
- Negative Overcurrent Limit
- Integrated Boost Diode
- Integrated OVP/UVP and Thermal Shutdown
- Powergood Signal
- Internal 1.2-ms Voltage Soft-Start
- Integrated Output Discharge (Soft-Stop)

2 Applications

- Notebook Computers
- I/O Supplies
- System Power Supplies

3 Description

The TPS5117 device is a cost-effective, synchronous buck controller for POL voltage regulation in notebook PC applications. The controller is dedicated for the operation of the Adaptive On-Time D-CAP mode. This mode provides ease-of-use, low external component count, and fast transient response. Auto-skip mode for high efficiency down to the milliampere load range, or PWM-only mode for low-noise operation is selectable.

The current-sensing scheme for positive overcurrent and negative overcurrent protection is loss-less low-side R_{DS(on)} sensing plus temperature compensation. The device receives a 5-V (4.5 V to 5.5 V) supply from another regulator such as the TPS51120 or TPS51020. The conversion input can be either VBAT or a 5-V rail, ranging from 1.8 V to 28 V, and the output voltage range is from 0.75 V to 5.5 V.

The TPS5117 is available in a 14-pin VQFN or a 14-pin TSSOP package and is specified from −40°C to 85°C.

Device Information

<table>
<thead>
<tr>
<th>PART NUMBER</th>
<th>PACKAGE</th>
<th>BODY SIZE (NOM)</th>
</tr>
</thead>
<tbody>
<tr>
<td>TPS51117</td>
<td>TSSOP (14)</td>
<td>4.40 mm × 5.00 mm</td>
</tr>
<tr>
<td></td>
<td>VQFN (14)</td>
<td>3.50 mm × 3.50 mm</td>
</tr>
</tbody>
</table>

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Typical Application Circuit

An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.
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4 Revision History
NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision B (September 2009) to Revision C  Page
• Added Feature Description section, Device Functional Modes, Application and Implementation section, Power Supply Recommendations section, Layout section, Device and Documentation Support section, and Mechanical, Packaging, and Orderable Information section. ................................................................. 1

Changes from Revision A (June 2009) to Revision B  Page
• Added Start-Up Sequence section .................................. 13
• Added Start-Up Timing Sequence diagram .......................... 13
5 Pin Configuration and Functions

### Pin Functions

<table>
<thead>
<tr>
<th>PIN</th>
<th>I/O</th>
<th>NAME</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>DRVH</td>
<td>O</td>
<td>13</td>
<td>High-side NFET gate driver output. Source 5 Ω, sink 1.5-Ω LL-node referenced driver. Drive voltage corresponds to VBST to LL voltage.</td>
</tr>
<tr>
<td>DRVL</td>
<td>O</td>
<td>9</td>
<td>Rectifying (low-side) NFET gate driver output. Source 5 Ω, sink 1.5-Ω PGND referenced driver. Drive voltage is V5DRV voltage.</td>
</tr>
<tr>
<td>EN_PSV</td>
<td>I</td>
<td>1</td>
<td>Enable / power save pin. Connect to ground to disable SMPS. Connect to 3.3 V or 5 V to turn on SMPS and activate skip mode. Float to turn on SMPS but disable skip mode (forced continuous conduction mode).</td>
</tr>
<tr>
<td>GND</td>
<td>I</td>
<td>7</td>
<td>Signal ground pin.</td>
</tr>
<tr>
<td>LL</td>
<td>I/O</td>
<td>12</td>
<td>High-side NFET gate driver return. Also serves as anode of overcurrent comparator.</td>
</tr>
<tr>
<td>PGND</td>
<td>I/O</td>
<td>8</td>
<td>Ground return for rectifying NFET gate driver. Also cathode of overcurrent protection and source node of the output discharge switch.</td>
</tr>
<tr>
<td>PGOOD</td>
<td>O</td>
<td>6</td>
<td>Powergood window comparator, open-drain, output. Pull up to 5-V rail with a pullup resistor. Current capability is 7.5 mA.</td>
</tr>
<tr>
<td>TON</td>
<td>I</td>
<td>2</td>
<td>On-time / frequency adjustment pin. Connect to LL with 100-kΩ to 600-kΩ resistor.</td>
</tr>
<tr>
<td>TRIP</td>
<td>I</td>
<td>11</td>
<td>Overcurrent trip point set input. Connect resistor from this pin to signal ground to set threshold for both overcurrent and negative overcurrent limit.</td>
</tr>
<tr>
<td>VBST</td>
<td>I</td>
<td>14</td>
<td>Supply input for high-side NFET gate driver (boost terminal). Connect capacitor from this pin to LL-node. An internal PN diode is connected between V5DRV to this pin. Designer can add external Schottky diode if forward drop is critical to drive the power NFET.</td>
</tr>
<tr>
<td>VFB</td>
<td>I</td>
<td>5</td>
<td>SMPS voltage feedback input. Connect the resistor divider here for adjustable output.</td>
</tr>
<tr>
<td>VOUT</td>
<td>I</td>
<td>3</td>
<td>Connect to SMPS output. This terminal serves two functions: output voltage monitor for on-time adjustment, and input for the output discharge switch.</td>
</tr>
<tr>
<td>V5DRV</td>
<td>I</td>
<td>10</td>
<td>5-V Power supply input for FET gate drivers. Internally connected to VBST by a PN diode. Connect 1 μF or more between this pin and PGND to support instantaneous current for gate drivers.</td>
</tr>
<tr>
<td>V5FILT</td>
<td>I</td>
<td>4</td>
<td>5-V Power supply input for all the control circuitry except gate drivers. Supply 5-V ramp rate should be 17 mV/µs or less and T&lt;sub&gt;j&lt;/sub&gt; &lt; 85°C to secure safe start-up of the internal reference circuit. Apply RC filter consists of 300 Ω + 1 μF or 100 Ω + 4.7 μF at the pin input.</td>
</tr>
</tbody>
</table>
6 Specifications

6.1 Absolute Maximum Ratings\(^{(1)}\)

<table>
<thead>
<tr>
<th>Input voltage</th>
<th>MIN</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>VBST</td>
<td>−0.3</td>
<td>36</td>
<td>V</td>
</tr>
<tr>
<td>VBST (with respect to LL)</td>
<td>−0.3</td>
<td>6</td>
<td>V</td>
</tr>
<tr>
<td>EN_PSV, TRIP, V5DRV, V5FILT</td>
<td>−0.3</td>
<td>6</td>
<td>V</td>
</tr>
<tr>
<td>VOUT</td>
<td>−0.3</td>
<td>6</td>
<td>V</td>
</tr>
<tr>
<td>TON</td>
<td>−0.3</td>
<td>6</td>
<td>V</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Output voltage</th>
<th>MIN</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>DRVH</td>
<td>−1</td>
<td>36</td>
<td>V</td>
</tr>
<tr>
<td>DRVH (with respect to LL)</td>
<td>−0.3</td>
<td>6</td>
<td>V</td>
</tr>
<tr>
<td>LL</td>
<td>−1</td>
<td>30</td>
<td>V</td>
</tr>
<tr>
<td>PGOOD, DRVL</td>
<td>−0.3</td>
<td>6</td>
<td>V</td>
</tr>
<tr>
<td>PGND</td>
<td>−0.3</td>
<td>0.3</td>
<td>V</td>
</tr>
</tbody>
</table>

\(T_A\) Operating free-air temperature

\(T_J\) Junction temperature

Lead temperature 1.6 mm (1/16 inch) from case for 10 seconds

\(T_{stg}\) Storage temperature

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\(\) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

<table>
<thead>
<tr>
<th>Supply input voltage</th>
<th>MIN</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>VBST</td>
<td>4.5</td>
<td>5.5</td>
<td>V</td>
</tr>
<tr>
<td>VBST (with respect to LL)</td>
<td>4.5</td>
<td>5.5</td>
<td>V</td>
</tr>
<tr>
<td>EN_PSV, TRIP, V5DRV, V5FILT</td>
<td>−0.1</td>
<td>5.5</td>
<td>V</td>
</tr>
<tr>
<td>VOUT</td>
<td>−0.1</td>
<td>5.5</td>
<td>V</td>
</tr>
<tr>
<td>TON</td>
<td>−0.1</td>
<td>5.5</td>
<td>V</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Input voltage</th>
<th>MIN</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>DRVH</td>
<td>−0.8</td>
<td>34</td>
<td>V</td>
</tr>
<tr>
<td>DRVH (with respect to LL)</td>
<td>−0.1</td>
<td>5.5</td>
<td>V</td>
</tr>
<tr>
<td>LL</td>
<td>−0.8</td>
<td>28</td>
<td>V</td>
</tr>
<tr>
<td>PGOOD, DRVL</td>
<td>−0.1</td>
<td>5.5</td>
<td>V</td>
</tr>
<tr>
<td>PGND</td>
<td>−0.1</td>
<td>0.1</td>
<td>V</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Operating free-air temperature, (T_A)</th>
<th>MIN</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>−40</td>
<td>85</td>
<td>°C</td>
</tr>
</tbody>
</table>
6.3 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>$I_{V5FILT_{PWM}}$ Supply current</td>
<td>V5FILT + V5DRV current, PWM, EN_PSV = float, VFB = 0.77 V, LL = –0.1 V</td>
<td>400</td>
<td>750</td>
<td></td>
<td>μA</td>
</tr>
<tr>
<td>$I_{V5FILT_{SKIP}}$ Supply current</td>
<td>V5FILT + V5DRV current, auto-skip, EN_PSV = 5 V, VFB = 0.77 V, LL = 0.5 V</td>
<td>250</td>
<td>470</td>
<td></td>
<td>μA</td>
</tr>
<tr>
<td>$V_{V5DRVS_SDN}$ V5DRV shutdown current</td>
<td>V5DRV current, EN_PSV = 0 V</td>
<td>0</td>
<td>1</td>
<td></td>
<td>μA</td>
</tr>
<tr>
<td>$I_{V5FILTS_SDN}$ V5FILT shutdown current</td>
<td>V5FILT current, EN_PSV = 0 V</td>
<td>4.5</td>
<td>7.5</td>
<td></td>
<td>μA</td>
</tr>
</tbody>
</table>

**VOUT AND VFB VOLTAGES**

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{VFB}$</td>
<td>Output voltage</td>
<td>Adjustable output range</td>
<td></td>
<td>0.75</td>
<td>5.5</td>
</tr>
<tr>
<td>$V_{VFB_TOL}$ VFB regulation voltage tolerance</td>
<td>$T_A = 25^\circ\text{C}$, bandgap initial accuracy</td>
<td>$–0.9%$</td>
<td>$0.9%$</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>$T_A = 0^\circ\text{C}$ to $85^\circ\text{C}$</td>
<td>$–1.3%$</td>
<td>$1.3%$</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>$T_A = –40^\circ\text{C}$ to $85^\circ\text{C}$</td>
<td>$–1.6%$</td>
<td>$1.6%$</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$I_{VFB}$ VFB input current</td>
<td>$V_{FB} = 0.75$ V, absolute value</td>
<td>0.02</td>
<td>0.1</td>
<td></td>
<td>μA</td>
</tr>
</tbody>
</table>

**ON-TIME TIMER AND INTERNAL SOFT-START**

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>$T_{ONN}$ Nominal on-time</td>
<td>$V_{LL} = 12$ V, $V_{OUT} = 2.5$ V, $R_{TON} = 250$ kΩ</td>
<td>750</td>
<td></td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>$T_{ONF}$ Fast on-time</td>
<td>$V_{LL} = 12$ V, $V_{OUT} = 2.5$ V, $R_{TON} = 100$ kΩ</td>
<td>264</td>
<td>330</td>
<td>396</td>
<td>ns</td>
</tr>
<tr>
<td>$T_{ONS}$ Slow on-time</td>
<td>$V_{LL} = 12$ V, $V_{OUT} = 2.5$ V, $R_{TON} = 400$ kΩ</td>
<td>1169</td>
<td></td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>$T_{ON_MIN}$ Minimum on-time</td>
<td>$V_{OUT} = 0.75$ V, $R_{TON} = 100$ kΩ to 28 V$^{(1)}$</td>
<td>80</td>
<td>110</td>
<td>140</td>
<td>ns</td>
</tr>
<tr>
<td>$T_{OFF_MIN}$ Minimum off-time</td>
<td>$V_{FB} = 0.7$ V, $LL = –0.1$ V, TRIP = open</td>
<td>440</td>
<td></td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>$T_{SS}$ Internal soft-start time</td>
<td>Time from EN_PSV &gt; 3 V to $V_{FB}$ regulation value = 0.735 V</td>
<td>0.82</td>
<td>1.2</td>
<td>1.5</td>
<td>ms</td>
</tr>
</tbody>
</table>

**OUTPUT DRIVERS**

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>$R_{DRVH}$ DRVH resistance</td>
<td>Source, $V_{VBST_DRVH} = 0.5$ V</td>
<td>5</td>
<td>7</td>
<td></td>
<td>Ω</td>
</tr>
<tr>
<td></td>
<td>Sink, $V_{DRVH_LL} = 0.5$ V</td>
<td>1.5</td>
<td>2.5</td>
<td> </td>
<td></td>
</tr>
<tr>
<td>$R_{DRVL}$ DRVL resistance</td>
<td>Source, $V_{V5DRV_DRVL} = 0.5$ V</td>
<td>5</td>
<td>7</td>
<td></td>
<td>Ω</td>
</tr>
<tr>
<td></td>
<td>Sink, $V_{DRVL_PGND} = 0.5$ V</td>
<td>1.5</td>
<td>2.5</td>
<td> </td>
<td></td>
</tr>
<tr>
<td>$T_D$ Dead time</td>
<td>DRVH-low (DRVH = 1 V) to DRVL-high (DRVL = 4 V), $LL = –0.05$ V</td>
<td>10</td>
<td>20</td>
<td>50</td>
<td>ns</td>
</tr>
<tr>
<td></td>
<td>DRVL-low (DRVL = 1 V) to DRVH-high (DRVH = 4 V), $LL = –0.05$ V</td>
<td>30</td>
<td>40</td>
<td>60</td>
<td>ns</td>
</tr>
</tbody>
</table>

**INTERNAL BST DIODE**

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{FBST}$ Forward voltage</td>
<td>$V_{V5DRV_VBST}$, IF = 10 mA, $T_A = 25^\circ\text{C}$</td>
<td>0.7</td>
<td>0.8</td>
<td>0.9</td>
<td>V</td>
</tr>
<tr>
<td>$I_{VBST_LK}$ VBST leakage current</td>
<td>VBST = 34 V, LL = 28 V</td>
<td>0.1</td>
<td>1</td>
<td> </td>
<td>μA</td>
</tr>
</tbody>
</table>

**UVLO/LOGIC THRESHOLD**

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{UVLO}$ V5FILT UVLO Threshold</td>
<td>Wake up</td>
<td>3.7</td>
<td>3.9</td>
<td>4.1</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td>Hysteresis</td>
<td>200</td>
<td>300</td>
<td>400</td>
<td>mV</td>
</tr>
<tr>
<td>$V_{EN_PSV}$ EN_PSV logic input voltage</td>
<td>EN_PSV low</td>
<td>0.7</td>
<td>1.0</td>
<td>1.3</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td>Hysteresis</td>
<td>150</td>
<td>200</td>
<td>250</td>
<td>mV</td>
</tr>
<tr>
<td></td>
<td>EN_PSV float (set PWM_only mode)</td>
<td>1.7</td>
<td>1.95</td>
<td>2.25</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td>EN_PSV high (set Auto_skip mode)</td>
<td>2.4</td>
<td>2.65</td>
<td>2.9</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td>Hysteresis</td>
<td>100</td>
<td>175</td>
<td>250</td>
<td>mV</td>
</tr>
<tr>
<td>$I_{EN_PSV}$ EN_PSV source current</td>
<td>EN_PSV = GND, absolute value$^{(2)}$</td>
<td>1</td>
<td></td>
<td></td>
<td>μA</td>
</tr>
</tbody>
</table>

---

(1) Design constraint, ensure actual on-time is larger than the maximum value (that is, design $R_{TON}$ such that the minimum tolerance is 100 kΩ).

(2) Ensured by design. Not production tested.
**Electrical Characteristics (continued)**

over operating free-air temperature range (unless otherwise noted)

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>POWERGOOD COMPARATOR</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$V_{T_{HPG}}$</td>
<td>PG threshold</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>PG in from lower (PGOOD goes high)</td>
<td>92.5%</td>
<td>95%</td>
<td>97.5%</td>
<td></td>
</tr>
<tr>
<td></td>
<td>PG low hysteresis (PGOOD goes low)</td>
<td>−4%</td>
<td>−5.5%</td>
<td>−7%</td>
<td></td>
</tr>
<tr>
<td></td>
<td>PG in from higher (PGOOD goes high)</td>
<td>102%</td>
<td>105%</td>
<td>107%</td>
<td></td>
</tr>
<tr>
<td></td>
<td>PG high hysteresis (PGOOD goes low)</td>
<td>4%</td>
<td>5.5%</td>
<td>7%</td>
<td></td>
</tr>
<tr>
<td>$I_{PGMAX}$</td>
<td>PG sink current</td>
<td>2.5</td>
<td>7.5</td>
<td></td>
<td>mA</td>
</tr>
<tr>
<td>$T_{PGDEL}$</td>
<td>PG delay</td>
<td>45</td>
<td>63</td>
<td>85</td>
<td>μs</td>
</tr>
<tr>
<td></td>
<td>delay for PGOOD in</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>CURRENT SENSE</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$I_{TRIP}$</td>
<td>TRIP source current</td>
<td>$V_{TRIP} &lt; 0.3$ V, $T_A = 25°C$</td>
<td>9</td>
<td>10</td>
<td>11</td>
</tr>
<tr>
<td>$T_{CITRIP}$</td>
<td>CITRIP temperature coefficient</td>
<td>On the basis of $25°C$</td>
<td>4500</td>
<td>ppm/°C</td>
<td></td>
</tr>
<tr>
<td>$V_{trip}$</td>
<td>Current limit threshold range setting range</td>
<td>$V_{TRIP-GND}$ voltage, all temperatures</td>
<td>30</td>
<td>200</td>
<td>mV</td>
</tr>
<tr>
<td>$V_{DCLoff}$</td>
<td>Overcurrent limit comparator offset</td>
<td>$(V_{TRIP-GND}-V_{PGND-LL})$ voltage $V_{TRIP-GND} = 60$ mV</td>
<td>−10</td>
<td>0</td>
<td>10</td>
</tr>
<tr>
<td>$V_{ULoff}$</td>
<td>Negative overcurrent limit comparator offset</td>
<td>$(V_{TRIP-GND}-V_{LL-PGND})$ voltage $V_{TRIP-GND} = 60$ mV, $EN_PSV = float$</td>
<td>−9.5</td>
<td>0.5</td>
<td>10.5</td>
</tr>
<tr>
<td>$V_{ZCoff}$</td>
<td>Zero crossing comparator offset</td>
<td>$V_{PGND-LL}$ voltage, $EN_PSV = 3.3$ V</td>
<td>−9.5</td>
<td>0.5</td>
<td>10.5</td>
</tr>
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<td><strong>UNDERVOLTAGE AND OVERVOLTAGE PROTECTION</strong></td>
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<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$V_{OVP}$</td>
<td>VFB OVP trip threshold</td>
<td>OVP detect</td>
<td>111%</td>
<td>115%</td>
<td>119%</td>
</tr>
<tr>
<td>$T_{OVPPDEL}$</td>
<td>VFB OVP propagation delay</td>
<td>See (2)</td>
<td>1.5</td>
<td></td>
<td>μs</td>
</tr>
<tr>
<td>$V_{UVP}$</td>
<td>VFB UVP trip threshold</td>
<td>UVP detect</td>
<td>65%</td>
<td>70%</td>
<td>75%</td>
</tr>
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<td>$T_{UVPDEL}$</td>
<td>VFB UVP delay</td>
<td>After $1.7 \times T_{SS}$, UVP protection engaged</td>
<td>22</td>
<td>32</td>
<td>42</td>
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<td>$T_{UVPEN}$</td>
<td>UVP enable delay</td>
<td>1.4</td>
<td>2</td>
<td>2.6</td>
<td>ms</td>
</tr>
<tr>
<td><strong>THERMAL SHUTDOWN</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$T_{SDN}$</td>
<td>Thermal shutdown threshold</td>
<td>Shutdown temperature</td>
<td>160</td>
<td></td>
<td>°C</td>
</tr>
<tr>
<td></td>
<td>Hysteresis</td>
<td>Hysteresis</td>
<td>12</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
6.4 Typical Characteristics

Figure 1. PWM Supply Current vs Junction Temperature

Figure 2. V5FILT Shutdown Current vs Junction Temperature

Figure 3. Trip Current vs Junction Temperature

Figure 4. OVP/UVP Threshold vs Junction Temperature

Figure 5. Measured Switching Frequency vs Ton Resistance

Figure 6. Switching Frequency vs Input Voltage
Typical Characteristics (continued)

Figure 7. Switching Frequency vs Output Current (1.05 V)

Figure 8. Switching Frequency vs Output Current (2.5 V)

Figure 9. 1.05-V Output Voltage vs Output Current

Figure 10. 2.5-V Output Voltage vs Output Current

Figure 11. 1.05-V Output Voltage vs Input Voltage

Figure 12. 2.5-V Output Voltage vs Input Voltage
Typical Characteristics (continued)

Figure 13. 1.05-V Efficiency vs Output Current

Figure 14. 2.5-V Efficiency vs Output Current

Figure 15. 1.05-V Load Transient Response

Figure 16. 2.5-V Load Transient Response

Figure 17. Mode Transition
   Auto-Skip to PWM

Figure 18. Mode Transition
   PWM to Auto-Skip
7 Detailed Description

7.1 Overview

The TPS51117 is a synchronous buck controller for POL voltage regulation in notebook PC applications. The controller is dedicated for the operation of the Adaptive On-Time D-CAP mode. This mode provides ease-of-use, low external component count, and fast transient response. Auto-skip mode for high efficiency down to the milliampere load range, or PWM-only mode for low-noise operation is selectable.

7.2 Functional Block Diagram
7.3 Feature Description

7.3.1 PWM Frequency and Adaptive On-Time Control

The TPS51117 employs an adaptive on-time control scheme and does not have a dedicated oscillator onboard. However, the device emulates a constant frequency by feed-forwarding the input and output voltages into the on-time one-shot timer. The ON time is controlled inverse proportional to the input voltage, and proportional to the output voltage, so that the duty ratio is kept as \( V_{OUT}/V_{IN} \) technically with the same cycle time. Equation 1 shows a simplified calculation of the ON time.

\[
T_{ON} = 19 \times 10^{-12} \times R_{TON} \left( \frac{2/3 N_{OUT} + 100 \text{ mV}}{V_{IN}} \right) + 50 \text{ ns}
\]  

(1)

Here, \( R_{TON} \) is the external resistor connected from TON pin to the LL node. In the equation, 19 pF represents the internal timing capacitor with some typical parasitic capacitance at the TON pin. Also, 50 ns is the turnoff delay time contributed by the internal circuit and that of the high-side MOSFET. Although this equation provides a good approximation with which to begin, the accuracy depends on each design and selection of the high-side MOSFET. Figure 19 shows the relationship of \( R_{TON} \) to the switching frequency.

![Figure 19. Switching Frequency vs R_{TON}](image)

The TPS51117 does not have a pin connected to VIN, but the input voltage information comes from the switch node (LL node) during the ON-state. An advantage of LL monitoring is that the loss in the high-side NFET is now a part of the ON-time calculation, thereby making the frequency more stable with load.

Another consideration about frequency is jitter. Jitter may be caused by many reasons, but the constant on-time D-CAP mode scheme has some amount of inherent jitter. Because the output voltage ripple height is in the range of a couple of tens of millivolts. A millivolt order of noise on the feedback signal can affect the frequency by a few to ten percent. This is normal operation and has little harm to the power supply performance.

7.3.2 Low-Side Driver

The low-side driver is designed to drive high-current, low \( R_{DS(on)} \) N-channel MOSFETs. The drive capability is represented by its internal resistance, which is 5 \( \Omega \) for V5DRV to DRVL and 1.5 \( \Omega \) for DRVL to PGND. A dead time to prevent shoot-through is internally generated between high-side MOSFET off to low-side MOSFET on, and low-side MOSFET off to high-side MOSFET on. A 5-V bias voltage is delivered from V5DRV supply. The average drive current is calculated by the FET gate charge at \( V_{GS} = 5 \text{ V} \) times the switching frequency. The instantaneous drive current is supplied by an input capacitor connected between V5DRV and GND.
Feature Description (continued)

7.3.3 High-Side Driver

The high-side driver is designed to drive high-current, low $R_{DS(on)}$ N-channel MOSFET(s). When configured as a floating driver, 5-V bias voltage is delivered from V5DRV supply. An internal PN diode is connected between V5DRV to VBST. The designer can add an external Schottky diode if forward drop is critical to drive the high-side NFET or to achieve the last 1% efficiency improvement. The average drive current is also estimated by the gate charge at $V_{gs} = 5$ V times the switching frequency. The instantaneous drive current is supplied by the flying capacitor between the VBST pin and LL pin. The drive capability is represented by its internal resistance, which is $5 \Omega$ for VBST to DRVH and $1.5 \Omega$ for DRVH to LL.

7.3.4 Soft-Start

The TPS51117 has an internal, 1.2-ms, voltage servo soft-start with overcurrent limit. When the EN_PSV pin becomes high, an internal DAC begins ramping up the reference voltage to the error amplifier. Smooth control of the output voltage is maintained during start-up.

7.3.5 Powergood

The TPS51117 has powergood output. PGOOD is an open-drain 7.5-mA pulldown output. This pin should be typically connected to a 5-V power supply node through a 100-k$\Omega$ resistor. The powergood function is activated after the soft start has finished. If the output voltage becomes within $\pm5\%$ of the target value, internal comparators detect the power good state and the powergood signal becomes high after a 64-μs internal delay. If the output voltage goes outside $\pm10\%$ of the target value, the powergood signal becomes low immediately.

7.3.6 Output Discharge Control (Soft-Stop)

The TPS51117 discharges output when EN_PSV is low or the converter is in a fault condition (UVP, OVP, UVLO, or thermal shutdown). The TPS51117 discharges output using an internal 20-Ω MOSFET, which is connected to VOUT and PGND. The discharge time-constant is a function of the output capacitance and resistance of the discharge transistor.

7.3.7 Overcurrent Limit

The TPS51117 has cycle-by-cycle overcurrent limiting control. Inductor current is monitored during the OFF-state and the controller keeps the OFF-state when inductor current is larger than the overcurrent trip level. To provide both good accuracy and a cost-effective solution, the TPS51117 supports temperature compensated MOSFET $R_{DS(on)}$ sensing. The TRIP pin should be connected to GND through the trip voltage setting resistor, $R_{TRIP}$. The TRIP terminal sources 10-μA $I_{TRIP}$ current, and the trip level is set to the OCL trip voltage, $V_{TRIP}$ as in the following equation.

$$V_{TRIP} (mV) = R_{TRIP} (k\Omega) \times 10(\mu A)$$

(2)

Inductor current is monitored by the voltage between the PGND pin and the LL pin so the LL pin should be connected to the drain terminal of the low-side MOSFET. $I_{TRIP}$ has 4500 ppm/°C temperature coefficient to compensate the temperature dependency of the $R_{DS(on)}$. PGND is used as the positive current sensing node so PGND should be connected to the source terminal of the bottom MOSFET.

As the comparison is done during the OFF-state, $V_{TRIP}$ sets the valley level of the inductor current. Thus, the load current at overcurrent threshold, $I_{ocp}$, can be calculated as follows;

$$I_{ocp} = \frac{V_{TRIP}}{R_{DS(on)}} + \frac{1}{2 \times L \times f} \times \frac{(V_{IN} - V_{OUT}) \times V_{OUT}}{V_{IN}}$$

(3)

In an overcurrent condition, the current to the load exceeds the current to the output capacitor, thus the output voltage tends to fall. Eventually, the output voltage crosses the undervoltage protection threshold and shutdown.
Feature Description (continued)

7.3.8 Negative Overcurrent Limit (PWM-Only Mode)

The TPS51117 also supports cycle-by-cycle negative overcurrent limiting in PWM-only mode. The overcurrent limit is set to be negative but is the same absolute value as the positive overcurrent limit. If output voltage continues to rise, the bottom MOSFET stays on, thus inductor current is reduced and reverses direction after it reaches zero. When there is too much negative current in the inductor, the bottom MOSFET is turned off and the current flows to VIN through the body diode of the top MOSFET. Because this protection reduces current to discharge the output capacitor, output voltage tends to rise, eventually hitting the overvoltage protection threshold and shutdown. To prevent false OVP from triggering, the bottom MOSFET is turned on again 400 ns after it is turned off. If the device hits the negative overcurrent threshold again before output voltage is discharged to the target level, the bottom MOSFET is turned off and the process repeats, which is called NOCL Buzz. The device ensures maximum allowable discharge capability when output voltage continues to rise. On the other hand, if the output voltage is discharged to the target level before the NOCL threshold is reached, the bottom MOSFET is turned off, the top MOSFET is then turned on, and the device resumes normal operation.

7.3.9 Overvoltage Protection

The TPS51117 monitors a resistor divided feedback voltage to detect overvoltage and undervoltage condition. When the feedback voltage becomes higher than 115% of the target value, the top MOSFET is turned off and the bottom MOSFET is turned on immediately. The output is also discharged by the internal 20-Ω transistor. Also, the TPS51117 monitors VOUT terminal voltage directly and if it becomes greater than 5.75 V, it turns off the top MOSFET driver.

7.3.10 Undervoltage Protection

When the feedback voltage becomes lower than 70% of the target value, the UVP comparator output goes high and an internal UVP delay counter begins counting. After 32 μs, the TPS51117 latches off the high-side and low-side MOSFETs and discharges the output with the internal 20-Ω transistor. This function is enabled after 2 ms from when EN_PSV is brought high, that is, UVP is disabled during start-up.

7.3.11 Start-Up Sequence

Referring to Figure 20 which shows the timing sequence, to ensure the proper start-up of the TPS51117, always ensure that VEN_PSV is less or equal to that of VVSFILT prior to VVSFILT reaching VUVLO.

![Figure 20. Start-Up Timing Sequence](image_url)
Feature Description (continued)

7.3.12 UVLO Protection

The TPS51117 has V5FILT undervoltage lockout protection (UVLO). When the V5FILT voltage is lower than the UVLO threshold voltage, the TPS51117 is shut off. This is a nonlatched protection.

7.3.13 Thermal Shutdown

The TPS51117 monitors the temperature of itself. If the temperature exceeds the threshold value (typically 160°C), the TPS51117 shuts itself off. Both top and bottom gate drivers are tied low with output discharged through the VOUT terminal. This is also a nonlatched protection. The device recovers once the temperature has decreased approximately 12°C.

7.4 Device Functional Modes

7.4.1 PWM Operation

The main control loop of the TPS51117 is designed as an adaptive on-time pulse width modulation (PWM) controller. It supports proprietary D-CAP Mode that uses an internal compensation circuit and is suitable for minimal external component count configuration when an appropriate amount of ESR at the output capacitor(s) is allowed. Basic operation of D-CAP Mode can be described as follows.

At the beginning of each cycle, the synchronous high-side MOSFET is turned on, or becomes ON-state. This MOSFET is turned off, or becomes OFF-state, after the internal one-shot timer expires. This one-shot is determined by \( V_{IN} \) and \( V_{OUT} \) to keep the frequency fairly constant over the input voltage range at steady-state, hence it is called adaptive on-time control or fixed frequency emulated on-time control (see PW Frequecy and Adaptive On-Time Control). The MOSFET is turned on again when both feedback information, monitored at \( V_{FB} \) voltage, indicates insufficient output voltage and inductor current information indicates below the overcurrent limit. Repeating the operation in this manner, the controller regulates the output voltage. The synchronous low-side or rectifying MOSFET is turned on each OFF-state to keep the conduction loss to a minimum.

The TPS51117 supports selectable PWM-only and auto-skip operation modes. If EN_PSV is grounded, the switching regulator is disabled. If the EN_PSV pin is connected to 3.3 V or 5 V, the regulator is enabled with auto-skip mode selected. The rectifying MOSFET is turned off when inductor current information detects zero level. This enables a seamless transition to reduced frequency operation during a light-load condition so that high efficiency is maintained over a broad range of load currents. If the EN_PSV pin is floated, it is internally pulled up to 1.95 V, and the regulator is enabled with PWM-only mode selected. The rectifying MOSFET is not turned off when inductor current reaches zero. The converter runs forced continuous conduction mode for the entire load range. System designers may want to use this mode to avoid a certain frequency during a light-load condition but with the cost of low efficiency. However, be aware the output has the capability to both source and sink current in this mode. If the output terminal is connected to a voltage source higher than the target of the regulator, the converter sinks current from the output and boosts the charge into the input capacitor. This may cause unexpected high voltage at VIN and may damage the power FETs.

DC output voltage can be set by the external resistor divider as follows (refer to Figure 21, Figure 24, and Figure 25).

\[
V_{OUT} = \left(1 + \frac{R_1}{R_2}\right) \times 0.75V
\]

7.4.2 Light-Load Condition With Auto-Skip Function

If auto-skip mode is selected, the TPS51117 automatically reduces the switching frequency during a light-load condition to maintain high efficiency. This reduction of frequency is achieved smoothly and without an increase of \( V_{\text{out}} \) ripple or load regulation. Detailed operation is described as follows. As the output current decreases from a heavy load condition, the inductor current is also reduced and eventually comes to the point that its valley touches zero current, which is the boundary between continuous conduction and discontinuous conduction modes. The rectifying MOSFET is turned off when this zero inductor current is detected. Because the output voltage is still higher than the reference at this moment, both high-side and low-side MOSFETs are turned off and wait for the next cycle. As the load current decreases further, the converter runs in discontinuous conduction...
Device Functional Modes (continued)

mode, taking longer time to discharge the output capacitor below the reference voltage. The ON time is kept the same as during the heavy load condition. In reverse, when the output current increases from a light load to a heavy load, the switching frequency increases to the preset value as the inductor current reaches to the continuous conduction. The transition load point to light-load operation, \( I_{OUT(LL)} \) (that is, the threshold between continuous and discontinuous conduction mode), can be calculated as follows:

\[
I_{OUT(LL)} = \frac{1}{2 \times L \times f_{SW}} \times \frac{(V_{IN} - V_{OUT}) \times V_{OUT}}{V_{IN}}
\]

where

- \( f_{SW} \) is the PWM switching frequency

Switching frequency versus output current in the light-load condition is a function of \( L, f_{SW}, V_{IN} \) and \( V_{OUT} \), but it decreases almost proportional to the output current from the \( I_{OUT(LL)} \) given in Equation 5. For example, it is about 60 kHz at \( I_{OUT(LL)}/5 \) if the PWM switching frequency is 300 kHz.
8 Application and Implementation

NOTE
Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI’s customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information
The TPS51117 is a cost-effective, synchronous buck controller for POL voltage regulation in notebook PC applications. The controller is dedicated for Adaptive On-Time D-CAP Mode operation. Use the following design procedure to select component values for each device.

8.2 Typical Application
A buck converter system using D-CAP Mode can be simplified as shown in Figure 21.

Figure 21. Simplified Diagram of the Modulator

8.2.1 Design Requirements
For this design example, use Table 1 as the input parameters.

Table 1. Design Parameters

<table>
<thead>
<tr>
<th>DESIGN PARAMETER</th>
<th>EXAMPLE VALUE</th>
</tr>
</thead>
<tbody>
<tr>
<td>Input Voltage Range</td>
<td>1.8 V to 28 V</td>
</tr>
<tr>
<td>Output Voltage</td>
<td>1.05 V</td>
</tr>
<tr>
<td>Output Current Rating</td>
<td>10 A</td>
</tr>
</tbody>
</table>
8.2.2 Detailed Design Procedure

8.2.2.1 D-CAP Mode Operation

The VFB voltage is compared with the internal reference voltage after the divider resistors. The PWM comparator determines the timing to turn on the top MOSFET. The gain and speed of the comparator is high enough to keep the voltage at the beginning of each on cycle (or the end of off cycle) substantially constant. The DC output voltage may have line regulation due to ripple amplitude that slightly increases as the input voltage increases.

For loop stability, the 0 dB frequency, \( f_0 \), defined in Equation 6 must be lower than 1/4 of the switching frequency.

\[
f_0 = \frac{1}{2\pi \times ESR \times C} \leq \frac{f_{SW}}{4}
\]  
(6)

As \( f_0 \) is determined solely by the output capacitor characteristics, loop stability of D-CAP Mode is determined by capacitor chemistry. For example, specialty polymer capacitors (SP-CAP) have \( C \) in the order of several 100 \( \mu F \) and ESR in range of 10 m\( \Omega \). These values make \( f_0 \) in the order of 100 kHz or less and the loop is stable. However, ceramic capacitors have \( f_0 \) at more than 700 kHz, which is not suitable for this operational mode.

Although D-CAP Mode provides many advantages such as ease-of-use, minimum external component configuration, and extremely short response time, due to not employing an error amplifier in the loop, a sufficient feedback signal must be provided by an external circuit to reduce the jitter level. The required signal level is approximately 15 mV at the comparing point. This generates \( V_{\text{ripple}} = (V_{\text{OUT}}/0.75) \times 15 \text{ mV} \) at the output node. The output capacitor ESR should meet this requirement.

The external component selection is simple in D-CAP Mode:

1. Determine the value of \( R1 \) and \( R2 \)

The recommended \( R2 \) value is 10 k\( \Omega \) to 100 k\( \Omega \). Calculate \( R1 \) by Equation 7.

\[
R1 = \frac{0.75}{V_{\text{OUT}}} \times R2
\]  
(7)

2. Choose \( R_{\text{TON}} \)

Switching frequency is usually determined by the overall view of the DC-DC converter design of: size, efficiency or cost, and mostly dictated by external component constraints such as the size of inductor and/or output capacitor. When an extremely low or high duty factor is expected, the minimum on-time or off-time also must be considered to satisfy the required duty factor. Once the switching frequency is decided, \( R_{\text{TON}} \) can be determined by Equation 8 and Equation 9.

\[
T_{\text{ON(max)}} = \frac{1}{f} \times \frac{V_{\text{OUT}}}{V_{\text{IN(min)}}}
\]  
(8)

\[
R_{\text{TON}} = \frac{3}{2} \times \left( \frac{50\text{ns}}{19 \times 10^{-12}} \right) \times \frac{V_{\text{IN(min)}}}{(V_{\text{OUT}} + 150\text{mV})}[\Omega]
\]  
(9)

3. Choose inductor

A good starting point inductance value is where the ripple current is approximately 1/4 to 1/2 of the maximum output current.

\[
L_{\text{IND}} = \frac{1}{l_{\text{IND(ripple)}} \times f} \times \left( \frac{V_{\text{IN(max)}}}{V_{\text{OUT}}} - \frac{V_{\text{OUT}}}{V_{\text{IN(max)}}} \right) \times V_{\text{OUT}} = \frac{3}{l_{\text{OUT(max)}} \times f} \times \left( \frac{V_{\text{IN(max)}} - V_{\text{OUT}}}{V_{\text{IN(max)}}} \right) \times V_{\text{OUT}}
\]  
(10)

For applications that require fast transient response with minimum \( V_{\text{OUT}} \) overshoot, consider a smaller inductance than above. The cost of a small inductance value is higher steady-state ripple, larger line regulation, and higher switching loss.
The inductor also needs to have low DCR to achieve good efficiency, as well as enough room above peak inductor current before saturation. The peak inductor current can be estimated in Equation 11:

\[ I_{\text{IND(peak)}} = \frac{V_{\text{TRIP}}}{R_{\text{DS(on)}}} + \frac{1}{L \times f} \left( \frac{V_{\text{IN(max)}} - V_{\text{OUT}}}{V_{\text{IN(max)}}} \right) \times V_{\text{OUT}} \]  

(11)

4. Choose output capacitor(s)

Organic semiconductor capacitor(s) or specialty polymer capacitor(s) are recommended. Determine ESR to meet the required ripple voltage above. A quick approximation is shown in Equation 12.

\[ \text{ESR} = \frac{V_{\text{OUT}} \times 0.015}{I_{\text{ripple}} \times 0.75} \approx \frac{V_{\text{OUT}}}{I_{\text{OUT(max)}}} \times 60 \text{[mΩ]} \]  

(12)

5. Choose MOSFETs

Loss-less current sensing and overcurrent protection of the TPS51117 is determined by \( R_{\text{DS(on)}} \) of the low-side MOSFET. So, \( R_{\text{DS(on)}} \) times the inductor current value at the overcurrent point should be in the range of 30 mV to 200 mV for the entire operational temperature range. Assuming a 20% guard band, \( R_{\text{DS(on)}} \) in Equation 13 should satisfy the full temperature range.

\[ \frac{30 \text{mV}}{1.2 \times I_{\text{OUT(max)}} - 0.5 \times I_{\text{ripple}}} \leq R_{\text{DS(on)}} \leq \frac{200 \text{mV}}{1.2 \times I_{\text{OUT(max)}} - 0.5 \times I_{\text{ripple}}} \]  

(13)

6. Choose \( R_{\text{trip}} \)

Once the low-side FET is decided, select an appropriate \( R_{\text{trip}} \) value that provides \( V_{\text{trip}} \) equal to \( R_{\text{DS(on)}} \) times \( I_{\text{peak}} \).

7. LPF for V5FILT

To reject high-frequency noise and also secure safe start-up of the internal reference circuit, apply 1 μF of MLCC closely at the V5FILT pin with a 300-Ω resistor to create a LPF between +5-V supply and the pin.

8. VBST capacitor, VBST diode

Apply 0.1-μF MLCC between VBST and the LL node as the flying capacitor for the high-side FET driver. The TPS51117 has its own boost diode onboard between V5DRV and VBST. This is a PN junction diode and strong enough for most typical applications. However, in case efficiency has priority over cost, the designer may add a Schottky diode externally to improve gate drive voltage of the high-side FET. A Schottky diode has a higher leakage current, especially at high temperature, than a PN junction diode. A low-leakage diode should be selected in order to maintain VBST voltage during low-frequency operation in skip mode.

### Table 2. Typical Application Circuit Components

<table>
<thead>
<tr>
<th>SYMBOL</th>
<th>SPECIFICATION</th>
<th>MANUFACTURER</th>
<th>PART NUMBER</th>
</tr>
</thead>
<tbody>
<tr>
<td>C1A, C1B</td>
<td>470 μF, 2.5 V, 12 mΩ</td>
<td>SANYO</td>
<td>2R5TPE470MC</td>
</tr>
<tr>
<td>C2</td>
<td>10 μF, 25 V, 2 pcs</td>
<td>Murata</td>
<td>GRM31CR61E106KA12B</td>
</tr>
<tr>
<td>L1</td>
<td>1.0 μH</td>
<td>Vishay, Toko</td>
<td>IHLP-5050, FDA1254-1R0M</td>
</tr>
<tr>
<td>Q1</td>
<td>30 V, 13 mΩ</td>
<td>International Rectifier</td>
<td>IRF7821</td>
</tr>
<tr>
<td>Q2</td>
<td>30 V, 5.8 mΩ</td>
<td>International Rectifier</td>
<td>IRF8113</td>
</tr>
<tr>
<td>R4</td>
<td>8.06 kΩ</td>
<td>—</td>
<td>Std</td>
</tr>
</tbody>
</table>
8.2.3 Application Curves

Figure 22. 2.5-V Start-Up Waveforms

Figure 23. 2.5-V Shutdown Waveforms
8.3 System Examples

Figure 24. 1.05-V/10-A Application from VBAT (PW Package)

Figure 25. 1.05-V/10-A Application from VBAT (RGY Package)
9 Power Supply Recommendations

The devices are designed to operate at 5 V (4.5 V to 5.5 V) supply from another regulator such as the Limit TPS51120 or TPS51020. The conversion input can be either VBAT or a 5-V rail, ranging from 1.8 V to 28 V. In order to reject high-frequency noise and also secure safe start-up of the internal reference circuit, apply 1 μF of MLCC closely at the V5FILT pin with a 300-Ω resistor to create a LPF between 5-V supply and the pin.

10 Layout

10.1 Layout Guidelines

Certain points must be considered before starting a layout work using the TPS51117.

• Connect the RC low-pass filter from 5-V supply to V5FILT, 300 Ω and 1 μF are recommended. Place the filter capacitor close to the device, within 12 mm (0.5 inches) if possible.

• Connect the overcurrent setting resistors from TRIP to GND close to the device, right next to the device, if possible. The trace from TRIP to resistor and resistor to GND should avoid coupling to a high-voltage switching node.

• The discharge path (VOUT) should have a dedicated trace to the output capacitor(s); separate from the output voltage sensing trace, and use a 1.5-mm (60 mils) or wider trace with no loops. Make sure the feedback current setting resistor (the resistor between VFB to GND) is tied close to the device GND. The trace from this resistor to the VFB pin should be short and thin. Place on the component side and avoid vias between this resistor and the device.

• Connections from the drivers to the respective gate of the high-side or the low-side MOSFET should be as short as possible to reduce stray inductance. Use a 0.65-mm (25 mils) or wider trace.

• All sensitive analog traces and components such as VOUT, VFB, GND, EN_PSV, PGOOD, TRIP, V5FILT, and TON should be placed away from high-voltage switching nodes such as LL, DRVL, DRVH or VBST to avoid coupling. Use internal layer(s) as ground plane(s) and shield feedback trace from power traces and components.

• Gather the ground terminals of the V_IN capacitor(s), V_OUT capacitor(s), and the source of the low-side MOSFETs as close as possible. GND (signal ground) and PGND (power ground) should be connected strongly together near the device. The PCB trace defined as LL node, which connects to the source of the high-side MOSFET, the drain of the low-side MOSFET, and the high-voltage side of the inductor, should be as short and wide as possible.
10.2 Layout Example

![Layout Recommendation](image)

**Figure 26. Layout Recommendation**

10.3 Thermal Considerations

Power dissipation of the TPS51117 is mainly generated from the FET drivers. Average drive current can be estimated by gate charge, $Q_g$, times the switching frequency.

$$I_G = Q_g \times f_{SW}$$  \hspace{1cm} (14)

$Q_g$ is the charge needed to charge gate capacitance up to the V5DRV voltage of 5 V. Actual values are shown on MOSFET datasheets provided by the manufacturer. Total power dissipation, therefore, to drive the top and bottom MOSFETs can be calculated by the following equation **Equation 15**.

$$W_{DRIVE} = V_{V5DRV} \times \left( Q_{g(top)} + Q_{g(btm)} \right) \times f_{SW}$$  \hspace{1cm} (15)

This power plus a small amount of dissipation (less than 5 mW) from controller circuitry needs to be effectively dissipated from the package. Maximum power dissipation allowed for the package is calculated by:

$$W_{PKG} = \frac{T_{J(max)} - T_{A(max)}}{R_{θJA}}$$

where

- $T_{J(max)}$ is 125°C.
- $T_{A(max)}$ is the maximum ambient temperature in the system.
- $R_{θJA}$ is the thermal resistance from the silicon junction to the ambient.  \hspace{1cm} (16)

This thermal resistance strongly depends on board layout. The TPS51117 is assembled in a standard TSSOP package and the heat mainly moves to the board through its leads.
11 Device and Documentation Support

11.1 Device Support

11.1.1 Third-Party Products Disclaimer

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Design Support  TI's Design Support  Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.3 Trademarks

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11.4 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.5 Glossary

SLYZ022 — TI Glossary.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.
# PACKAGING INFORMATION

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<th>Lead/Ball Finish</th>
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<td>TSSOP</td>
<td>PW</td>
<td>14</td>
<td>90</td>
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<td>CU NIPDAU</td>
<td>Level-1-260C-UNLIM</td>
<td>-40 to 85</td>
<td>51117</td>
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<td>-40 to 85</td>
<td>51117</td>
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(1) The marketing status values are defined as follows:
- **ACTIVE**: Product device recommended for new designs.
- **LIFEBUY**: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
- **NRND**: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
- **PREVIEW**: Device has been announced but is not in production. Samples may or may not be available.
- **OBSOLETE**: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check [http://www.ti.com/productcontent](http://www.ti.com/productcontent) for the latest availability information and additional product content details.
- **TBD**: The Pb-Free/Green conversion plan has not been defined.
- **Pb-Free (RoHS)**: TI’s terms “Lead-Free” or “Pb-Free” mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
- **Pb-Free (RoHS Exempt)**: This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
- **Green (RoHS & no Sb/Br)**: TI defines “Green” to mean Pb-Free (RoHS compliant), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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## TAPE AND REEL INFORMATION

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</table>

*All dimensions are nominal.*

### TAPE DIMENSIONS

- **A0**: Dimension designed to accommodate the component width
- **B0**: Dimension designed to accommodate the component length
- **K0**: Dimension designed to accommodate the component thickness
- **W**: Overall width of the carrier tape
- **P1**: Pitch between successive cavity centers

### REEL DIMENSIONS

- **Reel Diameter**: The diameter of the reel
- **Reel Width (W1)**: The width of the reel

### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

*Images showing quadrant assignments and sprocket holes.*
### TAPE AND REEL BOX DIMENSIONS

*All dimensions are nominal

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NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.25 each side.
E. Falls within JEDEC MO-153
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC-7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.
NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. OFN (Quad Flatpack No-Lead) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.

⚠️ Pin 1 identifiers are located on both top and bottom of the package and within the zone indicated.

The Pin 1 identifiers are either a molded, marked, or metal feature.
G. Package complies to JEDEC MO-241 variation BA.
THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal via, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.

NOTE: All linear dimensions are in millimeters.
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC-7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat-Pack QFN/SOPN PCB Attachment, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.
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