TPS53355 1.5-V to 15-V Input (4.5-V to 25-V bias), 30-A synch step-down SWIFT™
converter with Eco-mode™

1 Features

- 96% Maximum efficiency
- Conversion input voltage range: 1.5 V to 15 V
- VDD input voltage range: 4.5 V to 25 V
- Output voltage range: 0.6 V to 5.5 V
- 5-V LDO output
- Supports single rail input
- Integrated power MOSFETs with 30 A of continuous output current
- Auto-skip Eco-mode™ for light-load efficiency
- < 10-μA Shutdown current
- D-CAP™ mode with fast transient response
- Selectable switching frequency from 250 kHz to 1 MHz with external resistor
- Selectable auto-skip or PWM-only operation
- Built-in 1% 0.6-V reference
- 0.7-ms, 1.4-ms, 2.8-ms and 5.6-ms Selectable internal voltage servo soft start
- Integrated boost switch
- Precharged start-up capability
- Adjustable overcurrent limit with thermal compensation
- Overvoltage, undervoltage, UVLO and overtemperature protection
- Supports all ceramic output capacitors
- Open-drain power-good indication
- Incorporates NexFET™ power block technology
- 22-Pin QFN package With PowerPAD™
- For SWIFT™ power products documentation, see http://www.ti.com/swift
- Green (RoHS compatible), is optional

2 Applications

- Servers and storage
- Workstations and desktops
- Telecommunications infrastructure

3 Description

TPS53355 is a D-CAP™ mode, 30-A synchronous switcher with integrated MOSFETs. It is designed for ease of use, low external component count, and space-conscious power systems.

This device features 5-mΩ/2-mΩ integrated MOSFETs, accurate 1% 0.6-V reference, and integrated boost switch. A sample of competitive features include: 1.5-V to 15-V wide conversion input voltage range, very low external component count, D-CAP™ mode control for super fast transient, auto-skip mode operation, internal soft-start control, selectable frequency, and no need for compensation.

The conversion input voltage ranges from 1.5 V to 15 V, the supply voltage range is from 4.5 V to 25 V, and the output voltage range is from 0.6 V to 5.5 V.

The device is available in 6-mm × 5-mm, 22-pin QFN package and is specified from –40°C to +85°C.

Device Information

<table>
<thead>
<tr>
<th>PART NUMBER</th>
<th>PACKAGE</th>
<th>BODY SIZE (NOM)</th>
</tr>
</thead>
<tbody>
<tr>
<td>TPS53355</td>
<td>LSON-CLIP (22)</td>
<td>6.00 mm × 5.00 mm</td>
</tr>
</tbody>
</table>

(1) For all available packages, see the orderable addendum at the end of the datasheet.

Typical Application

An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.
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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision D (November 2016) to Revision E Page

- Added links for WEBENCH ......................................................................................... 1
- Deleted “Operating free-air temperature, T_A” row .................................................. 5

Changes from Revision C (February 2016) to Revision D Page

- Added Feature: Green (RoHS Compatible), is Optional ............................................ 1
- Added the VQP package to the Thermal Information .............................................. 5
- From: a SC5026-1R0 inductor is used. To: a 744355182 inductor is used .................. 8
- Changed Figure 32 and Figure 33 ........................................................................... 12
- 5-V LDO and VREG Start-Up, Changed the NOTE From: “The 5-V LDO is not controlled” To: “The 5-V LDO is controlled” ......................................................... 16
- Changed 250 µs To ~550 µs in Figure 34 .................................................................. 16

Changes from Revision B (January 2014) to Revision C Page

- Changed the datasheet Title From: “TPS53355 High-Efficiency 30-A Synchronous Buck Converter With Eco-mode™” To: “TPS53355 High-Efficiency 30-A Synchronous Buck SWIFT™ Converter With Eco-mode™” ......................... 1
- Added Features: “For SWIFT™ Power Products Documentation,...” ......................... 1

Changes from Revision A (September 2012) to Revision B Page

- Added Pin Configuration and Functions section, ESD Ratings table, Feature Description section, Device Functional Modes, Application and Implementation section, Power Supply Recommendations section, Layout section, Device and Documentation Support section, and Mechanical, Packaging, and Orderable Information section ......................................................... 1
Changes from Original (August 2011) to Revision A | Page
---|---
• Changed conversion input voltage from “3 V” to “1.5 V” | 1
• Changed VIN input voltage range minimum from “3 V” to “1.5 V” | 4
• Changed typographical error in THERMAL INFORMATION table | 5
• Changed VIN (main supply) input voltage range minimum from “3 V” to “1.5 V” in Recommended Operating Conditions | 5
• Changed VIN pin power conversion input minimum voltage from “3 V” to “1.5 V” in ELECTRICAL CHARACTERISTICS table | 6
• Changed conversion input voltage range from “3 V” to “1.5” in Overview | 14
• Added note to the Functional Block Diagram | 15
• Changed “ripple injection capacitor” to “ripple injection resistor” in Layout Guidelines section | 30
## 5 Pin Configuration and Functions

### Pin Functions

<table>
<thead>
<tr>
<th>PIN</th>
<th>I/O/P(1)</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>NAME</td>
<td>NO</td>
<td></td>
</tr>
<tr>
<td>EN</td>
<td>2</td>
<td>I</td>
</tr>
<tr>
<td>GND</td>
<td>—</td>
<td>—</td>
</tr>
<tr>
<td>LL</td>
<td>6, 7, 8, 9, 10, 11</td>
<td>B</td>
</tr>
<tr>
<td>MODE</td>
<td>20</td>
<td>I</td>
</tr>
<tr>
<td>N/C</td>
<td>5</td>
<td>No connect.</td>
</tr>
<tr>
<td>PGOOD</td>
<td>3</td>
<td>O</td>
</tr>
<tr>
<td>RF</td>
<td>22</td>
<td>I</td>
</tr>
<tr>
<td>TRIP</td>
<td>21</td>
<td>I</td>
</tr>
<tr>
<td>VBST</td>
<td>4</td>
<td>P</td>
</tr>
<tr>
<td>VDD</td>
<td>19</td>
<td>P</td>
</tr>
<tr>
<td>VFB</td>
<td>1</td>
<td>I</td>
</tr>
<tr>
<td>VIN</td>
<td>12, 13, 14, 15, 16, 17</td>
<td>P</td>
</tr>
<tr>
<td>VREG</td>
<td>18</td>
<td>P</td>
</tr>
</tbody>
</table>

(1) I=Input, O=Output, B=Bidirectional, P=Supply

---

**Note:**

- **VFB:** Voltage Feedback Input
- **EN:** Enable Pin
- **PGOOD:** Power Good Flag
- **VBST:** VBST (Boost Terminal)
- **GND:** Ground
- **LL:** Output of Converted Power
- **MODE:** Soft-Start and Skip/CCM Selection
- **N/C:** No Connection
- **RF:** Switching Frequency Selection
- **TRIP:** OCL Detection Threshold Setting Pin
- **VDD:** Controller Power Supply
- **VFB:** Voltage Feedback
- **VIN:** Conversion Power Input
- **VREG:** 5-V Low Dropout (LDO) Output

---

TPS53355
SLUSAE5E – AUGUST 2011 – REVISED MARCH 2019

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6 Specifications

6.1 Absolute Maximum Ratings (1)

<table>
<thead>
<tr>
<th>Input voltage</th>
<th>MIN</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>VIN (main supply)</td>
<td>–0.3</td>
<td>25</td>
<td>V</td>
</tr>
<tr>
<td>VDD</td>
<td>–0.3</td>
<td>28</td>
<td>V</td>
</tr>
<tr>
<td>VBST</td>
<td>–0.3</td>
<td>32</td>
<td>V</td>
</tr>
<tr>
<td>VBST (with respect to LL)</td>
<td>–0.3</td>
<td>7</td>
<td>V</td>
</tr>
<tr>
<td>EN, TRIP, VFB, RF, MODE</td>
<td>–0.3</td>
<td>7</td>
<td>V</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Output voltage</th>
<th>MIN</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>LL DC</td>
<td>–2</td>
<td>25</td>
<td>V</td>
</tr>
<tr>
<td>Pulse &lt; 20 ns, E = 5 μJ</td>
<td>–7</td>
<td>27</td>
<td>V</td>
</tr>
<tr>
<td>PGOOD, VREG</td>
<td>–0.3</td>
<td>7</td>
<td>V</td>
</tr>
<tr>
<td>GND</td>
<td>–0.3</td>
<td>0.3</td>
<td>mA</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Source/sink current</th>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>VBST</td>
<td>50</td>
<td></td>
<td>mA</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Junction temperature, T_J</th>
<th></th>
<th></th>
<th>°C</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>–40</td>
<td>150</td>
<td>°C</td>
</tr>
</tbody>
</table>

| Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds |     |     | °C   |
|                                                               | –55 | 150 | °C   |

<table>
<thead>
<tr>
<th>Storage temperature, T_stg</th>
<th></th>
<th></th>
<th>°C</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>–55</td>
<td>150</td>
<td>°C</td>
</tr>
</tbody>
</table>

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

<table>
<thead>
<tr>
<th>VALUE</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>±2000</td>
<td>V</td>
</tr>
<tr>
<td>±500</td>
<td>V</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Electrostatic discharge</th>
<th>VALUE</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1)</td>
<td>±2000</td>
<td>V</td>
</tr>
<tr>
<td>Charged-device model (CDM), per JEDEC specification JESD22-C101 (2)</td>
<td>±500</td>
<td>V</td>
</tr>
</tbody>
</table>

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

<table>
<thead>
<tr>
<th>Input voltage range</th>
<th>MIN</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>VIN (main supply)</td>
<td>1.5</td>
<td>15</td>
<td>V</td>
</tr>
<tr>
<td>VDD</td>
<td>4.5</td>
<td>25</td>
<td>V</td>
</tr>
<tr>
<td>VBST</td>
<td>4.5</td>
<td>28</td>
<td>V</td>
</tr>
<tr>
<td>VBST (with respect to LL)</td>
<td>–0.1</td>
<td>6.5</td>
<td>V</td>
</tr>
<tr>
<td>EN, TRIP, VFB, RF, MODE</td>
<td>–0.1</td>
<td>6.5</td>
<td>V</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Output voltage range</th>
<th>MIN</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>LL</td>
<td>–1</td>
<td>22</td>
<td>V</td>
</tr>
<tr>
<td>PGOOD, VREG</td>
<td>–0.1</td>
<td>6.5</td>
<td>V</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Junction temperature range, T_J</th>
<th>MIN</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>–40</td>
<td>125</td>
<td>°C</td>
</tr>
</tbody>
</table>

6.4 Thermal Information

<table>
<thead>
<tr>
<th>THERMAL METRIC (1)</th>
<th>TPS53355</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>DOP</td>
</tr>
<tr>
<td></td>
<td>22 PINS</td>
</tr>
<tr>
<td>( \theta_{JA} ) Junction-to-ambient thermal resistance</td>
<td>27.2</td>
</tr>
<tr>
<td>( \theta_{Jc} ) Junction-to-case (top) thermal resistance</td>
<td>17.1</td>
</tr>
<tr>
<td>( \theta_{JB} ) Junction-to-board thermal resistance</td>
<td>5.9</td>
</tr>
<tr>
<td>( \psi_{JT} ) Junction-to-top characterization parameter</td>
<td>0.8</td>
</tr>
</tbody>
</table>

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.
Thermal Information (continued)

<table>
<thead>
<tr>
<th>THERMAL METRIC(1)</th>
<th>TPS53355</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>DQP</td>
</tr>
<tr>
<td></td>
<td>22 PINS</td>
</tr>
<tr>
<td>$V_{JB}$</td>
<td>5.8</td>
</tr>
<tr>
<td>$\theta_{Jcb}$</td>
<td>1.2</td>
</tr>
</tbody>
</table>

6.5 Electrical Characteristics

Over recommended free-air temperature range, $V_{DD}=12$ V (unless otherwise noted)

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>SUPPLY CURRENT</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$V_{VIN}$</td>
<td>VIN pin power conversion input voltage</td>
<td>1.5</td>
<td>15</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>$V_{DD}$</td>
<td>Supply input voltage</td>
<td>4.5</td>
<td>25</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>$I_{VIN(leak)}$</td>
<td>VIN pin leakage current $V_{EN}=0$ V</td>
<td></td>
<td>1</td>
<td>µA</td>
<td></td>
</tr>
<tr>
<td>$I_{VDD}$</td>
<td>VDD supply current $T_A=25^\circ$C, No load, $V_{EN}=5$ V, $V_{VFB}=0.630$ V</td>
<td>420</td>
<td>590</td>
<td>µA</td>
<td></td>
</tr>
<tr>
<td>$I_{VDDSDN}$</td>
<td>VDD shutdown current $T_A=25^\circ$C, No load, $V_{EN}=0$ V</td>
<td>10</td>
<td></td>
<td>µA</td>
<td></td>
</tr>
<tr>
<td>INTERNAL REFERENCE VOLTAGE</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$V_{VFB}$</td>
<td>VFB regulation voltage CCM condition(1)</td>
<td>0.6</td>
<td></td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>$V_{VFB}$</td>
<td>VFB regulation voltage $T_A=25^\circ$C $0^\circ$C $\leq T_A \leq 85^\circ$C $-40^\circ$C $\leq T_A \leq 85^\circ$C</td>
<td>0.597</td>
<td>0.6</td>
<td>0.603 V</td>
<td></td>
</tr>
<tr>
<td>$I_{VFB}$</td>
<td>VFB input current $V_{VFB}=0.630$ V, $T_A=25^\circ$C</td>
<td>0.01</td>
<td>0.20</td>
<td>µA</td>
<td></td>
</tr>
<tr>
<td>LDO OUTPUT</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$V_{VREG}$</td>
<td>LDO output voltage $0$ mA $\leq I_{VREG} \leq 30$ mA</td>
<td>4.77</td>
<td>5</td>
<td>5.36</td>
<td>V</td>
</tr>
<tr>
<td>$I_{VREG}$</td>
<td>LDO output current(1) Maximum current allowed from LDO</td>
<td></td>
<td></td>
<td>30</td>
<td>mA</td>
</tr>
<tr>
<td>$V_{DO}$</td>
<td>Low drop out voltage $V_{VDD}=4.5$ V, $I_{VREG}=30$ mA</td>
<td></td>
<td></td>
<td>230</td>
<td>mV</td>
</tr>
<tr>
<td>BOOT-STRAP SWITCH</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$V_{FBST}$</td>
<td>Forward voltage $V_{VREG-VBST}$, $I_f=10$ mA, $T_A=25^\circ$C</td>
<td>0.1</td>
<td>0.2</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>$I_{VBSTLK}$</td>
<td>VBST leakage current $V_{VBST}=23$ V, $V_{SW}=17$ V, $T_A=25^\circ$C</td>
<td>0.01</td>
<td>1.50</td>
<td>µA</td>
<td></td>
</tr>
<tr>
<td>DUTY AND FREQUENCY CONTROL</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$I_{OFF(min)}$</td>
<td>Minimum off time $T_A=25^\circ$C</td>
<td>150</td>
<td>260</td>
<td>400</td>
<td>ns</td>
</tr>
<tr>
<td>$I_{ON(min)}$</td>
<td>Minimum on time $V_{IN}=17$ V, $V_{OUT}=0.6$ V, $R_{RF}=39$ kΩ, $T_A=25^\circ$C(1)</td>
<td>35</td>
<td></td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>SOFT START</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$I_{SS}$</td>
<td>Internal soft-start time from $V_{OUT}=0$ V to 95% of $V_{OUT}$ $R_{MODE}=39$ kΩ</td>
<td></td>
<td></td>
<td>0.7</td>
<td>ms</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>INTERNAL MOSFETS</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$R_{DS(on)H}$</td>
<td>High-side MOSFET on-resistance $T_A=25^\circ$C</td>
<td></td>
<td></td>
<td>5</td>
<td>mΩ</td>
</tr>
<tr>
<td>$R_{DS(on)L}$</td>
<td>Low-side MOSFET on-resistance $T_A=25^\circ$C</td>
<td></td>
<td></td>
<td>2</td>
<td>mΩ</td>
</tr>
</tbody>
</table>

(1) Ensured by design. Not production tested.
## Electrical Characteristics (continued)

Over recommended free-air temperature range, \( V_{\text{DD}} = 12 \) V (unless otherwise noted)

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>( V_{\text{THPG}} )</td>
<td>PG threshold</td>
<td>PG in from lower</td>
<td>92.5%</td>
<td>95.0%</td>
<td>98.5%</td>
</tr>
<tr>
<td></td>
<td></td>
<td>PG in from higher</td>
<td>107.5%</td>
<td>110.0%</td>
<td>112.5%</td>
</tr>
<tr>
<td></td>
<td></td>
<td>PG hysteresis</td>
<td>2.5%</td>
<td>5.0%</td>
<td>7.5%</td>
</tr>
<tr>
<td>( R_{\text{PG}} )</td>
<td>PG transistor on-resistance</td>
<td>15</td>
<td>30</td>
<td>55</td>
<td>Ω</td>
</tr>
<tr>
<td>( t_{\text{PGDEL}} )</td>
<td>PG delay</td>
<td>0.8</td>
<td>1</td>
<td>1.2</td>
<td>ms</td>
</tr>
</tbody>
</table>

### LOGIC THRESHOLD AND SETTING CONDITIONS

| \( V_{\text{EN}} \) | EN Voltage | Enable | 1.8 | V |
| | | Disable | 0.6 | |
| \( I_{\text{EN}} \) | EN Input current | \( V_{\text{EN}} = 5 \) V | 1.0 | μA |

### PROTECTION: CURRENT SENSE

| \( I_{\text{TRIP}} \) | TRIP source current | \( V_{\text{TRIP}} = 1 \) V, \( T_{A} = 25^\circ \)C | 9.4 | 10.0 | 10.6 | μA |
| \( T_{\text{CITRIP}} \) | TRIP current temperature coefficient | On the basis of 25°C(1) | 4700 | ppm/°C |

### PROTECTION: UVP and OVP

| \( V_{\text{OVP}} \) | OVP trip threshold | OVP detect | 115% | 120% | 125% |
| \( I_{\text{OVPPDEL}} \) | OVP propagation delay | VFB delay with 50-mV overdrive | 1 | μs |
| \( V_{\text{UVP}} \) | Output UVP trip threshold | UVP detect | 65% | 70% | 75% |
| \( I_{\text{UVPDEL}} \) | Output UVP propagation delay | | 0.8 | 1.0 | 1.2 | ms |
| \( I_{\text{UVPPEN}} \) | Output UVP enable delay | From enable to UVP workable | 1.8 | 2.6 | 3.2 | ms |

| \( V_{\text{UVVREG}} \) | VREG UVLO threshold | Wake up | 4.00 | 4.20 | 4.33 | V |
| | | Hysteresis | 0.25 | |

### THERMAL SHUTDOWN

| \( T_{\text{SDN}} \) | Thermal shutdown threshold | Shutdown temperature(1) | 145 | °C |
| | | Hysteresis(1) | 10 | |

(2) Not production tested. Test condition is \( V_{\text{IN}} = 12 \) V, \( V_{\text{OUT}} = 1.1 \) V, \( I_{\text{OUT}} = 10 \) A using application circuit shown in Figure 47.
6.6 Typical Characteristics

For $V_{OUT} = 5\, V$, a 744355182 inductor is used. For $1 \leq V_{OUT} \leq 3.3\, V$, a PA0513.441 inductor is used.

---

**Figure 1. VDD Supply Current vs Junction Temperature**

**Figure 2. VDD Shutdown Current vs Junction Temperature**

**Figure 3. TRIP Pin Current vs Junction Temperature**

**Figure 4. OVP/UVP Trip Threshold vs Junction Temperature**

**Figure 5. Switching Frequency vs Output Current**

**Figure 6. Switching Frequency vs Output Current**
Typical Characteristics (continued)

For $V_{OUT} = 5\, \text{V}$, a 744355182 inductor is used. For $1 \leq V_{OUT} \leq 3.3\, \text{V}$, a PA0513.441 inductor is used.

Figure 7. Switching Frequency vs Output Current

Figure 8. Switching Frequency vs Output Current

Figure 9. Switching Frequency vs Output Voltage

Figure 10. Output Voltage vs Output Current

Figure 11. Output Voltage vs Input Voltage

Figure 12. Efficiency vs Output Current
Typical Characteristics (continued)

For $V_{OUT} = 5\,\text{V}$, a 744355182 inductor is used. For $1 \leq V_{OUT} \leq 3.3\,\text{V}$, a PA0513.441 inductor is used.

---

**Figure 13. Efficiency vs Output Current**

**Figure 14. Efficiency vs Output Current**

**Figure 15. Efficiency vs Output Current**

**Figure 16. Efficiency vs Output Current**

**Figure 17. Efficiency vs Output Current**

**Figure 18. Efficiency vs Output Current**
**Typical Characteristics (continued)**

For $V_{\text{OUT}} = 5$ V, a 744355182 inductor is used. For $1 \leq V_{\text{OUT}} \leq 3.3$ V, a PA0513.441 inductor is used.

---

**Figure 19. Start-Up Waveforms**

**Figure 20. Pre-Bias Start-Up Waveforms**

**Figure 21. Shutdown Waveforms**

**Figure 22. UVLO Start-Up Waveforms**

**Figure 23. 1.1-V Output FCCM Mode Steady-State Operation**

**Figure 24. 1.1-V Output Skip Mode Steady-State Operation**
Typical Characteristics (continued)

For $V_{OUT} = 5$ V, a 744355182 inductor is used. For $1 \leq V_{OUT} \leq 3.3$ V, a PA0513.441 inductor is used.

![Figure 25. CCM to DCM Transition Waveforms](image1)

![Figure 26. DCM to CCM Transition Waveforms](image2)

![Figure 27. FCCM Load Transient](image3)

![Figure 28. Skip Mode Load Transient](image4)

![Figure 29. Overcurrent Protection Waveforms](image5)

![Figure 30. Output Short Circuit Protection Waveforms](image6)
Typical Characteristics (continued)

For \( V_{\text{OUT}} = 5 \text{ V} \), a 744355182 inductor is used. For \( 1 \leq V_{\text{OUT}} \leq 3.3 \text{ V} \), a PA0513.441 inductor is used.

![Over-temperature Protection Waveforms](image1)

![Safe Operating Area](image2)

![Safe Operating Area](image3)
7 Detailed Description

7.1 Overview

The TPS53355 is a high-efficiency, single channel, synchronous buck converter suitable for low output voltage point-of-load applications in computing and similar digital consumer applications. The device features proprietary D-CAP™ mode control combined with an adaptive on-time architecture. This combination is ideal for building modern low duty ratio, ultra-fast load step response DC-DC converters. The output voltage ranges from 0.6 V to 5.5 V. The conversion input voltage range is from 1.5 V up to 15 V and the VDD bias voltage is from 4.5 V to 25 V. The D-CAP™ mode uses the equivalent series resistance (ESR) of the output capacitor(s) to sense the device current. One advantage of this control scheme is that it does not require an external phase compensation network. This allows a simple design with a low external component count. Eight preset switching frequency values can be chosen using a resistor connected from the RF pin to ground or VREG. Adaptive on-time control tracks the preset switching frequency over a wide input and output voltage range while allowing the switching frequency to increase at the step-up of the load.

The TPS53355 has a MODE pin to select between auto-skip mode and forced continuous conduction mode (FCCM) for light load conditions. The MODE pin also sets the selectable soft-start time ranging from 0.7 ms to 5.6 ms as shown in Table 3.
7.2 Functional Block Diagram

NOTE
The thresholds in this block diagram are typical values. Refer to the Electrical Characteristics table for threshold limits.
7.3 Feature Description

7.3.1 5-V LDO and VREG Start-Up

TPS53355 provides an internal 5-V LDO function using input from VDD and output to VREG. When the VDD voltage rises above 2 V, the internal LDO is enabled and outputs voltage to the VREG pin. The VREG voltage provides the bias voltage for the internal analog circuitry and also provides the supply voltage for the gate drives.

NOTE
The 5-V LDO is controlled by the EN pin. The LDO starts-up any time VDD rises to approximately 2 V. Figure 34

7.3.2 Adaptive On-Time D-CAP Control and Frequency Selection

The TPS53355 does not have a dedicated oscillator to determine switching frequency. However, the device operates with pseudo-constant frequency by feed-forwarding the input and output voltages into the on-time one-shot timer. The adaptive on-time control adjusts the on-time to be inversely proportional to the input voltage and proportional to the output voltage ($t_{\text{ON}} \propto V_{\text{OUT}}/V_{\text{IN}}$).

This makes the switching frequency fairly constant in steady state conditions over a wide input voltage range. The switching frequency is selectable from eight preset values by a resistor connected between the RF pin and GND or between the RF pin and the VREG pin as shown in Table 1. (Maintaining open resistance sets the switching frequency to 500 kHz.)

<table>
<thead>
<tr>
<th>RESISTOR ($R_{\text{RF}}$)</th>
<th>CONNECTIONS</th>
<th>SWITCHING FREQUENCY ($f_{\text{SW}}$) (kHz)</th>
</tr>
</thead>
<tbody>
<tr>
<td>VALUE (kΩ)</td>
<td>CONNECT TO</td>
<td></td>
</tr>
<tr>
<td>0</td>
<td>GND</td>
<td>250</td>
</tr>
<tr>
<td>187</td>
<td>GND</td>
<td>300</td>
</tr>
<tr>
<td>619</td>
<td>GND</td>
<td>400</td>
</tr>
<tr>
<td>OPEN</td>
<td>n/a</td>
<td>500</td>
</tr>
<tr>
<td>866</td>
<td>VREG</td>
<td>650</td>
</tr>
<tr>
<td>309</td>
<td>VREG</td>
<td>750</td>
</tr>
<tr>
<td>124</td>
<td>VREG</td>
<td>850</td>
</tr>
<tr>
<td>0</td>
<td>VREG</td>
<td>970</td>
</tr>
</tbody>
</table>

The off-time is modulated by a PWM comparator. The VFB node voltage (the mid-point of resistor divider) is compared to the internal 0.6-V reference voltage added with a ramp signal. When both signals match, the PWM comparator asserts a set signal to terminate the off time (turn off the low-side MOSFET and turn on high-side MOSFET). The set signal is valid if the inductor current level is below the OCP threshold, otherwise the off time is extended until the current level falls below the threshold.

Figure 35 and Figure 36 show two on-time control schemes.
7.3.3 Ramp Signal

The TPS53355 adds a ramp signal to the 0.6-V reference in order to improve jitter performance. As described in the previous section, the feedback voltage is compared with the reference information to keep the output voltage in regulation. By adding a small ramp signal to the reference, the signal-to-noise ratio at the onset of a new switching cycle is improved. Therefore the operation becomes less jittery and more stable. The ramp signal is controlled to start with –7 mV at the beginning of an on-cycle and becomes 0 mV at the end of an off-cycle in steady state.

During skip mode operation, under discontinuous conduction mode (DCM), the switching frequency is lower than the nominal frequency and the off-time is longer than the off-time in CCM. Because of the longer off-time, the ramp signal extends after crossing 0 mV. However, it is clamped at 3 mV to minimize the DC offset.

7.3.4 Adaptive Zero Crossing

The TPS53355 has an adaptive zero crossing circuit which performs optimization of the zero inductor current detection at skip mode operation. This function pursues ideal low-side MOSFET turning off timing and compensates inherent offset voltage of the Z-C comparator and delay time of the Z-C detection circuit. It prevents SW-node swing-up caused by too late detection and minimizes diode conduction period caused by too early detection. As a result, better light load efficiency is delivered.

7.3.5 Power-Good

The TPS53355 has power-good output that indicates high when switcher output is within the target. The power-good function is activated after soft-start has finished. If the output voltage becomes within +10% and –5% of the target value, internal comparators detect power-good state and the power-good signal becomes high after a 1-ms internal delay. If the output voltage goes outside of +15% or –10% of the target value, the power-good signal becomes low after two microsecond (2-μs) internal delay. The power-good output is an open drain output and must be pulled up externally.
The power-good MOSFET is powered through the VDD pin. \( V_{\text{DD}} \) must be >1 V in order to have a valid power-good logic. It is recommended to pull PGOOD up to VREG (or a voltage divided from VREG) so that the power-good logic is still valid even without VDD supply.

### 7.3.6 Current Sense, Overcurrent and Short Circuit Protection

TPS53355 has cycle-by-cycle overcurrent limiting control. The inductor current is monitored during the \( \text{OFF} \) state and the controller maintains the \( \text{OFF} \) state during the period in that the inductor current is larger than the overcurrent trip level. In order to provide both good accuracy and cost effective solution, TPS53355 supports temperature compensated MOSFET \( R_{\text{DS(on)}} \) sensing. The TRIP pin should be connected to GND through the trip voltage setting resistor, \( R_{\text{TRIP}} \). The TRIP terminal sources current \( I_{\text{TRIP}} \) which is 10 \( \mu \)A typically at room temperature, and the trip level is set to the OCL trip voltage \( V_{\text{TRIP}} \) as shown in Equation 1.

\[
V_{\text{TRIP}} \ (mV) = R_{\text{TRIP}} \ (k\Omega) \times I_{\text{TRIP}} \ (\mu A)
\]  

(1)

The inductor current is monitored by the LL pin. The GND pin is used as the positive current sensing node and the LL pin is used as the negative current sense node. The trip current, \( I_{\text{TRIP}} \) has 4700ppm/°C temperature slope to compensate the temperature dependency of the \( R_{\text{DS(on)}} \).

As the comparison is made during the \( \text{OFF} \) state, \( V_{\text{TRIP}} \) sets the valley level of the inductor current. Thus, the load current at the overcurrent threshold, \( I_{\text{OCP}} \), can be calculated as shown in Equation 2.

\[
I_{\text{OCP}} = \frac{V_{\text{TRIP}}}{(32 \times R_{\text{DS(on)}})} + \frac{I_{\text{ND(ripple)}}}{2} = \frac{V_{\text{TRIP}}}{(32 \times R_{\text{DS(on)}})} + \frac{1}{2 \times L \times f_{\text{SW}}} \times \frac{(V_{\text{IN}} - V_{\text{OUT}})}{V_{\text{IN}}} \times V_{\text{OUT}}
\]  

(2)

In an overcurrent or short circuit condition, the current to the load exceeds the current to the output capacitor thus the output voltage tends to decrease. Eventually, it crosses the undervoltage protection threshold and shuts down. After a hiccup delay (16 ms with 0.7 ms sort-start), the controller restarts. If the overcurrent condition remains, the procedure is repeated and the device enters hiccup mode.

### Hiccup time calculation:

\[
\begin{align*}
&\quad t_{\text{HIC(wait)}} = (2^n + 257) \times 4 \mu s \\
&\text{where} \\
&\quad n = 8, 9, 10, \text{or} \ 11 \ \text{depending on soft start time selection} \\
&\quad t_{\text{HIC(dly)}} = 7 \times (2^n + 257) \times 4 \mu s
\end{align*}
\]  

(3)  

(4)

#### Table 2. Hiccup Delay

<table>
<thead>
<tr>
<th>SELECTED SOFT-START TIME (( t_{\text{SS}} )) (ms)</th>
<th>( n )</th>
<th>HICCUP WAIT TIME (( t_{\text{HIC(wait)}} )) (ms)</th>
<th>HICCUP DELAY TIME (( t_{\text{HIC(dly)}} )) (ms)</th>
</tr>
</thead>
<tbody>
<tr>
<td>0.7</td>
<td>8</td>
<td>2.052</td>
<td>14.364</td>
</tr>
<tr>
<td>1.4</td>
<td>9</td>
<td>3.076</td>
<td>21.532</td>
</tr>
<tr>
<td>2.8</td>
<td>10</td>
<td>5.124</td>
<td>35.868</td>
</tr>
<tr>
<td>5.6</td>
<td>11</td>
<td>9.220</td>
<td>64.540</td>
</tr>
</tbody>
</table>

### 7.3.7 Overvoltage and Undervoltage Protection

TPS53355 monitors a resistor divided feedback voltage to detect over and under voltage. When the feedback voltage becomes lower than 70% of the target voltage, the UVP comparator output goes high and an internal UVP delay counter begins counting. After 1ms, TPS53355 latches OFF both high-side and low-side MOSFETs drivers. The controller restarts after a hiccup delay (16 ms with 0.7 ms sort-start). This function is enabled 1.5-ms after the soft-start is completed.

When the feedback voltage becomes higher than 120% of the target voltage, the OVP comparator output goes high and the circuit latches OFF the high-side MOSFET driver and latches ON the low-side MOSFET driver. The output voltage decreases. If the output voltage reaches UV threshold, then both high-side MOSFET and low-side MOSFET driver will be OFF and the device restarts after a hiccup delay. If the OV condition remains, both high-side MOSFET and low-side MOSFET driver remains OFF until the OV condition is removed.
7.3.8 **UVLO Protection**

The TPS53355 uses VREG undervoltage lockout protection (UVLO). When the VREG voltage is lower than 3.95 V, the device shuts off. When the VREG voltage is higher than 4.2 V, the device restarts. This is a non-latch protection.

7.3.9 **Thermal Shutdown**

TPS53355 monitors the temperature of itself. If the temperature exceeds the threshold value (typically 145°C), TPS53355 is shut off. When the temperature falls about 10°C below the threshold value, the device will turn back on. This is a non-latch protection.

7.4 **Device Functional Modes**

7.4.1 **Enable, Soft Start, and Mode Selection**

When the EN pin voltage rises above the enable threshold voltage (typically 1.2 V), the controller enters its start-up sequence. The internal LDO regulator starts immediately and regulates to 5 V at the VREG pin. The controller then uses the first 250 μs to calibrate the switching frequency setting resistance attached to the RF pin and stores the switching frequency code in internal registers. During this period, the MODE pin also senses the resistance attached to this pin and determines the soft-start time. Switching is inhibited during this phase. In the second phase, an internal DAC starts ramping up the reference voltage from 0 V to 0.6 V. Depending on the MODE pin setting, the ramping up time varies from 0.7 ms to 5.6 ms. Smooth and constant ramp-up of the output voltage is maintained during start-up regardless of load current.

<table>
<thead>
<tr>
<th>MODE SELECTION</th>
<th>ACTION</th>
<th>SOFT-START TIME (ms)</th>
<th>R\text{MODE} (kΩ)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Auto Skip</td>
<td>Pull down to GND</td>
<td>0.7</td>
<td>39</td>
</tr>
<tr>
<td></td>
<td></td>
<td>1.4</td>
<td>100</td>
</tr>
<tr>
<td></td>
<td></td>
<td>2.8</td>
<td>200</td>
</tr>
<tr>
<td></td>
<td></td>
<td>5.6</td>
<td>475</td>
</tr>
<tr>
<td>Forced CCM(^{(1)})</td>
<td>Connect to PGOOD</td>
<td>0.7</td>
<td>39</td>
</tr>
<tr>
<td></td>
<td></td>
<td>1.4</td>
<td>100</td>
</tr>
<tr>
<td></td>
<td></td>
<td>2.8</td>
<td>200</td>
</tr>
<tr>
<td></td>
<td></td>
<td>5.6</td>
<td>475</td>
</tr>
</tbody>
</table>

\(^{(1)}\) Device enters FCCM after the PGOOD pin goes high when MODE is connected to PGOOD through the resistor R\text{MODE}.

After soft start begins, the MODE pin becomes the input of an internal comparator which determines auto skip or FCCM mode operation. If MODE voltage is higher than 1.3 V, the converter enters into FCCM mode. Otherwise it will be in auto skip mode at light load condition. Typically, when FCCM mode is selected, the MODE pin is connected to PGOOD through the R\text{MODE} resistor, so that before PGOOD goes high the converter remains in auto skip mode.
7.4.2 Auto-Skip Eco-mode™ Light Load Operation

While the MODE pin is pulled low via $R_{\text{MODE}}$, TPS53355 automatically reduces the switching frequency at light load conditions to maintain high efficiency. Detailed operation is described as follows. As the output current decreases from heavy load condition, the inductor current is also reduced and eventually comes to the point that its rippled valley touches zero level, which is the boundary between continuous conduction and discontinuous conduction modes. The synchronous MOSFET is turned off when this zero inductor current is detected. As the load current further decreases, the converter runs into discontinuous conduction mode (DCM). The on-time is kept almost the same as it was in the continuous conduction mode so that it takes longer time to discharge the output capacitor with smaller load current to the level of the reference voltage. The transition point to the light-load operation $I_{\text{OUT(LL)}}$ (i.e., the threshold between continuous and discontinuous conduction mode) can be calculated as shown in Equation 5.

$$I_{\text{OUT(LL)}} = \frac{1}{2L \times f_{\text{SW}}} \times \frac{(V_{\text{IN}} - V_{\text{OUT}}) \times V_{\text{OUT}}}{V_{\text{IN}}}$$

where
- $f_{\text{SW}}$ is the PWM switching frequency

Switching frequency versus output current in the light load condition is a function of $L$, $V_{\text{IN}}$ and $V_{\text{OUT}}$, but it decreases almost proportionally to the output current from the $I_{\text{OUT(LL)}}$ given in Equation 5. For example, it is 60 kHz at $I_{\text{OUT(LL)}}/5$ if the frequency setting is 300 kHz.

7.4.3 Forced Continuous Conduction Mode

When the MODE pin is tied to PGOOD through a resistor, the controller keeps continuous conduction mode (CCM) in light load condition. In this mode, switching frequency is kept almost constant over the entire load range which is suitable for applications that need tight control of the switching frequency at a cost of lower efficiency.
8 Application and Implementation

NOTE
Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The TPS53355 is a high-efficiency, single channel, synchronous buck converter suitable for low output voltage point-of-load applications in computing and similar digital consumer applications. The device features proprietary D-CAP mode control combined with an adaptive on-time architecture. This combination is ideal for building modern low duty ratio, ultra-fast load step response DC-DC converters. The output voltage ranges from 0.6 V to 5.5 V. The conversion input voltage range is from 1.5 V up to 15 V and the VDD bias voltage is from 4.5 V to 25 V. The D-CAP mode uses the equivalent series resistance (ESR) of the output capacitor(s) to sense the device current. One advantage of this control scheme is that it does not require an external phase compensation network. This allows a simple design with a low external component count. Eight preset switching frequency values can be chosen using a resistor connected from the RF pin to ground or VREG. Adaptive on-time control tracks the preset switching frequency over a wide input and output voltage range while allowing the switching frequency to increase at the step-up of the load.

8.1.1 Small Signal Model

From small-signal loop analysis, a buck converter using D-CAP™ mode can be simplified as shown in Figure 37.

![Figure 37. Simplified Modulator Model](image_url)

The output voltage is compared with the internal reference voltage (ramp signal is ignored here for simplicity). The PWM comparator determines the timing to turn on the high-side MOSFET. The gain and speed of the comparator can be assumed high enough to keep the voltage at the beginning of each cycle substantially constant.

\[
H(s) = \frac{1}{s \times \text{ESR} \times \text{C}_\text{OUT}}
\] (6)
Application Information (continued)

For loop stability, the 0-dB frequency, \( f_0 \), defined below need to be lower than 1/4 of the switching frequency.

\[
f_0 = \frac{1}{2\pi \times \text{ESR} \times C_{\text{OUT}}} \leq \frac{f_{\text{SW}}}{4}
\]  

(7)

According to the equation above, the loop stability of D-CAP\textsuperscript{TM} mode modulator is mainly determined by the capacitor's chemistry. For example, specialty polymer capacitors (SP-CAP) have an output capacitance in the order of several 100 µF and ESR in range of 10 mΩ. These makes \( f_0 \) on the order of 100 kHz or less, creating a stable loop. However, ceramic capacitors have an \( f_0 \) at more than 700 kHz, and need special care when used with this modulator. An application circuit for ceramic capacitor is described in External Component Selection Using All Ceramic Output Capacitors.

8.2 Typical Applications

8.2.1 Typical Application Circuit Diagram with Ceramic Output Capacitors

Figure 38. Typical Application Circuit Diagram with Ceramic Output Capacitors Schematic
Typical Applications (continued)

8.2.1.1 Design Requirements

<table>
<thead>
<tr>
<th>Table 4. Design Parameters</th>
</tr>
</thead>
<tbody>
<tr>
<td>PARAMETER</td>
</tr>
<tr>
<td>INPUT CHARACTERISTICS</td>
</tr>
<tr>
<td>$V_{IN}$</td>
</tr>
<tr>
<td>$I_{MAX}$</td>
</tr>
<tr>
<td>No load input current</td>
</tr>
<tr>
<td>OUTPUT CHARACTERISTICS</td>
</tr>
<tr>
<td>$V_{OUT}$</td>
</tr>
<tr>
<td></td>
</tr>
<tr>
<td></td>
</tr>
<tr>
<td>$V_{RIPPLE}$</td>
</tr>
<tr>
<td>$I_{LOAD}$</td>
</tr>
<tr>
<td>$I_{OCP}$</td>
</tr>
<tr>
<td>$t_{SS}$</td>
</tr>
<tr>
<td>SYSTEMS CHARACTERISTICS</td>
</tr>
<tr>
<td>$f_{SW}$</td>
</tr>
<tr>
<td>$\eta$</td>
</tr>
<tr>
<td>Full load efficiency</td>
</tr>
<tr>
<td>$T_A$</td>
</tr>
</tbody>
</table>

8.2.1.2 Detailed Design Procedure

8.2.1.2.1 Custom Design With WEBENCH® Tools

Click here to create a custom design using the TPS53355 device with the WEBENCH® Power Designer.

1. Start by entering the input voltage ($V_{IN}$), output voltage ($V_{OUT}$), and output current ($I_{OUT}$) requirements.
2. Optimize the design for key parameters such as efficiency, footprint, and cost using the optimizer dial.
3. Compare the generated design with other possible solutions from Texas Instruments.

The WEBENCH Power Designer provides a customized schematic along with a list of materials with real-time pricing and component availability.

In most cases, these actions are available:
- Run electrical simulations to see important waveforms and circuit performance
- Run thermal simulations to understand board thermal performance
- Export customized schematic and layout into popular CAD formats
- Print PDF reports for the design, and share the design with colleagues

Get more information about WEBENCH tools at www.ti.com/WEBENCH.
8.2.1.2.2 External Component Selection

The external components selection is a simple process when using organic semiconductors or special polymer output capacitors.

1. Select operation mode and soft-start time

Select operation mode and soft-start time using Table 3.

2. Select switching frequency

Select the switching frequency from 250 kHz to 1 MHz using Table 1.

3. Choose the inductor

The inductance value should be determined to give the ripple current of approximately 1/4 to 1/2 of maximum output current. Larger ripple current increases output ripple voltage and improves signal-to-noise ratio and helps ensure stable operation, but increases inductor core loss. Using 1/3 ripple current to maximum output current ratio, the inductance can be determined by Equation 8.

\[
L = \frac{1}{i_{\text{IND(ripple)}} \times f_{\text{SW}}} \times \frac{v_{\text{IN(max)}} - v_{\text{OUT}}} {v_{\text{IN(max)}}} \times \frac{v_{\text{OUT}}} {i_{\text{OUT(max)}} \times f_{\text{SW}}} = \frac{3}{v_{\text{IN(max)}}} \times \frac{v_{\text{OUT}}} {i_{\text{OUT(max)}}}
\]

(8)

The inductor requires a low DCR to achieve good efficiency. It also requires enough room above peak inductor current before saturation. The peak inductor current can be estimated in Equation 9.

\[
i_{\text{IND(peak)}} = \frac{v_{\text{TRIP}}}{32 \times R_{\text{DS(on)}}} + \frac{1}{L \times f_{\text{SW}}} \times \frac{v_{\text{IN(max)}} - v_{\text{OUT}}} {v_{\text{IN(max)}}} \times \frac{v_{\text{OUT}}} {v_{\text{IN}}}
\]

(9)

4. External component selection with all ceramic output capacitors

Refer to [external component selection using all ceramic output capacitors] to select external components because ceramic output capacitors are used in this design.

5. Choose the overcurrent setting resistor

The overcurrent setting resistor, \( R_{\text{TRIP}} \), can be determined by Equation 10.

\[
R_{\text{TRIP}} (\Omega) = \left( \frac{1}{i_{\text{TRIP}}} - \left( \frac{1}{2 \times L \times f_{\text{SW}}} \right) \times \frac{v_{\text{IN}} - v_{\text{OUT}}}{v_{\text{IN}}} \times v_{\text{OUT}} \right) \times 32 \times R_{\text{DS(on)}} (\text{m}\Omega)
\]

where

- \( i_{\text{TRIP}} \) is the TRIP pin sourcing current (10 µA)
- \( R_{\text{DS(on)}} \) is the thermally compensated on-time resistance value of the low-side MOSFET

Use an \( R_{\text{DS(on)}} \) value of 1.5 mΩ for an overcurrent level of approximately 30 A. Use an \( R_{\text{DS(on)}} \) value of 1.7 mΩ for overcurrent level of approximately 10 A.

8.2.1.2.3 External Component Selection Using All Ceramic Output Capacitors

When a ceramic output capacitor is used, the stability criteria in Equation 7 cannot be satisfied. The ripple injection approach as shown in Figure 38 is implemented to increase the ripple on the VFB pin and make the system stable. In addition to the selections made using steps 1 through step 6 in External Component Selection, the ripple injection components must be selected. The \( C_2 \) value can be fixed at 1 nF. The value of \( C_1 \) can be selected between 10 nF to 200 nF.

\[
\frac{L \times C_{\text{OUT}}}{R_7 \times C_1} > N \times \frac{t_{\text{ON}}}{2}
\]

where

- \( N \) is the coefficient to account for \( L \) and \( C_{\text{OUT}} \) variation

\[
N = \frac{1}{2}
\]

(11)
N is also used to provide enough margin for stability. It is recommended N=2 for V_{OUT} \leq 1.8 V and N=4 for V_{OUT} \geq 3.3 V or when L \leq 250 nH. The higher V_{OUT} needs a higher N value because the effective output capacitance is reduced significantly with higher DC bias. For example, a 6.3-V, 22-µF ceramic capacitor may have only 8 µF of effective capacitance when biased at 5 V.

Because the VFB pin voltage is regulated at the valley, the increased ripple on the VFB pin causes the increase of the VFB DC value. The AC ripple coupled to the VFB pin has two components, one coupled from SW node and the other coupled from the VOUT pin and they can be calculated using Equation 12 and Equation 13 when neglecting the output voltage ripple caused by equivalent series inductance (ESL).

\[
V_{\text{INJ}_\text{SW}} = \frac{V_{\text{IN}} - V_{\text{OUT}}}{R7 \times C1} \times \frac{D}{f_{\text{SW}}} + \frac{I_{\text{IND}(\text{ripple})}}{8 \times C_{\text{OUT}} \times f_{\text{SW}}}
\]

(12)

\[
V_{\text{INJ}_\text{OUT}} = ESR \times I_{\text{IND}(\text{ripple})} + \frac{I_{\text{IND}(\text{ripple})}}{8 \times C_{\text{OUT}} \times f_{\text{SW}}}
\]

(13)

It is recommended that V_{\text{INJ}_\text{SW}} to be less than 50 mV. If the calculated V_{\text{INJ}_\text{SW}} is higher than 50 mV, then other parameters need to be adjusted to reduce it. For example, C_{\text{OUT}} can be increased to satisfy Equation 11 with a higher R7 value, thereby reducing V_{\text{INJ}_\text{SW}}.

The DC voltage at the VFB pin can be calculated by Equation 14:

\[
V_{\text{VFB}} = 0.6 + \frac{V_{\text{INJ}_\text{SW}} + V_{\text{INJ}_\text{OUT}}}{2}
\]

(14)

And the resistor divider value can be determined by Equation 15:

\[
R1 = \frac{V_{\text{OUT}} - V_{\text{VFB}}}{V_{\text{VFB}}} \times R2
\]

(15)

8.2.1.3 Application Curves

![Figure 39. Enable Turn-on](image1)

![Figure 40. Enable Turn-off](image2)
TPS53355EVM
Over Current Protection
Test Condition: 12 Vin OCP
Ch1: 1.5 Vout
Ch2: LL
Ch3: PGOOD

TPS53355EVM
Short Circuit Protection
Ch1: 1.5 Vout
Ch2: LL
Ch3: PGOOD
Test condition: 12 Vin, 1.5 V Short Circuit

TPS5335EVM
Output Transient from 0 A to 15 A
FCCM Mode
Test Condition: 12 Vin, 1.5 V/0 A-15 A

TPS5335EVM
Output Transient from DCM to CCM
Test Condition: 12 Vin, 1.5 V/0 A-15 A

TPS5335EVM
Output Transient from CCM to DCM
Test Condition: 12 Vin, 1.5 V/0 A-15 A

TPS5335EVM
0.75 V Pre-bias Enable Start up
CH1: EN
CH2: 1.5 Vout
CH3: PGOOD
Test condition: 12 Vin, 1.5 V/0 A

TPS5335EVM
Output Transient from DCM to CCM
Test condition: 12 Vin, 0 A - 15 A

TPS5335EVM
Output Transient from CCM to DCM
Test condition: 12 Vin, 0 A - 15 A

Figure 41. Output Transient From DCM to CCM
Figure 42. Output Transient From CCM to DCM
Figure 43. Output Transient With FCCM Mode
Figure 44. Output 0.75-V Prebias Turn-on
Figure 45. Output Overcurrent Protection
Figure 46. Output Short Circuit Protection
8.2.2 Typical Application Circuit

![Typical Application Circuit Diagram](image)

Figure 47. Typical Application Circuit Diagram

### 8.2.2.1 Design Requirements

#### Table 5. Design Parameters

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITION</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
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<tr>
<td>INPUT CHARACTERISTICS</td>
<td></td>
<td></td>
<td></td>
<td></td>
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<tr>
<td>$V_{IN}$</td>
<td>Voltage range</td>
<td>8</td>
<td>12</td>
<td>14</td>
<td>V</td>
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<tr>
<td>$I_{MAX}$</td>
<td>Maximum input current $V_{IN} = 8,V$, $I_{OUT} = 30,A$</td>
<td>6.3</td>
<td></td>
<td></td>
<td>A</td>
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<tr>
<td></td>
<td>No load input current $V_{IN} = 14,V$, $I_{OUT} = 0,A$ with auto-skip mode</td>
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<td></td>
<td></td>
<td>mA</td>
</tr>
<tr>
<td>OUTPUT CHARACTERISTICS</td>
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<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$V_{OUT}$</td>
<td>Output voltage</td>
<td>1.5</td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td></td>
<td>Output voltage regulation</td>
<td></td>
<td>0.1%</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Line regulation, $8,V \leq V_{IN} \leq 15,V$</td>
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<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Load regulation, $V_{IN} = 12,V$, $0,A \leq I_{OUT} \leq 30,A$ with FCCM</td>
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<td>0.2%</td>
<td></td>
<td></td>
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<tr>
<td>$V_{RIPPLE}$</td>
<td>Output voltage ripple $V_{IN} = 12,V$, $I_{OUT} = 30,A$ with FCCM</td>
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<td></td>
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<td>$I_{LOAD}$</td>
<td>Output load current</td>
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<td>$I_{OCP}$</td>
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<td>$t_{SS}$</td>
<td>Soft-start time</td>
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<td></td>
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<tr>
<td>$f_{SW}$</td>
<td>Switching frequency</td>
<td>500</td>
<td></td>
<td></td>
<td>kHz</td>
</tr>
<tr>
<td>$\eta$</td>
<td>Peak efficiency $V_{IN} = 12,V$, $V_{OUT} = 1.1,V$, $I_{OUT} = 10,A$</td>
<td>91.87%</td>
<td></td>
<td></td>
<td></td>
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<tr>
<td></td>
<td>Full load efficiency $V_{IN} = 12,V$, $V_{OUT} = 1.1,V$, $I_{OUT} = 30,A$</td>
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<td>$T_{A}$</td>
<td>Operating temperature</td>
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<td></td>
<td></td>
<td>°C</td>
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</tbody>
</table>
8.2.2.2 Detailed Design Procedure

8.2.2.2.1 External Component Selection

Refer to External Component Selection Using All Ceramic Output Capacitors for guidelines for this design with all ceramic output capacitors.

The external components selection is a simple process when using organic semiconductors or special polymer output capacitors.

1. Select operation mode and soft-start time

   Select operation mode and soft-start time using Table 3.

2. Select switching frequency

   Select the switching frequency from 250 kHz to 1 MHz using Table 1.

3. Choose the inductor

   The inductance value should be determined to give the ripple current of approximately 1/4 to 1/2 of maximum output current. Larger ripple current increases output ripple voltage and improves signal-to-noise ratio and helps ensure stable operation, but increases inductor core loss. Using 1/3 ripple current to maximum output current ratio, the inductance can be determined by Equation 16.

\[
L = \frac{1}{L_{\text{IND(ripple)}} \times f_{SW}} \times \frac{(V_{\text{IN(max)}} - V_{\text{OUT}}) \times V_{\text{OUT}}}{V_{\text{IN(max)}}} = \frac{3}{L_{\text{OUT(max)}} \times f_{SW}} \times \frac{(V_{\text{IN(max)}} - V_{\text{OUT}}) \times V_{\text{OUT}}}{V_{\text{IN(max)}}}
\]  

Equation 16

The inductor requires a low DCR to achieve good efficiency. It also requires enough room above peak inductor current before saturation. The peak inductor current can be estimated in Equation 9.

\[
I_{\text{IND(peak)}} = \frac{32 \times V_{\text{TRIP}}}{R_{\text{DS(on)}}} + \frac{1}{L \times f_{SW}} \times \frac{(V_{\text{IN(max)}} - V_{\text{OUT}}) \times V_{\text{OUT}}}{V_{\text{IN(max)}}}
\]  

Equation 17

4. Choose the output capacitors

   When organic semiconductor capacitor(s) or specialty polymer capacitor(s) are used, for loop stability, capacitance and ESR should satisfy Equation 7. For jitter performance, Equation 18 is a good starting point to determine ESR.

\[
\text{ESR} = \frac{V_{\text{OUT}} \times 10 \text{ mV} \times (1 - D)}{0.6 \text{ V} \times L_{\text{IND(ripple)}}} = \frac{10 \text{ mV} \times L \times f_{SW}}{0.6 \text{ V}} = \frac{L \times f_{SW}}{60} (\Omega)
\]  

where

- D is the duty factor.
- The required output ripple slope is approximately 10 mV per t_{SW} (switching period) in terms of VFB terminal voltage.
5. **Determine the value of R1 and R2**

The output voltage is programmed by the voltage-divider resistor, R1 and R2 shown in Figure 37. R1 is connected between VFB pin and the output, and R2 is connected between the VFB pin and GND. Recommended R2 value is from 1 kΩ to 20 kΩ. Determine R1 using Equation 19.

\[
R1 = \frac{V_{OUT} \times I_{ND(ripple)} \times ESR}{2 \times 0.6} - 0.6 \times R2
\]  

(19)

6. **Choose the overcurrent setting resistor**

The overcurrent setting resistor, \(R_{TRIP}\), can be determined by Equation 10.

\[
R_{TRIP}(\Omega) = \frac{\left(\frac{1}{2 \times L \times f_{SW}} \times \left(\frac{V_{IN} - V_{OUT}}{V_{IN}}\right) \times V_{OUT}\right) \times 32 \times R_{DS(on)} (\Omega)}{I_{TRIP} (\mu A)}
\]

where

- \(I_{TRIP}\) is the TRIP pin sourcing current (10 µA)
- \(R_{DS(on)}\) is the thermally compensated on-time resistance value of the low-side MOSFET  

(20)

Use an \(R_{DS(on)}\) value of 1.5 mΩ for an overcurrent level of approximately 30 A. Use an \(R_{DS(on)}\) value of 1.7 mΩ for overcurrent level of approximately 10 A.

### 8.2.2.3 Application Curves

![Figure 48. Enable Turn-on](image1)

![Figure 49. Enable Turn-off](image2)
9 Power Supply Recommendations
The device is designed to operate from an input voltage supply range between 1.5 V and 22 V (4.5-V to 25-V biased). This input supply must be well regulated. Proper bypassing of input supplies and internal regulators is also critical for noise performance, as is PCB layout and grounding scheme. See the recommendations in Layout.

10 Layout

10.1 Layout Guidelines
Certain points must be considered before starting a layout work using the TPS53355.

• The power components (including input/output capacitors, inductor and TPS53355) must be placed on one side of the PCB (solder side). At least one inner plane should be inserted, connected to ground, in order to shield and isolate the small signal traces from noisy power lines.

• All sensitive analog traces and components such as VFB, PGOOD, TRIP, MODE and RF should be placed away from high-voltage switching nodes such as LL, VBST to avoid coupling. Use internal layer(s) as ground plane(s) and shield feedback trace from power traces and components.

• Place the VIN decoupling capacitors as close to the VIN and PGND pins as possible to minimize the input AC current loop.

• Because the TPS53355 controls output voltage referring to voltage across VOUT capacitor, the top-side resistor of the voltage divider should be connected to the positive node of the VOUT capacitor. Connect the GND of the bottom side resistor to the GND pad of the device. The trace from these resistors to the VFB pin should be short and thin.

• Place the frequency setting resistor (RF), OCP setting resistor (RTRIP) and mode setting resistor (RMODE) as close to the device as possible. Use the common GND via to connect them to GND plane if applicable.

• Place the VDD and VREG decoupling capacitors as close as possible to the device. Make sure GND vias are provided for each decoupling capacitor and make the loop as small as possible.

• The PCB trace defined as switch node, which connects the LL pins and high-voltage side of the inductor, should be as short and wide as possible.

• Connect the ripple injection VOUT signal (VOUT side of the C1 capacitor in Figure 38) from the terminal of ceramic output capacitor. The AC coupling capacitor (C2 in Figure 38) should be placed near the device, and R7 and C1 can be placed near the power stage.

• Use separate vias or trace to connect LL node to snubber, boot strap capacitor and ripple injection resistor. Do not combine these connections.
10.2 Layout Example

Figure 50. Layout Recommendation
11 Device and Documentation Support

11.1 Device Support

11.1.1 Development Support

11.1.1.1 Custom Design With WEBENCH® Tools

Click here to create a custom design using TPS53355 device with the WEBENCH® Power Designer.

1. Start by entering the input voltage \( V_{\text{IN}} \), output voltage \( V_{\text{OUT}} \), and output current \( I_{\text{OUT}} \) requirements.
2. Optimize the design for key parameters such as efficiency, footprint, and cost using the optimizer dial.
3. Compare the generated design with other possible solutions from Texas Instruments.

The WEBENCH Power Designer provides a customized schematic along with a list of materials with real-time pricing and component availability.

In most cases, these actions are available:

- Run electrical simulations to see important waveforms and circuit performance
- Run thermal simulations to understand board thermal performance
- Export customized schematic and layout into popular CAD formats
- Print PDF reports for the design, and share the design with colleagues

Get more information about WEBENCH tools at www.ti.com/WEBENCH.

11.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on Alert me to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI’s views; see TI’s Terms of Use.

**TI E2E™ Online Community** **TI's Engineer-to-Engineer (E2E) Community.** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

**Design Support** **TI's Design Support** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.4 Trademarks

Eco-mode, NexFET, PowerPAD, SWIFT, D-CAP, E2E are trademarks of Texas Instruments. WEBENCH is a registered trademark of Texas Instruments. All other trademarks are the property of their respective owners.

11.5 Electrostatic Discharge Caution

*These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.*

11.6 Glossary

**SLYZ022 — Ti Glossary.**

This glossary lists and explains terms, acronyms, and definitions.
12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.
### PACKAGING INFORMATION

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<th>Orderable Device</th>
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<th>Package Type</th>
<th>Package Drawing</th>
<th>Pins</th>
<th>Package Qty</th>
<th>Eco Plan</th>
<th>Lead/Ball Finish</th>
<th>MSL Peak Temp</th>
<th>Op Temp (°C)</th>
<th>Device Marking</th>
<th>Samples</th>
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<td>ACTIVE</td>
<td>LSON-CLIP</td>
<td>DQP</td>
<td>22</td>
<td>2500</td>
<td>Pb-Free</td>
<td>CU NIPDAU</td>
<td>Level-2-260C-1 YEAR</td>
<td>-40 to 85</td>
<td>53355DQP</td>
<td></td>
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<td>TPS33355DQPR</td>
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<td>LSON-CLIP</td>
<td>DQP</td>
<td>22</td>
<td>2500</td>
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<td>CU NIPDAU</td>
<td>CU SN</td>
<td>Level-2-260C-1 YEAR</td>
<td>-40 to 85</td>
<td>53355DQP</td>
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<td>CU SN</td>
<td>Level-2-260C-1 YEAR</td>
<td>-40 to 85</td>
<td>53355DQP</td>
</tr>
</tbody>
</table>

(1) The marketing status values are defined as follows:
- **ACTIVE**: Product device recommended for new designs.
- **LIFEBUY**: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
- **NRND**: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
- **PREVIEW**: Device has been announced but is not in production. Samples may or may not be available.
- **OBSOLETE**: TI has discontinued the production of the device.

(2) **RoHS**: TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substances do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
- **RoHS Exempt**: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
- **Green**: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) **MSL, Peak Temp.** - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) **Lead/Ball Finish** - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.
TAPE AND REEL INFORMATION

**Device** | **Package Type** | **Package Drawing** | **Pins** | **SPQ** | **Reel Diameter (mm)** | **Reel Width W1 (mm)** | **A0 (mm)** | **B0 (mm)** | **K0 (mm)** | **P1 (mm)** | **W (mm)** | **Pin1 Quadrant**
--- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | ---
TPS53355DQPR | LSON-CLIP | DQP | 22 | 2500 | 330.0 | 15.4 | 5.3 | 6.3 | 1.8 | 8.0 | 12.0 | Q1
TPS53355DQPT | LSON-CLIP | DQP | 22 | 250 | 330.0 | 15.4 | 5.3 | 6.3 | 1.8 | 8.0 | 12.0 | Q1

*All dimensions are nominal.*

A0: Dimension designed to accommodate the component width
B0: Dimension designed to accommodate the component length
K0: Dimension designed to accommodate the component thickness
W: Overall width of the carrier tape
P1: Pitch between successive cavity centers
## TAPE AND REEL BOX DIMENSIONS

*All dimensions are nominal

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<thead>
<tr>
<th>Device</th>
<th>Package Type</th>
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<th>SPQ</th>
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<th>Width (mm)</th>
<th>Height (mm)</th>
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</tbody>
</table>
NOTES:

A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
B. This drawing is subject to change without notice.
C. Small Outline No-Lead (SON) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.

⚠️ Pin 1 identifiers are located on both top and bottom of the package and within the zone indicated. The Pin 1 identifiers are either a molded, marked, or metal feature.
THERMAL PAD MECHANICAL DATA

DQP (R-PSON-N22) PLASTIC SMALL OUTLINE NO-LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.

![Exposed Thermal Pad Dimensions Diagram]

NOTE: All linear dimensions are in millimeters
NOTES:  
A. All linear dimensions are in millimeters.  
B. This drawing is subject to change without notice.  
C. Publication IPC-7351 is recommended for alternate designs.  
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com (http://www.ti.com).  
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.  
F. Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for vias placed in the thermal pad.
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