TPS54202H 4.5-V to 28-V Input, 2-A Output, SWIFT™ Synchronous Step Down Voltage Converter

1 Features

• 4.5-V to 28-V Wide Input voltage Range
• Integrated 148-mΩ and 78-mΩ MOSFETs for 2-A, Continuous Output Current
• Low 2-μA Shutdown, 45-μA Quiescent Current
• Internal 5-mS Soft-Start
• Fixed 500-kHz Switching Frequency
• Advanced Eco-mode™ Pulse Skip
• Peak Current Mode Control
• Internal Loop compensation
• Overcurrent Protection for Both MOSFETs with Hiccup Mode Protection
• Over Voltage Protection
• Thermal Shutdown
• SOT-23 (6) Package

2 Applications

• 12-V, 24-V Distributed Power-Bus Supply
• Industry Application
  – White Goods
• Consumer Application
  – Audio
  – STB, DTV
  – Printer

3 Description

The TPS54202H is a 4.5-V to 28-V input voltage range, 2-A synchronous buck converter. The device includes two integrated switching FETs, internal loop compensation and 5-ms internal soft start to reduce component count.

By integrating the MOSFETs and employing the SOT-23 package, the TPS54202H achieves the high power density and offers a small footprint on the PCB.

Advanced Eco-mode implementation maximizes the light load efficiency and reduces the power loss.

Cycle-by-cycle current limit in both high-side MOSFET protects the converter in an overload condition and is enhanced by a low-side MOSFET freewheeling current limit which prevents current runaway. Hiccup mode protection is triggered if the overcurrent condition has persisted for longer than the present time.

Device Information

<table>
<thead>
<tr>
<th>PART NUMBER</th>
<th>PACKAGE</th>
<th>BODY SIZE (NOM)</th>
</tr>
</thead>
<tbody>
<tr>
<td>TPS54202H</td>
<td>SOT-23(6)</td>
<td>1.60 mm × 2.90 mm</td>
</tr>
</tbody>
</table>

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Simplified Schematic

Efficiency vs Output Current

An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.
4 Revision History

<table>
<thead>
<tr>
<th>DATE</th>
<th>REVISION</th>
<th>NOTES</th>
</tr>
</thead>
<tbody>
<tr>
<td>April 2016</td>
<td>*</td>
<td>Initial release.</td>
</tr>
</tbody>
</table>
## 5 Pin Configuration and Functions

**DDC Package**
6-Pin SOT-23
Top View

<table>
<thead>
<tr>
<th>Pin</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>BOOT</td>
<td>Supply input for the high-side NFET gate drive circuit. Connect a 0.1-μF capacitor between BOOT and SW pins.</td>
</tr>
<tr>
<td>EN</td>
<td>This pin is the enable pin. Float the EN pin to disable.</td>
</tr>
<tr>
<td>FB</td>
<td>Converter feedback input. Connect to output voltage with feedback resistor divider.</td>
</tr>
<tr>
<td>GND</td>
<td>Ground pin. Source terminal of low-side power NFET as well as the ground terminal for controller circuit. Connect sensitive VFB to this GND at a single point.</td>
</tr>
<tr>
<td>SW</td>
<td>Switch node connection between high-side NFET and low-side NFET.</td>
</tr>
<tr>
<td>VIN</td>
<td>Input voltage supply pin. The drain terminal of high-side power NFET.</td>
</tr>
</tbody>
</table>

---

(1) **O** = Output; **I** = Input
6 Specifications

6.1 Absolute Maximum Ratings
over operating free-air temperature range (unless otherwise noted)\(^1\)

<table>
<thead>
<tr>
<th>Description</th>
<th>MIN</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>Input voltage range, (V_i)</td>
<td>VIN</td>
<td>–0.3</td>
<td>30</td>
</tr>
<tr>
<td></td>
<td>EN</td>
<td>–0.3</td>
<td>7</td>
</tr>
<tr>
<td></td>
<td>FB</td>
<td>–0.3</td>
<td>7</td>
</tr>
<tr>
<td>Output voltage range, (V_o)</td>
<td>BOOT-SW</td>
<td>–0.3</td>
<td>7</td>
</tr>
<tr>
<td></td>
<td>SW</td>
<td>–0.3</td>
<td>30</td>
</tr>
<tr>
<td></td>
<td>SW (20 ns transient)</td>
<td>–5</td>
<td>30</td>
</tr>
<tr>
<td>Operating junction temperature, (T_J)</td>
<td>–40</td>
<td>150</td>
<td>°C</td>
</tr>
<tr>
<td>Storage temperature range, (T_{stg})</td>
<td>–65</td>
<td>150</td>
<td>°C</td>
</tr>
</tbody>
</table>

\(^1\) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

<table>
<thead>
<tr>
<th>Description</th>
<th>VALUE</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(^1)</td>
<td>±4000</td>
<td>V</td>
</tr>
<tr>
<td>Charged-device model (CDM), per JEDEC specification JESD22-C101(^2)</td>
<td>±1500</td>
<td>V</td>
</tr>
</tbody>
</table>

\(^1\) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

\(^2\) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions
over operating free-air temperature range (unless otherwise noted)

<table>
<thead>
<tr>
<th>Description</th>
<th>MIN</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>(V_i)</td>
<td>4.5</td>
<td>28</td>
<td>V</td>
</tr>
<tr>
<td>EN</td>
<td>–0.1</td>
<td>7</td>
<td>V</td>
</tr>
<tr>
<td>FB</td>
<td>–0.1</td>
<td>7</td>
<td>V</td>
</tr>
<tr>
<td>(V_o)</td>
<td>–0.1</td>
<td>7</td>
<td>V</td>
</tr>
<tr>
<td>SW</td>
<td>–0.1</td>
<td>28</td>
<td>V</td>
</tr>
<tr>
<td>Operating junction temperature, (T_J)</td>
<td>–40</td>
<td>125</td>
<td>°C</td>
</tr>
</tbody>
</table>

6.4 Thermal Information

<table>
<thead>
<tr>
<th>THERMAL METRIC(^1)</th>
<th>TPS54202H DDC (SOT23)</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>(R_{UA}) Junction-to-ambient thermal resistance</td>
<td>89.2</td>
<td>°C/W</td>
</tr>
<tr>
<td>(R_{UJC(top)}) Junction-to-case (top) thermal resistance</td>
<td>39.5</td>
<td>°C/W</td>
</tr>
<tr>
<td>(R_{UB}) Junction-to-board thermal resistance</td>
<td>14.7</td>
<td>°C/W</td>
</tr>
<tr>
<td>(\psi_{JT}) Junction-to-top characterization parameter</td>
<td>1.2</td>
<td>°C/W</td>
</tr>
<tr>
<td>(\psi_{JB}) Junction-to-board characterization parameter</td>
<td>14.7</td>
<td>°C/W</td>
</tr>
</tbody>
</table>

\(^1\) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report, SPRA953.
6.5 Electrical Characteristics

The electrical ratings specified in this section apply to all specifications in this document, unless otherwise noted. These specifications are interpreted as conditions that do not degrade the device parametric or functional specifications for the life of the product containing it. \( T_J = -40^\circ C \) to \( +125^\circ C \), \( V_{IN} = 4.5 \) V to 28 V, (unless otherwise noted).

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>INPUT SUPPLY</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>( V_{IN} )</td>
<td>Input voltage range</td>
<td>4.5</td>
<td>28</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>( I_Q )</td>
<td>Non switching quiescent current</td>
<td>EN =5 V, VFB = 1 V</td>
<td>45</td>
<td>( \mu A )</td>
<td></td>
</tr>
<tr>
<td>( I_{OFF} )</td>
<td>Shut down current</td>
<td>EN = GND</td>
<td>2</td>
<td>( \mu A )</td>
<td></td>
</tr>
<tr>
<td>( V_{IN(UVLO)} )</td>
<td>VIN under voltage lockout</td>
<td>Rising ( V_{IN} )</td>
<td>3.9</td>
<td>4.2</td>
<td>4.4</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Falling ( V_{IN} )</td>
<td>3.4</td>
<td>3.7</td>
<td>3.9</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Hysteresis</td>
<td>400</td>
<td>480</td>
<td>560</td>
</tr>
<tr>
<td>ENABLE (EN PIN)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>( V_{EN(RISING)} )</td>
<td>Enable threshold</td>
<td>Rising</td>
<td>1.28</td>
<td>1.35</td>
<td>V</td>
</tr>
<tr>
<td>( V_{EN(FALLING)} )</td>
<td>Hysteresis current</td>
<td>( V_{EN} = 1.5 ) V</td>
<td>1.16</td>
<td>1.25</td>
<td>V</td>
</tr>
<tr>
<td>( I_{EN,HYS} )</td>
<td>Hysteresis current</td>
<td>( V_{EN} = 1.5 ) V</td>
<td>1</td>
<td>( \mu A )</td>
<td></td>
</tr>
<tr>
<td>FEEDBACK AND ERROR AMPLIFIER</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>( V_{FB} )</td>
<td>Feedback Voltage</td>
<td>( V_{IN} = 12 ) V</td>
<td>0.581</td>
<td>0.596</td>
<td>0.611</td>
</tr>
<tr>
<td>PULSE SKIP MODE</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>( I_{(SKIP)}^{(1)} )</td>
<td>Pulse skip mode peak inductor current threshold</td>
<td>( V_{IN} = 24 ) V, ( V_{OUT} = 5 ) V, ( L = 15 \mu H )</td>
<td>300</td>
<td>mA</td>
<td></td>
</tr>
<tr>
<td>POWER STAGE</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>( R_{(HSD)} )</td>
<td>High-side FET on resistance</td>
<td>( T_A = 25^\circ C ), ( V_{BST} - SW = 6 ) V</td>
<td>148</td>
<td>m( \Omega )</td>
<td></td>
</tr>
<tr>
<td>( R_{(LSD)} )</td>
<td>Low-side FET on resistance</td>
<td>( T_A = 25^\circ C ), ( V_{IN} = 12 )</td>
<td>78</td>
<td>m( \Omega )</td>
<td></td>
</tr>
<tr>
<td>CURRENT LIMIT</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>( I_{LIM,HS} )</td>
<td>High side current limit</td>
<td>Inductor peak current</td>
<td>2.5</td>
<td>3.2</td>
<td>3.9</td>
</tr>
<tr>
<td>( I_{LIM,LS} )</td>
<td>Low side source current limit</td>
<td>Inductor valley current</td>
<td>2</td>
<td>3</td>
<td>4</td>
</tr>
<tr>
<td>OSCILLATOR</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>( F_{sw} )</td>
<td>Centre switching frequency</td>
<td></td>
<td>390</td>
<td>500</td>
<td>590</td>
</tr>
<tr>
<td>OVER TEMPERATURE PROTECTION</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Thermal Shutdown( ^{(1)} )</td>
<td>Rising temperature</td>
<td></td>
<td>155</td>
<td>( ^\circ C )</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Hysteresis</td>
<td></td>
<td>10</td>
<td>( ^\circ C )</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Hiccup time</td>
<td></td>
<td>32768</td>
<td>Cycles</td>
<td></td>
</tr>
</tbody>
</table>

(1) Not production tested

6.6 Timing Requirements

<table>
<thead>
<tr>
<th>OVER CURRENT PROTECTION</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>( t_{HIC_WAIT} )</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>( t_{HIC_RESTART} )</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>( t_{SS} )</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>( I_{MIN_ON}^{(1)} )</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

ON TIME CONTROL

<table>
<thead>
<tr>
<th>OVER CURRENT PROTECTION</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>( t_{HIC_WAIT} )</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>( t_{HIC_RESTART} )</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>( t_{SS} )</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>( I_{MIN_ON}^{(1)} )</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

(1) Not production tested
6.7 Typical Characteristics

\( V_{IN} = 12 \), unless otherwise specified

---

![Figure 1. Shutdown Quiescent Current vs Junction Temperature](image1)

![Figure 2. Non-Switching Operating Quiescent Current vs Junction Temperature](image2)

![Figure 3. High-Side Resistance vs Junction Temperature](image3)

![Figure 4. Low-Side FET On Resistance vs Junction Temperature](image4)

![Figure 5. Reference Voltage vs Junction Temperature](image5)

![Figure 6. Centre Switching Frequency vs Junction Temperature](image6)
Typical Characteristics (continued)

Figure 7. High-Side Current Limit Threshold vs Junction Temperature

Figure 8. Low-Side Current Limit Threshold vs Junction Temperature

Figure 9. BOOT-SW UVLO Threshold vs Junction Temperature

Figure 10. VIN UVLO Threshold vs Junction Temperature

Figure 11. EN UVLO Threshold vs Junction Temperature

Figure 12. EN Hysteresis Current vs Junction Temperature
7 Detailed Description

7.1 Overview

The device is a 28-V, 2-A, synchronous step-down (buck) converter with two integrated n-channel MOSFETs. To improve performance during line and load transients the device implements a constant-frequency, peak current mode control which reduces output capacitance. The optimized internal compensation network minimizes the external component counts and simplifies the control loop design.

The TPS54202H's switching frequency is fixed to 500 kHz.

The TPS54202H starts switching at VIN equal to 4.5 V. The operating current is 45 μA typically when not switching and under no load. When the device is disabled, the supply current is 2 μA typically.

The integrated 148-mΩ high-side MOSFET and 78-mΩ allow for high efficiency power supply designs with continuous output currents up to 2 A.

The TPS54202H reduces the external component count by integrating the boot recharge diode. The bias voltage for the integrated high-side MOSFET is supplied by an external capacitor on the BOOT to PH pins. The boot capacitor voltage is monitored by an UVLO circuit and will turn the high-side MOSFET off when the voltage falls below a preset threshold of 2.1 V typically.

The device minimizes excessive output overvoltage transients by taking advantage of the overvoltage comparator. When the regulated output voltage is greater than 108% of the nominal voltage, the overvoltage comparator is activated, and the high-side MOSFET is turned off and masked from turning on until the output voltage is lower than 104%.

The TPS54202H device has internal 5-ms soft-start time to minimize inrush currents.

7.2 Functional Block Diagram
7.3 Feature Description

7.3.1 Fixed-Frequency PWM Control

The device uses a fixed-frequency, peak current-mode control. The output voltage is compared through external resistors on the FB pin to an internal voltage reference by an error amplifier. An internal oscillator initiates the turn on of the high-side power switch. The error amplifier output is compared to the current of the high-side power switch. When the power-switch current reaches the error amplifier output voltage level, the high side power switch is turned off and the low-side power switch is turned on. The error amplifier output voltage increases and decreases as the output current increases and decreases. The device implements a current-limit by clamping the error amplifier voltage to a maximum level and also implements a minimum clamp for improved transient-response performance.

7.3.2 Pulse Skip Mode

The TPS54202H is designed to operate in pulse skipping mode at light load currents to boost light load efficiency. When the peak inductor current is lower than 300 mA typically, the device enters pulse skipping mode. When the device is in pulse skipping mode, the error amplifier output voltage is clamped which prevents the high side integrated MOSFET from switching. The peak inductor current must rise above 300 mA and exit pulse skip mode. Since the integrated current comparator catches the peak inductor current only, the average load current entering pulse skipping mode varies with the applications and external output filters.

7.3.3 Error Amplifier

The device has a trans-conductance amplifier as the error amplifier. The error amplifier compares the FB voltage to the lower of the internal soft-start voltage or the internal 0.596-V voltage reference. The transconductance of the error amplifier is 240 µA/V typically. The frequency compensation components are placed internal between the output of the error amplifier and ground.

7.3.4 Slope Compensation and Output Current

The device adds a compensating ramp to the signal of the switch current. This slope compensation prevents sub-harmonic oscillations as the duty cycle increases. The available peak inductor current remains constant over the full duty-cycle range.

7.3.5 Device Enable

The EN pin provides electrical on and off control of the device. When the EN pin voltage exceeds the threshold voltage, the device begins operation. If the EN pin voltage is pulled below the threshold voltage, the regulator stops switching and enters the low-quiescent (IQ) state.

The EN pin has an internal pull down resistance Rpd (typical 1 MΩ) which allows the user to float the EN pin to disable the device, a Zener diode (typical break down voltage 6.9 V) is used to clamp the EN input voltage. To enable the device, connect a pull up resistor R4 (typical 510 KΩ) between EN and VIN, R4 is used to limit the quiet scent current of the device for light load efficiency improvement.
Feature Description (continued)

![Figure 13. Adjustable VIN Undervoltage Lockout](image)

7.3.6 Adjusting Under Voltage Lockout

The device implements internal under voltage-lockout (UVLO) circuitry on the VIN pin. The device is disabled when the VIN pin voltage falls below the internal VIN UVLO threshold. The internal VIN UVLO threshold has a hysteresis of 480 mV. To enable the device, connect a pull-up resistor R4 (typical 510 KΩ to limit the quiescent current) to the VIN pin.

If an application requires a higher UVLO threshold on the VIN pin, then the EN pin can be configured as shown in Figure 13. When using the external UVLO function, setting the hysteresis at a value greater than 500 mV is recommended.

The EN pin has a pull-down resistance Rpd (typical 1 MΩ), which sets the default state of the pin to disable when no external components are connected. Use Equation 1 and Equation 2 to calculate the values of R4 and R5 for a specified UVLO threshold.

\[
R4 = \frac{V_{ENfalling} \times V_{START} - V_{STOP}}{I_h} \quad (1)
\]

\[
R5 = \frac{R4 \times Rpd}{\left(\frac{V_{START}}{V_{ENrising}} - 1\right) \times Rpd - R4} \quad (2)
\]

Where:

- \(I_h = 1 \mu A\)
- \(V_{ENrising} = 1.28 \text{ V}\)
- \(V_{ENfalling} = 1.25 \text{ V}\)

7.3.7 Safe Startup into Pre-Biased Outputs

The device has been designed to prevent the low-side MOSFET from discharging a pre-biased output. During monotonic pre-biased startup, both high-side and low-side MOSFETs are not allowed to be turned on until the internal soft-start voltage is higher than FB pin voltage.

7.3.8 Voltage Reference

The voltage reference system produces a precise ±2.5% voltage-reference over temperature by scaling the output of a temperature stable bandgap circuit. The typical voltage reference is designed at 0.596 V.
Feature Description (continued)

7.3.9 Adjusting Output Voltage
The output voltage is set with a resistor divider from the output node to the FB pin. It is recommended to use divider resistors with 1% tolerance or better. Start with a 100 kΩ for the upper resistor divider, use Equation 3 to calculate the output voltage. To improve efficiency at light loads consider using larger value resistors. If the values are too high the regulator is more susceptible to noise and voltage errors from the FB input current are noticeable.

\[ V_{\text{out}} = V_{\text{ref}} \times \left( \frac{R2}{R3} + 1 \right) \]  
(3)

7.3.10 Internal Soft-Start
The TPS54202H device uses the internal soft-start function. The internal soft start time is set to 5 ms typically.

7.3.11 Bootstrap Voltage (BOOT)
The TPS54202H has an integrated boot regulator and requires a 0.1-µF ceramic capacitor between the BOOT and SW pins to provide the gate drive voltage for the high-side MOSFET. A ceramic capacitor with an X7R or X5R grade dielectric is recommended because of the stable characteristics over temperature and voltage. To improve drop out, the TPS54202H is designed to operate at 100% duty cycle as long as the BOOT to SW pin voltage is greater than 2.1 V typically.

7.3.12 Overcurrent Protection
The device is protected from overcurrent conditions by cycle-by-cycle current limiting on both the high-side MOSFET and the low-side MOSFET.

7.3.12.1 High-Side MOSFET Overcurrent Protection
The device implements current mode control which uses the internal COMP voltage to control the turn off of the high-side MOSFET and the turn on of the low-side MOSFET on a cycle-by-cycle basis. During each cycle, the switch current and the current reference generated by the internal COMP voltage are compared. When the peak switch current intersects the current reference the high-side switch turns off.

7.3.12.2 Low-Side MOSFET Overcurrent Protection
While the low-side MOSFET is turned on, the conduction current is monitored by the internal circuitry. During normal operation the low-side MOSFET sources current to the load. At the end of every clock cycle, the low-side MOSFET sourcing current is compared to the internally set low-side sourcing current-limit. If the low-side sourcing current-limit is exceeded, the high-side MOSFET does not turn on and the low-side MOSFET stays on for the next cycle. The high-side MOSFET turns on again when the low-side current is below the low-side sourcing current-limit at the start of a cycle which is the inductor current valley value.

Furthermore, if an output overload condition occurs for more than the hiccup wait time, which is programmed for 512 switching cycles, the device shuts down and restarts after the hiccup time of 16384 cycles. The hiccup mode helps to reduce the device power dissipation under severe overcurrent conditions.

7.3.13 Output Overvoltage Protection (OVP)
The TPS54202H incorporates an overvoltage transient protection (OVTP) circuit to minimize output voltage overshoot when recovering from output fault conditions or strong unload transients. The OVTP circuit includes an overvoltage comparator to compare the FB pin voltage and internal thresholds. When the FB pin voltage goes above 108% × Vref, the high-side MOSFET will be forced off. When the FB pin voltage falls below 104% × Vref, the high-side MOSFET will be enabled again.

7.3.14 Thermal Shutdown
The internal thermal-shutdown circuitry forces the device to stop switching if the junction temperature exceeds 155°C typically. When the junction temperature drops below 145°C typically, the internal thermal-hiccup timer begins to count. The device initiates the power-up sequence after the built-in thermal-shutdown hiccup time (32768 cycles) is over.
7.4 Device Functional Modes

7.4.1 Normal Operation
When the input voltage is above the UVLO threshold, the TPS54202H can operate in their normal switching modes. Normal continuous conduction mode (CCM) occurs when inductor peak current is above 0 A. In CCM, the TPS54202H operates at a fixed frequency.

7.4.2 Eco-mode™ Operation
The devices are designed to operate in high-efficiency pulse-skipping mode under light load conditions. Pulse skipping initiates when the switch current falls to 0 A. During pulse skipping, the low-side FET turns off when the switch current falls to 0 A. The switching node (the SW pin) waveform takes on the characteristics of discontinuous conduction mode (DCM) operation and the apparent switching frequency decreases. As the output current decreases, the perceived time between switching pulses increases.
8 Application and Implementation

NOTE
Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information
The TPS54202H are typically used as a step down converter, which convert an input voltage from 8 V - 28 V to fixed output voltage 5 V.

8.2 Typical Application

8.2.1 TPS54202H 8-V to 28-V Input, 5-V Output Converter

Figure 14. 5-V, 2-A Reference Design

8.2.2 Design Requirements
For this design example, use the parameters in Table 1.

Table 1. Design Parameters

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>VALUE</th>
</tr>
</thead>
<tbody>
<tr>
<td>Input voltage range</td>
<td>8 V to 28 V</td>
</tr>
<tr>
<td>Output voltage</td>
<td>5 V</td>
</tr>
<tr>
<td>Output current</td>
<td>2 A</td>
</tr>
<tr>
<td>Transient response, 1.5 A load step</td>
<td>$\Delta V_{OUT} = \pm 5%$</td>
</tr>
<tr>
<td>Input ripple voltage</td>
<td>400 mV</td>
</tr>
<tr>
<td>Output voltage ripple</td>
<td>30 mVpp</td>
</tr>
<tr>
<td>Switching frequency</td>
<td>500 kHz</td>
</tr>
</tbody>
</table>
8.2.3 Detailed Design Procedure

8.2.3.1 Input Capacitor Selection

The device requires an input decoupling capacitor and a bulk capacitor is needed depending on the application. A ceramic capacitor over 10 µF is recommended for the decoupling capacitor. An additional 0.1 µF capacitor (C2) from VIN to GND is optional to provide additional high frequency filtering. The capacitor voltage rating needs to be greater than the maximum input voltage.

Use Equation 4 to calculate the input ripple voltage \( \Delta V_{IN} \).

\[
\Delta V_{IN} = \frac{I_{OUT(MAX)} \times 0.25}{C_{BULK} \times f_{SW}} + \left( I_{OUT(MAX)} \times ESR_{MAX} \right)
\]

where:
- \( C_{BULK} \) is the bulk capacitor value
- \( f_{SW} \) is the switching frequency
- \( I_{OUT(MAX)} \) is the maximum loading current
- \( ESR_{MAX} \) is maximum series resistance of the bulk capacitor

The maximum RMS (root mean square) ripple current must also be checked. For worst case conditions, use Equation 5 to calculate \( I_{CIN(RMS)} \).

\[
I_{CIN(RMS)} = \frac{I_{O(MAX)}}{2}
\]

The actual input-voltage ripple is greatly affected by parasitic associated with the layout and the output impedance of the voltage source. Design Requirements show the actual input voltage ripple for this circuit which is larger than the calculated value. This measured value is still below the specified input limit of 400 mV. The maximum voltage across the input capacitors is \( VIN(MAX) + \Delta VIN/2 \). The selected bypass capacitor is rated for 35 V and the ripple current capacity is greater than 2 A. Both values provide ample margin. The maximum ratings for voltage and current must not be exceeded under any circumstance.

8.2.3.2 Bootstrap Capacitor Selection

A 0.1 µF ceramic capacitor must be connected between the BOOT to SW pin for proper operation. It is recommended to use a ceramic capacitor.

8.2.3.3 Output Voltage Set Point

The output voltage of the TPS54202H device is externally adjustable using a resistor divider network. In the application circuit of Figure 14, this divider network is comprised of R2 and R3. Use Equation 6 and Equation 7 to calculate the relationship of the output voltage to the resistor divider.

\[
R3 = \frac{R2 \times V_{ref}}{V_{OUT} - V_{ref}}
\]

\[
V_{out} = V_{ref} \times \left[ \frac{R2}{R3} + 1 \right]
\]

Select a value of R2 to be approximately 100 kΩ. Slightly increasing or decreasing R3 can result in closer output voltage matching when using standard value resistors. In this design, \( R2 = 100 \) kΩ and \( R3 = 13.3 \) kΩ which results in a 5-V output voltage. The 49.9-Ω resistor, R1, is provided as a convenient location to break the control loop for stability testing.

8.2.3.4 Enable Pin Setup

To enable the chip, a pull-up resistor R4 (typical 511 KΩ) connecting between VIN and EN R4 is used to limit the quiet scent current which should be less than 50 µA.
8.2.3.5 Output Filter Components

Two components must be selected for the output filter, the output inductor \( L_O \) and \( C_O \).

8.2.3.5.1 Inductor Selection

Use Equation 8 to calculate the minimum value of the output inductor \( L_{\text{MIN}} \).

\[
L_{\text{MIN}} = \frac{V_{\text{OUT}} \times (V_{\text{IN(MAX)}} - V_{\text{OUT}})}{V_{\text{IN(MAX)}} \times K_{\text{IND}} \times I_{\text{OUT}} \times f_{\text{SW}}}
\]  

(8)

Where:

- \( K_{\text{IND}} \) is a coefficient that represents the amount of inductor ripple current relative to the maximum output current.

In general, the value of \( K_{\text{IND}} \) is at the discretion of the designer; however, the following guidelines may be used.

For designs using low-ESR output capacitors, such as ceramics, a value as high as \( K_{\text{IND}} = 0.3 \) can be used. When using higher ESR output capacitors, \( K_{\text{IND}} = 0.2 \) yields better results.

For this design example, use \( K_{\text{IND}} = 0.3 \). The minimum inductor value is calculated as \( 13.7 \, \mu H \). For this design, a close standard value of \( 15 \, \mu H \) was selected for \( L_{\text{MIN}} \).

For the output filter inductor, the RMS current and saturation current ratings must not be exceeded. Use Equation 9 to calculate the RMS inductor current \( I_{L(RMS)} \).

\[
I_{L(\text{MAX})} = \sqrt{\frac{2 \times V_{\text{OUT}} \times (V_{\text{IN(MAX)}} - V_{\text{OUT}})}{V_{\text{IN(MAX)}} \times L_{\text{OUT}} \times f_{\text{SW}} \times 0.8}}
\]  

(9)

Use Equation 10 to calculate the peak inductor current \( I_{L(\text{PK})} \).

\[
I_{L(\text{PK})} = I_{\text{OUT(MAX)}} + \frac{V_{\text{OUT}} \times (V_{\text{IN(MAX)}} - V_{\text{OUT}})}{1.6 \times V_{\text{IN(MAX)}} \times L_{\text{OUT}} \times f_{\text{SW}}}
\]  

(10)

Smaller or larger inductor values can be used depending on the amount of ripple current the designer wants to allow so long as the other design requirements are met. Larger value inductors have lower AC current and result in lower output voltage ripple. Smaller inductor values increase AC current and output voltage ripple.

8.2.3.5.2 Output Capacitor Selection

Consider three primary factors when selecting the value of the output capacitor. The output capacitor determines the modulator pole, the output voltage ripple, and how the regulator responds to a large change in load current. The output capacitance must be selected based on the more stringent of these three criteria.

The desired response to a large change in the load current is the first criterion. The output capacitor must supply the load with current when the regulator cannot. This situation occurs if the desired hold-up times are present for the regulator. In this case, the output capacitor must hold the output voltage above a certain level for a specified amount of time after the input power is removed. The regulator is also temporarily unable to supply sufficient output current if a large, fast increase occurs affecting the current requirements of the load, such as a transition from no load to full load. The regulator usually requires two or more clock cycles for the control loop to notice the change in load current and output voltage and to adjust the duty cycle to react to the change. The output capacitor must be sized to supply the extra current to the load until the control loop responds to the load change. The output capacitance must be large enough to supply the difference in current for 2 clock cycles while only allowing a tolerable amount of drop in the output voltage. Use Equation 11 to calculate the minimum required output capacitance.
\[ C_0 > \frac{2 \times \Delta I_{\text{OUT}}}{f_{\text{sw}} \times \Delta V_{\text{OUT}}} \]

where:
- \( \Delta I_{\text{OUT}} \) is the change in output current
- \( f_{\text{sw}} \) is the switching frequency of the regulator
- \( \Delta V_{\text{OUT}} \) is the allowable change in the output voltage

For this example, the transient load response is specified as a 5% change in the output voltage, \( V_{\text{OUT}} \), for a load step of 1.5 A. For this example, \( \Delta I_{\text{OUT}} = 1.5 \text{ A} \) and \( \Delta V_{\text{OUT}} = 0.05 \times 5 = 0.25 \text{ V} \). Using these values results in a minimum capacitance of 24 \( \mu \text{F} \). This value does not consider the ESR of the output capacitor in the output voltage change. For ceramic capacitors, the ESR is usually small enough to ignore in this calculation.

Equation 12 calculates the minimum output capacitance required to meet the output voltage ripple specification. In this case, the maximum output voltage ripple is 30 mV. Under this requirement, Equation 12 yields 4.56 \( \mu \text{F} \).

\[ C_0 > \frac{1}{8 \times f_{\text{SW}}} \times \frac{1}{\frac{V_{\text{OUTripple}}}{I_{\text{ripple}}}} \]

where:
- \( f_{\text{SW}} \) is the switching frequency
- \( V_{\text{OUTripple}} \) is the maximum allowable output voltage ripple
- \( I_{\text{ripple}} \) is the inductor ripple current

Use Equation 13 to calculate the maximum ESR an output capacitor can have to meet the output-voltage ripple specification. Equation 13 indicates the ESR should be less than 54.8 m\( \Omega \). In this case, the ESR of the ceramic capacitor is much smaller than 54.8 m\( \Omega \).

\[ R_{\text{ESR}} < \frac{V_{\text{OUTripple}}}{I_{\text{ripple}}} \]

The output capacitor can affect the crossover frequency \( f_o \). Considering to the loop stability and effect of the internal parasitic parameters, choose the crossover frequency less than 40 kHz without considering the feed forward capacitor. A simple estimation for the crossover frequency without feed forward capacitor \( C_6 \) is shown in Equation 14, assuming \( C_{\text{OUT}} \) has small ESR.

\[ f_o = \frac{3.95}{V_{\text{OUT}} \times C_{\text{OUT}}} \]

Additional capacitance deratings for aging, temperature, and DC bias should be considered which increases this minimum value. For this example, two 22-uF 25-V, X7R ceramic capacitors are used. Capacitors generally have limits to the amount of ripple current they can handle without failing or producing excess heat. An output capacitor that can support the inductor ripple current must be specified. Some capacitor data sheets specify the RMS value of the maximum ripple current. Use Equation 15 to calculate the RMS ripple current that the output capacitor must support. For this application, Equation 15 yields 79 mA for each capacitor.

\[ I_{\text{OUT(RMS)}} = \frac{1}{\sqrt{12}} \times \left( \frac{V_{\text{OUT}} \times (V_{\text{IN(MAX)}} - V_{\text{OUT}})}{V_{\text{IN(MAX)}} \times L_{\text{OUT}} \times f_{\text{SW}} \times N_c} \right) \]
8.2.3.5.3 Feed-Forward Capacitor

The TPS54202H is internally compensated and the internal compensation network is composed of two capacitors and one resistor shown on the block diagram. Depending on the $V_{OUT}$, if the output capacitor $C_{OUT}$ is dominated by low ESR (ceramic types) capacitors, it could result in low phase margin. To improve the phase boost an external feedforward capacitor $C_6$ can be added in parallel with $R_2$. $C_6$ is chosen such that phase margin is boosted at the crossover frequency.

**Equation 16** for $C_6$ was tested:

$$C_6 = \frac{1}{\frac{1}{2\pi f_0} \times \frac{1}{R_2}}$$

For this design, $C_6 = 75$ pF. $C_6$ is not needed when $C_{OUT}$ has high ESR, and $C_6$ calculated from **Equation 16** should be reduced with medium ESR. **Table 2** can be used as a starting point.

<table>
<thead>
<tr>
<th>$V_{OUT}$ (V)</th>
<th>$L$ (µH)</th>
<th>$C_{OUT}$ (µF)</th>
<th>$R_2$ (kΩ)</th>
<th>$R_3$ (kΩ)</th>
<th>$C_6$ (pF)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1.8</td>
<td>5.6</td>
<td>66</td>
<td>100</td>
<td>49.9</td>
<td>47</td>
</tr>
<tr>
<td>2.5</td>
<td>8.2</td>
<td>44</td>
<td>100</td>
<td>31.6</td>
<td>33</td>
</tr>
<tr>
<td>3.3</td>
<td>10</td>
<td>44</td>
<td>100</td>
<td>22.1</td>
<td>56</td>
</tr>
<tr>
<td>5</td>
<td>15</td>
<td>44</td>
<td>100</td>
<td>13.3</td>
<td>75</td>
</tr>
<tr>
<td>12</td>
<td>22</td>
<td>44</td>
<td>100</td>
<td>5.23</td>
<td>100</td>
</tr>
</tbody>
</table>
8.2.4 Application Curves

---

**Figure 15. Efficiency**

---

**Figure 16. Line Regulation**

---

**Figure 17. Load Regulation**

---

**Figure 18. Input Voltage Ripple**

---

**Figure 19. Output Voltage Ripple**

---

**Figure 20. Output Voltage Ripple**
Figure 21. Output Voltage Ripple

Figure 22. Output Voltage Ripple

Figure 23. Transient Response

Figure 24. Transient Response

Figure 25. Start-Up Relative to VIN

Figure 26. Shutdown Relative to VIN
9 Power Supply Recommendations

The devices are designed to operate from an input voltage supply range between 4.5 V and 28 V. This input supply must be well regulated. If the input supply is located more than a few inches from the device or converter, additional bulk capacitance may be required in addition to the ceramic bypass capacitors. An electrolytic capacitor with a value of 47 µF is a typical choice.
10 Layout

10.1 Layout Guidelines

• VIN and GND traces should be as wide as possible to reduce trace impedance. The wide areas are also of advantage from the view point of heat dissipation.
• The input capacitor and output capacitor should be placed as close to the device as possible to minimize trace impedance.
• Provide sufficient vias for the input capacitor and output capacitor.
• Keep the SW trace as physically short and wide as practical to minimize radiated emissions.
• Do not allow switching current to flow under the device.
• A separate VOUT path should be connected to the upper feedback resistor.
• Make a Kelvin connection to the GND pin for the feedback path.
• Voltage feedback loop should be placed away from the high-voltage switching trace, and preferably has ground shield.
• The trace of the VFB node should be as small as possible to avoid noise coupling.
• The GND trace between the output capacitor and the GND pin should be as wide as possible to minimize its trace impedance.

10.2 Layout Example

Figure 29. Board Layout
11 Device and Documentation Support

11.1 Community Resources
The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

**TI E2E™ Online Community** *TI's Engineer-to-Engineer (E2E) Community.* Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

**Design Support** *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.2 Trademarks
Eco-mode, E2E are trademarks of Texas Instruments. All other trademarks are the property of their respective owners.

11.3 Electrostatic Discharge Caution
These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.4 Glossary
**SLYZ022 — TI Glossary.**

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information
The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.
## PACKAGING INFORMATION

<table>
<thead>
<tr>
<th>Orderable Device</th>
<th>Status</th>
<th>Package Type</th>
<th>Package Drawing</th>
<th>Pins</th>
<th>Package Qty</th>
<th>Eco Plan (2)</th>
<th>Lead/Ball Finish</th>
<th>MSL Peak Temp (3)</th>
<th>Op Temp (°C)</th>
<th>Device Marking (4/5)</th>
<th>Samples</th>
</tr>
</thead>
<tbody>
<tr>
<td>TPS54202HDDCR</td>
<td>ACTIVE</td>
<td>SOT-23-THIN</td>
<td>DDC</td>
<td>6</td>
<td>3000</td>
<td>Green (RoHS &amp; no Sb/Br)</td>
<td>CU SN</td>
<td>Level-1-260C-UNLIM</td>
<td>-40 to 125</td>
<td>202H</td>
<td>Samples</td>
</tr>
<tr>
<td>TPS54202HDDCT</td>
<td>ACTIVE</td>
<td>SOT-23-THIN</td>
<td>DDC</td>
<td>6</td>
<td>250</td>
<td>Green (RoHS &amp; no Sb/Br)</td>
<td>CU SN</td>
<td>Level-1-260C-UNLIM</td>
<td>-40 to 125</td>
<td>202H</td>
<td>Samples</td>
</tr>
</tbody>
</table>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check [http://www.ti.com/productcontent](http://www.ti.com/productcontent) for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

**Important Information and Disclaimer:** The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.
### TAPE AND REEL INFORMATION

#### TAPE DIMENSIONS

- **A0**: Dimension designed to accommodate the component width
- **B0**: Dimension designed to accommodate the component length
- **K0**: Dimension designed to accommodate the component thickness
- **W**: Overall width of the carrier tape
- **P1**: Pitch between successive cavity centers

#### REEL DIMENSIONS

- **Reel Diameter**
- **Reel Width (W1)**

#### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

*All dimensions are nominal.*

<table>
<thead>
<tr>
<th>Device</th>
<th>Package Type</th>
<th>Package Drawing</th>
<th>Pins</th>
<th>SPQ</th>
<th>Reel Diameter (mm)</th>
<th>Reel Width W1 (mm)</th>
<th>A0 (mm)</th>
<th>B0 (mm)</th>
<th>K0 (mm)</th>
<th>P1 (mm)</th>
<th>W (mm)</th>
<th>Pin1 Quadrant</th>
</tr>
</thead>
<tbody>
<tr>
<td>TPS54202HDDCR</td>
<td>SOT-23-THIN</td>
<td>DDC</td>
<td>6</td>
<td>3000</td>
<td>180.0</td>
<td>9.5</td>
<td>3.1</td>
<td>1.1</td>
<td>4.0</td>
<td>8.0</td>
<td>Q3</td>
<td></td>
</tr>
<tr>
<td>TPS54202HDDCT</td>
<td>SOT-23-THIN</td>
<td>DDC</td>
<td>6</td>
<td>250</td>
<td>180.0</td>
<td>9.5</td>
<td>3.1</td>
<td>1.1</td>
<td>4.0</td>
<td>8.0</td>
<td>Q3</td>
<td></td>
</tr>
</tbody>
</table>
# TAPE AND REEL BOX DIMENSIONS

*All dimensions are nominal

<table>
<thead>
<tr>
<th>Device</th>
<th>Package Type</th>
<th>Package Drawing</th>
<th>Pins</th>
<th>SPQ</th>
<th>Length (mm)</th>
<th>Width (mm)</th>
<th>Height (mm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>TPS54202HDDCR</td>
<td>SOT-23-THIN</td>
<td>DDC</td>
<td>6</td>
<td>3000</td>
<td>184.0</td>
<td>184.0</td>
<td>19.0</td>
</tr>
<tr>
<td>TPS54202HDDCT</td>
<td>SOT-23-THIN</td>
<td>DDC</td>
<td>6</td>
<td>250</td>
<td>184.0</td>
<td>184.0</td>
<td>19.0</td>
</tr>
</tbody>
</table>
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
NOTES: (continued)

4. Publication IPC-7351 may have alternate designs.
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate
design recommendations.

7. Board assembly site may have different recommendations for stencil design.
IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale (www.ti.com/legal/termsofsale.html) or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2019, Texas Instruments Incorporated