4.5V to 18V Input, 3-A SYNCHRONOUS STEP DOWN CONVERTER

Check for Samples: TPS54329

FEATURES

• D-CAP2™ Mode Enables Fast Transient Response
• Low Output Ripple and Allows Ceramic Output Capacitor
• Wide VIN Input Voltage Range: 4.5 V to 18 V
• Output Voltage Range: 0.76 V to 7.0 V
• Highly Efficient Integrated FETs Optimized for Lower Duty Cycle Applications
  – 100 mΩ (High Side) and 74 mΩ (Low Side)
• High Efficiency, Less Than 10 μA at Shutdown
• High Initial Bandgap Reference Accuracy
• Adjustable Soft Start
• Pre-Biased Soft Start
• 650-kHz Switching Frequency (fSW)
• Cycle By Cycle Over Current Limit

APPLICATIONS

• Wide Range of Applications for Low Voltage System
  – Digital TV Power Supply
  – High Definition Blu-ray Disc™ Players
  – Networking Home Terminal
  – Digital Set Top Box (STB)

DESCRIPTION

The TPS54329 is an adaptive on-time D-CAP2™ mode synchronous buck converter. The TPS54329 enables system designers to complete the suite of various end equipment’s power bus regulators with a cost effective, low component count, low standby current solution. The main control loop for the TPS54329 uses the D-CAP2™ mode control which provides a fast transient response with no external compensation components. The TPS54329 also has a proprietary circuit that enables the device to adopt to both low equivalent series resistance (ESR) output capacitors, such as POSCAP or SP-CAP, and ultra-low ESR ceramic capacitors. The device operates from 4.5-V to 18-V VIN input. The output voltage can be programmed between 0.76 V and 7 V. The device also features an adjustable soft start time. The TPS54329 is available in the 8-pin DDA package, and designed to operate from –40°C to 85°C.
This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

**ORDERING INFORMATION**

<table>
<thead>
<tr>
<th>T_A</th>
<th>PACKAGE(2) (3)</th>
<th>ORDERABLE PART NUMBER</th>
<th>PIN</th>
<th>TRANSPORT MEDIA</th>
</tr>
</thead>
<tbody>
<tr>
<td>–40°C to 85°C</td>
<td>DDA</td>
<td>TPS54329DDA</td>
<td>8</td>
<td>Tube</td>
</tr>
<tr>
<td></td>
<td></td>
<td>TPS54329DDAR</td>
<td></td>
<td>Tape and Reel</td>
</tr>
</tbody>
</table>

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.

(2) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.

(3) All package options have Cu NiPDAU lead/ball finish.

**ABSOLUTE MAXIMUM RATINGS**

over operating free-air temperature range (unless otherwise noted) (1)

<table>
<thead>
<tr>
<th>VALUE</th>
<th>MIN</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>VIN, EN</td>
<td>–0.3</td>
<td>20</td>
<td>V</td>
</tr>
<tr>
<td>VBST</td>
<td>–0.3</td>
<td>26</td>
<td>V</td>
</tr>
<tr>
<td>VBST (10 ns transient)</td>
<td>–0.3</td>
<td>28</td>
<td>V</td>
</tr>
<tr>
<td>VBST (vs SW)</td>
<td>–0.3</td>
<td>6.5</td>
<td>V</td>
</tr>
<tr>
<td>VFB, SS</td>
<td>–0.3</td>
<td>6.5</td>
<td>V</td>
</tr>
<tr>
<td>SW</td>
<td>–2</td>
<td>20</td>
<td>V</td>
</tr>
<tr>
<td>SW (10 ns transient)</td>
<td>–3</td>
<td>22</td>
<td>V</td>
</tr>
<tr>
<td>VREG5</td>
<td>–0.3</td>
<td>6.5</td>
<td>V</td>
</tr>
<tr>
<td>GND</td>
<td>–0.3</td>
<td>0.3</td>
<td>V</td>
</tr>
<tr>
<td>Voltage from GND to thermal pad, Vdiff</td>
<td>–0.2</td>
<td>0.2</td>
<td>V</td>
</tr>
<tr>
<td>Electrostatic discharge Human Body Model (HBM)</td>
<td>2</td>
<td>kV</td>
<td></td>
</tr>
<tr>
<td>Electrostatic discharge Charged Device Model (CDM)</td>
<td>500</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>Operating junction temperature, T_J</td>
<td>–40</td>
<td>150</td>
<td>°C</td>
</tr>
<tr>
<td>Storage temperature, T_stg</td>
<td>–55</td>
<td>150</td>
<td>°C</td>
</tr>
</tbody>
</table>

(1) Stresses beyond those listed under **absolute maximum ratings** may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under **recommended operating conditions** is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

**THERMAL INFORMATION**

<table>
<thead>
<tr>
<th>THERMAL METRIC</th>
<th>TPS54329 DDA (8 PINS)</th>
<th>UNITS</th>
</tr>
</thead>
<tbody>
<tr>
<td>θ_JA</td>
<td>42.1</td>
<td>°C/W</td>
</tr>
<tr>
<td>θ_JCtop</td>
<td>50.9</td>
<td></td>
</tr>
<tr>
<td>θ_JB</td>
<td>31.8</td>
<td></td>
</tr>
<tr>
<td>Ψ_JT</td>
<td>5</td>
<td></td>
</tr>
<tr>
<td>Ψ_JB</td>
<td>13.5</td>
<td></td>
</tr>
<tr>
<td>θ_JCbottom</td>
<td>7.1</td>
<td></td>
</tr>
</tbody>
</table>

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### RECOMMENDED OPERATING CONDITIONS

Over operating free-air temperature range (unless otherwise noted)

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{IN}$</td>
<td>Supply input voltage range</td>
<td>$4.5$</td>
<td>$18$</td>
<td>$V$</td>
<td></td>
</tr>
<tr>
<td>$V_{BST}$</td>
<td>$-0.1$</td>
<td>$24$</td>
<td>$V$</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$V_{BST}$ (10 ns transient)</td>
<td>$-0.1$</td>
<td>$27$</td>
<td>$V$</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$V_{BST}$ (vs SW)</td>
<td>$-0.1$</td>
<td>$5.7$</td>
<td>$V$</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$SS$</td>
<td>$-0.1$</td>
<td>$5.7$</td>
<td>$V$</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$EN$</td>
<td>$-0.1$</td>
<td>$18$</td>
<td>$V$</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$V_{FB}$</td>
<td>$-0.1$</td>
<td>$5.5$</td>
<td>$V$</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$SW$</td>
<td>$-1.8$</td>
<td>$18$</td>
<td>$V$</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$SW$ (10 ns transient)</td>
<td>$-3$</td>
<td>$21$</td>
<td>$V$</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$GND$</td>
<td>$-0.1$</td>
<td>$0.1$</td>
<td>$V$</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$V_{O}$</td>
<td>Output voltage range</td>
<td>$-0.1$</td>
<td>$5.7$</td>
<td>$V$</td>
<td></td>
</tr>
<tr>
<td>$I_{O}$</td>
<td>Output Current range</td>
<td>$0$</td>
<td>$10$</td>
<td>$mA$</td>
<td></td>
</tr>
<tr>
<td>$T_{A}$</td>
<td>Operating free-air temperature</td>
<td>$-40$</td>
<td>$85$</td>
<td>$°C$</td>
<td></td>
</tr>
<tr>
<td>$T_{J}$</td>
<td>Operating junction temperature</td>
<td>$-40$</td>
<td>$150$</td>
<td>$°C$</td>
<td></td>
</tr>
</tbody>
</table>

### ELECTRICAL CHARACTERISTICS

Over operating free-air temperature range, $V_{IN} = 12$ V (unless otherwise noted)

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>$I_{VIN}$</td>
<td>Operating - non-switching supply current</td>
<td>$800$</td>
<td>$1200$</td>
<td>$μA$</td>
<td></td>
</tr>
<tr>
<td>$I_{VINSDN}$</td>
<td>Shutdown supply current</td>
<td>$4.3$</td>
<td>$10$</td>
<td>$μA$</td>
<td></td>
</tr>
<tr>
<td>$V_{ENH}$</td>
<td>EN high-level input voltage</td>
<td>$1.6$</td>
<td>$V$</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$V_{ENL}$</td>
<td>EN low-level input voltage</td>
<td>$0.45$</td>
<td>$V$</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$R_{EN}$</td>
<td>EN pin resistance to GND</td>
<td>$220$</td>
<td>$440$</td>
<td>$880$</td>
<td>$kΩ$</td>
</tr>
<tr>
<td>$V_{FBTH}$</td>
<td>$V_{FB}$ threshold voltage</td>
<td>$749$</td>
<td>$781$</td>
<td>$mV$</td>
<td></td>
</tr>
<tr>
<td>$I_{VFB}$</td>
<td>$V_{FB}$ input current</td>
<td>$0$</td>
<td>$±0.1$</td>
<td>$μA$</td>
<td></td>
</tr>
<tr>
<td>$V_{VREG5}$</td>
<td>$V_{REGS}$ output voltage</td>
<td>$5.5$</td>
<td>$V$</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$I_{VREG5}$</td>
<td>Output current</td>
<td>$60$</td>
<td>$mA$</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$R_{DS(on)}$</td>
<td>High side switch resistance</td>
<td>$100$</td>
<td>$mΩ$</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$R_{DS(on)}$</td>
<td>Low side switch resistance</td>
<td>$74$</td>
<td>$mΩ$</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$I_{OCL}$</td>
<td>Current limit</td>
<td>$3.5$</td>
<td>$5.7$</td>
<td>$A$</td>
<td></td>
</tr>
</tbody>
</table>

(1) Not production tested.
**ELECTRICAL CHARACTERISTICS (continued)**

over operating free-air temperature range, \( V_{IN} = 12 \) V (unless otherwise noted)

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>THERMAL SHUTDOWN</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>( T_{SDN} )</td>
<td>Thermal shutdown threshold</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Shutdown temperature (^{(2)})</td>
<td></td>
<td>165</td>
<td></td>
<td></td>
<td>°C</td>
</tr>
<tr>
<td>Hysteresis (^{(2)})</td>
<td></td>
<td>35</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>ON-TIME TIMER CONTROL</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>( I_{ON} )</td>
<td>On time</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>( V_{IN} = 12 ) V, ( V_O = 1.05 ) V</td>
<td></td>
<td>150</td>
<td></td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>( I_{OFF(MIN)} )</td>
<td>Minimum off time</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>( T_A = 25) ^{\circ}C, ( V_{FB} = 0.7 ) V (^{(2)})</td>
<td></td>
<td>260</td>
<td></td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>SOFT START</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>( I_{SSC} )</td>
<td>SS charge current</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>( V_{SS} = 1 ) V</td>
<td></td>
<td>4.2</td>
<td>6.0</td>
<td>7.8</td>
<td>μA</td>
</tr>
<tr>
<td>( I_{SSD} )</td>
<td>SS discharge current</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>( V_{SS} = 0.5 ) V</td>
<td></td>
<td>0.1</td>
<td>0.2</td>
<td></td>
<td>mA</td>
</tr>
<tr>
<td>UVLO</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>UVLO</td>
<td>UVLO threshold</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Wake up ( V_{REG5} ) voltage</td>
<td></td>
<td>3.75</td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>Hysteresis ( V_{REG5} ) voltage</td>
<td></td>
<td>0.33</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

\(^{(2)}\) Not production tested.
### PIN FUNCTIONS

<table>
<thead>
<tr>
<th>PIN DESCRIPTION</th>
<th>NAME</th>
<th>NO.</th>
</tr>
</thead>
<tbody>
<tr>
<td>Supply input for the high-side FET gate drive circuit. Connect 0.1µF capacitor between VBST and SW pins. An internal diode is connected between VREG5 and VBST.</td>
<td>VBST</td>
<td>1</td>
</tr>
<tr>
<td>Input voltage supply pin.</td>
<td>VIN</td>
<td>2</td>
</tr>
<tr>
<td>Switch node connection between high-side NFET and low-side NFET.</td>
<td>SW</td>
<td>3</td>
</tr>
<tr>
<td>Ground pin. Power ground return for switching circuit. Connect sensitive SS and VFB returns to GND at a single point.</td>
<td>GND</td>
<td>4</td>
</tr>
<tr>
<td>Converter feedback input. Connect to output voltage with feedback resistor divider.</td>
<td>VFB</td>
<td>5</td>
</tr>
<tr>
<td>5.5 V power supply output. A capacitor (typical 0.47µF) should be connected to GND. VREG5 is not active when EN is low.</td>
<td>VREG5</td>
<td>6</td>
</tr>
<tr>
<td>Enable input control. EN is active high and must be pulled up to enable the device.</td>
<td>EN</td>
<td>7</td>
</tr>
<tr>
<td>Soft-start control. An external capacitor should be connected to GND.</td>
<td>SS</td>
<td>8</td>
</tr>
<tr>
<td>Thermal pad of the package. Must be soldered to achieve appropriate dissipation. Must be connected to GND.</td>
<td>Exposed Thermal Pad</td>
<td>Back side</td>
</tr>
</tbody>
</table>
OVERVIEW

The TPS54329 is a 3-A synchronous step-down (buck) converter with two integrated N-channel MOSFETs. It operates using D-CAP2™ mode control. The fast transient response of D-CAP2™ control reduces the output capacitance required to meet a specific level of performance. Proprietary internal circuitry allows the use of low ESR output capacitors including ceramic and special polymer types.

DETAILED DESCRIPTION

PWM Operation

The main control loop of the TPS54329 is an adaptive on-time pulse width modulation (PWM) controller that supports a proprietary D-CAP2™ mode control. D-CAP2™ mode control combines constant on-time control with an internal compensation circuit for pseudo-fixed frequency and low external component count configuration with both low ESR and ceramic output capacitors. It is stable even with virtually no ripple at the output.

At the beginning of each cycle, the high-side MOSFET is turned on. This MOSFET is turned off after internal one shot timer expires. This one shot is set by the converter input voltage, VIN, and the output voltage, VO, to maintain a pseudo-fixed frequency over the input voltage range, hence it is called adaptive on-time control. The one-shot timer is reset and the high-side MOSFET is turned on again when the feedback voltage falls below the reference voltage. An internal ramp is added to reference voltage to simulate output ripple, eliminating the need for ESR induced output ripple from D-CAP2™ mode control.

PWM Frequency and Adaptive On-Time Control

TPS54329 uses an adaptive on-time control scheme and does not have a dedicated on board oscillator. The TPS54329 runs with a pseudo-constant frequency of 650 kHz by using the input voltage and output voltage to set the on-time one-shot timer. The on-time is inversely proportional to the input voltage and proportional to the output voltage, therefore, when the duty ratio is VOUT/VIN, the frequency is constant.

Soft Start and Pre-Biased Soft Start

The soft start function is adjustable. When the EN pin becomes high, 6 μA current begins charging the capacitor which is connected from the SS pin to GND. Smooth control of the output voltage is maintained during start up. The equation for the slow start time is shown in Equation 1. VFB voltage is 0.765 V and SS pin source current is 6 μA.

\[ t_{SS}(ms) = \frac{C_{SS}(nF) \times V_{REF} \times 1.1}{I_{SS}(\mu A)} = \frac{C_{SS}(nF) \times 0.765 \times 1.1}{6} \]  

(1)

The TPS54329 contains a unique circuit to prevent current from being pulled from the output during startup if the output is pre-biased. When the soft-start commands a voltage higher than the pre-bias level (internal soft start becomes greater than feedback voltage VFB), the controller slowly activates synchronous rectification by starting the first low side FET gate driver pulses with a narrow on-time. It then increments that on-time on a cycle-by-cycle basis until it coincides with the time dictated by (1-D), where D is the duty cycle of the converter. This scheme prevents the initial sinking of the pre-bias output, and ensure that the out voltage (VO) starts and ramps up smoothly into regulation and the control loop is given time to transition from pre-biased start-up to normal mode operation.

Current Protection

The output overcurrent protection (OCP) is implemented using a cycle-by-cycle valley detect control circuit. The switch current is monitored by measuring the low-side FET switch voltage between the SW pin and GND. This voltage is proportional to the switch current. To improve accuracy, the voltage sensing is temperature compensated.

During the on time of the high-side FET switch, the switch current increases at a linear rate determined by Vin, Vout, the on-time and the output inductor value. During the on time of the low-side FET switch, this current decreases linearly. The average value of the switch current is the load current IOUT. The TPS54329 constantly monitors the low-side FET switch voltage, which is proportional to the switch current, during the low-side on-time. If the measured voltage is above the voltage proportional to the current limit, an internal counter is incremented per each SW cycle and the converter maintains the low-side switch on until the measured voltage is below the voltage corresponding to the current limit at which time the switching cycle is terminated and a new switching
cycle begins. In subsequent switching cycles, the on-time is set to a fixed value and the current is monitored in the same manner. If the over current condition exists for 7 consecutive switching cycles, the internal OCL threshold is set to a lower level, reducing the available output current. When a switching cycle occurs where the switch current is not above the lower OCL threshold, the counter is reset and the OCL limit is returned to the higher value.

There are some important considerations for this type of over-current protection. The load current one half of the peak-to-peak inductor current higher than the over-current threshold. Also when the current is being limited, the output voltage tends to fall as the demanded load current may be higher than the current available from the converter. This may cause the output voltage to fall. When the over current condition is removed, the output voltage will return to the regulated value. This protection is non-latching.

**UVLO Protection**

Undervoltage lock out protection (UVLO) monitors the voltage of the \( V_{\text{REGS}} \) pin. When the \( V_{\text{REGS}} \) voltage is lower than UVLO threshold voltage, the TPS54329 is shut off. This is protection is non-latching.

**Thermal Shutdown**

TPS54329 monitors the temperature of itself. If the temperature exceeds the threshold value (typically 165°C), the device is shut off. This is non-latch protection.
TYPICAL CHARACTERISTICS

$V_{IN} = 12\, \text{V}, \; T_A = 25\, \text{°C}$ (unless otherwise noted).

Figure 1. $V_{IN}$ CURRENT vs JUNCTION TEMPERATURE

Figure 2. $V_{IN}$ SHUTDOWN CURRENT vs JUNCTION TEMPERATURE

Figure 3. EN CURRENT vs EN VOLTAGE

Figure 4. 1.05-V OUTPUT VOLTAGE vs OUTPUT CURRENT

Figure 5. 1.05-V OUTPUT VOLTAGE vs INPUT VOLTAGE

Figure 6. 1.05-V, 50-mA to 2-A LOAD TRANSIENT RESPONSE
TYPICAL CHARACTERISTICS

$V_{IN} = 12 \text{V}, T_A = 25^\circ\text{C}$ (unless otherwise noted).

Figure 7. START-UP WAVE FORM

Figure 8. EFFICIENCY vs OUTPUT CURRENT

Figure 9. SWITCHING FREQUENCY vs INPUT VOLTAGE

Figure 10. SWITCHING FREQUENCY vs OUTPUT CURRENT

Figure 11. V fb VOLTAGE vs JUNCTION TEMPERATURE

Figure 12. VOLTAGE RIPPLE AT OUTPUT ($I_O = 3 \text{ A}$)
TYPICAL CHARACTERISTICS

$V_{IN} = 12\, \text{V}, \quad T_{A} = 25\, ^\circ\text{C}$ (unless otherwise noted).

Figure 13. VOLTAGE RIPPLE AT INPUT ($I_O = 3\, \text{A}$)


**DESIGN GUIDE**

**Step By Step Design Procedure**
To begin the design process, you must know a few application parameters:

- Input voltage range
- Output voltage
- Output current
- Output voltage ripple
- Input voltage ripple

![Schematic Diagram](image)

**Output Voltage Resistors Selection**
The output voltage is set with a resistor divider from the output node to the VFB pin. It is recommended to use 1% tolerance or better divider resistors. Start by using Equation 2 to calculate $V_{OUT}$.

To improve efficiency at very light loads consider using larger value resistors, too high of resistance will be more susceptible to noise and voltage errors from the VFB input current will be more noticeable.

\[
V_{OUT} = 0.765 \times \left(1 + \frac{R_1}{R_2}\right)
\]  
(2)

**Output Filter Selection**
The output filter used with the TPS54329 is an LC circuit. This LC filter has double pole at:

\[
F_P = \frac{1}{2\pi \sqrt{L_{OUT} \times C_{OUT}}}
\]  
(3)

At low frequencies, the overall loop gain is set by the output set-point resistor divider network and the internal gain of the TPS54329. The low frequency phase is 180 degrees. At the output filter pole frequency, the gain rolls off at a −40 dB per decade rate and the phase drops rapidly. D-CAP2™ introduces a high frequency zero that reduces the gain roll off to −20 dB per decade and increases the phase to 90 degrees one decade above the zero frequency. The inductor and capacitor selected for the output filter must be selected so that the double pole of Equation 3 is located below the high frequency zero but close enough that the phase boost provided be the high frequency zero provides adequate phase margin for a stable circuit. To meet this requirement use the values recommended in Table 1.
Table 1. Recommended Component Values

<table>
<thead>
<tr>
<th>Output Voltage (V)</th>
<th>R1 (kΩ)</th>
<th>R2 (kΩ)</th>
<th>C4 (pF)(^{1})</th>
<th>L1 (µH)</th>
<th>C8 + C9 + C10 (µF)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>6.81</td>
<td>22.1</td>
<td></td>
<td>1.5</td>
<td>20 - 68</td>
</tr>
<tr>
<td>1.05</td>
<td>8.25</td>
<td>22.1</td>
<td></td>
<td>1.5</td>
<td>20 - 68</td>
</tr>
<tr>
<td>1.2</td>
<td>12.7</td>
<td>22.1</td>
<td></td>
<td>1.5</td>
<td>20 - 68</td>
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<tr>
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<td>21.5</td>
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<td>20 - 68</td>
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<tr>
<td>1.8</td>
<td>30.1</td>
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<td>5 - 22</td>
<td>2.2</td>
<td>20 - 68</td>
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<td>2.5</td>
<td>49.9</td>
<td>22.1</td>
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<td>2.2</td>
<td>20 - 68</td>
</tr>
<tr>
<td>3.3</td>
<td>73.2</td>
<td>22.1</td>
<td>5 - 22</td>
<td>2.2</td>
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<tr>
<td>5</td>
<td>124</td>
<td>22.1</td>
<td>5 - 22</td>
<td>3.3</td>
<td>20 - 68</td>
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<tr>
<td>6.5</td>
<td>165</td>
<td>22.1</td>
<td>5 - 22</td>
<td>3.3</td>
<td>20 - 68</td>
</tr>
</tbody>
</table>

\(^{1}\) Optional

Since the DC gain is dependent on the output voltage, the required inductor value will increase as the output voltage increases. For higher output voltages at or above 1.8 V, additional phase boost can be achieved by adding a feed forward capacitor (C4) in parallel with R1.

The inductor peak-to-peak ripple current, peak current and RMS current are calculated using Equation 4, Equation 5 and Equation 6. The inductor saturation current rating must be greater than the calculated peak current and the RMS or heating current rating must be greater than the calculated RMS current. Use 650 kHz for f\(_{SW}\).

Make sure the chosen inductor is rated for the peak current of Equation 5 and the RMS current of Equation 6.

\[
I_{\text{PP}} = \frac{V_{\text{OUT}}}{V_{\text{IN(max)}}} \times \frac{V_{\text{IN(max)}} - V_{\text{OUT}}}{L_{O} \times f_{SW}}
\]  
(4)

\[
I_{\text{peak}} = I_{O} + \frac{I_{\text{PP}}}{2}
\]  
(5)

\[
I_{L_{O}(\text{RMS})} = \sqrt{I_{O}^{2} + \frac{1}{12} I_{\text{PP}}^{2}}
\]  
(6)

For this design example, the calculated peak current is 3.49 A and the calculated RMS current is 3.01 A. The inductor used is a TDK CLF7045T-1R5M with a peak current rating of 7.3 A and an RMS current rating of 4.9 A.

The capacitor value and ESR determines the amount of output voltage ripple. The TPS54329 is intended for use with ceramic or other low ESR capacitors. Recommended values range from 20 µF to 68 µF. Use Equation 7 to determine the required RMS current rating for the output capacitor.

\[
I_{C_{O}(\text{RMS})} = \frac{V_{\text{OUT}}(V_{\text{IN}} - V_{\text{OUT}})}{\sqrt{12} \times V_{\text{IN}} \times L_{O} \times f_{SW}}
\]  
(7)

For this design three TDK C3216X5R0J106M 10 µF output capacitors are used. The typical ESR is 2 mΩ each. The calculated RMS current is 0.284 A and each output capacitor is rated for 4A.

**Input Capacitor Selection**

The TPS54229 requires an input decoupling capacitor and a bulk capacitor is needed depending on the application. A ceramic capacitor over 10 µF is recommended for the decoupling capacitor. An additional 0.1 µF capacitor (C3) is required to provide additional high frequency filtering and insure accurate current limit operation. This capacitor must be placed as close to the IC pins 2 (VIN) and 4 (GND) as possible. The capacitor voltage rating needs to be greater than the maximum input voltage.

**Bootstrap Capacitor Selection**

A 0.1 µF ceramic capacitor must be connected between the VBST to SW pin for proper operation. It is recommended to use a ceramic capacitor.
VREG5 Capacitor Selection

A 0.47 µF ceramic capacitor must be connected between the VREG5 to GND pin for proper operation. It is recommended to use a ceramic capacitor.

THERMAL INFORMATION

This 8-pin DDA package incorporates an exposed thermal pad that is designed to be directly to an external heatsink. The thermal pad must be soldered directly to the printed board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the exposed thermal pad and how to use the advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD™ Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD™ Made Easy, Texas Instruments Literature No. SLMA004.

The exposed thermal pad dimensions for this package are shown in the following illustration.

![Figure 15. Thermal Pad Dimensions (Top View)](image-url)
LAYOUT CONSIDERATIONS

1. Keep the input switching current loop as small as possible.

2. Keep the SW node as physically small and short as possible to minimize parasitic capacitance and inductance and to minimize radiated emissions. Kelvin connections should be brought from the output to the feedback pin of the device.

3. Keep analog and non-switching components away from switching components.

4. Make a single point connection from the signal ground to power ground.

5. Do not allow switching current to flow under the device.

6. Keep the pattern lines for VIN and PGND broad.

7. Exposed pad of device must be connected to PGND with solder.

8. VREG5 capacitor should be placed near the device, and connected PGND.

9. Output capacitor should be connected to a broad pattern of the PGND.

10. Voltage feedback loop should be as short as possible, and preferably with ground shield.

11. Lower resistor of the voltage divider which is connected to the VFB pin should be tied to analog ground trace.

12. Providing sufficient vias for VIN, SW and PGND connection.

13. VIN input bypass capacitor and VIN high frequency bypass capacitor must be placed as near as possible to the device.

14. Performance based on four layer printed circuit board.
Figure 16. PCB Layout

- VIA to Power Ground Plane
- VIA to SW Copper Pour on Bottom or Internal Layer

- VIN
  - INPUT
  - BYPASS CAPACITOR

- VIN
  - HIGH FREQUENCY BYPASS CAPACITOR

- BOOST CAPACITOR

- VFB

- VREG5

- SS

- GND

- ENVIN

- VBST

- SW

- EXPOSED THERMAL PAD AREA

- VOUT

- VIA to Power Ground Plane

- OUTPUT CAPACITOR

- FEEDBACK RESISTORS

- TO ENABLE CONTROL

- SLOW START CAP

- ANALOG GROUND TRACE

- CONNECTION TO POWER GROUND on internal or bottom layer

- SW node copper pour area on internal or bottom layer
## REVISION HISTORY

Changes from Original (September 2011) to Revision A

<table>
<thead>
<tr>
<th>Change</th>
<th>Page</th>
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</thead>
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<tr>
<td>Removed (SWIFT™) from the data sheet title</td>
<td>1</td>
</tr>
<tr>
<td>Deleted from ELECTRICAL CHARACTERISTICS table, $V_{LNS}$ and $V_{LDS}$, deleted $V_{VREG5}$ MIN and MAX values</td>
<td>3</td>
</tr>
<tr>
<td>Added in ELECTRICAL CHARACTERISTICS table, $I_{VREG5}$, $R_{DS(on)h}$, and $R_{DS(on)l}$ footnote references</td>
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</tr>
<tr>
<td>Added $t_{OFF(MIN)}$ footnote reference and deleted MAX value</td>
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<tr>
<td>Deleted from ELECTRICAL CHARACTERISTICS, UVLO MIN and MAX values</td>
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<tr>
<td>Added TYPICAL CHARACTERISTICS Condition</td>
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# Packaging Information

<table>
<thead>
<tr>
<th>Orderable Device</th>
<th>Status</th>
<th>Package Type</th>
<th>Package Drawing</th>
<th>PIns</th>
<th>Package Qty</th>
<th>Eco Plan</th>
<th>Lead/Ball Finish</th>
<th>MSL Peak Temp</th>
<th>Op Temp (°C)</th>
<th>Device Marking</th>
<th>Samples</th>
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<tbody>
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<td>SO PowerPAD</td>
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<td>-40 to 85</td>
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<td>Level-2-260C-1 YEAR</td>
<td>-40 to 85</td>
<td>54329</td>
<td></td>
</tr>
</tbody>
</table>

**Notes:**

1. The marketing status values are defined as follows:
   - **ACTIVE:** Product device recommended for new designs.
   - **LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
   - **NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
   - **PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
   - **OBSOLETE:** TI has discontinued the production of the device.

2. **Eco Plan -** The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check [http://www.ti.com/productcontent](http://www.ti.com/productcontent) for the latest availability information and additional product content details.

3. **MSL, Peak Temp.** - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

4. **Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.**

5. **Important Information and Disclaimer:** The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.
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# TAPE AND REEL INFORMATION

## REEL DIMENSIONS

![Reel Diagram](image)

## TAPE DIMENSIONS

<table>
<thead>
<tr>
<th>Device</th>
<th>Package Type</th>
<th>Package Drawing</th>
<th>Pins</th>
<th>SPQ</th>
<th>Reel Diameter (mm)</th>
<th>Reel Width W1 (mm)</th>
<th>A0 (mm)</th>
<th>B0 (mm)</th>
<th>K0 (mm)</th>
<th>P1 (mm)</th>
<th>W (mm)</th>
<th>Pin1 Quadrant</th>
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</thead>
<tbody>
<tr>
<td>TPS54329DDAR</td>
<td>SO Power PAD</td>
<td>DDA</td>
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<td>2.1</td>
<td>8.0</td>
<td>12.0</td>
<td>Q1</td>
</tr>
</tbody>
</table>

*All dimensions are nominal.

- **A0**: Dimension designed to accommodate the component width
- **B0**: Dimension designed to accommodate the component length
- **K0**: Dimension designed to accommodate the component thickness
- **W**: Overall width of the carrier tape
- **P1**: Pitch between successive cavity centers
### TAPE AND REEL BOX DIMENSIONS

*All dimensions are nominal

<table>
<thead>
<tr>
<th>Device</th>
<th>Package Type</th>
<th>Package Drawing</th>
<th>Pins</th>
<th>SPQ</th>
<th>Length (mm)</th>
<th>Width (mm)</th>
<th>Height (mm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>TPS54329DDAR</td>
<td>SO PowerPAD</td>
<td>DDA</td>
<td>8</td>
<td>2500</td>
<td>366.0</td>
<td>364.0</td>
<td>50.0</td>
</tr>
</tbody>
</table>
NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5–1994.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.15.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http://www.ti.com>.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. This package complies to JEDEC MS-012 variation BA

PowerPAD™ is a trademark of Texas Instruments.
THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.

NOTE: A. All linear dimensions are in millimeters

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NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC-7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>. Publication IPC-7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.
F. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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