TPS61086 18.5-V PFM – PWM Step-Up DC – DC Converter With 2.0-A Switch

1 Features
- 2.3-V to 6.0-V Input Voltage Range
- 18.5-V Boost Converter With 2.0-A Switch Current
- 1.2-MHz Switching Frequency
- Power Save Mode for Improved Efficiency at Low-Output Power or Forced PWM
- Adjustable Soft-Start
- Thermal Shutdown
- Undervoltage Lockout
- 10-Pin VSON Package

2 Applications
- Handheld Devices
- GPS Receivers
- Digital Still Cameras
- Portable Applications
- DSL Modems
- PCMCIA Cards
- TFT LCD Bias Supply

3 Description
The TPS61086 device is a high-frequency, high-efficiency DC-to-DC converter with an integrated 2.0-A, 0.13-Ω power switch capable of providing an output voltage up to 18.5 V. The implemented boost converter is based on a fixed frequency of 1.2-MHz, pulse-width-modulation (PWM) controller that allows the use of small external inductors and capacitors and provides fast transient response.

At light-load, the device can operate in Power Save Mode with pulse-frequency-modulation (PFM) to improve the efficiency while keeping a low-output voltage ripple. For very noise-sensitive applications, the device can be forced to PWM Mode operation over the entire load range by pulling the MODE pin high. The external compensation allows optimizing the application for specific conditions. A capacitor connected to the soft-start pin minimizes inrush current at start-up.

Device Information

<table>
<thead>
<tr>
<th>PART NUMBER</th>
<th>PACKAGE</th>
<th>BODY SIZE (NOM)</th>
</tr>
</thead>
<tbody>
<tr>
<td>TPS61086</td>
<td>VSON (10)</td>
<td>3.00 mm × 3.00 mm</td>
</tr>
</tbody>
</table>

(1) For all available packages, see the orderable addendum at the end of the data sheet.

An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.
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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (June 2015) to Revision B

<table>
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<tr>
<th>Page</th>
</tr>
</thead>
<tbody>
<tr>
<td>Changes from Original (August 2009) to Revision A</td>
</tr>
<tr>
<td>Page</td>
</tr>
</tbody>
</table>

- Changed "FREQ" to "MODE" in Absolute Maximum Ratings table .......................... 4
- Changed "mA" to "A" in X-axis label for Figure 4 .................................................. 6
- Changed $V_S$ from "12V/50 mA" to "12V/500 mA" in Figure 7. ................................ 10
- Added Pin Configuration and Functions section, ESD Ratings table, Feature Description section, Device Functional Modes, Application and Implementation section, Power Supply Recommendations section, Layout section, Device and Documentation Support section, and Mechanical, Packaging, and Orderable Information section ..................... 1
- Deleted Ordering Information table ........................................................................ 1

Product Folder Links: TPS61086
## 5 Pin Configuration and Functions

### DRC Package

<table>
<thead>
<tr>
<th>Pin</th>
<th>Name</th>
<th>No.</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>PIN</td>
<td>I/O</td>
<td>DESCRIPTION</td>
</tr>
<tr>
<td>COMP</td>
<td>1</td>
<td>I/O</td>
<td>Compensation pin</td>
</tr>
<tr>
<td>FB</td>
<td>2</td>
<td>I</td>
<td>Feedback pin</td>
</tr>
<tr>
<td>EN</td>
<td>3</td>
<td>I</td>
<td>Shutdown control input. Connect this pin to logic high level to enable the device</td>
</tr>
<tr>
<td>AGND</td>
<td>4</td>
<td>—</td>
<td>Analog ground</td>
</tr>
<tr>
<td>PGND</td>
<td>5</td>
<td>—</td>
<td>Power ground</td>
</tr>
<tr>
<td>SW</td>
<td>6</td>
<td>—</td>
<td>Switch pin</td>
</tr>
<tr>
<td>IN</td>
<td>7</td>
<td>—</td>
<td>Input supply pin</td>
</tr>
<tr>
<td>MODE</td>
<td>9</td>
<td>I</td>
<td>Operating mode selection pin. MODE = 'high' for forced PWM operation. MODE = 'low' for PFM operation</td>
</tr>
<tr>
<td>SS</td>
<td>10</td>
<td>—</td>
<td>Soft-start control pin. Connect a capacitor to this pin if soft-start needed. Open = no soft-start</td>
</tr>
</tbody>
</table>
6 Specifications

6.1 Absolute Maximum Ratings

<table>
<thead>
<tr>
<th>Parameter</th>
<th>MIN</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>Input voltage IN</td>
<td>−0.3</td>
<td>7</td>
<td>V</td>
</tr>
<tr>
<td>Voltage on pins EN, FB, SS, MODE, COMP</td>
<td>−0.3</td>
<td>7</td>
<td>V</td>
</tr>
<tr>
<td>Voltage on pin SW</td>
<td>−0.3</td>
<td>20</td>
<td>V</td>
</tr>
<tr>
<td>Operating junction temperature</td>
<td>−40</td>
<td>150</td>
<td>°C</td>
</tr>
<tr>
<td>Storage temperature</td>
<td>−65</td>
<td>150</td>
<td>°C</td>
</tr>
</tbody>
</table>

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) All voltage values are with respect to network ground terminal.

6.2 ESD Ratings

<table>
<thead>
<tr>
<th>Electrostatic discharge</th>
<th>Value</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)</td>
<td>±2000</td>
<td>V</td>
</tr>
<tr>
<td>Charged-device model (CDM), per JEDEC specification JESD22-C101(2)</td>
<td>±500</td>
<td>V</td>
</tr>
</tbody>
</table>

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. Pins listed as ±2000 V may actually have higher performance.

(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process. Pins listed as ±500 V may actually have higher performance.

6.3 Recommended Operating Conditions

<table>
<thead>
<tr>
<th>Parameter</th>
<th>MIN</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>IN</td>
<td>2.3</td>
<td>6</td>
<td>V</td>
</tr>
<tr>
<td>VS</td>
<td>V\text{IN} + 0.5</td>
<td>18.5</td>
<td>V</td>
</tr>
<tr>
<td>TA</td>
<td>−40</td>
<td>85</td>
<td>°C</td>
</tr>
<tr>
<td>TJ</td>
<td>−40</td>
<td>125</td>
<td>°C</td>
</tr>
</tbody>
</table>

6.4 Thermal Information

<table>
<thead>
<tr>
<th>THERMAL METRIC(1)</th>
<th>TPS61086</th>
</tr>
</thead>
<tbody>
<tr>
<td>DRC (VSON) 10 PINS</td>
<td></td>
</tr>
<tr>
<td>R_{JA} Junction-to-ambient thermal resistance</td>
<td>54.7 °C/W</td>
</tr>
<tr>
<td>R_{JC(top)} Junction-to-case (top) thermal resistance</td>
<td>67.2 °C/W</td>
</tr>
<tr>
<td>R_{JB} Junction-to-board thermal resistance</td>
<td>29.6 °C/W</td>
</tr>
<tr>
<td>\psi_{JT} Junction-to-top characterization parameter</td>
<td>2.3 °C/W</td>
</tr>
<tr>
<td>\psi_{JB} Junction-to-board characterization parameter</td>
<td>29.8 °C/W</td>
</tr>
<tr>
<td>R_{JC(bot)} Junction-to-case (bottom) thermal resistance</td>
<td>15.6 °C/W</td>
</tr>
</tbody>
</table>

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report, SPRA953.
## 6.5 Electrical Characteristics

\( V_{IN} = 3.3 \text{ V}, EN = IN, V_S = 12 \text{ V}, T_A = -40°C \) to 85°C, typical values are at \( T_A = 25°C \) (unless otherwise noted)

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>SUPPLY</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>( V_{IN} )</td>
<td>Input voltage range</td>
<td>2.3</td>
<td>6</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>( I_Q )</td>
<td>Operating quiescent current into IN</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>( I_{SDVIN} )</td>
<td>Shutdown current into IN</td>
<td>Device not switching, ( V_{FB} = 1.3 \text{ V} )</td>
<td>75</td>
<td>100</td>
<td>( \mu \text{A} )</td>
</tr>
<tr>
<td>( V_{UVLO} )</td>
<td>Undervoltage lockout threshold</td>
<td>( V_{IN} ) falling</td>
<td>2.2</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td></td>
<td></td>
<td>( V_{IN} ) rising</td>
<td>2.3</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>( T_{SD} )</td>
<td>Thermal shutdown</td>
<td>Temperature rising</td>
<td>150</td>
<td></td>
<td>°C</td>
</tr>
<tr>
<td>( T_{SDHYS} )</td>
<td>Thermal shutdown hysteresis</td>
<td></td>
<td>14</td>
<td></td>
<td>°C</td>
</tr>
<tr>
<td><strong>LOGIC SIGNALS EN, FREQ</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>( V_{IH} )</td>
<td>High level input voltage</td>
<td>( V_{IN} = 2.3 \text{ V} ) to 6 V</td>
<td>2</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>( V_{IL} )</td>
<td>Low level input voltage</td>
<td>( V_{IN} = 2.3 \text{ V} ) to 6 V</td>
<td>0.5</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>( I_{INLEAK} )</td>
<td>Input leakage current</td>
<td>( EN = GND )</td>
<td>0.1</td>
<td></td>
<td>( \mu \text{A} )</td>
</tr>
<tr>
<td><strong>BOOST CONVERTER</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>( V_S )</td>
<td>Boost output voltage</td>
<td>( V_{IN} + 0.5 )</td>
<td>18.5</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>( V_{FB} )</td>
<td>Feedback regulation voltage</td>
<td></td>
<td>1.23</td>
<td>1.238</td>
<td>1.246</td>
</tr>
<tr>
<td>( g_m )</td>
<td>Transconductance error amplifier</td>
<td></td>
<td>107</td>
<td></td>
<td>( \mu \text{A/V} )</td>
</tr>
<tr>
<td>( I_{FB} )</td>
<td>Feedback input bias current</td>
<td>( V_{FB} = 1.238 \text{ V} )</td>
<td>0.1</td>
<td></td>
<td>( \mu \text{A} )</td>
</tr>
<tr>
<td>( r_{DS(on)} )</td>
<td>N-channel MOSFET on-resistance</td>
<td>( V_{IN} = V_{GS} = 5 \text{ V}, I_{SW} = \text{current limit} )</td>
<td>0.13</td>
<td>0.2</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>( V_{IN} = V_{GS} = 3.3 \text{ V}, I_{SW} = \text{current limit} )</td>
<td>0.16</td>
<td>0.23</td>
<td></td>
</tr>
<tr>
<td>( I_{SWLEAK} )</td>
<td>SW leakage current</td>
<td>( EN = GND, V_{SW} = 6 \text{ V} )</td>
<td>2</td>
<td>2.6</td>
<td>3.2</td>
</tr>
<tr>
<td>( I_{LIM} )</td>
<td>N-channel MOSFET current limit</td>
<td></td>
<td>7</td>
<td>10</td>
<td>13</td>
</tr>
<tr>
<td>( I_{SS} )</td>
<td>Soft-start current</td>
<td>( V_{SS} = 1.238 \text{ V} )</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>( f_S )</td>
<td>Oscillator frequency</td>
<td></td>
<td>0.9</td>
<td>1.2</td>
<td>1.5</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0.0002</td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>Line regulation</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
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<td></td>
<td></td>
</tr>
<tr>
<td><strong>Load regulation</strong></td>
<td></td>
<td></td>
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<td></td>
<td></td>
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<td></td>
</tr>
</tbody>
</table>

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6.6 Typical Characteristics

The typical characteristics are measured with the inductor CDRH6D12 3.3 µH from Sumida and the rectifier diode SL22.

Table 1. Table of Graphs

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Description</th>
<th>Conditions</th>
<th>FIGURE</th>
</tr>
</thead>
<tbody>
<tr>
<td>η</td>
<td>Efficiency vs Load current - PFM</td>
<td>$V_{\text{IN}} = 3.3 , \text{V}, , V_S = 9 , \text{V}, , 12 , \text{V}, , 15 , \text{V}$</td>
<td>Figure 1</td>
</tr>
<tr>
<td>η</td>
<td>Efficiency vs Load current - Forced PWM</td>
<td>$V_{\text{IN}} = 3.3 , \text{V}, , V_S = 9 , \text{V}, , 12 , \text{V}, , 15 , \text{V}$</td>
<td>Figure 2</td>
</tr>
<tr>
<td>$I_{\text{out(max)}}$</td>
<td>Maximum output current</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$f_S$</td>
<td>Switching frequency - Forced PWM</td>
<td>vs Load current, $V_{\text{IN}} = 3.3 , \text{V}, , V_S = 12 , \text{V}$</td>
<td>Figure 4</td>
</tr>
<tr>
<td>$f_S$</td>
<td>Switching frequency - Forced PWM</td>
<td>vs Supply voltage, $V_S = 12 , \text{V}, , I_{\text{out}} = 200 , \text{mA}$</td>
<td>Figure 5</td>
</tr>
<tr>
<td></td>
<td>Supply current</td>
<td>vs Supply voltage, $V_{\text{IN}} = 3.3 , \text{V}, , V_S = 12 , \text{V}$</td>
<td>Figure 6</td>
</tr>
</tbody>
</table>

Figure 1. PFM Mode Efficiency vs Output Current

Figure 2. Force PWM Mode Efficiency vs Output Current

Figure 3. Output Current vs Supply Voltage

Figure 4. Frequency vs Load Current
Figure 5. Frequency vs Supply Voltage

Figure 6. Supply Current vs Supply Voltage
7 Detailed Description

7.1 Overview

The boost converter is designed for output voltages up to 18.5 V with a switch peak current limit of 2.0 A minimum. The device, which operates in a current mode scheme with quasi-constant frequency, is externally compensated for maximum flexibility and stability. The switching frequency is fixed to 1.2 MHz and the minimum input voltage is 2.3 V. To limit the inrush current at start-up a soft-start pin is available.

TPS61086 boost converter’s novel topology using adaptive OFF-time provides superior load and line transient responses and operates also over a wider range of applications than conventional converters.

7.2 Functional Block Diagram

![Functional Block Diagram]

7.3 Feature Description

7.3.1 Soft-Start

The boost converter has an adjustable soft-start to prevent high inrush current during start-up. To minimize the inrush current during start-up an external capacitor, connected to the soft-start pin SS and charged with a constant current, is used to slowly ramp up the internal current limit of the boost converter. When the EN pin is pulled high, the soft-start capacitor \(C_{SS}\) is immediately charged to 0.3 V. The capacitor is then charged at a constant current of 10 \(\mu\)A typically until the output of the boost converter \(V_S\) has reached its Power Good threshold (90% of \(V_S\) nominal value). During this time, the SS voltage directly controls the peak inductor current, starting with 0 A at \(V_{SS} = 0.3\) V up to the full current limit at \(V_{SS} \approx 800\) mV. The maximum load current is available after the soft-start is completed. The larger the capacitor the slower the ramp of the current limit and the longer the soft-start time. A 100 nF capacitor is usually sufficient for most of the applications. When the EN pin is pulled low, the soft-start capacitor is discharged to ground.
Feature Description (continued)

7.3.2 Undervoltage Lockout (UVLO)

To avoid mis-operation of the device at low input voltages an undervoltage lockout is included that disables the device, if the input voltage falls below 2.2 V.

7.3.3 Thermal Shutdown

A thermal shutdown is implemented to prevent damages due to excessive heat and power dissipation. Typically the thermal shutdown happens at a junction temperature of 150°C. When the thermal shutdown is triggered the device stops switching until the junction temperature falls below typically 136°C. Then the device starts switching again.

7.3.4 Overvoltage Prevention

If overvoltage is detected on the FB pin (typically 3% above the nominal value of 1.238 V) the part stops switching immediately until the voltage on this pin drops to its nominal value. This prevents overvoltage on the output and secures the circuits connected to the output from excessive overvoltage.

7.4 Device Functional Modes

7.4.1 Power Save Mode

Connecting the MODE pin to GND (or any low logic level) enables the Power Save Mode operation. The converter operates in quasi fixed frequency PWM (Pulse Width Modulation) mode at moderate to heavy load and in the PFM (Pulse Frequency Modulation) mode during light loads, which maintains high efficiency over a wide load current range.

In PFM mode the converter is skipping switch pulses. However, within a PFM pulse, the switching frequency is still fixed to 1.2 MHz typically and the duty cycle determined by the input and output voltage. Therefore, the inductor peak current will remain constant for a defined application. With an increasing output load current, the PFM pulses become closer and closer (the PFM mode frequency gets higher) until no pulse is skipped anymore: the device operates then in CCM (Continuous Conduction Mode) with normal PWM mode.

The PFM mode frequency (between each PFM pulse) depends on the load current, the external components like the inductor or the output capacitor values as well as the output voltage. The device enters Power Save Mode as the inductor peak current falls below a 0.6A typically and switches until $V_S$ is 1% higher than its nominal value. The converter stops switching when $V_S = V_S + 0.5%$. The output voltage will therefore oscillate between 0.5% and 1% more than its nominal value which will provide excellent transient response to sudden load change, since the output voltage drop will be reduced due to this slight positive offset (see Figure 12).

7.4.2 Forced PWM Mode

Pulling the MODE pin high forces the converter to operate in a continuous PWM mode even at light load currents. The advantage is that the converter operates with a quasi constant frequency that allows simple filtering of the switching frequency for noise-sensitive applications. In this mode and at light load, the efficiency is lower compared to the Power Save Mode.

For additional flexibility, it is possible to switch from Power Save Mode to Forced PWM Mode during operation. This allows efficient power management by adjusting the operation of the converter to the specific system requirements.
8 Application and Implementation

NOTE
Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The TPS61086 is designed for output voltages up to 18.5 V with a switch peak current limit of 2.0 A minimum. The device, which operates in a current mode scheme with quasi-constant frequency, is externally compensated for maximum flexibility and stability. The switching frequency is fixed to 1.2 MHz and the minimum input voltage is 2.3 V. To limit the inrush current at start-up, a soft-start pin is available.

TPS61086 boost converter's novel topology using adaptive off-time provides superior load and line transient responses and operates also over a wider range of applications than conventional converters.

8.2 Typical Applications

8.2.1 3.3-V to 12-V Boost Converter With PFM Mode at Light Load

Figure 7. Typical Application, 3.3 V to 12 V (PFM Mode)

8.2.1.1 Design Requirements

For this example, the design parameters are listed in Table 2.

Table 2. Design Parameters

<table>
<thead>
<tr>
<th>DESIGN PARAMETERS</th>
<th>EXAMPLE VALUES</th>
</tr>
</thead>
<tbody>
<tr>
<td>Input Voltage</td>
<td>3.3 V ± 20%</td>
</tr>
<tr>
<td>Output Voltage</td>
<td>12 V</td>
</tr>
<tr>
<td>Output Current</td>
<td>500 mA</td>
</tr>
<tr>
<td>Operation Mode at Light Load</td>
<td>PFM</td>
</tr>
</tbody>
</table>
8.2.1.2 Detailed Design Procedure

The first step in the design procedure is to verify that the maximum possible output current of the boost converter supports the specific application requirements. A simple approach is to estimate the converter efficiency, by taking the efficiency numbers from the provided efficiency curves or to use a worst case assumption for the expected efficiency, for example, 90%.

1. Duty cycle, \( D \):
\[
D = 1 - \frac{V_{IN} \cdot \eta}{V_S}
\]  

2. Maximum output current, \( I_{out(max)} \):
\[
I_{out(max)} = \left( I_{LIM(min)} - \frac{\Delta I_L}{2} \right) \cdot (1 - D)
\]

3. Peak switch current in application, \( I_{swpeak} \):
\[
I_{swpeak} = \frac{\Delta I_L}{2} + \frac{I_{out}}{1 - D}
\]

with the inductor peak-to-peak ripple current, \( \Delta I_L \)
\[
\Delta I_L = \frac{V_{IN} \cdot D}{f_S \cdot L}
\]

where
- \( V_{IN} \) is Minimum input voltage.
- \( V_S \) is Output voltage.
- \( I_{LIM(min)} \) is Converter switch current limit (minimum switch current limit = 2.0 A).
- \( f_S \) is Converter switching frequency (typically 1.2 MHz).
- \( L \) is Selected inductor value.
- \( \eta \) is Estimated converter efficiency (please use the number from the efficiency plots or 90% as an estimation).

The peak switch current is the steady-state peak switch current that the integrated switch, inductor and external Schottky diode has to be able to handle. The calculation must be done for the minimum input voltage where the peak switch current is the highest.

8.2.1.2.1 Inductor Selection

The TPS61086 is designed to work with a wide range of inductors. The main parameter for the inductor selection is the saturation current of the inductor which should be higher than the peak switch current as calculated in the Detailed Design Procedure section with additional margin to cover for heavy load transients. An alternative, more conservative, is to choose an inductor with a saturation current at least as high as the maximum switch current limit of 3.2 A. The other important parameter is the inductor DC resistance. Usually the lower the DC resistance the higher the efficiency.

\[\text{NOTE}\]
The inductor DC resistance is not the only parameter determining the efficiency. Especially for a boost converter where the inductor is the energy storage element, the type and core material of the inductor influences the efficiency as well.

Usually an inductor with a larger form factor gives higher efficiency. The efficiency difference between different inductors can vary between 2% to 10%. For the TPS61086, inductor values between 3 \( \mu \)H and 6 \( \mu \)H are a good choice. Possible inductors are shown in Table 3.

Typically, TI recommends that the inductor current ripple is below 35% of the average inductor current. The following equation can therefore be used to calculate the inductor value, \( L \):
\[ L = \left( \frac{V_{IN}}{V_s} \right)^2 \cdot \left( \frac{V_s - V_{IN}}{I_{out} \cdot f_S} \right) \cdot \left( \frac{\eta}{0.35} \right) \]

where
- \( V_{IN} \) is Minimum input voltage.
- \( V_s \) is Output voltage.
- \( I_{out} \) is Maximum output current in the application.
- \( f_S \) is Converter switching frequency (typically 1.2 MHz).
- \( \eta \) is Estimated converter efficiency (please use the number from the efficiency plots or 90% as an estimation).

Table 3. Inductor Selection

<table>
<thead>
<tr>
<th>L (μH)</th>
<th>SUPPLIER</th>
<th>COMPONENT CODE</th>
<th>SIZE (LxWxH mm)</th>
<th>DCR TYP (mΩ)</th>
<th>I_{sat} (A)</th>
</tr>
</thead>
<tbody>
<tr>
<td>3.3</td>
<td>Sumida</td>
<td>CDH38D09</td>
<td>4 x 4 x 1</td>
<td>240</td>
<td>1.25</td>
</tr>
<tr>
<td>4.7</td>
<td>Sumida</td>
<td>CDPH36D13</td>
<td>5 x 5 x 1.5</td>
<td>155</td>
<td>1.36</td>
</tr>
<tr>
<td>3.3</td>
<td>Sumida</td>
<td>CDPH4D19F</td>
<td>5.2 x 5.2 x 2</td>
<td>33</td>
<td>1.5</td>
</tr>
<tr>
<td>3.3</td>
<td>Sumida</td>
<td>CDRH6D12</td>
<td>6.7 x 6.7 x 1.5</td>
<td>62</td>
<td>2.2</td>
</tr>
<tr>
<td>4.7</td>
<td>Würth Elektronik</td>
<td>7447785004</td>
<td>5.9 x 6.2 x 3.3</td>
<td>60</td>
<td>2.5</td>
</tr>
<tr>
<td>5</td>
<td>Coilcraft</td>
<td>MSS7341</td>
<td>7.3 x 7.3 x 4.1</td>
<td>24</td>
<td>2.9</td>
</tr>
</tbody>
</table>

8.2.1.2.2 Rectifier Diode Selection

To achieve high efficiency a Schottky type should be used for the rectifier diode. The reverse voltage rating should be higher than the maximum output voltage of the converter. The averaged rectified forward current \( I_{avg} \), the Schottky diode needs to be rated for, is equal to the output current \( I_{out} \):

\[ I_{avg} = I_{out} \]

(6)

Usually a Schottky diode with 1-A maximum average rectified forward current rating is sufficient for most applications. The Schottky rectifier can be selected with lower forward current capability depending on the output current \( I_{out} \) but has to be able to dissipate the power. The dissipated power, \( P_D \), is the average rectified forward current times the diode forward voltage, \( V_{forward} \):

\[ P_D = I_{avg} \cdot V_{forward} \]

(7)

Typically the diode should be able to dissipate around 500 mW depending on the load current and forward voltage.

Table 4. Rectifier Diode Selection

<table>
<thead>
<tr>
<th>CURRENT RATING ( I_{avg} )</th>
<th>( V_s )</th>
<th>( V_{forward}/I_{avg} )</th>
<th>SUPPLIER</th>
<th>COMPONENT CODE</th>
<th>PACKAGE TYPE</th>
</tr>
</thead>
<tbody>
<tr>
<td>750 mA</td>
<td>20 V</td>
<td>0.425 V / 1 A</td>
<td>Fairchild Semiconductor</td>
<td>FYV0704S</td>
<td>SOT 23</td>
</tr>
<tr>
<td>1 A</td>
<td>20 V</td>
<td>0.39 V / 1 A</td>
<td>NXP</td>
<td>PMEG2010AEH</td>
<td>SOD 123</td>
</tr>
<tr>
<td>1 A</td>
<td>20 V</td>
<td>0.5 V / 1 A</td>
<td>Vishay Semiconductor</td>
<td>SS12</td>
<td>SMA</td>
</tr>
<tr>
<td>1 A</td>
<td>20 V</td>
<td>0.44 V / 1 A</td>
<td>Vishay Semiconductor</td>
<td>MSS1P2L</td>
<td>Âµ -SMP</td>
</tr>
<tr>
<td>2 A</td>
<td>20 V</td>
<td>0.44 V / 2 A</td>
<td>Vishay Semiconductor</td>
<td>SL22</td>
<td>SMB</td>
</tr>
</tbody>
</table>
8.2.1.2.3 Setting the Output Voltage

The output voltage is set by an external resistor divider. Typically, a minimum current of 50 μA flowing through the feedback divider gives good accuracy and noise covering. A standard low side resistor of 18 kΩ is typically selected. The resistors are then calculated as:

\[
R_2 = \frac{V_{FB}}{70 \mu A} \approx 18 k\Omega \quad R_1 = R_2 \cdot \left( \frac{V_S}{V_{FB}} - 1 \right)
\]

\[V_{FB} = 1.238V\]

(8)

8.2.1.2.4 Compensation (COMP)

The regulator loop can be compensated by adjusting the external components connected to the COMP pin. The COMP pin is the output of the internal transconductance error amplifier.

Standard values of \( R_{COMP} = 16 k\Omega \) and \( C_{COMP} = 2.7 nF \) will work for the majority of the applications.

Please refer to Table 5 for dedicated compensation networks giving an improved load transient response. The following equations can be used to calculate \( R_{COMP} \) and \( C_{COMP} \):

\[
R_{COMP} = \frac{110 \cdot V_{IN} \cdot V_S \cdot C_{out}}{L \cdot I_{out}} \quad C_{COMP} = \frac{V_S \cdot C_{out}}{7.5 \cdot I_{out} \cdot R_{COMP}}
\]

where

- \( V_{IN} \) is Minimum input voltage.
- \( V_S \) is Output voltage.
- \( C_{out} \) is Output capacitance.
- \( L \) is Inductor value, for example, 3.3 μH or 4.7 μH.
- \( I_{out} \) is Maximum output current in the application.

(9)

Make sure that \( R_{COMP} < 120 k\Omega \) and \( C_{COMP} > 820 pF \), independent of the results of the above formulas.

### Table 5. Recommended Compensation Network Values at High/Low Frequency

<table>
<thead>
<tr>
<th>( L )</th>
<th>( V_S )</th>
<th>( V_{IN \pm 20%} )</th>
<th>( R_{COMP} )</th>
<th>( C_{COMP} )</th>
</tr>
</thead>
<tbody>
<tr>
<td>3.3 μH</td>
<td>15 V</td>
<td>5 V</td>
<td>100 kΩ</td>
<td>820 pF</td>
</tr>
<tr>
<td></td>
<td></td>
<td>3.3 V</td>
<td>91 kΩ</td>
<td>1.2 nF</td>
</tr>
<tr>
<td></td>
<td>12 V</td>
<td>5 V</td>
<td>68 kΩ</td>
<td>820 pF</td>
</tr>
<tr>
<td></td>
<td></td>
<td>3.3 V</td>
<td>68 kΩ</td>
<td>1.2 nF</td>
</tr>
<tr>
<td></td>
<td>9 V</td>
<td>5 V</td>
<td>39 kΩ</td>
<td>820 pF</td>
</tr>
<tr>
<td></td>
<td></td>
<td>3.3 V</td>
<td>39 kΩ</td>
<td>1.2 nF</td>
</tr>
</tbody>
</table>

Table 5 gives conservative \( R_{COMP} \) and \( C_{COMP} \) values for certain inductors, input and output voltages providing a very stable system. For a faster response time, a higher \( R_{COMP} \) value can be used to enlarge the bandwidth, as well as a slightly lower value of \( C_{COMP} \) to keep enough phase margin. These adjustments should be performed in parallel with the load transient response monitoring of TPS61086.

8.2.1.2.5 Input Capacitor Selection

For good input voltage filtering low-ESR ceramic capacitors are recommended. TPS61086 has an analog input IN. Therefore, a 1-μF bypass is highly recommended as close as possible to the IC from IN to GND.

One 10-μF ceramic input capacitors are sufficient for most of the applications. For better input voltage filtering this value can be increased. Refer to Table 6 and typical applications for input capacitor recommendation.
8.2.1.2.6 Output Capacitor Selection

For best output voltage filtering a low-ESR output capacitor like ceramic capacitor is recommended. Two to four 10-μF ceramic output capacitors (or two 22 μF) work for most of the applications. Higher capacitor values can be used to improve the load transient response. Refer to Table 6 for the selection of the output capacitor.

<table>
<thead>
<tr>
<th>CAPACITOR/SIZE</th>
<th>VOLTAGE RATING</th>
<th>SUPPLIER</th>
<th>COMPONENT CODE</th>
</tr>
</thead>
<tbody>
<tr>
<td>C_IN</td>
<td>22 μF/1206</td>
<td>Taiyo Yuden</td>
<td>EMK316 BJ 226ML</td>
</tr>
<tr>
<td>IN bypass</td>
<td>1 μF/0603</td>
<td>Taiyo Yuden</td>
<td>EMK107 BJ 105KA</td>
</tr>
<tr>
<td>C_OUT</td>
<td>10 μF/1206</td>
<td>Taiyo Yuden</td>
<td>TPK316 BJ 106KL</td>
</tr>
</tbody>
</table>

To calculate the output voltage ripple, the following equation can be used:

\[
\Delta V_C = \frac{V_S - V_IN}{V_S \cdot f_S \cdot C_{out}} \\
\Delta V_{C_{ESR}} = I_{L,\text{peak}} \cdot R_{C_{ESR}}
\]

where

- \(\Delta V_C\) is Output voltage ripple dependent on output capacitance, output current and switching frequency.
- \(V_S\) is Output voltage.
- \(V_IN\) is Minimum input voltage of boost converter.
- \(f_S\) is Converter switching frequency (typically 1.2 MHz).
- \(C_{out}\) is Output capacitance.
- \(\Delta V_{C_{ESR}}\) is Output voltage ripple due to output capacitors ESR (equivalent series resistance).
- \(I_{L,\text{peak}}\) is Inductor peak switch current in the application.
- \(R_{C_{ESR}}\) is Output capacitors equivalent series resistance (ESR).

\(\Delta V_{C_{ESR}}\) can be neglected in many cases since ceramic capacitors provide very low ESR.

8.2.1.3 Application Curves

![Figure 8. PFM Mode Switching Pulse](image_url)

![Figure 9. PFM Mode Switching Pulses](image_url)
Figure 10. PFM Mode - Light Load

Figure 11. Forced PWM / PFM Mode - Heavy Load

Figure 12. Load Transient Response PFM Mode

Figure 13. Line Transient Response Light Load

Figure 14. Soft-Start
8.2.2 3.3-V to 12-V Boost Converter With Forced PWM Mode at Light Load

![Diagram of 3.3-V to 12-V Boost Converter](image)

**Figure 15. Typical Application, 3.3 V to 12 V (Force PWM Mode)**

8.2.2.1 Design Requirements

For this example, the design parameters are listed in Table 7.

<table>
<thead>
<tr>
<th>DESIGN PARAMETERS</th>
<th>EXAMPLE VALUES</th>
</tr>
</thead>
<tbody>
<tr>
<td>Input Voltage</td>
<td>3.3 V ± 20%</td>
</tr>
<tr>
<td>Output Voltage</td>
<td>12 V</td>
</tr>
<tr>
<td>Output Current</td>
<td>500 mA</td>
</tr>
<tr>
<td>Operation Mode at Light Load</td>
<td>Forced PWM</td>
</tr>
</tbody>
</table>

Table 7. Design Parameters
8.2.2.2 Detailed Design Procedure
Refer to Detailed Design Procedure in the 3.3-V to 12-V Boost Converter With PFM Mode at Light Load section.

8.2.2.3 Application Curves

Figure 16. Forced PWM Mode - Light Load

Figure 17. Forced PWM / PFM Mode - Heavy Load

Figure 18. Load Transient Response Force PWM Mode

Figure 19. Line Transient Response Heavy Load
8.3 System Examples

Figure 20. Typical Application 5 V to 15 V (Force PWM Mode) for TFT LCD With External Charge Pumps (VGH, VGL)

Figure 21. Typical Application With External Load Disconnect Switch
System Examples (continued)

Figure 22. Typical Application, 3.3 V to 15 V (PFM Mode) With Overvoltage Protection

Figure 23. Simple Application (3.3-V Input Voltage - Forced PWM Mode) for wLED Supply (3S3P) (With Optional Clamping Zener Diode)
System Examples (continued)

Figure 24. Simple Application (3.3-V Input Voltage - Forced PWM Mode) for wLED Supply (3S3P) With Adjustable Brightness Control Using a PWM Signal on the Enable Pin (With Optional Clamping Zener Diode)

Figure 25. Simple Application (3.3-V Input Voltage - Forced PWM Mode) for wLED Supply (3S3P) With Adjustable Brightness Control Using an Analog Signal on the Feedback Pin (With Optional Clamping Zener Diode)
9 Power Supply Recommendations

The TPS61086 is designed to operate from an input voltage supply range between 2.3 V and 6.0 V. The power supply to the TPS61086 needs to have a current rating according to the supply voltage, output voltage, and output current of the TPS61086.

10 Layout

10.1 Layout Guidelines

For all switching power supplies, the layout is an important step in the design, especially at high peak currents and high switching frequencies. If the layout is not carefully done, the regulator could show stability problems as well as EMI problems. Therefore, use wide and short traces for the main current path and for the power ground tracks. The input capacitor, output capacitor, and the inductor should be placed as close as possible to the IC. Use a common ground node for power ground connecting to the PGND terminal and a different one for control ground connecting to the AGND terminal to minimize the effects of ground noise. Connect these ground nodes at the PGND terminal of the IC. The most critical current path for all boost converters is from the switching FET, through the rectifier diode, then the output capacitors, and back to ground of the switching FET. Therefore, the output capacitors and their traces should be placed on the same board layer as the IC and as close as possible between the IC's SW and PGND terminal.

10.2 Layout Example

![TPS61086 Layout Example](image)

Figure 26. TPS61086 Layout Example
11 Device and Documentation Support

11.1 Community Resources
The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

**TI E2E™ Online Community**  *TI's Engineer-to-Engineer (E2E) Community*. Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

**Design Support**  *TI's Design Support*  Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.2 Trademarks
E2E is a trademark of Texas Instruments. All other trademarks are the property of their respective owners.

11.3 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.4 Glossary

**SLYZ022 — TI Glossary.**

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information
The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.
### PACKAGING INFORMATION

<table>
<thead>
<tr>
<th>Orderable Device</th>
<th>Status (1)</th>
<th>Package Type</th>
<th>Package Drawing</th>
<th>Pins</th>
<th>Package Qty</th>
<th>Eco Plan (2)</th>
<th>Lead/Ball Finish</th>
<th>MSL Peak Temp</th>
<th>Op Temp (°C)</th>
<th>Device Marking (4/5)</th>
<th>Samples</th>
</tr>
</thead>
<tbody>
<tr>
<td>TPS61086DRCR</td>
<td>ACTIVE</td>
<td>VSON</td>
<td>DRC</td>
<td>10</td>
<td>3000</td>
<td>Green (RoHS &amp; no Sb/Br)</td>
<td>CU NIPDAU</td>
<td>Level-2-260C-1 YEAR</td>
<td>-40 to 85</td>
<td>PSRI</td>
<td>Samples</td>
</tr>
<tr>
<td>TPS61086DRCT</td>
<td>ACTIVE</td>
<td>VSON</td>
<td>DRC</td>
<td>10</td>
<td>250</td>
<td>Green (RoHS &amp; no Sb/Br)</td>
<td>CU NIPDAU</td>
<td>Level-2-260C-1 YEAR</td>
<td>-40 to 85</td>
<td>PSRI</td>
<td>Samples</td>
</tr>
</tbody>
</table>

(1) The marketing status values are defined as follows:
- **ACTIVE:** Product device recommended for new designs.
- **LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
- **NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
- **PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
- **OBSOLETE:** TI has discontinued the production of the device.

(2) **Eco Plan** - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check [http://www.ti.com/productcontent](http://www.ti.com/productcontent) for the latest availability information and additional product content details.
- **TBD:** The Pb-Free/Green conversion plan has not been defined.
- **Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
- **Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
- **Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) **MSL, Peak Temp.** - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

**Important Information and Disclaimer:** The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.
In no event shall TI’s liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.
## TAPE AND REEL INFORMATION

### REEL DIMENSIONS

- **Diameter**: Dimension designed to accommodate the component width
- **W1**: Dimension designed to accommodate the component length
- **W**: Overall width of the carrier tape
- **P1**: Pitch between successive cavity centers

### TAPE DIMENSIONS

- **K0**: Cavity
- **A0**: Reel width

### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

- **Q1, Q2, Q3, Q4**: Pocket Quandrants
- **Sprocket Holes**: User Direction of Feed

*All dimensions are nominal.*

<table>
<thead>
<tr>
<th>Device</th>
<th>Package Type</th>
<th>Package Drawing</th>
<th>Pins</th>
<th>SPQ</th>
<th>Reel Diameter (mm)</th>
<th>Reel Width W1 (mm)</th>
<th>A0  (mm)</th>
<th>B0  (mm)</th>
<th>K0  (mm)</th>
<th>P1  (mm)</th>
<th>W (mm)</th>
<th>Pin1 Quadrant</th>
</tr>
</thead>
<tbody>
<tr>
<td>TPS61086DRCR</td>
<td>VSON</td>
<td>DRC</td>
<td>10</td>
<td>3000</td>
<td>330.0</td>
<td>12.4</td>
<td>3.3</td>
<td>3.3</td>
<td>1.1</td>
<td>8.0</td>
<td>12.0</td>
<td>Q2</td>
</tr>
<tr>
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<td>VSON</td>
<td>DRC</td>
<td>10</td>
<td>250</td>
<td>180.0</td>
<td>12.5</td>
<td>3.3</td>
<td>3.3</td>
<td>1.1</td>
<td>8.0</td>
<td>12.0</td>
<td>Q2</td>
</tr>
</tbody>
</table>
### TAPE AND REEL BOX DIMENSIONS

*All dimensions are nominal

<table>
<thead>
<tr>
<th>Device</th>
<th>Package Type</th>
<th>Package Drawing</th>
<th>Pins</th>
<th>SPQ</th>
<th>Length (mm)</th>
<th>Width (mm)</th>
<th>Height (mm)</th>
</tr>
</thead>
<tbody>
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<td>VSON</td>
<td>DRC</td>
<td>10</td>
<td>3000</td>
<td>338.0</td>
<td>355.0</td>
<td>50.0</td>
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<td>TPS61086DRCT</td>
<td>VSON</td>
<td>DRC</td>
<td>10</td>
<td>250</td>
<td>205.0</td>
<td>200.0</td>
<td>33.0</td>
</tr>
</tbody>
</table>
NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Small Outline No–Lead (SON) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance, if present.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions, if present.
THERMAL INFORMATION
This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SOIC PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.

NOTE:  A. All linear dimensions are in millimeters
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com<http://www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.
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