TPS61240-Q1 3.5-MHz High Efficiency Step-Up Converter

1 Features

- Qualified for Automotive Applications
- AEC-Q100 Qualified With the Following Results:
  - Device Temperature Grade
    - TPS61240IDRVRQ1: Grade 3, –40°C to +85°C Ambient Operating Temperature
    - TPS61240TDRVRQ1: Grade 2, –40°C to +105°C Ambient Operating Temperature
  - Device HBM ESD Classification Level 2
  - Device CDM ESD Classification Level C6
- Efficiency > 90% at Nominal Operating Conditions
- Total DC Output Voltage Accuracy 5 V ±2%
- Typical 30 µA Quiescent Current
- Best in Class Line and Load Transient
- Wide VIN Range From 2.3 V to 5.5 V
- Output current up to 450 mA
- Automatic PFM/PWM Mode transition
- Low Ripple Power Save Mode for Improved Efficiency at Light Loads
- Internal Softstart, 250 µs typical Start-Up time
- 3.5 MHz Typical Operating Frequency
- Load Disconnect During Shutdown
- Current Overload and Thermal Shutdown Protection
- Only Three Surface-Mount External Components Required (One MLCC Inductor, Two Ceramic Capacitors)
- Total Solution Size < 13 mm²
- Available in a 2 mm × 2 mm WSON Package

2 Applications

- Advanced Driver Assistance Systems (ADAS)
  - Front Camera
  - Surround View System ECU
  - Radar and LIDAR
- Automotive Infotainment and Cluster
  - Head Unit
  - HMI and Display
- Body Electronics and Lighting
- Factory Automation and Control

3 Description

The TPS61240-Q1 device is a high efficient synchronous step up DC-DC converter optimized for products powered by either a three-cell alkaline, NiCd or NiMH, or one-cell Li-Ion or Li-Polymer battery. The TPS61240-Q1 supports output currents up to 450 mA. The TPS61240-Q1 has an input valley current limit of 500 mA.

TPS61240-Q1 device provides fixed output voltage of 5V-typ with an input voltage range of 2.3 V to 5.5 V and the device supports batteries with extended voltage range. During shutdown, the load is completely disconnected from the battery. The TPS61240-Q1 boost converter is based on a quasi-constant on-time valley current mode control scheme.

The TPS61240-Q1 presents a high impedance at the VOUT pin when shut down. This allows for use in applications that require the regulated output bus to be driven by another supply while the TPS61240-Q1 is shut down.

During light loads the device will automatically pulse skip allowing maximum efficiency at lowest quiescent currents. In the shutdown mode, the current consumption is reduced to less than 1 µA.

TPS61240-Q1 allows the use of a small inductor and capacitors to achieve a small solution size. The TPS61240-Q1 is available in a 2 mm × 2 mm WSON package.

Device Information(1)

<table>
<thead>
<tr>
<th>PART NUMBER</th>
<th>PACKAGE</th>
<th>BODY SIZE (NOM)</th>
</tr>
</thead>
<tbody>
<tr>
<td>TPS61240-Q1</td>
<td>WSON (6)</td>
<td>2.00 mm × 2.00 mm</td>
</tr>
</tbody>
</table>

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Simplified Schematic

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4 Revision History
NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (October 2016) to Revision B

- Added the AEC-Q100 qualified information to the Features section ................................................................. 1
- Added operating ambient temperature for T version of device (TPS61240TDRVRQ1) in the Recommended Operating Conditions table ........................................................................................................... 5
- Added shutdown current for T version of device (TPS61240TDRVRQ1) in the Electrical Characteristics table ........................................................................................................................................... 6
- Changed the Electrostatic Discharge Caution statement ............................................................................................................. 18

Changes from Original (December 2010) to Revision A

- Added Applications section, ESD Ratings table, Feature Description section, Device Functional Modes, Application and Implementation section, Power Supply Recommendations section, Layout section, Device and Documentation Support section, and Mechanical, Packaging, and Orderable Information section ................................................................................................................. 1
- Changed TPS6124x to TPS61240-Q1 throughout document ............................................................................................................. 1
- Changed Description section ......................................................................................................................................................... 1
- Deleted Ordering Information table ................................................................................................................................. 1
- Changed Pin Functions figure and table ........................................................................................................................................ 4
- Deleted Dissipation Ratings table .................................................................................................................................................. 5
- Added Inductance and Output capacitance values and table note to Recommended Operating Conditions ........................................................................................................................................... 5
- Added Thermal Information table ................................................................................................................................................... 5
- Changed reference to Typical Applications section .............................................................................................................. 5
- Changed $V_{OUT}$ test condition to $2.3 \, \text{V} \leq V_{IN} \leq V_{OUT}$ ................................................................................................................. 6
- Added equals before $2.3 \, \text{V}$ in Output current test condition .............................................................................................................. 6
- Removed $I_{SW}$ from all rows except Switch valley current limit .................................................................................................... 6
- Changed Operating quiescent current test condition by adding device not switching ........................................................................................................... 6
- Added equals before 600 mVp-p in Line transient response test condition ............................................................................................................. 6
- Moved figures 8 through 16 to Application Curves section ................................................................................................................. 7
- Updated titles of figures 2 through 7 for better clarity Figure 2 ........................................................................................................... 7
• Deleted Parameter Measurement Information section ................................................................. 9
• Changed Updated Overview section for more clarity .................................................................. 9
• Changed Figure 8 Inductor/Rectifier Currents in Current Limit Operation waveform.................. 10
• Added Under no load conditions to Soft Start section .............................................................. 11
• Deleted HDMI / USB-OTG Application title ............................................................................ 12
• Updated Inductor Selection section .......................................................................................... 13
• Deleted List of Inductors table and listed one example inductor in description ......................... 13
• Changed 2.7 µF to 2.3 µF in Output Capacitor section .............................................................. 14
### 5 Pin Configuration and Functions

**DRV Package**  
6-Pin WSON With Exposed Thermal Pad  
Top View

<table>
<thead>
<tr>
<th>PIN</th>
<th>TYPE</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>GND</td>
<td>Power ground and IC ground</td>
</tr>
<tr>
<td>2</td>
<td>VOUT</td>
<td>Output Supply pin. Connected to the load</td>
</tr>
<tr>
<td>3</td>
<td>FB</td>
<td>Feedback for regulation.</td>
</tr>
<tr>
<td>4</td>
<td>EN</td>
<td>Positive polarity. Low = IC shutdown.</td>
</tr>
<tr>
<td>5</td>
<td>L</td>
<td>Inductor connection to FETs</td>
</tr>
<tr>
<td>6</td>
<td>VIN</td>
<td>Supply from battery</td>
</tr>
<tr>
<td>—</td>
<td>PAD</td>
<td>For good thermal performance, this pad must be soldered to the land pattern on the PCB</td>
</tr>
</tbody>
</table>

Not to scale
6 Specifications

6.1 Absolute Maximum Ratings
over operating free-air temperature range (unless otherwise noted)\(^{(1)(2)}\)

<table>
<thead>
<tr>
<th></th>
<th>MIN</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>Input voltage, (V_i)</td>
<td>–0.3</td>
<td>7</td>
<td>V</td>
</tr>
<tr>
<td>Voltage on (V_{OUT})</td>
<td>–2</td>
<td>7</td>
<td>V</td>
</tr>
<tr>
<td>Voltage on FB</td>
<td>–2</td>
<td>14</td>
<td>V</td>
</tr>
<tr>
<td>Peak output current</td>
<td>Internally limited</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Operating junction temp.</td>
<td>–40</td>
<td>125</td>
<td>°C</td>
</tr>
<tr>
<td>Storage temp. (T_{stg})</td>
<td>–65</td>
<td>150</td>
<td>°C</td>
</tr>
</tbody>
</table>

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) All voltage values are with respect to network ground terminal.

6.2 ESD Ratings

<table>
<thead>
<tr>
<th></th>
<th>VALUE</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>(V_{(ESD)}) Electrostatic discharge</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Human-body model (HBM), per AEC Q100-002(^{(1)})</td>
<td>±2000</td>
<td>V</td>
</tr>
<tr>
<td>Charged-device model (CDM), per AEC Q100-011</td>
<td>±1000</td>
<td>V</td>
</tr>
</tbody>
</table>

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Recommended Operating Conditions
over operating free-air temperature range (unless otherwise noted)

<table>
<thead>
<tr>
<th></th>
<th>MIN</th>
<th>NOM</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>Supply voltage at (V_{IN})</td>
<td>2.3</td>
<td>5.5</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>(L) Inductance</td>
<td>1</td>
<td>2.2</td>
<td>µH</td>
<td></td>
</tr>
<tr>
<td>(C_{out}) Output capacitance</td>
<td>1</td>
<td>20</td>
<td>µF</td>
<td></td>
</tr>
<tr>
<td>(T_A) Operating ambient temperature(^{(1)})</td>
<td>TPS61240IDRVRQ1</td>
<td>–40</td>
<td>85</td>
<td>°C</td>
</tr>
<tr>
<td></td>
<td>TPS61240TDRVRQ1</td>
<td>–40</td>
<td>105</td>
<td>°C</td>
</tr>
</tbody>
</table>

(1) In applications where high power dissipation, poor package thermal resistance, or both are present, the maximum ambient temperature may have to be derated. Maximum ambient temperature \(T_{A(max)}\) is dependent on the maximum operating junction temperature \(T_{J(max)}\), the maximum power dissipation of the device in the application \(P_{D(max)}\), and the junction-to-ambient thermal resistance of the device or package in the application \(R_{JA}\), as given by the following equation: \(T_{A(max)} = T_{J(max)} – (R_{JA} \times P_{D(max)})\)

6.4 Thermal Information

<table>
<thead>
<tr>
<th>THERMAL METRIC(^{(1)})</th>
<th>TPS61240-Q1</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>(R_{JA}) Junction-to-ambient thermal resistance</td>
<td>67.8</td>
<td>°C/W</td>
</tr>
<tr>
<td>(R_{JUC(top)}) Junction-to-case (top) thermal resistance</td>
<td>71.4</td>
<td>°C/W</td>
</tr>
<tr>
<td>(R_{JUB}) Junction-to-board thermal resistance</td>
<td>37.5</td>
<td>°C/W</td>
</tr>
<tr>
<td>(\psi_{JT}) Junction-to-top characterization parameter</td>
<td>1.8</td>
<td>°C/W</td>
</tr>
<tr>
<td>(\psi_{JB}) Junction-to-board characterization parameter</td>
<td>37.8</td>
<td>°C/W</td>
</tr>
<tr>
<td>(R_{JUC(bot)}) Junction-to-case (bottom) thermal resistance</td>
<td>8.7</td>
<td>°C/W</td>
</tr>
</tbody>
</table>

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.
### 6.5 Electrical Characteristics

Over full operating ambient temperature range with typical values at $T_A = 25^\circ C$. Specifications apply for condition $V_{IN} = EN = 3.6$ V (unless otherwise noted). External components $C_{IN} = 2.2 \mu F$, $C_{OUT} = 4.7 \mu F$ (0603), and $L = 1\mu H$ (refer to Typical Applications section).

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>DC/DC STAGE</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$V_{IN}$</td>
<td>Input voltage range</td>
<td>2.3</td>
<td>5.5</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>$V_{OUT}$</td>
<td>Fixed output voltage range</td>
<td>$2.3 \leq V_{IN} \leq V_{OUT}$, $0 \leq I_{OUT} \leq 200$ mA</td>
<td>4.9</td>
<td>5.1</td>
<td>V</td>
</tr>
<tr>
<td>$V_{O_{Ripple}}$</td>
<td>Ripple voltage, PWM mode</td>
<td>$I_{LOAD} = 150$ mA</td>
<td>20</td>
<td>mVpp</td>
<td></td>
</tr>
<tr>
<td>Output current</td>
<td>$V_{IN} = 2.3$ V to 5.5 V</td>
<td>200</td>
<td>mA</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$I_{SW}$</td>
<td>Switch valley current limit</td>
<td>$V_{OUT} = V_{GS} = 5$ V</td>
<td>500</td>
<td>600</td>
<td>mA</td>
</tr>
<tr>
<td>Short circuit current</td>
<td>$V_{OUT} = V_{GS} = 5$ V</td>
<td>200</td>
<td>350</td>
<td>mA</td>
<td></td>
</tr>
<tr>
<td>High side MOSFET on-resistance</td>
<td>$V_{IN} = V_{GS} = 5$ V, $T_A = 25^\circ C$</td>
<td>290</td>
<td>mΩ</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Low Side MOSFET on-resistance</td>
<td>$V_{IN} = V_{GS} = 5$ V, $T_A = 25^\circ C$</td>
<td>250</td>
<td>mΩ</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Operating quiescent current</td>
<td>$I_{OUT} = 0$ mA, power save mode, device not switching</td>
<td>30</td>
<td>40</td>
<td>μA</td>
<td></td>
</tr>
<tr>
<td>Shutdown current</td>
<td>TPS61240IDRVRQ1, EN = GND</td>
<td>1.5</td>
<td>μA</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Reverse leakage current $V_{OUT}$</td>
<td>TPS61240TDRVRQ1, EN = GND</td>
<td>2.5</td>
<td>μA</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Leakage current from battery to $V_{OUT}$</td>
<td>$EN = GND$</td>
<td>2.5</td>
<td>μA</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Line transient response</td>
<td>$V_{IN} = 600$ mVp-p AC square wave, 200 Hz, 12.5% DC at 50 mA or 200 mA load</td>
<td>25</td>
<td>50</td>
<td>mVpk</td>
<td></td>
</tr>
<tr>
<td>Load transient response</td>
<td>$0$ mA to 50 mA, 50 mA to 0 mA, $V_{IN} = 3.6$ V, $T_{Rise} = T_{Fall} = 0.1$ μs</td>
<td>50</td>
<td>mVpk</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>$50$ mA to 200 mA, 200 mA to 50 mA, $V_{IN} = 3.6$ V, $T_{Rise} = T_{Fall} = 0.1$ μs</td>
<td>150</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$I_{IN}$</td>
<td>Input bias current, EN</td>
<td>$EN = GND$ or $V_{IN}$</td>
<td>0.01</td>
<td>1.0</td>
<td>μA</td>
</tr>
<tr>
<td>$V_{UVLO}$</td>
<td>Undervoltage lockout threshold</td>
<td>Falling</td>
<td>2.0</td>
<td>2.1</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Rising</td>
<td>2.1</td>
<td>2.2</td>
<td>V</td>
</tr>
<tr>
<td><strong>CONTROL STAGE</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$V_{IH}$</td>
<td>High level input voltage, EN</td>
<td>$2.3 \leq V_{IN} \leq 5.5$ V</td>
<td>1.0</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>$V_{IL}$</td>
<td>Low level input voltage, EN</td>
<td>$2.3 \leq V_{IN} \leq 5.5$ V</td>
<td>0.4</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>OVC</td>
<td>Input over-voltage threshold</td>
<td>Falling</td>
<td>5.9</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>Rising</td>
<td>6</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$t_{Start}$</td>
<td>Start-up time</td>
<td>Time from active EN to start switching, no-load until $V_{OUT}$ is stable 5 V</td>
<td>300</td>
<td>μs</td>
<td></td>
</tr>
<tr>
<td><strong>DC/DC STAGE</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Freq</td>
<td>See Figure 7</td>
<td>3.5</td>
<td>MHz</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$T_{SD}$</td>
<td>Thermal shutdown</td>
<td>Increasing junction temperature</td>
<td>140</td>
<td>°C</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Thermal shutdown hysteresis</td>
<td>Decreasing junction temperature</td>
<td>20</td>
<td>°C</td>
<td></td>
</tr>
</tbody>
</table>

(1) DRV package has an increased $R_{DSon}$ of about 40 mΩ due to bond wire resistance.
6.6 Typical Characteristics

Table 1. Table of Graphs

<table>
<thead>
<tr>
<th></th>
<th>Figure</th>
</tr>
</thead>
<tbody>
<tr>
<td>Maximum output current</td>
<td>vs Input voltage</td>
</tr>
<tr>
<td>Efficiency</td>
<td>vs Output current, $V_{\text{OUT}} = 5$ V, $V_{\text{IN}} = [2.3 \text{ V}, 3 \text{ V}, 3.6 \text{ V}, 4.2 \text{ V}]$</td>
</tr>
<tr>
<td></td>
<td>vs Input voltage, $V_{\text{OUT}} = 5$ V, $I_{\text{OUT}} = [100 \mu\text{A}, 1 \text{ mA}, 10 \text{ mA}, 100 \text{ mA}, 200 \text{ mA}]$</td>
</tr>
<tr>
<td>Input current</td>
<td>at No output load (PFM Mode)</td>
</tr>
<tr>
<td>Output voltage</td>
<td>vs Output current, $V_{\text{OUT}} = 5$ V, $V_{\text{IN}} = [2.3 \text{ V}, 3 \text{ V}, 3.6 \text{ V}, 4.2 \text{ V}]$</td>
</tr>
<tr>
<td></td>
<td>vs Input voltage</td>
</tr>
<tr>
<td>Frequency</td>
<td>vs Output load, $V_{\text{OUT}} = 5$ V, $V_{\text{IN}} = [3 \text{ V}, 4 \text{ V}, 5 \text{ V}]$</td>
</tr>
</tbody>
</table>

Figure 1. Maximum Output Current vs Input Voltage

Figure 2. Efficiency vs Output Current for Different $V_{\text{IN}} (V_i)$

Figure 3. Efficiency vs Input Voltage for Different Output Current ($I_0$)

Figure 4. Input Current at No Output Load (PFM Mode) for Different $T_A$
Figure 5. Output Voltage vs Output Current for Different V\textsubscript{IN} (V\textsubscript{I})

Figure 6. Output Voltage vs Input Voltage for Different Output Current (I\textsubscript{O})

Figure 7. Frequency vs Output Load for Different V\textsubscript{IN}
7  Detailed Description

7.1  Overview

The TPS61240-Q1 boost converter operates with typically a 3.5-MHz fixed-frequency pulse width modulation (PWM) at moderate to heavy load currents. At light load currents, the converter automatically enters Power Save Mode and then operates in pulse frequency modulation (PFM) mode.

During PWM operation the converter uses a unique fast response quasi-constant on-time valley current mode controller scheme, which allows best in class line and load regulation allowing the use of small ceramic input and output capacitors and a small inductor. During shutdown, the load is completely disconnected from the battery.

Based on the \( \frac{V_{IN}}{V_{OUT}} \) ratio, a simple circuit predicts the required on-time. At the beginning of the switching cycle, the low-side N-MOS switch is turned-on and the inductor current ramps up to a peak current that is defined by the on-time and the inductance. In the second phase, once the peak current is reached, the current comparator trips and the on-timer is reset and this turns off N-MOS switch. Now rectifier switch (P-MOS) is turned on and the inductor current decays to an internally set valley current threshold. Finally, the switching cycle repeats by setting the on timer again and activating the low-side N-MOS switch.

In general, a DC-to-DC step-up converter can only operate in true boost mode, that is, the output is boosted by a certain amount above the input voltage. The TPS61240-Q1 device operates differently as it can smoothly transition in and out of zero duty-cycle operation. Therefore, the output can be kept as close as possible to its regulation limits even though the converter is subject to an input voltage that tends to be excessive.

7.2  Functional Block Diagram
7.3 Feature Description

7.3.1 Current Limit Operation

The current limit circuit employs a valley current sensing scheme. Current limit detection occurs during the off time through sensing of the voltage drop across the synchronous rectifier.

During the current limit operation, the output voltage is reduced as the power stage of the device operates in a constant current mode. The maximum continuous output current (I_{OUT(CL)}), before entering current limit operation, can be defined by Equation 1.

\[
I_{OUT(CL)} = (1 - D) \times (I_{VALLEY} + \frac{1}{2} \Delta I_L) \quad \text{with} \quad \Delta I_L = \frac{V_{IN}}{L} \times \frac{D}{f} \quad \text{and} \quad D = \frac{V_{OUT} - V_{IN}}{V_{OUT}}
\]  

(1)

Figure 8 illustrates the inductor and rectifier current waveforms during current limit operation. The output current, \(I_{OUT}\), is the average of the rectifier ripple current waveform. When the load current is increased such that the lower peak is above the current limit threshold, the off time is lengthened to allow the current to decrease to this threshold before the next on-time begins (so called frequency fold-back mechanism).

7.3.2 Undervoltage Lockout

The undervoltage lockout circuit prevents the device from malfunctioning at low input voltages and from excessive discharge of the battery. It disables the output stage of the converter once the falling \(V_{IN}\) trips the undervoltage lockout threshold \(V_{UVLO}\). The undervoltage lockout threshold \(V_{UVLO}\) for falling \(V_{IN}\) is 2 V (typical). The device starts operation once the rising \(V_{IN}\) trips undervoltage lockout threshold \(V_{UVLO}\) again at 2.1 V (typical).

7.3.3 Input Overvoltage Protection

In the event of an overvoltage condition on the input rail, the output voltage will also experience the overvoltage due to being in dropout condition. An input overvoltage protection feature has been implemented into the TPS61240-Q1, which has an input overvoltage threshold of 6 V. Once this level is triggered, the device will go into shutdown mode to protect itself. If the voltage drops to 5.9 V or below, the device will startup once more into normal operation.
Feature Description (continued)

7.3.4 Enable

Setting EN pin to high, enables the device. At first, the internal reference is activated and the internal analog circuits are settled. Afterwards, the soft start activates and the output voltage ramps up. The output voltages reach nominal values in typically 250 μs after the device has been enabled.

The EN input can control power sequencing in a system with various DC/DC converters. The EN pin can be connected to the output of another converter, to drive the EN pin high and get a sequencing of supply rails. With EN = GND, the device enters shutdown mode.

7.3.5 Soft Start

The TPS61240-Q1 has an internal soft start circuit that controls the ramp up of the output voltage. Under no load conditions, the output voltage reaches nominal values within $t_{\text{Start}}$ of typically 250 μs after EN pin has been pulled to a high level.

This limits the inrush current in the converter during start up and prevents possible input voltage drops when a battery or high impedance power source is used.

During soft start, the switch current limit is reduced to 300 mA until the output voltage reaches $V_{\text{IN}}$. Once the output voltage trips this threshold, the device operates with its nominal current limit $I_{\text{LIMF}}$.

7.3.6 Load Disconnect

Load disconnect electrically removes the output from the input of the power supply when the supply is disabled. This is especially important during shutdown. In shutdown of a boost converter, the load is still connected to the input through the inductor and catch diode. Since the input voltage is still connected to the output, a small current continues to flow, even when the supply is disabled. Even small leakage currents significantly reduce battery life during extended periods of off time.

The benefit of this implemented feature for a system design is that the battery is not depleted during shutdown of the converter. No additional components must be added to the design to make sure that the battery is disconnected from the output of the converter.

7.3.7 Thermal Shutdown

As soon as the junction temperature, $T_J$, exceeds 140°C (typical) the device goes into thermal shutdown. In this mode, the High Side and Low Side MOSFETs are turned off. When the junction temperature falls below the thermal shutdown hysteresis, the device continues operation.

7.4 Device Functional Modes

7.4.1 Power-Save Mode

The TPS61240-Q1 family of devices integrates a power save mode to improve efficiency at light load. In power save mode, the converter only operates when the output voltage trips below a set threshold voltage. It ramps up the output voltage with several pulses and goes into power save mode once the output voltage exceeds the set threshold voltage.

The PFM mode is left and PWM mode entered in case the output current can not longer be supported in PFM mode.
8 Application and Implementation

NOTE
Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI’s customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information
The TPS61240-Q1 boost regulator has fixed output voltage of 5 V typical with an input voltage range of 2.3 V to 5.5 V. TPS61240-Q1 allows the use of small inductors and capacitors to achieve a small solution size and supports output currents up to 450 mA. When shut down, the TPS61240-Q1 presents a high impedance at the VOUT pin and the load is disconnected completely from the battery. This allows for use in applications that require the regulated output bus to be driven by another supply while the TPS61240-Q1 is shut down.

8.2 Typical Applications

8.2.1 Design Requirements
Table 2 lists the design parameters for this application example.

<table>
<thead>
<tr>
<th>PARAMETERS</th>
<th>VALUE</th>
</tr>
</thead>
<tbody>
<tr>
<td>Input voltage</td>
<td>3 V to 4.2 V</td>
</tr>
<tr>
<td>Output voltage</td>
<td>5 V</td>
</tr>
<tr>
<td>Output current</td>
<td>200 mA</td>
</tr>
</tbody>
</table>

8.2.2 Detailed Design Procedure

8.2.2.1 Programming the Output Voltage
The output voltage is set by an internal resistor divider. The FB pin is used to sense the output voltage. To configure the output properly, the FB pin has to be connected directly to the output.
### 8.2.2.2 Inductor Selection

For correct operation of TPS61240-Q1 device, an inductor must be connected between pin \( V_{IN} \) and pin \( L \). A boost converter requires two main passive components for storing energy during the conversion. A boost inductor and a storage capacitor at the output are required. To select the boost inductor, it is recommended to keep the possible peak inductor current below the current limit threshold of the power switch in the chosen configuration. The highest peak current through the inductor and the switch depends on the output load, the input \( (V_{IN}) \), and the output voltage \( (V_{OUT}) \). Estimation of the maximum average inductor current can be done using Equation 2.

\[
I_{L,\text{MAX}} \approx I_{OUT} \times \frac{V_{OUT}}{\eta \times V_{IN}}
\]

where

- \( \eta \) is the efficiency of the switching regulator \hspace{1cm} (2)

For example, for an output current of 200 mA at 5 V \( V_{OUT} \), with efficiency of 85%, at least 392 mA of average current flows through the inductor at a minimum input voltage of 3 V.

The second parameter for choosing the inductor is the desired current ripple in the inductor. Normally, it is advisable to work with a ripple of less than 20% of the average inductor current. A smaller ripple (or larger inductor value) reduces the magnetic hysteresis losses in the inductor, as well as output voltage ripple and EMI. But with larger inductor, regulation time during load transients rises. In addition, a larger inductor increases the total system size and cost. With these parameters, it is possible to calculate the value of the minimum inductance by using Equation 3.

\[
L_{\text{MIN}} = \frac{V_{IN} \times (V_{OUT} - V_{IN})}{\Delta I_L \times f \times V_{OUT}}
\]

where

- \( f \) is the switching frequency
- \( \Delta I_L \) is the ripple current in the inductor \hspace{1cm} (3)

With \( V_{IN} = 4.2 \text{ V} \), \( V_{OUT} = 5 \text{ V} \), assuming inductor ripple current = 30% of minimum current limit of 0.5 A, the resulting inductor value = 1.28 \( \mu \text{H} \). In typical applications, a 1.0 \( \mu \text{H} \) inductance is recommended. The device has been optimized to operate with inductance values between 1.0 \( \mu \text{H} \) and 2.2 \( \mu \text{H} \). It is recommended that inductance values of at least 1.0 \( \mu \text{H} \) is used, even if Equation 3 yields something lower. Care has to be taken that load transients and losses in the circuit can lead to higher currents as estimated in Equation 3. Also, the losses in the inductor caused by magnetic hysteresis losses and copper losses are a major parameter for total circuit efficiency.

With the chosen inductance value, the peak current for the inductor in steady state operation can be calculated. Equation 4 shows how to calculate the peak current \( I \).

\[
I_{L,\text{peak}} = \frac{V_{IN} \times D}{2 \times f \times L} + \frac{I_{OUT}}{(1 - D) \times \eta} \quad \text{with} \quad D = \frac{V_{OUT} - V_{IN}}{V_{OUT}}
\]

This would be the critical value for the current rating for selecting the inductor. It also needs to be taken into account that load transients and error conditions may cause higher inductor currents. Inductor with part number, LQM21PN1R0MC0 is one example of an inductor that can be used with this device. Customers need to verify and validate whether it is suitable for their application.

### 8.2.2.3 Input Capacitor

At least 2.2-\( \mu \text{F} \) input capacitor is recommended to improve transient behavior of the regulator and EMI behavior of the total power supply circuit. It is recommended to place a ceramic capacitor as close as possible to the \( V_{IN} \) and GND pins.
8.2.2.4 Output Capacitor

For the output capacitor, it is recommended to use small ceramic capacitors placed as close as possible to the \(V_{OUT}\) and GND pins of the IC. If, for any reason, the application requires the use of large capacitors which cannot be placed close to the IC, using a smaller ceramic capacitor in parallel to the large one is recommended. This small capacitor should be placed as close as possible to the \(V_{OUT}\) and GND pins of the IC. To get an estimate of the recommended minimum output capacitance, Equation 5 can be used.

\[
C_{\text{min}} = \frac{I_{\text{OUT}} \times (V_{\text{OUT}} - V_{\text{IN}})}{f \times \Delta V \times V_{\text{OUT}}}
\]

where
- \(\Delta V\) is the maximum allowed ripple

With a chosen ripple voltage of 10 mV, a minimum effective capacitance of 2.3 \(\mu\)F is needed. The total ripple is larger due to the ESR of the output capacitor. This additional component of the ripple can be calculated using

\[
\Delta V_{\text{ESR}} = I_{\text{OUT}} \times R_{\text{ESR}}
\]

A capacitor with a value equal to or higher than the calculated minimum should be used. This is required to maintain control loop stability. There are no additional requirements regarding minimum ESR. There is no upper limit for the output capacitance value. Larger capacitors cause lower output voltage ripple as well as lower output voltage drop during load transients.

Note that ceramic capacitors have a DC bias effect, which will have a strong influence on the final effective capacitance. Therefore the correct capacitor value has to be chosen carefully. Package size and voltage rating in combination with material are responsible for differences between the rated capacitor value and the effective capacitance.

8.2.2.5 Checking Loop Stability

The first step of circuit and stability evaluation is to look from a steady-state perspective at the following signals:
- Switching node, \(SW\)
- Inductor current, \(I_{L}\)
- Output ripple voltage, \(V_{O(AC)}\)

These are the basic signals that need to be measured when evaluating a switching converter. When the switching waveform shows large duty cycle jitter or the output voltage or inductor current shows oscillations, the regulation loop may be unstable. This is often a result of board layout and/or L-C combination.

As a next step in the evaluation of the regulation loop, the load transient response is tested. Time between the load transient and the turn on of the P-channel MOSFET, the output capacitor must supply all of the current required by the load. \(V_O\) immediately shifts by an amount equal to \(\Delta I_{\text{(LOAD)}} \times \text{ESR}\), where ESR is the effective series resistance of \(C_O\). \(\Delta I_{\text{(LOAD)}}\) begins to charge or discharge \(C_O\) generating a feedback error signal used by the regulator to return \(V_O\) to its steady-state value. The results are very easily interpreted when the device operates in PWM mode. During recovery time, \(V_O\) can be monitored for settling time, overshoot or ringing to judge the converter’s stability. Without any ringing, the loop has usually more than 45° of phase margin. Because the damping factor of the circuitry is directly related to several resistive parameters (for example, MOSFET \(r_{DS(on)}\)) that are temperature dependant, the loop stability analysis has to be done over the input voltage range, load current range, and temperature range.
8.2.3 Application Curves

Table 3. Table of Application Curves

<table>
<thead>
<tr>
<th>Waveforms</th>
<th>Figure</th>
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<td>Output voltage ripple, PFM mode, $I_{OUT} = 10$ mA</td>
<td>Figure 10</td>
</tr>
<tr>
<td>Output voltage ripple, PWM mode, $I_{OUT} = 150$ mA</td>
<td>Figure 11</td>
</tr>
<tr>
<td>Load transient response, $V_{IN}$, 3.6 V, 0 mA to 50 mA</td>
<td>Figure 12</td>
</tr>
<tr>
<td>Load transient response, $V_{IN}$, 3.6 V, 50 mA to 200 mA</td>
<td>Figure 13</td>
</tr>
<tr>
<td>Line transient response, $V_{IN}$, 3.6 V to 4.2 V, $I_{OUT} = 50$ mA</td>
<td>Figure 14</td>
</tr>
<tr>
<td>Line transient response, $V_{IN}$, 3.6 V to 4.2 V, $I_{OUT} = 200$ mA</td>
<td>Figure 15</td>
</tr>
<tr>
<td>Startup after enable, $V_{IN}$, 3.6 V, $V_{OUT} = 5$ V, Load = 5 kΩ</td>
<td>Figure 16</td>
</tr>
<tr>
<td>Startup after enable, $V_{IN}$, 3.6 V, $V_{OUT} = 5$ V, Load = 16.5 kΩ</td>
<td>Figure 17</td>
</tr>
<tr>
<td>Startup and shutdown, $V_{IN}$, 3.6 V, $V_{OUT} = 5$ V, Load = 16.5 kΩ</td>
<td>Figure 18</td>
</tr>
</tbody>
</table>

Figure 10. Output Voltage Ripple – PFM Mode

Figure 11. Output Voltage Ripple – PWM Mode

Figure 12. Load Transient Response
0 mA to 50 mA and 50 mA to 0 mA

Figure 13. Load Transient Response
0 mA to 200 mA and 200 mA to 0 mA
Figure 14. Line Transient Response
3.6 V to 4.2 V at 50 mA Load

Figure 15. Line Transient Response
3.6 V to 4.2 V at 200 mA Load

Figure 16. Startup After Enable – No Load

Figure 17. Startup After Enable – With Load

Figure 18. Startup and Shutdown
8.3 System Example

Figure 19 is another example for using the TPS61240-Q1 with fixed 5 V and a Schottky diode for output overvoltage protection.

![Diagram of TPS61240-Q1 system example](image)

Figure 19. TPS61240-Q1 Fixed 5 V With Schottky Diode for Output Overvoltage Protection

9 Power Supply Recommendations

The input supply should be in the range from 2.3 V to 5.5 V. The input supply can be a regulated supply voltage or a three-cell alkaline, NiCd or NiMH, or one-cell Li-Ion or Li-Polymer battery. If the input supply is located more than a few inches from the device, additional bulk capacitance may be required in addition to the ceramic bypass capacitors. An electrolytic or tantalum capacitor with a value of 47 \( \mu F \) is a typical choice for the bulk capacitance.

10 Layout

10.1 Layout Guidelines

As for all switching power supplies, the layout is an important step in the design, especially at high peak currents and high switching frequencies. If the layout is not carefully done, the regulator could show stability problems as well as EMI problems. The following are some guidelines for good layout design.

Figure 20 provides an example of layout design with the TPS61240-Q1 device. Follow the guidelines for a good layout.

- Use wide and short traces for the main current path and for the power ground tracks.
- The input and output capacitor, as well as the inductor, should be placed as close as possible to the IC.
- Connect the exposed thermal pad to the GND plane and place multiple thermal vias below the thermal pad to enhance the thermal performance.

10.2 Layout Example

![Diagram of PCB layout example](image)

Figure 20. PCB Layout Example
11 Device and Documentation Support

11.1 Documentation Support

11.1.1 Related Documentation
For related documentation see the following:

- QFN/SON PCB Attachment
- Performing Accurate PFM Mode Efficiency Measurements

11.2 Receiving Notification of Documentation Updates
To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on Alert me to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.3 Community Resources
The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

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**Design Support** *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.4 Trademarks
E2E is a trademark of Texas Instruments.
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11.5 Electrostatic Discharge Caution
This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.6 Glossary
SLYZ022 — *TI Glossary.*
This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information
The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This information is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.
## PACKAGING INFORMATION

<table>
<thead>
<tr>
<th>Orderable Device</th>
<th>Status</th>
<th>Package Type</th>
<th>Package Drawing</th>
<th>Pins</th>
<th>Package Qty</th>
<th>Eco Plan</th>
<th>Lead/Ball Finish</th>
<th>MSL Peak Temp</th>
<th>Op Temp (°C)</th>
<th>Device Marking</th>
<th>Samples</th>
</tr>
</thead>
<tbody>
<tr>
<td>TPS61240IDRVRQ1</td>
<td>ACTIVE</td>
<td>WSON</td>
<td>DRV</td>
<td>6</td>
<td>3000</td>
<td>Green (RoHS &amp; no Sb/Br)</td>
<td>NIPDAU</td>
<td>Level-2-260C-1 YEAR</td>
<td>-40 to 85</td>
<td>QVL</td>
<td></td>
</tr>
<tr>
<td>TPS61240TDRVRQ1</td>
<td>ACTIVE</td>
<td>WSON</td>
<td>DRV</td>
<td>6</td>
<td>3000</td>
<td>Green (RoHS &amp; no Sb/Br)</td>
<td>NIPDAU</td>
<td>Level-2-260C-1 YEAR</td>
<td>-40 to 105</td>
<td>14T</td>
<td></td>
</tr>
</tbody>
</table>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBsolete:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines “RoHS” to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, “RoHS” products are suitable for use in specified lead-free processes. TI may reference these types of products as “Pb-Free”.

**RoHS Exempt:** TI defines “RoHS Exempt” to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines “Green” to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) **MSL, Peak Temp:** The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a ”~” will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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OTHER QUALIFIED VERSIONS OF TPS61240-Q1:

- Catalog: TPS61240

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
## TAPE AND REEL INFORMATION

- **All dimensions are nominal**

<table>
<thead>
<tr>
<th>Device</th>
<th>Package Type</th>
<th>Package Drawing</th>
<th>Pins</th>
<th>SPQ</th>
<th>Reel Diameter (mm)</th>
<th>Reel Width W1 (mm)</th>
<th>A0 (mm)</th>
<th>B0 (mm)</th>
<th>K0 (mm)</th>
<th>P1 (mm)</th>
<th>W (mm)</th>
<th>Pin1 Quadrant</th>
</tr>
</thead>
<tbody>
<tr>
<td>TPS61240IDRVRQ1</td>
<td>WSON</td>
<td>DRV</td>
<td>6</td>
<td>3000</td>
<td>179.0</td>
<td>8.4</td>
<td>2.2</td>
<td>2.2</td>
<td>1.2</td>
<td>4.0</td>
<td>8.0</td>
<td>Q2</td>
</tr>
<tr>
<td>TPS61240TDRVRQ1</td>
<td>WSON</td>
<td>DRV</td>
<td>6</td>
<td>3000</td>
<td>179.0</td>
<td>8.4</td>
<td>2.2</td>
<td>2.2</td>
<td>1.2</td>
<td>4.0</td>
<td>8.0</td>
<td>Q2</td>
</tr>
</tbody>
</table>

**Dimensions:**
- **A0**: Dimension designed to accommodate the component width
- **B0**: Dimension designed to accommodate the component length
- **K0**: Dimension designed to accommodate the component thickness
- **W**: Overall width of the carrier tape
- **P1**: Pitch between successive cavity centers
### TAPE AND REEL BOX DIMENSIONS

*All dimensions are nominal*

<table>
<thead>
<tr>
<th>Device</th>
<th>Package Type</th>
<th>Package Drawing</th>
<th>Pins</th>
<th>SPQ</th>
<th>Length (mm)</th>
<th>Width (mm)</th>
<th>Height (mm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>TPS61240IDRVRQ1</td>
<td>WSON</td>
<td>DRV</td>
<td>6</td>
<td>3000</td>
<td>195.0</td>
<td>200.0</td>
<td>45.0</td>
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<tr>
<td>TPS61240TDRVRQ1</td>
<td>WSON</td>
<td>DRV</td>
<td>6</td>
<td>3000</td>
<td>195.0</td>
<td>200.0</td>
<td>45.0</td>
</tr>
</tbody>
</table>
Images above are just a representation of the package family, actual package may vary. Refer to the product data sheet for package details.
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).

5. Vias are optional depending on application, refer to device data sheet. If some or all are implemented, recommended via locations are shown.
NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
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