TPS6212x 15-V, 75-mA Highly Efficient Buck Converter

1 Features
- Wide Input Voltage Range: 2 V to 15 V
- Up to 96% Efficiency
- Power Save Mode With 11-µA Quiescent Current
- Output Current 75 mA
- Output Voltage Range: 1.2 V to 5.5 V
- Up to 800-kHz Switch Frequency
- Synchronous Converter, No External Rectifier
- Low Output Ripple Voltage
- 100% Duty Cycle for Lowest Dropout
- Small SOT 8-Pin (TPS62120) and 2-mm x 2-mm DFN 6-Pin (TPS62122) Package
- Internal Soft Start
- Power Good Open Drain Output (TPS62120)
- Open-Drain Output for Output Discharge (TPS62120)
- 2.5-V Rising and 1.85-V Falling UVLO Thresholds

2 Applications
- Low Power RF Applications
- Ultra Low Power Microprocessors
- Energy Harvesting
- Industrial Measuring

3 Description
The TPS6212x device is a highly efficient synchronous step-down DC-DC converter optimized for low-power applications. The device supports up to 75-mA output current and allows the use of tiny external inductors and capacitors.

The wide operating input voltage range of 2 V to 15 V supports energy harvesting, battery powered and as well 9-V or 12-V line powered applications.

With its advanced hysteretic control scheme, the converter provides power save mode operation. At light loads the converter operates in pulse frequency modulation (PFM) mode and transitions automatically in pulse width modulation (PWM) mode at higher load currents. The power save mode maintains high efficiency over the entire load current range. The hysteretic control scheme is optimized for low output ripple voltage in PFM mode in order to reduce output noise to a minimum. The device consumes only 10-µA quiescent current from VIN in PFM mode operation.

In shutdown mode, the device is turned off.

An open-drain power good output is available in the TPS62120 and indicates once the output voltage is in regulation.

The TPS62120 has an additional SGND pin which is connected to GND during shutdown mode. This output can be used to discharge the output capacitor.

The TPS6212x operates over an free air temperature range of –40°C to 85°C. The TPS62120 is available in a small 8-pin SOT-23 package and the TPS62122 in a 2 mm x 2 mm 6-pin DFN package.

Device Information(1)

<table>
<thead>
<tr>
<th>PART NUMBER</th>
<th>PACKAGE</th>
<th>BODY SIZE (NOM)</th>
</tr>
</thead>
<tbody>
<tr>
<td>TPS62120</td>
<td>SOT-23 (8)</td>
<td>2.90 mm x 1.63 mm</td>
</tr>
<tr>
<td>TPS62122</td>
<td>SON (6)</td>
<td>2.00 mm x 2.00 mm</td>
</tr>
</tbody>
</table>

(1) For all available packages, see the orderable addendum at the end of the data sheet.
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4 Revision History
NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (July 2010) to Revision A

• Added Pin Configuration and Functions section, Handling Rating table, Feature Description section, Device Functional Modes, Application and Implementation section, Power Supply Recommendations section, Layout section, Device and Documentation Support section, and Mechanical, Packaging, and Orderable Information section ............................................................... 1
5 Device Comparison Table

<table>
<thead>
<tr>
<th>PART NUMBER</th>
<th>ACTIVE DISCHARGE SWITCH</th>
<th>POWER GOOD</th>
<th>VOUT</th>
</tr>
</thead>
<tbody>
<tr>
<td>TPS62120(1)</td>
<td>yes</td>
<td>Open-Drain</td>
<td>adjustable</td>
</tr>
<tr>
<td>TPS62122(2)</td>
<td>no</td>
<td>no</td>
<td>adjustable</td>
</tr>
</tbody>
</table>

(1) The DCN package is available in tape on reel. Add R suffix to order quantities of 3000 parts per reel, T suffix for 250 parts per reel.
(2) The DRV package is available in tape on reel. Add R suffix to order quantities of 3000 parts per reel, T suffix for 250 parts per reel.

6 Pin Configuration and Functions

<table>
<thead>
<tr>
<th>PIN</th>
<th>I/O</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>EN</td>
<td>4</td>
<td>3</td>
</tr>
<tr>
<td>FB</td>
<td>3</td>
<td>5</td>
</tr>
<tr>
<td>GND</td>
<td>6</td>
<td>2</td>
</tr>
<tr>
<td>PG</td>
<td>—</td>
<td>6</td>
</tr>
<tr>
<td>SGND</td>
<td>—</td>
<td>4</td>
</tr>
<tr>
<td>SW</td>
<td>1</td>
<td>7</td>
</tr>
<tr>
<td>VIN</td>
<td>5</td>
<td>1</td>
</tr>
<tr>
<td>VOUT</td>
<td>2</td>
<td>8</td>
</tr>
<tr>
<td>— Exposed Thermal Pad</td>
<td>—</td>
<td>—</td>
</tr>
</tbody>
</table>
# 7 Specifications

## 7.1 Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted)\(^1\)

<table>
<thead>
<tr>
<th></th>
<th>MIN</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>Voltage at VIN(^2)</td>
<td>–0.3</td>
<td>17</td>
<td>V</td>
</tr>
<tr>
<td>Voltage at SW PIN</td>
<td>–0.3</td>
<td>17</td>
<td>V</td>
</tr>
<tr>
<td>Voltage at EN PIN(^2)</td>
<td>–0.3</td>
<td>6</td>
<td>V</td>
</tr>
<tr>
<td>Voltage on FB Pin</td>
<td>–0.3</td>
<td>3.6</td>
<td>V</td>
</tr>
<tr>
<td>Voltage at PG, VOUT, SGND(^2)</td>
<td>–0.3</td>
<td>6</td>
<td>V</td>
</tr>
<tr>
<td>Current into PG pin</td>
<td>0.5</td>
<td></td>
<td>mA</td>
</tr>
<tr>
<td>Maximum operating junction temperature, (T_J)</td>
<td>–40</td>
<td>125</td>
<td>°C</td>
</tr>
<tr>
<td>Storage temperature, (T_{stg})</td>
<td>–65</td>
<td>150</td>
<td>°C</td>
</tr>
</tbody>
</table>

\(^1\) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

\(^2\) All voltage values are with respect to network ground terminal GND.

## 7.2 ESD Ratings

<table>
<thead>
<tr>
<th>(V_{(ESD)})</th>
<th>VALUE</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>Electrostatic discharge</td>
<td>Human body model (HBM), per ANSI/ESDAJEDEC JS-001(^1)</td>
<td>±2000</td>
</tr>
<tr>
<td></td>
<td>Charged device model (CDM), per JEDEC specification JESD22-C101(^2)</td>
<td>±1000</td>
</tr>
</tbody>
</table>

\(^1\) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

\(^2\) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

## 7.3 Recommended Operating Conditions

<table>
<thead>
<tr>
<th></th>
<th>MIN</th>
<th>NOM</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>Supply voltage VIN, device in operation</td>
<td>2</td>
<td>15</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>Output current capability (V_{IN} = 2) V, (V_{OUT} = 1.8) V, (DCR_L = 0.7) Ω</td>
<td>25</td>
<td></td>
<td>mA</td>
<td></td>
</tr>
<tr>
<td></td>
<td>75</td>
<td></td>
<td>mA</td>
<td></td>
</tr>
<tr>
<td>Effective inductance</td>
<td>10</td>
<td>22</td>
<td>33</td>
<td>µH</td>
</tr>
<tr>
<td>Effective output capacitance</td>
<td>1.0</td>
<td>2</td>
<td>33</td>
<td>µF</td>
</tr>
<tr>
<td>Output voltage</td>
<td>1.2</td>
<td>5.5</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>Operating ambient temperature (T_A)(^1), (unless otherwise noted)</td>
<td>–40</td>
<td>85</td>
<td>°C</td>
<td></td>
</tr>
<tr>
<td>Operating junction temperature, (T_J)</td>
<td>–40</td>
<td>125</td>
<td>°C</td>
<td></td>
</tr>
</tbody>
</table>

\(^1\) In applications where high power dissipation and/or poor package thermal resistance is present, the maximum ambient temperature may have to be derated. Maximum ambient temperature \(T_{A(max)}\) is dependent on the maximum operating junction temperature \(T_{J(max)}\), the maximum power dissipation of the device in the application \(P_{D(max)}\), and the junction-to-ambient thermal resistance of the part/package in the application \(R_{JA}\), as given by the following equation: \(T_{A(max)} = T_{J(max)} - (R_{JA} \times P_{D(max)})\).
### 7.4 Thermal Information

<table>
<thead>
<tr>
<th>THERMAL METRIC(1)</th>
<th>TPS62120 DCN [SOT-23]</th>
<th>TPS62122 DRV [DFN]</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>$R_{JA}$ Junction-to-ambient thermal resistance</td>
<td>259.7</td>
<td>114.4</td>
<td>°C/W</td>
</tr>
<tr>
<td>$R_{JC(top)}$ Junction-to-case(top) thermal resistance</td>
<td>114.1</td>
<td>73.7</td>
<td>°C/W</td>
</tr>
<tr>
<td>$R_{JB}$ Junction-to-board thermal resistance</td>
<td>185.8</td>
<td>201.9</td>
<td>°C/W</td>
</tr>
<tr>
<td>$\psi_{JT}$ Junction-to-top characterization parameter</td>
<td>21.6</td>
<td>0.8</td>
<td>°C/W</td>
</tr>
<tr>
<td>$\psi_{JB}$ Junction-to-board characterization parameter</td>
<td>121.6</td>
<td>94.9</td>
<td>°C/W</td>
</tr>
<tr>
<td>$R_{JC(bot)}$ Junction-to-case(bottom) thermal resistance</td>
<td>n/a</td>
<td>122.7</td>
<td>°C/W</td>
</tr>
</tbody>
</table>

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report, SPRA953.

### 7.5 Electrical Characteristics

$V_{IN} = 8$ V, $V_{OUT} = 1.8$ V, $EN = V_{IN}$, $T_J = -40^\circ$C to $85^\circ$C, typical values are at $T_J = 25^\circ$C (unless otherwise noted), $C_{IN} = 4.7$ µF, $L = 22$ µH, $C_{OUT} = 4.7$ µF.

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{IN}$</td>
<td>Input voltage range(1)</td>
<td>Device operating</td>
<td>2</td>
<td>15</td>
<td>V</td>
</tr>
<tr>
<td>$I_Q$</td>
<td>Quiescent current</td>
<td>$I_{OUT} = 0$ mA, device not switching, $EN = VIN$, regulator sleeps</td>
<td>11</td>
<td>18</td>
<td>µA</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$I_{OUT} = 0$ mA, device switching, $V_{IN} = 8$ V, $V_{OUT} = 1.8$ V</td>
<td>13</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$I_{Active}$</td>
<td>Active mode current consumption</td>
<td>$V_{IN} = 5.5$ V = $V_{OUT}$, $T_J = 25^\circ$C, high-side MOSFET switch fully turned on</td>
<td>240</td>
<td>275</td>
<td>µA</td>
</tr>
<tr>
<td>$I_{SD}$</td>
<td>Shutdown current</td>
<td>$EN = GND$, $V_{OUT} = SW = 0$ V, $V_{IN} = 3.6$ V (2)</td>
<td>0.3</td>
<td>1.2</td>
<td>µA</td>
</tr>
<tr>
<td>$V_{UVLO}$</td>
<td>Undervoltage lockout threshold</td>
<td>Failing $V_{IN}$</td>
<td>1.85</td>
<td>1.95</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Rising $V_{IN}$</td>
<td>2.5</td>
<td>2.61</td>
<td></td>
</tr>
<tr>
<td>ENABLE, THRESHOLD</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$V_{IH\ TH}$</td>
<td>Threshold for detecting high EN</td>
<td>$2$ V ≤ $V_{IN}$ ≤ $15$ V, rising edge</td>
<td>0.8</td>
<td>1.1</td>
<td>V</td>
</tr>
<tr>
<td>$V_{IL\ TH\ HYS}$</td>
<td>Threshold for detecting low EN</td>
<td>$2$ V ≤ $V_{IN}$ ≤ $15$ V, falling edge</td>
<td>0.4</td>
<td>0.6</td>
<td></td>
</tr>
<tr>
<td>$I_{IN}$</td>
<td>Input bias current, EN</td>
<td>$EN = GND$ or $V_{IN}$</td>
<td>0</td>
<td>50</td>
<td>nA</td>
</tr>
<tr>
<td>POWER SWITCH</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$R_{DS(ON)}$</td>
<td>High-side MOSFET ON-resistance</td>
<td>$V_{IN} = 3.6$ V</td>
<td>2.3</td>
<td>3.4</td>
<td>Ω</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$V_{IN} = 8$ V</td>
<td>1.75</td>
<td>2.5</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Low-side MOSFET ON-resistance</td>
<td>$V_{IN} = 3.6$ V</td>
<td>1.3</td>
<td>2.5</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>$V_{IN} = 8$ V</td>
<td>1.2</td>
<td>1.75</td>
<td></td>
</tr>
<tr>
<td>$I_{LIMF}$</td>
<td>Forward current limit MOSFET high-side</td>
<td>$V_{IN} = 8$ V, open loop</td>
<td>200</td>
<td>250</td>
<td>400</td>
</tr>
<tr>
<td>$T_{SD}$</td>
<td>Thermal shutdown</td>
<td>Increasing junction temperature</td>
<td>150</td>
<td></td>
<td>°C</td>
</tr>
<tr>
<td></td>
<td>Thermal shutdown hysteresis</td>
<td>Decreasing junction temperature</td>
<td>20</td>
<td></td>
<td>°C</td>
</tr>
<tr>
<td>REGULATOR</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$I_{On\ min}$</td>
<td>Minimum ON time</td>
<td>$V_{IN} = 3.6$ V, $V_{OUT} = 1.8$ V</td>
<td>700</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>$I_{Off\ min}$</td>
<td>Minimum OFF time</td>
<td>$V_{IN} = 3.6$ V, $V_{OUT} = 1.8$ V</td>
<td>60</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>$V_{REF}$</td>
<td>Internal reference voltage</td>
<td></td>
<td>0.8</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>$V_{FB}$</td>
<td>Feedback FB voltage comparator threshold</td>
<td>Referred to $0.8$-V internal reference</td>
<td>~2.5%</td>
<td>0%</td>
<td>2.5%</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Feedback FB voltage line regulation</td>
<td>$I_{OUT} = 50$ mA (3)</td>
<td>0.04</td>
<td></td>
</tr>
<tr>
<td>$I_{IN}$</td>
<td>Input bias current FB</td>
<td>$V_{FB} = 0.8$ V</td>
<td>0</td>
<td>50</td>
<td>nA</td>
</tr>
</tbody>
</table>

(1) The typical required supply voltage for startup is 2.5 V. The part is functional down to the falling UVLO (undervoltage lockout) threshold.
(2) Shutdown current into VIN pin, includes internal leakage.
(3) $V_{OUT} + 1$ V ≤ $V_{IN}$ : $V_{OUT} ≤ 5.5$ V.
Electrical Characteristics (continued)

$V_{IN} = 8$ V, $V_{OUT} = 1.8$ V, $EN = V_{IN}$, $T_J = -40^\circ$C to 85°C, typical values are at $T_J = 25^\circ$C (unless otherwise noted), $C_{IN} = 4.7$ µF, $L = 22$ µH, $C_{OUT} = 4.7$ µF

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>$I_{Start}$</td>
<td>Regulator start-up time</td>
<td></td>
<td></td>
<td></td>
<td>µs</td>
</tr>
<tr>
<td></td>
<td>Time from active EN to device starts switching, $V_{IN} = 2.6$ V</td>
<td>50</td>
<td>150</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$I_{Ramp}$</td>
<td>Output voltage ramp time</td>
<td></td>
<td></td>
<td></td>
<td>µs</td>
</tr>
<tr>
<td></td>
<td>Time to ramp up $V_{OUT} = 1.8$ V, no load (4)</td>
<td>120</td>
<td>300</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$I_{Lk,SW}$</td>
<td>Leakage current into SW pin</td>
<td></td>
<td></td>
<td></td>
<td>µA</td>
</tr>
<tr>
<td></td>
<td>$V_{OUT} = V_{IN} = V_{SW} = 1.8$ V, $EN = GND$, device in shutdown mode</td>
<td>1</td>
<td>1.5</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**POWER GOOD OUTPUT (TPS62120)**

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{THPG}$</td>
<td>Power good threshold voltage</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Rising $V_{FB}$ feedback voltage</td>
<td>93%</td>
<td>95%</td>
<td>97%</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Falling $V_{FB}$ feedback voltage</td>
<td>87%</td>
<td>90%</td>
<td>93%</td>
<td></td>
</tr>
<tr>
<td>$V_{OL}$</td>
<td>Output low voltage</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Current into PG pin $I = 500$ µA, $V_{OUT} &gt; 1.5$ V</td>
<td>165</td>
<td></td>
<td></td>
<td>mV</td>
</tr>
<tr>
<td></td>
<td>Current into PG pin $I = 100$ µA, $1.2$ V $&lt; V_{OUT} &lt; 1.5$ V</td>
<td>50</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$V_{HI}$</td>
<td>Output high voltage</td>
<td></td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td></td>
<td>Open drain output, external pull up resistor</td>
<td>5.5</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$I_{LKG}$</td>
<td>Leakage current into PG pin</td>
<td></td>
<td></td>
<td></td>
<td>nA</td>
</tr>
<tr>
<td></td>
<td>$V_{PG} = 1.8$ V, $EN = high$, $FB = 0.85$ V</td>
<td>0</td>
<td>50</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Leakage into VOUT pin</td>
<td></td>
<td></td>
<td></td>
<td>nA</td>
</tr>
<tr>
<td></td>
<td>$V_{OUT} = 1.8$ V</td>
<td>0</td>
<td>50</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$T_{PGDL}$</td>
<td>Internal power good comparator delay time</td>
<td></td>
<td></td>
<td></td>
<td>µs</td>
</tr>
<tr>
<td></td>
<td>$V_{OUT} = 1.8$ V</td>
<td>2</td>
<td>5</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**SGND OPEN DRAIN OUTPUT (TPS62120)**

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>$R_{DS(ON)}$</td>
<td>NMOS drain source resistance</td>
<td></td>
<td></td>
<td></td>
<td>Ω</td>
</tr>
<tr>
<td></td>
<td>SGND $= 1.8$ V, $V_{IN} = 2$ V</td>
<td>370</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$I_{LKG}$</td>
<td>Leakage current into SGND pin</td>
<td></td>
<td></td>
<td></td>
<td>nA</td>
</tr>
<tr>
<td></td>
<td>$EN = V_{IN}$, SGND $= 1.8$ V</td>
<td>0</td>
<td>50</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

(4) Maximum value not production tested.
7.6 Typical Characteristics

Figure 1. Low-Side Switch Resistance $R_{DS(ON)}$ vs $V_{IN}$

Figure 2. Quiescent Current vs $V_{IN}$

Figure 3. Shutdown Current vs $V_{IN}$

Figure 4. Switch Frequency vs Output Current $I_{OUT}$ ($V_{OUT} = 2$ V)

Figure 5. Switch Frequency vs Output Current $I_{OUT}$ ($V_{OUT} = 3.3$ V)

Figure 6. Switch Frequency vs Output Current $I_{OUT}$ ($V_{OUT} = 5$ V)
8 Detailed Description

8.1 Overview
The TPS6212x synchronous step-down converter family uses an unique hysteretic PFM/PWM controller scheme which enables switching frequencies of up to 800 kHz, excellent transient response and AC load regulation at operation with small output capacitors.

At high load currents the converter operates in quasi fixed frequency pulse width modulation (PWM) mode operation and at light loads in pulse frequency modulation (PFM) mode to maintain highest efficiency over the full load current range. In PFM mode, the device generates a single switch pulse to ramp the inductor current and charge the output capacitor, followed by a sleep period where most of the internal circuits are shutdown to achieve a quiescent current of typically 10 µA. During this time, the load current is supported by the output capacitor. The duration of the sleep period depends on the load current and the inductor peak current.

A significant advantage of TPS6212x compared to other hysteretic controller topologies is its excellent DC and AC load regulation capability in combination with low output voltage ripple over the entire load range which makes this part well suited for audio and RF applications.

8.2 Functional Block Diagram

---

Note 1: Function available in TPS62120

---
8.3 Feature Description

8.3.1 Undervoltage Lockout

The undervoltage lockout circuit prevents the device from misoperation at low input voltages. The circuit prevents the converter from turning on the high-side MOSFET switch or low-side MOSFET under undefined conditions. The UVLO threshold is set to 2.5 V typical for rising \( V_{IN} \) and 1.85 V typical for falling \( V_{IN} \). The hysteresis between rising and falling UVLO threshold ensures proper start-up even with high-impedance sources. Fully functional operation is permitted for an input voltage down to the falling UVLO threshold level. The converter starts operation again once the input voltage trips the rising UVLO threshold level.

8.3.2 Enable and Shutdown

The device starts operation when EN pin is set high and the input voltage \( V_{IN} \) has tripped the UVLO threshold for rising \( V_{IN} \). It starts switching after the regulator start-up time \( t_{\text{Start}} \) of typically 50 \( \mu \)s has expired and enters the soft start as previously described. For proper operation, the EN pin must be terminated and must not be left floating.

EN pin low forces the device into shutdown, with a shutdown quiescent current of typically 0.3 \( \mu \)A.

In this mode, the high-side and low-side MOSFET switches as well as the entire internal-control circuitry are switched off.

In TPS62120 the internal N-MOSFET at pin SGND is activated and connects SGND to GND.

8.3.3 Power Good Output

The Power Good Output is an open-drain output available in TPS62120. The circuit is active once the device is enabled. It is driven by an internal comparator connected to the FB voltage and internal reference. The PG output provides a high level (open-drain high impedance) once the feedback voltage exceeds typical 95% of its nominal value. The PG output is driven to low level once the feedback voltage falls below typical 90% of its nominal value. The PG output is high (high impedance) with an internal delay of typically 2 \( \mu \)s. A pullup resistor is needed to generate a high level and limit the current into the PG pin to 0.5 mA. The PG pin can be connected through pullup resistors to a voltage up to 5.5 V.

The PG output is pulled low if the device is enabled but the input voltage is below the UVLO threshold or the device is turned into shutdown mode.

8.3.4 SGND Open-Drain Output

This is an NMOS open-drain output with a typical \( R_{DS(ON)} \) of 370 \( \Omega \) and can be used to discharge the output capacitor. The internal NMOS connects SGND pin to GND once the device is in shutdown mode or \( V_{IN} \) falls below the UVLO threshold during operation. SGND becomes high impedance once the device is enabled and \( V_{IN} \) is above the UVLO threshold. If SGND is connected to the output, the output capacitor is discharged through SGND.

8.3.5 Thermal Shutdown

As soon as the junction temperature, \( T_J \), exceeds 150°C (typical) the device goes into thermal shutdown. In this mode, the high-side and low-side MOSFETs are turned off. The device continues its operation when the junction temperature falls below the thermal shutdown hysteresis.
8.4 Device Functional Modes

8.4.1 Soft Start

The TPS6212x has an internal soft-start circuit which controls the ramp-up of the output voltage and limits the inrush current during start-up. This limits input voltage drop when a battery or a high-impedance power source is connected to the input of the converter.

The soft-start system generates a monotonic ramp up of the output voltage with a ramp of typically 15 mV/µs and reaches an output voltage of 1.8 V in typically 170 µs after EN pin was pulled high. The TPS6212x is able to start into a prebiased output capacitor. The converter starts with the applied bias voltage and ramps the output voltage to its nominal value.

During start-up the device can provide an output current of half of the high-side MOSFET switch current limit \( I_{\text{LIMF}} \). Large output capacitors and high load currents may exceed the current capability of the device during start-up. In this case the start-up ramp of the output voltage will be slower.

8.4.2 Main Control Loop

The feedback comparator monitors the voltage on the FB pin and compares it to an internal 800-mV reference voltage.

The feedback comparator trips once the FB voltage falls below the reference voltage. A switching pulse is initiated and the high-side MOSFET switch is turned on. The switch remains turned on at least for the minimum on-time \( T_{\text{ONmin}} \) of typical 700 ns until the feedback voltage is above the reference voltage or the inductor current reaches the high-side MOSFET switch current limit \( I_{\text{LIMF}} \). Once the high-side MOSFET switch turns off, the low-side MOSFET switch is turned on and the inductor current ramps down. The switch is turned on at least for the minimum off time \( T_{\text{OFFmin}} \) of typically 60 ns. The low-side MOSFET switch stays turned on until the FB voltage falls below the internal reference and trips the FB comparator again. This will turn on the high-side MOSFET switch for a new switching cycle.

If the feedback voltage stays above the internal reference the low-side MOSFET switch is turned on until the zero current comparator trips and indicates that the inductor current has ramped down to zero. In this case, the load current is much lower than the average inductor current provided during one switching cycle. The regulator turns the low-side and high-side MOSFET switches off (high impedance state) and enters a sleep cycle with reduced quiescent current of typically 10 uA until the output voltage falls below the internal reference voltage and the feedback comparator trips again. This is called PFM mode and the switching frequency depends on the load current, input voltage, output voltage and the external inductor value.

Once the high-side switch current limit comparator has tripped its threshold of \( I_{\text{LIMF}} \), the high-side MOSFET switch is turned off and the low-side MOSFET switch is turned on until the inductor current has ramped down to zero.

The minimum on time \( T_{\text{ONmin}} \) for a single pulse can be estimated to:

\[
T_{\text{ON}} = \frac{V_{\text{OUT}}}{V_{\text{IN}}} \times 1.3 \, \mu\text{s}
\]  

Therefore the peak inductor current in PFM mode is approximately:

\[
I_{\text{LPFMpeak}} = \left( \frac{V_{\text{IN}} - V_{\text{OUT}}}{L} \right) \times T_{\text{ON}}
\]  

The transition from PFM mode to PWM mode operation and back occurs at a load current of approximately 0.5 \( \times I_{\text{LPFMpeak}} \).

With:

- \( T_{\text{ON}} = \) High-side MOSFET switch on time [µs]
- \( V_{\text{IN}} = \) Input voltage [V]
- \( V_{\text{OUT}} = \) Output voltage [V]
- \( L = \) Inductance [µH]
- \( I_{\text{LPFMpeak}} = \) PFM inductor peak current [mA]

The maximum switch frequency can be estimated to:
Device Functional Modes (continued)

\[ f_{SW_{max}} \approx \frac{1}{1.3 \, \mu s} = 770 \, kHz \]  

(3)

8.4.3 100% Duty Cycle Low-Dropout Operation

The device will increase the on time of the high-side MOSFET switch once the input voltage comes close to the output voltage in order to keep the output voltage in regulation. This will reduce the switch frequency.

With further decreasing input voltage \( V_{IN} \) the high-side MOSFET switch is turned on completely. In this case the converter provides a low input-to-output voltage difference. This is particularly useful in applications with widely variable supply voltage to achieve longest operation time by taking full advantage of the whole supply voltage span.

The minimum input voltage to maintain regulation depends on the load current and output voltage, and can be calculated as:

\[ V_{in_{min}} = V_{out_{max}} + I_{out_{max}} \times (R_{DS(ON)_{max}} + R_L) \]

where

- \( I_{OUT_{max}} \) = maximum output current
- \( R_{DS(ON)_{max}} \) = maximum P-channel switch \( R_{DS(ON)} \)
- \( R_L \) = DC resistance of the inductor
- \( V_{OUT_{max}} \) = nominal output voltage plus maximum output voltage tolerance

(4)

8.4.4 Short-Circuit Protection

The TPS6212x integrates a high-side MOSFET switch current limit \( I_{LIMF} \) to protect the device against short circuit. The current in the high-side MOSFET switch is monitored by current limit comparator and once the current reaches the limit of \( I_{LIMF} \), the high-side MOSFET switch is turned off and the low-side MOSFET switch is turned on to ramp down the inductor current. The high-side MOSFET switch is turned on again once the zero current comparator trips and the inductor current has become zero. In this case, the output current is limited to half of the high-side MOSFET switch current limit \( 0.5 \times I_{LIMF} \).
9 Application and Implementation

NOTE
Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI’s customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information
The TPS6212x device is a highly efficient synchronous step-down DC-DC converter optimized for low-power applications. With its wide input voltage range, the device also fits for energy harvesting applications to convert electrical power from electromagnetic transducers.

9.2 Typical Applications

9.2.1 TPS62120 With Open-Drain Output

9.2.1.1 Design Requirements
The device operates over an input voltage range from 2 V to 15V. The output voltage is adjustable using an external feedback divider network.

The design guideline provides a component selection to operate the device within the Recommended Operating Conditions.

9.2.1.2 Detailed Design Procedure

9.2.1.2.1 Output Voltage Setting
The output voltage can be calculated to:

\[ V_{\text{OUT}} = V_{\text{REF}} \times \left( 1 + \frac{R_1}{R_2} \right) \]

with an internal reference voltage \( V_{\text{REF}} \) typical 0.8 V

\[ R_1 = \left( \frac{V_{\text{OUT}}}{V_{\text{REF}}} - 1 \right) \times R_2 \]  

(5)

To minimize the current through the feedback divider network, \( R_2 \) should be within the range of 82 kΩ to 360 kΩ. The sum of \( R_1 \) and \( R_2 \) should not exceed approximately 1 MΩ, to keep the network robust against noise. An external feedforward capacitor \( C_{\text{ff}} \) is required for optimum regulation performance. \( R_1 \) and \( C_{\text{ff}} \) places a zero in the feedback loop.

Figure 7. Standard Circuit for TPS62120 With Open-Drain Output

L = 18 µH LPS3015 Coilcraft
22 µH LQH3NPN Murata
\( C_{\text{IN}} \): 4.7µF GRM21B series X5R (0805size) 25V Murata
\( C_{\text{OUT}} \): 4.7µF GRM188 series X5R (0603size) 6.3V Murata
Typical Applications (continued)

\[ \frac{1}{f_L} = \frac{1}{2 \times \pi \times R_1 \times C_{\text{ff}}} = 25 \text{ kHz} \]  

(6)

The value for \( C_{\text{ff}} \) can be calculated as:

\[ C_{\text{ff}} = \frac{1}{2 \times \pi \times R_1 \times 25 \text{ kHz}} \]  

(7)

Table 1 shows a selection of suggested values for the feedback divider network for most common output voltages.

<table>
<thead>
<tr>
<th>VOLTAGE SETTING (V)</th>
<th>3.06</th>
<th>3.29</th>
<th>2.00</th>
<th>1.80</th>
<th>1.20</th>
<th>5.00</th>
</tr>
</thead>
<tbody>
<tr>
<td>( R_1 ) [kΩ]</td>
<td>510</td>
<td>560</td>
<td>360</td>
<td>300</td>
<td>180</td>
<td>430</td>
</tr>
<tr>
<td>( R_2 ) [kΩ]</td>
<td>180</td>
<td>180</td>
<td>240</td>
<td>240</td>
<td>360</td>
<td>82</td>
</tr>
<tr>
<td>( C_{\text{ff}} ) [pF]</td>
<td>15</td>
<td>22</td>
<td>22</td>
<td>22</td>
<td>27</td>
<td>15</td>
</tr>
</tbody>
</table>

9.2.1.2.2 Output Filter Design (Inductor and Output Capacitor)

The TPS6212x operates with effective inductance values in the range of 10 µH to 33 µH and with effective output capacitance in the range of 1 µF to 33 µF. The device is optimized to operate for an output filter of \( L = 22 \mu \text{H} \) and \( C_{\text{OUT}} = 4.7 \mu \text{F} \). Larger or smaller inductor and capacitor values can be used to optimize the performance of the device for specific operation conditions. For more details, see Checking Loop Stability.

9.2.1.2.3 Inductor Selection

The inductor value affects its peak-to-peak ripple current, the PWM-to-PFM transition point, the output voltage ripple, and the efficiency. The selected inductor has to be rated for its DC resistance and saturation current. The inductor ripple current (\( \Delta I_L \)) decreases with higher inductance and increases with higher \( V_{\text{IN}} \) or \( V_{\text{OUT}} \) and can be estimated according to Equation 8.

\[ \Delta I_L = \frac{(V_{\text{IN}} - V_{\text{OUT}})}{L} \times T_{\text{ON}} \]  

(8)

\[ I_{\text{Lmax}} = I_{\text{outmax}} + \frac{\Delta I_L}{2} \]  

where

\begin{itemize}
  \item \( T_{\text{ON}} = \) See Equation 1
  \item \( L = \) Inductor value
  \item \( \Delta I_L = \) Peak-to-peak inductor ripple current
  \item \( I_{\text{Lmax}} = \) Maximum inductor current
\end{itemize}

In DC-DC converter applications, the efficiency is essentially affected by the inductor AC resistance (that is, quality factor) and by the inductor DCR value. To achieve high efficiency operation, care should be taken in selecting inductors featuring a quality factor above 25 at the switching frequency. Increasing the inductor value produces lower RMS currents, but degrades transient response. For a given physical inductor size, increased inductance usually results in an inductor with lower saturation current.

The total losses of the coil consist of both the losses in the DC resistance (\( R_{\text{(DC)}} \)) and the following frequency-dependent components:

- the losses in the core material (magnetic hysteresis loss, especially at high switching frequencies)
- additional losses in the conductor from the skin effect (current displacement at high frequencies)
- magnetic field losses of the neighboring windings (proximity effect)
• radiation losses

The following inductor series from different suppliers have been used with the TPS6212x converters.

### Table 2. List of Inductors

<table>
<thead>
<tr>
<th>INDUCTANCE (µH)</th>
<th>DIMENSIONS (mm³)</th>
<th>INDUCTOR TYPE</th>
<th>SUPPLIER</th>
</tr>
</thead>
<tbody>
<tr>
<td>22</td>
<td>3 × 3 × 1.5</td>
<td>LQH3NPN</td>
<td>Murata</td>
</tr>
<tr>
<td>18/22</td>
<td>3 × 3 × 1.5</td>
<td>LPS3015</td>
<td>Coilcraft</td>
</tr>
</tbody>
</table>

#### 9.2.1.2.4 Output Capacitor Selection

The unique hysteretic PFM/PWM control scheme of the TPS6212x allows the use of ceramic capacitors. Ceramic capacitors with low ESR values have the lowest output voltage ripple and are recommended. The output capacitor requires either an X7R or X5R dielectric. Y5V and Z5U dielectric capacitors, aside from their wide variation in capacitance over temperature, become resistive at high frequencies.

At light load currents the converter operates in power save mode and the output voltage ripple is dependent on the output capacitor value and the PFM peak inductor current. Higher output capacitor values minimize the voltage ripple in PFM mode and tighten DC output accuracy in PFM mode.

#### 9.2.1.2.5 Input Capacitor Selection

Because of the nature of the buck converter having a pulsating input current, a low ESR input capacitor is required for best input voltage filtering and minimizing the interference with other circuits caused by high input voltage spikes. For most applications a 4.7 µF to 10 µF ceramic capacitor is recommended. The voltage rating and DC bias characteristic of ceramic capacitors need to be considered. The input capacitor can be increased without any limit for better input voltage filtering.

For specific applications like energy harvesting a tantalum or tantalum polymer capacitor can be used to achieve a specific DC-DC converter input capacitance. Tantalum capacitors provide much better DC bias performance compared to ceramic capacitors. In this case a 1-µF or 2.2-µF ceramic capacitor should be used in parallel to provide low ESR.

Take care when using only small ceramic input capacitors. When a ceramic capacitor is used at the input and the power is being supplied through long wires, such as from a wall adapter, a load step at the output or \( V_{\text{IN}} \) step on the input can induce large ringing at the \( V_{\text{IN}} \) pin. This ringing can couple to the output and be mistaken as loop instability or could even damage the part by exceeding the maximum ratings.

Table 3 shows a list of input and output capacitors.

### Table 3. List of Capacitors

<table>
<thead>
<tr>
<th>CAPACITANCE (µF)</th>
<th>SIZE</th>
<th>CAPACITOR TYPE</th>
<th>USAGE</th>
<th>SUPPLIER</th>
</tr>
</thead>
<tbody>
<tr>
<td>4.7</td>
<td>0603</td>
<td>GRM188 series 6.3 V X5R</td>
<td>( C_{\text{OUT}} )</td>
<td>Murata</td>
</tr>
<tr>
<td>2.2</td>
<td>0603</td>
<td>GRM188 series 6.3 V X5R</td>
<td>( C_{\text{OUT}} )</td>
<td>Murata</td>
</tr>
<tr>
<td>4.7</td>
<td>0805</td>
<td>GRM21Bseries 25 V X5R</td>
<td>( C_{\text{IN}} )</td>
<td>Murata</td>
</tr>
<tr>
<td>10</td>
<td>0805</td>
<td>GRM21Bseries 16 V X5R</td>
<td>( C_{\text{IN}} )</td>
<td>Murata</td>
</tr>
<tr>
<td>8.2</td>
<td>B2 (3.5 × 2.8 × 1.9)</td>
<td>20TQC8R2M (20 V)</td>
<td>( C_{\text{IN}} )</td>
<td>Sanyo</td>
</tr>
</tbody>
</table>

#### 9.2.1.2.6 Checking Loop Stability

The first step of circuit and stability evaluation is to look from a steady-state perspective at the following signals:

- Switching node, \( \text{SW} \)
- Inductor current, \( I_L \)
- Output ripple voltage, \( V_{\text{O(AC)}} \)

These are the basic signals that need to be measured when evaluating a switching converter. When the switching waveform shows large duty cycle jitter or the output voltage or inductor current shows oscillations, the regulation loop may be unstable. This is often a result of board layout and/or L-C combination.
As a next step in the evaluation of the regulation loop, the load transient response is tested. During application of
the load transient and the turn on of the high-side MOSFET switch, the output capacitor must supply all of
the current required by the load. \( V_{OUT} \) immediately shifts by an amount equal to \( \Delta I_{LOAD} \times \text{ESR} \), where ESR is the
effective series resistance of \( C_{OUT} \). \( \Delta I_{LOAD} \) begins to charge or discharge \( C_{OUT} \) generating a feedback error
signal used by the regulator to return \( V_{OUT} \) to its steady-state value. The results are most easily interpreted when
the device operates in PWM mode.

During this recovery time, \( V_{OUT} \) can be monitored for settling time, overshoot or ringing that helps judge the
converter’s stability. Without any ringing, the loop has usually more than 45° of phase margin. Because the
damping factor of the circuitry is directly related to several resistive parameters (for example, MOSFET \( R_{DS(on)} \))
which are temperature dependent, the loop stability analysis should be done over the input voltage range, load
current range, and temperature range

### 9.2.1.3 Application Curves

All graphs have been generated using the circuit as shown in Figure 7 unless otherwise noted.
Figure 12. Efficiency vs Output Current $I_{OUT}$ ($V_{OUT} = 3\, V$)

Figure 13. Efficiency vs Input Voltage $V_{IN}$ ($V_{OUT} = 3\, V$)

Figure 14. Efficiency vs Output Current $I_{OUT}$ ($V_{OUT} = 2\, V$)

Figure 15. Efficiency vs Input Voltage $V_{IN}$ ($V_{OUT} = 2\, V$)

Figure 16. Efficiency vs Output Current $I_{OUT}$ ($V_{OUT} = 1.2\, V$)

Figure 17. Efficiency vs Input Voltage $V_{IN}$ ($V_{OUT} = 1.2\, V$)
Figure 18. 3.0-V Output Voltage DC Regulation

Figure 19. 2.0-V Output Voltage DC Regulation

Figure 20. $V_{OUT}$ 2.0-V Output Ripple Voltage Peak to Peak

Figure 21. Typical Operation $I_{OUT}$ 60mA

Figure 22. Typical Operation $I_{OUT}$ 10mA

Figure 23. Line Transient Response for 3-V Output Voltage
Figure 30. Startup $V_{OUT} = 3\, \text{V}$

Figure 31. Power Good Output During Startup

Figure 32. Startup $V_{OUT} = 1.8\, \text{V}$

Figure 33. Output Overload Protection

Figure 34. Input Voltage Ramp Up/Down

Figure 35. Startup From a High-Impedance Source
9.2.2 Standard Circuit for TPS62122

Beside the power good open drain output (PG pin) and the open drain output for output discharge (SGND pin) the TPS62122 provides the same functionality as the TPS62120.

![Diagram of Standard Circuit for TPS62122](image)

**L = 18 μH LPS3015 Coilcraft**
**22 μH LQH3NPN Murata**
**C_{in}: 4.7 μF GRM21B series X5R (0805size) 25V Murata**
**C_{out}: 4.7 μF GRM188 series X5R (0603size) 6.3V Murata**

*Figure 36. Standard Circuit for TPS62122*

9.3 System Examples

The TPS6212x is operating with a wide input voltage range from 2 V to 15 V. An open-drain power good output and an additional SGND pin is available in the TPS62120 for output voltage regulation and to discharge the output capacitor.

9.3.1 TPS62120 1.8-V Output Voltage Configuration

![Diagram of TPS62120 1.8-V Output Voltage Configuration](image)

*Figure 37. TPS62120 1.8-V Output Voltage Configuration*
System Examples (continued)

9.3.2 TPS62120 3.06-V Output Voltage Configuration

9.3.3 TPS62122 2.0-V Output Voltage Configuration

9.3.4 TPS62120 1.8-V VOUT Configuration Powered From a High-Impedance Source

Figure 38. TPS62120 3.06-V Output Voltage Configuration

Figure 39. TPS62122 2.0-V Output Voltage Configuration

Figure 40. TPS62120 1.8-V VOUT Configuration Powered From a High-Impedance Source
10 Power Supply Recommendations

The TPS6212x device family has no special requirements for its input power supply. The output current of the input power supply needs to be rated according to the supply voltage, output voltage, and output current of the TPS6212x.

11 Layout

11.1 Layout Guidelines

As for all switching power supplies, the layout is an important step in the design. Proper function of the device demands careful attention to PCB layout. Care must be taken in board layout to get the specified performance. If the layout is not carefully done, the regulator could show poor line and/or load regulation, stability issues, as well as EMI problems. It is critical to provide a low inductance, impedance ground path. Therefore, use wide and short traces for the main current paths. The input capacitor should be placed as close as possible to the IC pins as well as the inductor and output capacitor.

Use a common Power GND node and a different node for the signal GND to minimize the effects of ground noise. Keep the common path to the GND PIN, which returns the small signal components and the high current of the output capacitors as short as possible to avoid ground noise. The FB divider network and the VOUT line must be connected to the output capacitor. The VOUT pin of the converter should be connected through a short trace to the output capacitor. The FB line must be routed away from noisy components and traces (for example, SW line).

11.2 Layout Examples

![Figure 41. PCB Layout - DCN Package](image-url)

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**Figure 41. PCB Layout - DCN Package**
Figure 42. PCB Layout - DRV Package
12 Device and Documentation Support

12.1 Device Support

12.1.1 Third-Party Products Disclaimer

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12.2 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

<table>
<thead>
<tr>
<th>Parts</th>
<th>Product Folder</th>
<th>Sample &amp; Buy</th>
<th>Technical Documents</th>
<th>Tools &amp; Software</th>
<th>Support &amp; Community</th>
</tr>
</thead>
<tbody>
<tr>
<td>TPS62120</td>
<td>Click here</td>
<td>Click here</td>
<td>Click here</td>
<td>Click here</td>
<td>Click here</td>
</tr>
<tr>
<td>TPS62122</td>
<td>Click here</td>
<td>Click here</td>
<td>Click here</td>
<td>Click here</td>
<td>Click here</td>
</tr>
</tbody>
</table>

12.3 Community Resources

The following links connect to TI community resources. Linked contents are provided “AS IS” by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI’s views; see TI’s Terms of Use.

**TI E2E™ Online Community**  **TI’s Engineer-to-Engineer (E2E) Community.** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

**Design Support**  **TI’s Design Support** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.4 Trademarks

E2E is a trademark of Texas Instruments. All other trademarks are the property of their respective owners.

12.5 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.6 Glossary

**SLYZ022 — TI Glossary.**

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.
### PACKAGING INFORMATION

<table>
<thead>
<tr>
<th>Orderable Device</th>
<th>Status</th>
<th>Package Type</th>
<th>Package Drawing</th>
<th>Pins</th>
<th>Package Qty</th>
<th>Eco Plan</th>
<th>Lead/Ball Finish</th>
<th>MSL Peak Temp</th>
<th>Op Temp (°C)</th>
<th>Device Marking</th>
<th>Samples</th>
</tr>
</thead>
<tbody>
<tr>
<td>TPS62120DCNR</td>
<td>ACTIVE</td>
<td>SOT-23</td>
<td>DCN</td>
<td>8</td>
<td>3000</td>
<td>Green (RoHS &amp; no Sb/Br)</td>
<td>CU NIPDAU</td>
<td>Level-1-260C-UNLIM</td>
<td>-40 to 85</td>
<td>QTX</td>
<td></td>
</tr>
<tr>
<td>TPS62120DCNT</td>
<td>ACTIVE</td>
<td>SOT-23</td>
<td>DCN</td>
<td>8</td>
<td>250</td>
<td>Green (RoHS &amp; no Sb/Br)</td>
<td>CU NIPDAU</td>
<td>Level-1-260C-UNLIM</td>
<td>-40 to 85</td>
<td>QTX</td>
<td></td>
</tr>
<tr>
<td>TPS62122DRVR</td>
<td>ACTIVE</td>
<td>WSON</td>
<td>DRV</td>
<td>6</td>
<td>3000</td>
<td>Green (RoHS &amp; no Sb/Br)</td>
<td>CU NIPDAU</td>
<td>CU NIPDAUAG</td>
<td>Level-2-260C-1 YEAR</td>
<td>-40 to 85</td>
<td>OFZ</td>
</tr>
<tr>
<td>TPS62122DRVT</td>
<td>ACTIVE</td>
<td>WSON</td>
<td>DRV</td>
<td>6</td>
<td>250</td>
<td>Green (RoHS &amp; no Sb/Br)</td>
<td>CU NIPDAU</td>
<td>CU NIPDAUAG</td>
<td>Level-2-260C-1 YEAR</td>
<td>-40 to 85</td>
<td>OFZ</td>
</tr>
</tbody>
</table>

(1) The marketing status values are defined as follows:
- **ACTIVE:** Product device recommended for new designs.
- **LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
- **NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
- **PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
- **OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) **MSL, Peak Temp.** - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) **Lead/Ball Finish** - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.
**TAPE AND REEL INFORMATION**

*All dimensions are nominal.*

<table>
<thead>
<tr>
<th>Device</th>
<th>Package Type</th>
<th>Package Drawing</th>
<th>Pins</th>
<th>SPQ</th>
<th>Reel Diameter (mm)</th>
<th>Reel Width W1 (mm)</th>
<th>A0 (mm)</th>
<th>B0 (mm)</th>
<th>K0 (mm)</th>
<th>P1 (mm)</th>
<th>W (mm)</th>
<th>Pin 1 Quadrant</th>
</tr>
</thead>
<tbody>
<tr>
<td>TPS62120DCNR</td>
<td>SOT-23</td>
<td>DCN</td>
<td>8</td>
<td>3000</td>
<td>179.0</td>
<td>8.4</td>
<td>3.2</td>
<td>1.4</td>
<td>4.0</td>
<td>8.0</td>
<td>Q3</td>
<td></td>
</tr>
<tr>
<td>TPS62120DCNR</td>
<td>SOT-23</td>
<td>DCN</td>
<td>8</td>
<td>3000</td>
<td>180.0</td>
<td>8.4</td>
<td>3.23</td>
<td>1.37</td>
<td>4.0</td>
<td>8.0</td>
<td>Q3</td>
<td></td>
</tr>
<tr>
<td>TPS62120DCNT</td>
<td>SOT-23</td>
<td>DCN</td>
<td>8</td>
<td>250</td>
<td>180.0</td>
<td>8.4</td>
<td>3.23</td>
<td>1.37</td>
<td>4.0</td>
<td>8.0</td>
<td>Q3</td>
<td></td>
</tr>
<tr>
<td>TPS62122DRVR</td>
<td>WSON</td>
<td>DRV</td>
<td>6</td>
<td>3000</td>
<td>178.0</td>
<td>8.4</td>
<td>2.25</td>
<td>1.0</td>
<td>4.0</td>
<td>8.0</td>
<td>Q3</td>
<td></td>
</tr>
<tr>
<td>TPS62122DRVT</td>
<td>WSON</td>
<td>DRV</td>
<td>6</td>
<td>250</td>
<td>179.0</td>
<td>8.4</td>
<td>2.2</td>
<td>1.2</td>
<td>4.0</td>
<td>8.0</td>
<td>Q2</td>
<td></td>
</tr>
<tr>
<td>TPS62122DRVT</td>
<td>WSON</td>
<td>DRV</td>
<td>6</td>
<td>250</td>
<td>178.0</td>
<td>8.4</td>
<td>2.25</td>
<td>1.0</td>
<td>4.0</td>
<td>8.0</td>
<td>Q2</td>
<td></td>
</tr>
</tbody>
</table>
### TAPE AND REEL BOX DIMENSIONS

*All dimensions are nominal*

<table>
<thead>
<tr>
<th>Device</th>
<th>Package Type</th>
<th>Package Drawing</th>
<th>Pins</th>
<th>SPQ</th>
<th>Length (mm)</th>
<th>Width (mm)</th>
<th>Height (mm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>TPS62120DCNR</td>
<td>SOT-23</td>
<td>DCN</td>
<td>8</td>
<td>3000</td>
<td>203.0</td>
<td>203.0</td>
<td>35.0</td>
</tr>
<tr>
<td>TPS62120DCNR</td>
<td>SOT-23</td>
<td>DCN</td>
<td>8</td>
<td>3000</td>
<td>183.0</td>
<td>183.0</td>
<td>20.0</td>
</tr>
<tr>
<td>TPS62120DCNT</td>
<td>SOT-23</td>
<td>DCN</td>
<td>8</td>
<td>250</td>
<td>183.0</td>
<td>183.0</td>
<td>20.0</td>
</tr>
<tr>
<td>TPS62120DCNT</td>
<td>SOT-23</td>
<td>DCN</td>
<td>8</td>
<td>250</td>
<td>203.0</td>
<td>203.0</td>
<td>35.0</td>
</tr>
<tr>
<td>TPS62122DRVR</td>
<td>WSON</td>
<td>DRV</td>
<td>6</td>
<td>3000</td>
<td>205.0</td>
<td>200.0</td>
<td>33.0</td>
</tr>
<tr>
<td>TPS62122DRVT</td>
<td>WSON</td>
<td>DRV</td>
<td>6</td>
<td>250</td>
<td>203.0</td>
<td>203.0</td>
<td>35.0</td>
</tr>
<tr>
<td>TPS62122DRVT</td>
<td>WSON</td>
<td>DRV</td>
<td>6</td>
<td>250</td>
<td>205.0</td>
<td>200.0</td>
<td>33.0</td>
</tr>
</tbody>
</table>
Images above are just a representation of the package family, actual package may vary. Refer to the product data sheet for package details.
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).

5. Vias are optional depending on application, refer to device data sheet. If some or all are implemented, recommended via locations are shown.
NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Package outline exclusive of metal burr & dambar protrusion/intrusion.
D. Package outline inclusive of solder plating.
E. A visual index feature must be located within the Pin 1 index area.
F. Falls within JEDEC MO-178 Variation BA.
G. Body dimensions do not include flash or protrusion. Mold flash and protrusion shall not exceed 0.25 per side.
NOTES:  
A. All linear dimensions are in millimeters.  
B. This drawing is subject to change without notice.  
C. Publication IPC-7351 is recommended for alternate designs.  
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525.  
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.
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