1 Features
- Input Voltage Range $V_{\text{IN}}$ from 2.2V to 5.5V
- Typ. 360nA Quiescent Current
- Up to 90% Efficiency at 10μA Output Current
- Up to 300mA / 400mA Output Current (TPS62740/TPS62742)
- RF Friendly DCS-Control™
- Up to 2 MHz Switching Frequency
- Low Output Ripple Voltage
- 16 Selectable Output Voltages in 100mV Steps between 1.8V to 3.3V
- Automatic Transition to No Ripple 100% Mode
- Slew Rate Controlled Load Switch
- Discharge Function on VOUT / LOAD
- Power Good Output
- Optimized for Operation with a Tiny 2.2μH Inductor and 10μF $C_{\text{OUT}}$
- Total Solution Size <31mm²
- Small 2 x 3 mm² WSON Package

2 Applications
- Bluetooth® Low Energy, RF4CE, Zigbee
- Industrial Metering
- Energy Harvesting

3 Description
The TPS6274x is industry's first step down converter featuring typ. 360nA quiescent current and operating with a tiny 2.2μH inductor and 10μF output capacitor. This new DCS-Control™ based device extends the light load efficiency range below 10μA load currents. TPS62740 supports output currents up to 300mA, TPS62742 up to 400mA. The device operates from rechargeable Li-Ion batteries, Li-primary battery chemistries such as Li-SOCl2, Li-MnO2 and two or three cell alkaline batteries. The input voltage range up to 5.5V allows also operation from a USB port and thin-film solar modules. The output voltage is user selectable by four VSEL pins within a range from 1.8V to 3.3V in 100mV steps. TPS6274x features low output ripple voltage and low noise with a small output capacitor. Once the battery voltage comes close to the output voltage (close to 100% duty cycle) the device enters no ripple 100% mode operation to prevent an increase of output ripple voltage. The device then stops switching and the output is connected to the input voltage. The integrated slew rate controlled load switch provides typ. 0.6Ω on-resistance and can distribute the selected output voltage to a temporarily used sub-system. The TPS6274x is available in a small 12 pin 2 x 3mm² WSON package and supports a total solutions size of 31mm².

4 Typical Application

---

**Device Information**

<table>
<thead>
<tr>
<th>PART NUMBER</th>
<th>PACKAGE</th>
<th>BODY SIZE (NOM)</th>
</tr>
</thead>
<tbody>
<tr>
<td>TPS62740</td>
<td>WSON</td>
<td>3.00 mm × 2.00 mm</td>
</tr>
<tr>
<td>TPS62742</td>
<td>WSON</td>
<td>3.00 mm × 2.00 mm</td>
</tr>
</tbody>
</table>

(1) For all available packages, see the orderable addendum at the end of the datasheet.

---

An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.
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5 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (November 2013) to Revision B

| Added TPS62742 device | 1 |
| Added efficiency graph, Figure 11 | 15 |
6 Device Comparison Table

<table>
<thead>
<tr>
<th>$T_A$</th>
<th>PART NUMBER</th>
<th>OUTPUT VOLTAGE SETTING VSEL 1 - 4</th>
<th>OUTPUT CURRENT [mA]</th>
<th>PACKAGE MARKING</th>
</tr>
</thead>
<tbody>
<tr>
<td>$-40^\circ$C to $85^\circ$C</td>
<td>TPS62740</td>
<td>1.8V to 3.3V in 100mV steps</td>
<td>300mA</td>
<td>62740</td>
</tr>
<tr>
<td></td>
<td>TPS62741(1)</td>
<td>1.3V to 2.8V in 100mV steps</td>
<td>300mA</td>
<td>/-/</td>
</tr>
<tr>
<td></td>
<td>TPS62742</td>
<td>1.8V to 3.3V in 100mV steps</td>
<td>400mA</td>
<td>62742</td>
</tr>
</tbody>
</table>

(1) Device option, contact TI for more details

7 Pin Configuration and Functions

Vin 1 Power supply pin. Connect this pin close to the VIN terminal of the input capacitor. A ceramic capacitor of 4.7µF is required.

SW 2 This is the switch pin and is connected to the internal MOSFET switches. Connect the inductor to this terminal.

GND 3 GND supply pin. Connect this pin close to the GND terminal of the input and output capacitor.

CTRL 4 This pin controls the output LOAD pin. With CTRL = low, the output LOAD is disabled. This pin must be terminated.

VOUT 5 Feedback pin for the internal feedback divider network and regulation loop. An internal load switch is connected between this pin and the LOAD pin. Connect this pin directly to the output capacitor with a short trace.

LOAD 6 This output is controlled by the CTRL Pin. With CTRL high, an internal load switch connects the LOAD pin to the VOUT pin. The LOAD pin allows to connect / disconnect other system components to the output of the DC/DC converter. This pin is pulled to GND with CTRL pin = low. The LOAD pin features a soft switching. If not used, leave the pin open.

PG 7 Power good open drain output. This pin is high impedance to indicate "Power Good". Connect a external pull up resistor to generate a "high" level. If not used, this pin can be left open.

VSEL4 8 Output voltage selection pins. See Table 1 for $V_{OUT}$ selection. These pins must be terminated and can be changed during operation.

VSEL3 9

VSEL2 10

VSEL1 11

EN 12 High level enables the devices, low level turns the device into shutdown mode. This pin must be terminated.

EXPOSED THERMAL PAD NC Not electrically connected to the IC, but must be soldered. Connect this pad to GND and use it as a central GND plane.
Table 1. Output Voltage Setting

<table>
<thead>
<tr>
<th>Device</th>
<th>VOUT</th>
<th>VSEL 4</th>
<th>VSEL 3</th>
<th>VSEL 2</th>
<th>VSEL 1</th>
</tr>
</thead>
<tbody>
<tr>
<td>1.8</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>1.9</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>2.0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>2.1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>2.2</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>2.3</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>2.4</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>2.5</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>2.6</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>2.7</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>2.8</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>2.9</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>3.0</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>3.1</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>3.2</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>3.3</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
</tr>
</tbody>
</table>

8 Specifications

8.1 Absolute Maximum Ratings\(^{(1)}\)

Over operating free-air temperature range (unless otherwise noted)

<table>
<thead>
<tr>
<th>Pin voltage(^{(2)})</th>
<th>MIN</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>VIN</td>
<td>–0.3</td>
<td>6</td>
<td>V</td>
</tr>
<tr>
<td>SW (^{(3)})</td>
<td>–0.3</td>
<td>VIN +0.3V</td>
<td>V</td>
</tr>
<tr>
<td>EN, CTRL, VSEL1-4</td>
<td>–0.3</td>
<td>VIN +0.3V</td>
<td>V</td>
</tr>
<tr>
<td>PG</td>
<td>–0.3</td>
<td>VIN +0.3V</td>
<td>V</td>
</tr>
<tr>
<td>VOUT, LOAD</td>
<td>–0.3</td>
<td>3.7</td>
<td>V</td>
</tr>
<tr>
<td>PG pin I(_G)</td>
<td></td>
<td>10</td>
<td>mA</td>
</tr>
<tr>
<td>Maximum operating junction temperature, T(_J)</td>
<td>–40</td>
<td>150</td>
<td>°C</td>
</tr>
</tbody>
</table>

\(^{(1)}\) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute–maximum–rated conditions for extended periods may affect device reliability.

\(^{(2)}\) All voltage values are with respect to network ground terminal GND.

\(^{(3)}\) The MAX value VIN +0.3V applies for applicative operation (device switching), DC voltage applied to this pin may not exceed 4V

8.2 Handling Ratings

<table>
<thead>
<tr>
<th>Parameter</th>
<th>MIN</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>T(_{stg})</td>
<td>–65</td>
<td>150</td>
<td>°C</td>
</tr>
<tr>
<td>V(_{ESD}) Electrostatic discharge (^{(1)}) Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(^{(1)})</td>
<td></td>
<td>2000</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td></td>
<td>1000</td>
<td></td>
</tr>
</tbody>
</table>

\(^{(1)}\) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. The human body model is a 100-pF capacitor discharged through a 1.5-k\(\Omega\) resistor into each pin.

\(^{(2)}\) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.
8.3 Recommended Operating Conditions

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>MIN</th>
<th>NOM</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>( V_{IN} ) Supply voltage ( V_{IN} ) (^{(1)} )</td>
<td>2.2</td>
<td>5.5</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>( I_{OUT} + I_{LOAD} ) Device output current (sum of ( I_{OUT} ) and ( I_{LOAD} ))</td>
<td>( V_{OUTnom} + 0.7V \leq V_{IN} \leq 5.5V )</td>
<td>TPS62740</td>
<td>300</td>
<td>mA</td>
</tr>
<tr>
<td></td>
<td>( 3V \leq V_{IN}, V_{OUTnom} + 0.7V \leq V_{IN} \leq 5.5V )</td>
<td>TPS62742</td>
<td>400</td>
<td>mA</td>
</tr>
<tr>
<td></td>
<td>( V_{OUTnom} \leq V_{IN} \leq V_{OUTnom} + 0.7V )</td>
<td>TPS62740</td>
<td>100</td>
<td>mA</td>
</tr>
<tr>
<td>( I_{LOAD} ) Load current (current from LOAD pin)</td>
<td>100</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>( L ) Inductance</td>
<td>1.5</td>
<td>2.2</td>
<td>3.3</td>
<td>( \mu H )</td>
</tr>
<tr>
<td>( C_{OUT} ) Output capacitance connected to VOUT pin (not including LOAD pin)</td>
<td>22</td>
<td></td>
<td></td>
<td>( \mu F )</td>
</tr>
<tr>
<td>( C_{LOAD} ) Capacitance connected to LOAD pin</td>
<td>10</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>( T_J ) Operating junction temperature range</td>
<td>-40</td>
<td>125</td>
<td>°C</td>
<td></td>
</tr>
<tr>
<td>( T_A ) Ambient temperature range</td>
<td>-40</td>
<td>85</td>
<td>°C</td>
<td></td>
</tr>
</tbody>
</table>

(1) The minimum required supply voltage for startup is 2.15V (undervoltage lockout threshold \( V_{TH_{UVLO}+} \)). The device is functional down to 2V supply voltage (falling undervoltage lockout threshold \( V_{TH_{UVLO}-} \)).

8.4 Thermal Information

<table>
<thead>
<tr>
<th>THERMAL METRIC</th>
<th>DSS / 12 PINS</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>( R_{JUA} ) Junction-to-ambient thermal resistance</td>
<td>61.8</td>
<td>°C/W</td>
</tr>
<tr>
<td>( R_{JUCtop} ) Junction-to-case (top) thermal resistance</td>
<td>70.9</td>
<td></td>
</tr>
<tr>
<td>( R_{JUB} ) Junction-to-board thermal resistance</td>
<td>25.7</td>
<td></td>
</tr>
<tr>
<td>( \psi_{JT} ) Junction-to-top characterization parameter</td>
<td>1.9</td>
<td></td>
</tr>
<tr>
<td>( \psi_{JB} ) Junction-to-board characterization parameter</td>
<td>25.7</td>
<td></td>
</tr>
<tr>
<td>( R_{JUCbot} ) Junction-to-case (bottom) thermal resistance</td>
<td>7.2</td>
<td></td>
</tr>
</tbody>
</table>

8.5 Electrical Characteristics

\( V_{IN} = 3.6V, T_A = -40°C \) to 85°C typical values are at \( T_A = 25°C \) (unless otherwise noted)

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>( V_{IN} ) Input voltage range</td>
<td>EN = ( V_{IN} ), CTRL = GND, ( I_{OUT} ) = 0µA, ( V_{OUT} ) = 1.8V, device not switching.</td>
<td>2.2</td>
<td>5.5</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>( I_O ) Operating quiescent current</td>
<td>EN = ( V_{IN} ), IOUT = 0mA, CTRL = GND, VOUT = 1.8V, device switching</td>
<td>360</td>
<td>1800</td>
<td>nA</td>
<td></td>
</tr>
<tr>
<td></td>
<td>EN = ( V_{IN} ), IOUT = 0mA, CTRL = VIN, VOUT = 1.8V, device not switching</td>
<td>460</td>
<td></td>
<td>nA</td>
<td></td>
</tr>
<tr>
<td>( I_{SD} ) Shutdown current</td>
<td>EN = GND, shutdown current into ( V_{IN} ),</td>
<td>12.5</td>
<td></td>
<td>µA</td>
<td></td>
</tr>
<tr>
<td></td>
<td>EN = GND, shutdown current into ( V_{IN} ), ( T_A = 60°C )</td>
<td>150</td>
<td>450</td>
<td>µA</td>
<td></td>
</tr>
<tr>
<td>( V_{TH_{UVLO}+} ) Undervoltage lockout threshold Rising ( V_{IN} )</td>
<td>2.075</td>
<td></td>
<td>V</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Falling ( V_{IN} )</td>
<td>1.925</td>
<td>2</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>( V_{TH_{UVLO}-} ) Undervoltage lockout threshold Falling ( V_{IN} )</td>
<td>2.155</td>
<td></td>
<td>V</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>INPUTS EN, CTRL, VSEL 1-4</th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>( V_{IH TH} ) High level input threshold</td>
<td>2.2V \leq V_{IN} \leq 5.5V</td>
</tr>
<tr>
<td>( V_{IL TH} ) Low level input threshold</td>
<td>2.2V \leq V_{IN} \leq 5.5V</td>
</tr>
<tr>
<td>( I_{IN} ) Input bias Current</td>
<td>( T_A = 25°C )</td>
</tr>
<tr>
<td></td>
<td>( T_A = -40°C ) to 85°C</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>POWER SWITCHES</th>
</tr>
</thead>
<tbody>
<tr>
<td>( R_{DS(on)} ) High side MÖSFET on-resistance</td>
</tr>
<tr>
<td>Low Side MÖSFET on-resistance</td>
</tr>
</tbody>
</table>
Electrical Characteristics (continued)

\( V_{IN} = 3.6\,\text{V},\, T_A = -40^\circ\text{C} \) to 85\(^\circ\text{C} \) typical values are at \( T_A = 25^\circ\text{C} \) (unless otherwise noted)

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>( I_{Lim} )</td>
<td>High side MOSFET switch current limit</td>
<td>2.2V ( \leq V_{IN} \leq 5.5,\text{V}, ) TPS62740</td>
<td>480</td>
<td>600</td>
<td>720</td>
</tr>
<tr>
<td></td>
<td>Low side MOSFET switch current limit</td>
<td>TPS62740</td>
<td>600</td>
<td></td>
<td>mA</td>
</tr>
</tbody>
</table>

| | | | | | |
| \( R_{Disch, VOUT} \) | MOSFET on-resistance | \( V_{IN} = 3.6\,\text{V},\, EN = GND,\, I_{OUT} = -10\,\text{mA} \) into \( VOUT \) pin | 30 | 65 | | \( \Omega \) |
| \( I_{IN, VOUT} \) | Bias current into \( VOUT \) pin | \( V_{IN} = 3.6\,\text{V},\, EN = V_{IN},\, VOUT = 2\,\text{V},\, CTRL = \) GND | \( T_A = 25^\circ\text{C} \) | 40 | 100 | nA |
| | | \( T_A = -40^\circ\text{C} \) to 85\(^\circ\text{C} \) | 100 | | |

| \( \text{LOAD OUTPUT (LOAD)} \) | \( R_{LOAD} \) | High side MOSFET on-resistance | \( I_{LOAD} = 50\,\text{mA},\, CTRL = V_{IN},\, VOUT = 2.0\,\text{V},\, 2.2\,\text{V} \leq V_{IN} \leq 5.5\,\text{V} \) | 0.6 | 1.25 | | \( \Omega \) |
| | \( R_{Disch, LOAD} \) | Low side MOSFET on-resistance | \( CTRL = GND,\, 2.2\,\text{V} \leq V_{IN} \leq 5.5\,\text{V},\, I_{LOAD} = -10\,\text{mA} \) | 30 | 65 | | |
| \( I_{Rise, LOAD} \) | \( V_{LOAD} \) rise time | Starting with \( CTRL \) low to high transition, time to ramp \( V_{LOAD} \) from 0V to 95\% \( VOUT \) = 1.8\,\text{V}, 2.2\,\text{V} \leq V_{IN} \leq 5.5\,\text{V}, \( I_{LOAD} = 1\,\text{mA} \) | 315 | 800 | | \( \mu\text{s} \) |

| \( \text{AUTO 100\% MODE TRANSITION} \) | \( V_{TH, 100-} \) | Auto 100\% Mode leave detection threshold \( (1) \) | Rising \( V_{IN} \), 100\% Mode is left with \( V_{IN} = V_{OUT} + V_{TH, 100-} \), max value at \( T_J = 85^\circ\text{C} \) | 170 | 250 | 340 | | mV |
| | \( V_{TH, 100+} \) | Auto 100\% Mode enter detection threshold \( (1) \) | Falling \( V_{IN} \), 100\% Mode is entered with \( V_{IN} = V_{OUT} + V_{TH, 100+} \), max value at \( T_J = 85^\circ\text{C} \) | 110 | 200 | 280 | | |

| \( \text{POWER GOOD OUTPUT (PG, OPEN DRAIN)} \) | \( V_{TH, PG+} \) | Power good threshold voltage | Rising output voltage on \( VOUT \) pin, referred to \( V_{VOUT} \) | 97.5\% | | |
| \( V_{PG, Hys} \) | Hysteresis | \( -3\% \) | | | |
| \( V_{OL} \) | Low level output voltage | \( 2.2\,\text{V} \leq V_{IN} \leq 5.5\,\text{V},\, EN = GND, \) current into \( PG \) pin \( I_{PG} = 4\,\text{mA} \) | 0.3 | | | V |
| \( I_{IN, PG} \) | Bias current into \( PG \) pin | \( PG \) pin is high impedance, \( VOUT = 2\,\text{V},\, EN = V_{IN},\, CTRL = GND,\, I_{OUT} = 0\,\text{mA} \) \( T_A = 25^\circ\text{C} \) | 0 | 10 | | nA |
| \( T_A = -40^\circ\text{C} \) to 85\(^\circ\text{C} \) | 25 | | |

| \( \text{OUTPUT} \) | \( t_{Conmin} \) | Minimum ON time | \( V_{IN} = 3.6\,\text{V},\, V_{OUT} = 2.0\,\text{V},\, I_{OUT} = 0\,\text{mA} \) | 225 | | ns |
| | \( t_{Offmin} \) | Minimum OFF time | \( V_{IN} = 2.3\,\text{V} \) | 50 | | ns |
| | \( t_{Startup, delay} \) | Regulator start up delay time | \( V_{IN} = 3.6\,\text{V}, \) from transition \( EN = \) low to high until device starts switching | 10 | 25 | | ms |
| | \( t_{Softstart} \) | Softstart time with reduced switch current limit | \( 2.2\,\text{V} \leq V_{IN} \leq 5.5\,\text{V},\, EN = V_{IN} \) | 700 | 1200 | | \( \mu\text{s} \) |
| \( I_{Lim, softstart} \) | High side MOSFET switch current limit | Reduced switch current limit during softstart | TPS62740 | 80 | 150 | 200 | mA |
| | Low side MOSFET switch current limit | TPS62742 | 150 | | | |
| \( V_{VOUT} \) | Output voltage range | Output voltages are selected with pins VSEL 1 - 4 | 1.8 | 3.3 | | V |
| | Output voltage accuracy | \( V_{IN} = 3.6\,\text{V},\, I_{OUT} = 10\,\text{mA},\, V_{OUT} = 1.8\,\text{V} \) | -2.5 | 0 | | % |
| | | \( V_{IN} = 3.6\,\text{V},\, I_{OUT} = 100\,\text{mA},\, V_{OUT} = 1.8\,\text{V} \) | -2 | 0 | | % |
| | DC output voltage load regulation | \( V_{OUT} = 1.8\,\text{V},\, V_{IN} = 3.6\,\text{V},\, CTRL = V_{IN} \) | 0.001 | | | %/mA |
| | DC output voltage line regulation | \( V_{OUT} = 1.8\,\text{V},\, CTRL = V_{IN}, I_{OUT} = 10\,\text{mA}, 2.5\,\text{V} \leq V_{IN} \leq 5.5\,\text{V} \) | 0 | | | %/V |

\( (1) \) \( V_{IN} \) is compared to the programmed output voltage \( (V_{OUT}) \). When \( V_{IN} - V_{OUT} \) falls below \( V_{TH, 100} \), the device enters 100\% Mode by turning the high side MOSFET on. The 100\% Mode is exited when \( V_{IN} - V_{OUT} \) exceeds \( V_{TH, 100} \), and the device starts switching. The hysteresis for the 100\% Mode detection threshold \( V_{TH, 100-} \), \( V_{TH, 100+} \), will always be positive and will be approximately 50 mV (typ.)
8.6 Typical Characteristics

**Figure 1. Quiescent Current**

**Figure 2. Shutdown Current $I_{SD}$**

**Figure 3. $R_{DS(ON)}$ High Side Mosfet**

**Figure 4. $R_{DS(ON)}$ Low Side Mosfet**

**Figure 5. Load Switch Resistance $R_{LOAD}$**
9 Detailed Description

9.1 Overview
The TPS6274x is the first step down converter with an ultra low quiescent current consumption (360nA typ.) and featuring TI's DCS-Control™ topology while maintaining a regulated output voltage. The device extends high efficiency operation to output currents down to a few micro amperes.

9.2 Functional Block Diagram

9.3 Feature Description

9.3.1 DCS-Control™
TI's DCS-Control™ (Direct Control with Seamless Transition into Power Save Mode) is an advanced regulation topology, which combines the advantages of hysteretic and voltage mode control. Characteristics of DCS-Control™ are excellent AC load regulation and transient response, low output ripple voltage and a seamless transition between PFM and PWM mode operation. DCS-Control™ includes an AC loop which senses the output voltage (VOUT pin) and directly feeds the information to a fast comparator stage. This comparator sets the switching frequency, which is constant for steady state operating conditions, and provides immediate response to dynamic load changes. In order to achieve accurate DC load regulation, a voltage feedback loop is used. The internally compensated regulation network achieves fast and stable operation with small external components and low ESR capacitors.
Feature Description (continued)

The DCS-Control™ topology supports PWM (Pulse Width Modulation) mode for medium and high load conditions and a Power Save Mode at light loads. During PWM mode, it operates in continuous conduction. The switching frequency is up to 2MHz with a controlled frequency variation depending on the input voltage. If the load current decreases, the converter seamlessly enters Power Save Mode to maintain high efficiency down to very light loads. In Power Save Mode the switching frequency varies nearly linearly with the load current. Since DCS-Control™ supports both operation modes within one single building block, the transition from PWM to Power Save Mode is seamless without effects on the output voltage. The TPS6274x offers both excellent DC voltage and superior load transient regulation, combined with very low output voltage ripple, minimizing interference with RF circuits. At high load currents, the converter operates in quasi fixed frequency PWM mode operation and at light loads, in PFM (Pulse Frequency Modulation) mode to maintain highest efficiency over the full load current range. In PFM Mode, the device generates a single switching pulse to ramp up the inductor current and recharge the output capacitor, followed by a sleep period where most of the internal circuits are shutdown to achieve a lowest quiescent current. During this time, the load current is supported by the output capacitor. The duration of the sleep period depends on the load current and the inductor peak current.

During the sleep periods, the current consumption of TPS6274x is reduced to 360nA. This low quiescent current consumption is achieved by an ultra low power voltage reference, an integrated high impedance (typ. 50MΩ) feedback divider network and an optimized DCS-Control™ block.

9.3.2 CTRL / Output Load

With the CTRL pin set to high, the LOAD pin is connected to the VOUT pin via an load switch and can power up an additional, temporarily used sub-system. The load switch is slew rate controlled to support soft switching and not to impact the regulated output VOUT. If CTRL pin is pulled to GND, the LOAD pin is disconnected from the VOUT pin and internally connected to GND by an internal discharge switch. When CTRL pin is set to high, the Quiescent current of the DCS control block is increased to typ. 12.5µA. This ensures excellent transient response on both outputs VOUT and LOAD in case of a sudden load step at the LOAD output. The CTRL pin can be controlled by a micro controller.

9.3.3 Enable / Shutdown

The DC/DC converter is activated when the EN pin is set to high. For proper operation, the pin must be terminated and must not be left floating. With the EN pin set to low, the device enters shutdown mode with less than typ. 70nA current consumption.

9.3.4 Power Good Output (PG)

The Power Good comparator features an open drain output. The PG comparator is active with EN pin set to high and VIN is above the threshold VTH_UVLO+. It is driven to high impedance once VOUT trips the threshold VTH_PG+ for rising VOUT. The output is pulled to low level once VOUT falls below the PG hysteresis, VPG_hys. The output is also pulled to low level in case the input voltage VIN falls below the undervoltage lockout threshold VTH_UVLO- or the device is disabled with EN = low. The power good output (PG) can be used as an indicator for the system to signal that the converter has started up and the output voltage is in regulation.

9.3.5 Output Voltage Selection (VSEL1 – 4)

The TPS6274x doesn't require an external resistor divider network to program the output voltage. The device integrates a high impedance (typ. 50MΩ) feedback resistor divider network which is programmed by the pins VSEL 1-4. TPS6274x supports an output voltage range of 1.8V to 3.3V in 100mV steps. The output voltage can be changed during operation and supports a simple dynamic output voltage scaling, shown in Figure 47. The output voltage is programmed according to table Table 1.

9.3.6 Softstart

When the device is enabled, the internal reference is powered up and after the startup delay time tStartup_delay has expired, the device enters softstart, starts switching and ramps up the output voltage. During softstart the device operates with a reduced current limit, ILIM_softstart, of typ. 1/4 of the nominal current limit. This reduced current limit is active during the softstart time tSoftstart. The current limit is increased to its nominal value, ILIMF, once the softstart time has expired.
Feature Description (continued)

9.3.7 Undervoltage Lockout UVLO

The device includes an under-voltage lockout (UVLO) comparator which prevents the device from misoperation at too low input voltages. The UVLO comparator becomes active once the device is enabled with EN set to high. Once the input voltage trips the UVLO threshold $V_{TH\_UVLO\_+}$ (typically 2.075V) for rising $V_{IN}$, the UVLO comparator releases the device for start up and operation. With a falling input voltage, the device operates down to the UVLO threshold level $V_{TH\_UVLO\_-}$ (typically 1.925V). Once this threshold is tripped, the device stops switching, the load switch at pin LOAD is disabled and both rails, VOUT and LOAD are discharged. The converter starts operation again once the input voltage trips the rising UVLO threshold level $V_{TH\_UVLO\_+}$.

9.4 Device Functional Modes

9.4.1 VOUT And LOAD Output Discharge

Both the VOUT pin and the LOAD pin feature a discharge circuit to connect each rail to GND, once they are disabled. This feature prevents residual charge voltages on capacitors connected to these pins, which may impact proper power up of the main- and sub-system. With CTRL pin pulled to low, the discharge circuit at the LOAD pin becomes active. With the EN pin pulled to low, the discharge circuits at both pins VOUT and Load are active. The discharge circuits of both rails VOUT and LOAD are associated with the UVLO comparator as well. Both discharge circuits become active once the UVLO comparator triggers and the input voltage $V_{IN}$ has dropped below the UVLO comparator threshold $V_{TH\_UVLO\_-}$ (typ. 1.925V).

9.4.2 Automatic Transition Into 100% Mode

Once the input voltage comes close to the output voltage, the DC/DC converter stops switching and enters 100% duty cycle operation. It connects the output VOUT via the inductor and the internal high side MOSFET switch to the input VIN, once the input voltage $V_{IN}$ falls below the 100% mode enter threshold, $V_{TH\_100\_-}$. The DC/DC regulator is turned off, not switching and therefore it generates no output ripple voltage. Because the output is connected to the input, the output voltage tracks the input voltage minus the voltage drop across the internal high side switch and the inductor caused by the output current. Once the input voltage increases and trips the 100% mode leave threshold, $V_{TH\_100\_+}$, the DC/DC regulator turns on and starts switching again. See Figure 6, Figure 49, Figure 50, Figure 51.

![Figure 6. Automatic 100% Mode Transition](image-url)
Device Functional Modes (continued)

9.4.3 Internal Current Limit

The TPS6274x integrates a current limit on the high side, as well the low side MOSFETs to protect the device against overload or short circuit conditions. The peak current in the switches is monitored cycle by cycle. If the high side MOSFET current limit is reached, the high side MOSFET is turned off and the low side MOSFET is turned on until the current decreases below the low side MOSFET current limit.

9.4.4 Dynamic Voltage Scaling with VSEL Interface

During operation, the output voltage of the device can be changed, see Figure 47. The device will not actively ramp down the output voltage from a higher to a lower level.
10 Application and Implementation

10.1 Application Information

The TPS6274x devices are a step down converter family featuring typ. 360nA quiescent current and operating with a tiny 2.2µH inductor and 10µF output capacitor. This new DCS-Control™ based devices extend the light load efficiency range below 10µA load currents. TPS62740 supports output currents up to 300mA, TPS62742 up to 400mA. The devices operate from rechargeable Li-Ion batteries, Li-primary battery chemistries such as Li-SOCI2, Li-MnO2 and two or three cell alkaline batteries.

10.2 Typical Application

10.2.1 Design Requirements

The TPS6274x is a highly integrated DC/DC converter. The output voltage is set via a VSEL pin interface without any additional external components. For proper operation only a input- and output capacitor and an inductor is required. The integrated load switch doesn’t require a capacitor on its LOAD pin. Table 2 shows the components used for the application characteristic curves.

<table>
<thead>
<tr>
<th>Reference</th>
<th>Description</th>
<th>Value</th>
<th>Manufacturer</th>
</tr>
</thead>
<tbody>
<tr>
<td>TPS62740/42</td>
<td>360nA Iq step down converter</td>
<td></td>
<td>Texas Instruments</td>
</tr>
<tr>
<td>CIN, COUT, CLOAD</td>
<td>Ceramic capacitor GRM188R60J106M</td>
<td>10µF</td>
<td>Murata</td>
</tr>
<tr>
<td>L</td>
<td>Inductor LPS3314</td>
<td>2.2µH</td>
<td>Coilcraft</td>
</tr>
</tbody>
</table>
10.2.2 Detailed Design Procedure

Table 3 shows the recommended output filter components. The TPS6274x is optimized for operation with a 2.2µH inductor and with 10µF output capacitor.

Table 3. Recommended LC Output Filter Combinations

<table>
<thead>
<tr>
<th>Inductor Value <a href="1">µH</a></th>
<th>Output Capacitor Value <a href="2">µF</a></th>
<th>4.7µF</th>
<th>10µF</th>
<th>22µF</th>
</tr>
</thead>
<tbody>
<tr>
<td>2.2</td>
<td></td>
<td>√</td>
<td>√(3)</td>
<td>√</td>
</tr>
</tbody>
</table>

(1) Inductor tolerance and current de-rating is anticipated. The effective inductance can vary by 20% and -30%.
(2) Capacitance tolerance and bias voltage de-rating is anticipated. The effective capacitance can vary by 20% and -50%.
(3) This LC combination is the standard value and recommended for most applications.

10.2.2.1 Inductor Selection

The inductor value affects its peak-to-peak ripple current, the PWM-to-PFM transition point, the output voltage ripple and the efficiency. The selected inductor has to be rated for its DC resistance and saturation current. The inductor ripple current (ΔIL) decreases with higher inductance and increases with higher VIN or VOUT and can be estimated according to Equation 1.

Equation 2 calculates the maximum inductor current under static load conditions. The saturation current of the inductor should be rated higher than the maximum inductor current, as calculated with Equation 2. This is recommended because during a heavy load transient the inductor current rises above the calculated value. A more conservative way is to select the inductor saturation current above the high-side MOSFET switch current limit, ILIMF.

\[
\Delta I_L = V_{out} \times \frac{1 - \frac{V_{out}}{V_{in}}}{L \times f}
\]

(1)

\[
I_{L_{max}} = I_{out_{max}} + \frac{\Delta I_L}{2}
\]

(2)

With:
- f = Switching Frequency
- L = Inductor Value
- ΔIL = Peak to Peak inductor ripple current
- IL_{max} = Maximum Inductor current

In DC/DC converter applications, the efficiency is essentially affected by the inductor AC resistance (i.e. quality factor) and by the inductor DCR value. Increasing the inductor value produces lower RMS currents, but degrades transient response. For a given physical inductor size, increased inductance usually results in an inductor with lower saturation current.

The total losses of the coil consist of both the losses in the DC resistance (R_{DC}) and the following frequency-dependent components:
- The losses in the core material (magnetic hysteresis loss, especially at high switching frequencies)
- Additional losses in the conductor from the skin effect (current displacement at high frequencies)
- Magnetic field losses of the neighboring windings (proximity effect)
- Radiation losses
The following inductor series from different suppliers have been used:

### Table 4. List Of Inductors\(^{(1)}\)

<table>
<thead>
<tr>
<th>INDUCTANCE [(\mu\text{H})]</th>
<th>DIMENSIONS [mm(^3)]</th>
<th>INDUCTOR TYPE</th>
<th>SUPPLIER</th>
</tr>
</thead>
<tbody>
<tr>
<td>2.2</td>
<td>3.3 x 3.3 x 1.4</td>
<td>LPS3314</td>
<td>Coilcraft</td>
</tr>
<tr>
<td>2.2</td>
<td>2.5 x 3.0 x 1.5</td>
<td>VLF302515MT</td>
<td>TDK</td>
</tr>
<tr>
<td>2.2</td>
<td>2.0 x 1.2 x 1.0</td>
<td>MIPSZ2012 2R2</td>
<td>FDK</td>
</tr>
<tr>
<td>2.2</td>
<td>2.5 x 2.0 x 1.2</td>
<td>MIPSZ2520 2R2</td>
<td>FDK</td>
</tr>
<tr>
<td>2.2</td>
<td>2.0 x 1.2 x 1.0</td>
<td>MDT2012CH2R2</td>
<td>TOKO</td>
</tr>
</tbody>
</table>

\(^{(1)}\) See Third-party Products Disclaimer

### 10.2.2.2 DC/DC Output Capacitor Selection

The DCS-Control™ scheme of the TPS6274x allows the use of tiny ceramic capacitors. Ceramic capacitors with low ESR values have the lowest output voltage ripple and are recommended. The output capacitor requires either an X7R or X5R dielectric. Y5V and Z5U dielectric capacitors, aside from their wide variation in capacitance over temperature, become resistive at high frequencies. At light load currents, the converter operates in Power Save Mode and the output voltage ripple is dependent on the output capacitor value and the PFM peak inductor current. A larger output capacitors can be used, but it should be considered that larger output capacitors lead to an increased leakage current in the capacitor and may reduce overall conversion efficiency. Furthermore, larger output capacitors impact the start up behavior of the DC/DC converter.

### 10.2.2.3 Input Capacitor Selection

Because the buck converter has a pulsating input current, a low ESR input capacitor is required for best input voltage filtering to ensure proper function of the device and to minimize input voltage spikes. For most applications a 10\(\mu\text{F}\) is sufficient. The input capacitor can be increased without any limit for better input voltage filtering.

Table 5 shows a list of tested input/output capacitors.

### Table 5. List Of Capacitors\(^{(1)}\)

<table>
<thead>
<tr>
<th>CAPACITANCE [(\mu\text{F})]</th>
<th>SIZE</th>
<th>CAPACITOR TYPE</th>
<th>SUPPLIER</th>
</tr>
</thead>
<tbody>
<tr>
<td>10</td>
<td>0603</td>
<td>GRM188R60J106ME84</td>
<td>Murata</td>
</tr>
</tbody>
</table>

\(^{(1)}\) See Third-party Products Disclaimer
10.2.3 Application Curves

C\textsubscript{OUT} = 10 µF (0603)  
CTRL = GND  
L = 2.2 µH (LPS3314 2R2)

Figure 9. Efficiency V\textsubscript{OUT} = 1.8V

C\textsubscript{OUT} = 10 µF (0603)  
CTRL = GND  
L = 2.2 µH (LPS3314 2R2)

Figure 10. Efficiency V\textsubscript{OUT} = 2.1V

C\textsubscript{OUT} = 10 µF (0603)  
CTRL = GND  
L = 2.2 µH (LPS3314 2R2)

Figure 11. Efficiency V\textsubscript{OUT} = 3.3V TPS62742

C\textsubscript{OUT} = 10 µF (0603)  
CTRL = GND  
L = 2.2 µH (LPS3314 2R2)

Figure 12. Efficiency V\textsubscript{OUT} = 2.5V

C\textsubscript{OUT} = 10 µF (0603)  
CTRL = GND  
L = 2.2 µH (LPS3314 2R2)

Figure 13. Efficiency V\textsubscript{OUT} = 3.3V

C\textsubscript{OUT} = 10 µF (0603)  
CTRL = GND  
L = 2.2 µH (LPS3314 2R2)

Figure 14. Efficiency V\textsubscript{OUT} = 1.8V
Figure 15. Efficiency $V_{OUT} = 2.1V$

Figure 16. Efficiency $V_{OUT} = 2.5V$

Figure 17. Efficiency $V_{OUT} = 3.3V$

Figure 18. Output Voltage $V_{OUT} = 1.8V$

Figure 19. Output Voltage $V_{OUT} = 2.1V$

Figure 20. Output Voltage $V_{OUT} = 2.5V$
$C_{\text{OUT}} = 10 \ \mu\text{F} (0603)$  
$L = 2.2 \ \mu\text{H} (\text{LPS3314 2R2})$

**Figure 21. Output Voltage $V_{\text{OUT}} = 3.3\text{V}$**

$C_{\text{OUT}} = 10 \ \mu\text{F} (0603)$  
$\text{CTRL} = \text{GND}$  
$L = 2.2 \ \mu\text{H}$

**Figure 22. Typical Switching Frequency $V_{\text{OUT}} = 1.8\text{V}$**

$C_{\text{OUT}} = 10 \ \mu\text{F} (0603)$  
$\text{CTRL} = \text{GND}$  
$L = 2.2 \ \mu\text{H}$

**Figure 23. Typical Output Ripple Voltage $V_{\text{OUT}} = 1.8\text{V}$**

$C_{\text{OUT}} = 10 \ \mu\text{F} (0603)$  
$\text{CTRL} = \text{GND}$  
$L = 2.2 \ \mu\text{H}$

**Figure 24. Typical Switching Frequency $V_{\text{OUT}} = 2.1\text{V}$**

$C_{\text{OUT}} = 10 \ \mu\text{F} (0603)$  
$\text{CTRL} = \text{GND}$  
$L = 2.2 \ \mu\text{H}$

**Figure 25. Typical Output Ripple Voltage $V_{\text{OUT}} = 2.1\text{V}$**

$C_{\text{OUT}} = 10 \ \mu\text{F} (0603)$  
$\text{CTRL} = \text{GND}$  
$L = 2.2 \ \mu\text{H}$

**Figure 26. Typical Switching Frequency $V_{\text{OUT}} = 3.0\text{V}$**
Figure 27. Typical Output Ripple Voltage $V_{OUT} = 3.0V$

Figure 28. 100% Mode Transition $V_{OUT} 2.1V$

Figure 29. 100% Mode Transition $V_{OUT} 2.5V$

Figure 30. 100% Mode Transition $V_{OUT} 3.3V$

Figure 31. Typical Operation $I_{Load} = 10µA, V_{OUT} = 1.8V$

Figure 32. Typical Operation $I_{Load} = 1mA, V_{OUT} = 1.8V$
Figure 33. Typical Operation $I_{\text{Load}} = 25\text{mA}, V_{\text{OUT}} = 1.8\text{V}$

Figure 34. Typical Operation $I_{\text{Load}} = 150\text{ma}, V_{\text{OUT}} = 1.8\text{V}$

Figure 35. Load Transient Response $V_{\text{OUT}} = 1.8\text{V}$

Figure 36. Load Transient Response $V_{\text{OUT}} = 2.1\text{V}$

Figure 37. Load Transient Response $CTRL = \text{GND}$

Figure 38. Load Transient Response $CTRL = V_{\text{IN}}$
V_{IN} = 3.6 V / 4.2 V  \quad V_{OUT} = 2.1 V  \quad L = 2.2 \mu H  
C_{OUT} = 10 \mu F  \quad CTRL = GND

Figure 39. Line Transient Response I_{OUT} = 10 mA

V_{IN} = 3.6 V / 4.2 V  \quad V_{OUT} = 2.1 V  \quad L = 2.2 \mu H  
C_{OUT} = 10 \mu F  \quad CTRL = GND

Figure 40. Line Transient Response I_{OUT} = 100 mA

V_{IN} = 3.6 V  \quad I_{OUT} = 50 \mu A to 300 mA  
C_{OUT} = 10 \mu F  \quad CTRL = GND

Figure 41. AC Load Sweep V_{OUT} = 2.1 V

V_{IN} = 3.6 V,  \quad V_{LOAD} = 2.1 V  \quad CTRL = V_{IN}  
C_{LOAD} = 10 \mu F  \quad I_{LOAD} = 0 to 50 mA to 0 mA

Figure 42. Load Step At Load Output

V_{IN} = 3.6 V  \quad I_{OUT} = 0 mA  
C_{OUT} = 10 \mu F  \quad L = 2.2 \mu H

Figure 43. Load Output On / Off

V_{IN} = 3.6 V  \quad V_{OUT} = 2.1 V  \quad CTRL = GND  
C_{LOAD} = 10 \mu F  \quad L = 2.2 \mu H

Figure 44. Device Enable And Start Up
100% mode operation, high side MOSFET turned on

TPS62740, TPS62742

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10.3 System Example

Figure 51. Enter/Leave 100% Mode Operation

Figure 52. Example Of Implementation In A Master MCU Based System

TPS62740, TPS62742

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VOUT = 3.0 V
COUT = 10 µF
L = 2.2 µH, CTRL = GND
VIN = ramp up/down 2.8 V to 3.7 V,
Output resistance 50 Ω

High side mosfet turned on
100% Mode
Leave / Enter

Figure 51. Enter/Leave 100% Mode Operation

TPS62740

VSEL1
VSEL2
VSEL3
VSEL4

Vin
VOUT Main
CIN
CTRL
EN
GND
SW
LOAD

VOUT Main
RPull Up

Master MCU

Control Sub-System

Power Good

Voltage Selection

Figure 52. Example Of Implementation In A Master MCU Based System

Sensor
Sub-System

Radio

Switched Supply

TPS62740, TPS62742

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VOUT = 3.0 V
COUT = 10 µF
L = 2.2 µH, CTRL = GND
VIN = ramp up/down 2.8 V to 3.7 V,
Output resistance 50 Ω

High side mosfet turned on
100% Mode
Leave / Enter

Figure 51. Enter/Leave 100% Mode Operation

TPS62740

VSEL1
VSEL2
VSEL3
VSEL4

Vin
VOUT Main
CIN
CTRL
EN
GND
SW
LOAD

VOUT Main
RPull Up

Master MCU

Control Sub-System

Power Good

Voltage Selection

Figure 52. Example Of Implementation In A Master MCU Based System

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11 Power Supply Recommendations
The power supply to the TPS6274x needs to have a current rating according to the supply voltage, output voltage and output current of the TPS6274x.

12 Layout

12.1 Layout Guidelines
As for all switching power supplies, the layout is an important step in the design. Care must be taken in board layout to get the specified performance. If the layout is not carefully done, the regulator could show poor line and/or load regulation, stability issues as well as EMI problems and interference with RF circuits. It is critical to provide a low inductance, impedance ground path. Therefore, use wide and short traces for the main current paths. The input capacitor should be placed as close as possible to the IC pins VIN and GND. The output capacitor should be placed close between VOUT and GND pins. The VOUT line should be connected to the output capacitor and routed away from noisy components and traces (e.g. SW line) or other noise sources. The exposed thermal pad of the package and the GND pin should be connected. See Figure 53 for the recommended PCB layout.

12.2 Layout Example

![Figure 53. Recommended PCB Layout](image-url)
13 Device and Documentation Support

13.1 Device Support

13.1.1 Third-Party Products Disclaimer

TI’s publication of information regarding third-party products or services does not constitute an endorsement regarding the suitability of such products or services or a warranty, representation or endorsement of such products or services, either alone or in combination with any TI product or service.

13.2 Documentation Support

13.2.1 Related Documentation

See also TPS62740EVM-186 Evaluation Module User’s Guide, SLVU949; and application note Accurately measuring efficiency of ultralow-IQ devices, SLYT558 for accurate efficiency measurements in PFM mode operation.

13.3 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

<table>
<thead>
<tr>
<th>PARTS</th>
<th>PRODUCT FOLDER</th>
<th>SAMPLE &amp; BUY</th>
<th>TECHNICAL DOCUMENTS</th>
<th>TOOLS &amp; SOFTWARE</th>
<th>SUPPORT &amp; COMMUNITY</th>
</tr>
</thead>
<tbody>
<tr>
<td>TPS62740</td>
<td>Click here</td>
<td>Click here</td>
<td>Click here</td>
<td>Click here</td>
<td>Click here</td>
</tr>
<tr>
<td>TPS62742</td>
<td>Click here</td>
<td>Click here</td>
<td>Click here</td>
<td>Click here</td>
<td>Click here</td>
</tr>
</tbody>
</table>

13.4 Trademarks

DCS-Control is a trademark of Texas Instruments. Bluetooth is a registered trademark of Bluetooth SIG, Inc.

13.5 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

13.6 Glossary

SLYZ022 — TI Glossary.

This glossary lists and explains terms, acronyms, and definitions.

14 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.
### PACKAGING INFORMATION

<table>
<thead>
<tr>
<th>Orderable Device</th>
<th>Status</th>
<th>Package Type</th>
<th>Package Drawing</th>
<th>Pins</th>
<th>Package Qty</th>
<th>Eco Plan</th>
<th>Lead/Ball Finish</th>
<th>MSL Peak Temp</th>
<th>Op Temp (°C)</th>
<th>Device Marking</th>
<th>Samples</th>
</tr>
</thead>
<tbody>
<tr>
<td>TPS62740DSSR</td>
<td>ACTIVE</td>
<td>WSON</td>
<td>DSS</td>
<td>12</td>
<td>3000</td>
<td>Green (RoHS &amp; no Sb/Br)</td>
<td>CU NIPDAU</td>
<td>Level-2-260C-1 YEAR</td>
<td>-40 to 85</td>
<td>62740</td>
<td>Samples</td>
</tr>
<tr>
<td>TPS62740DSST</td>
<td>ACTIVE</td>
<td>WSON</td>
<td>DSS</td>
<td>12</td>
<td>250</td>
<td>Green (RoHS &amp; no Sb/Br)</td>
<td>CU NIPDAU</td>
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<td>-40 to 85</td>
<td>62742</td>
<td>Samples</td>
</tr>
</tbody>
</table>

(1) The marketing status values are defined as follows:
- **ACTIVE**: Product device recommended for new designs.
- **LIFEBUY**: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
- **NRND**: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
- **PREVIEW**: Device has been announced but is not in production. Samples may or may not be available.
- **OBSOLETE**: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check [http://www.ti.com/productcontent](http://www.ti.com/productcontent) for the latest availability information and additional product content details.

- **TBD**: The Pb-Free/Green conversion plan has not been defined.
- **Pb-Free (RoHS)**: TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
- **Pb-Free (RoHS Exempt)**: This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe, The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
- **Green (RoHS & no Sb/Br)**: TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.
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## TAPE AND REEL INFORMATION

*All dimensions are nominal*

<table>
<thead>
<tr>
<th>Device</th>
<th>Package Type</th>
<th>Package Drawing</th>
<th>Pins</th>
<th>SPQ</th>
<th>Reel Diameter (mm)</th>
<th>Reel Width W1 (mm)</th>
<th>A0 (mm)</th>
<th>B0 (mm)</th>
<th>K0 (mm)</th>
<th>P1 (mm)</th>
<th>W (mm)</th>
<th>Pin 1 Quadrant</th>
</tr>
</thead>
<tbody>
<tr>
<td>TPS62740DSSR</td>
<td>WSON</td>
<td>DSS</td>
<td>12</td>
<td>3000</td>
<td>180.0</td>
<td>8.4</td>
<td>2.25</td>
<td>3.25</td>
<td>1.05</td>
<td>4.0</td>
<td>8.0</td>
<td>Q1</td>
</tr>
<tr>
<td>TPS62740DSST</td>
<td>WSON</td>
<td>DSS</td>
<td>12</td>
<td>250</td>
<td>180.0</td>
<td>8.4</td>
<td>2.25</td>
<td>3.25</td>
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<td>4.0</td>
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<td>Q1</td>
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<td>WSON</td>
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<td>8.4</td>
<td>2.25</td>
<td>3.25</td>
<td>1.05</td>
<td>4.0</td>
<td>8.0</td>
<td>Q1</td>
</tr>
</tbody>
</table>
## TAPE AND REEL BOX DIMENSIONS

*All dimensions are nominal*

<table>
<thead>
<tr>
<th>Device</th>
<th>Package Type</th>
<th>Package Drawing</th>
<th>Pins</th>
<th>SPQ</th>
<th>Length (mm)</th>
<th>Width (mm)</th>
<th>Height (mm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>TPS62740DSSR</td>
<td>WSON</td>
<td>DSS</td>
<td>12</td>
<td>3000</td>
<td>210.0</td>
<td>185.0</td>
<td>35.0</td>
</tr>
<tr>
<td>TPS62740DSST</td>
<td>WSON</td>
<td>DSS</td>
<td>12</td>
<td>250</td>
<td>210.0</td>
<td>185.0</td>
<td>35.0</td>
</tr>
<tr>
<td>TPS62742DSSR</td>
<td>WSON</td>
<td>DSS</td>
<td>12</td>
<td>3000</td>
<td>210.0</td>
<td>185.0</td>
<td>35.0</td>
</tr>
<tr>
<td>TPS62742DSST</td>
<td>WSON</td>
<td>DSS</td>
<td>12</td>
<td>250</td>
<td>210.0</td>
<td>185.0</td>
<td>35.0</td>
</tr>
</tbody>
</table>
Images above are just a representation of the package family, actual package may vary. Refer to the product data sheet for package details.
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).

5. Vias are optional depending on application, refer to device data sheet. If some or all are implemented, recommended via locations are shown. It is recommended that vias located under solder paste be filled, plugged or tented.
NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
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