1 Features
- Qualified for Automotive Applications
- AEC-Q100 Qualified With the Following Results:
  - Device Temperature Grade 1: −40°C to 125°C Ambient Operating Temperature Range
  - Device HBM ESD Classification Level 2
  - Device CDM ESD Classification Level C4A (RHA Package) or C5 (RSB Package)
- 1.5 A, 90% Efficient Step-Down Converter for Processor Core (VDCDC1)
- 1.2 A, Up to 95% Efficient Step-Down Converter for System Voltage (VDCDC2)
- 1 A, 92% Efficient Step-Down Converter for Memory Voltage (VDCDC3)
- 30 mA LDO/Switch for Real Time Clock (VRTC)
- 2 × 200 mA General-Purpose Low Dropout (LDO)
- Dynamic Voltage Management for Processor Core
- Preselectable LDO Voltage Using Two Digital Input Pins
- Externally Adjustable Reset Delay Time
- Battery Backup Functionality
- Separate Enable Pins for Inductive Converters
- I2C-Compliant Serial Interface
- 85-μA Quiescent Current
- Low-Ripple Pulse-Frequency Modulation (PFM) Mode
- Thermal Shutdown Protection

2 Applications
- Automotive Clusters
- Automotive Infotainment Systems
- Digital Radios
- Supply DaVinci™ Digital Signal Processor (DSP) Family Solutions

3 Description
The TPS65023-Q1 device is an integrated power-management integrated circuit (IC) for applications powered by one Li-Ion or Li-Polymer cell, which require multiple power rails. The TPS65023-Q1 device provides three highly efficient, step-down converters targeted at providing the core voltage, peripheral, input and output (I/O), and memory rails in a processor-based system. The core converter allows for on-the-fly voltage changes through a serial interface, allowing the system to implement dynamic power savings. All three step-down converters enter a low-power mode at light load for maximum efficiency across the widest possible range of load currents.

Device Information (1)

<table>
<thead>
<tr>
<th>PART NUMBER</th>
<th>PACKAGE</th>
<th>BODY SIZE (NOM)</th>
</tr>
</thead>
<tbody>
<tr>
<td>TPS65023-Q1</td>
<td>VQFN (40)</td>
<td>6.00 mm × 6.00 mm</td>
</tr>
<tr>
<td></td>
<td>WQFN (40)</td>
<td>5.00 mm × 5.00 mm</td>
</tr>
</tbody>
</table>

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Simplified Schematic
Table of Contents

1 Features ................................................................. 1
2 Applications .......................................................... 1
3 Description .................................................................. 1
4 Revision History .......................................................... 2
5 Description (continued) .................................................. 3
6 Pin Configuration and Functions ..................................... 3
7 Specifications ............................................................. 5
   7.1 Absolute Maximum Ratings ...................................... 5
   7.2 ESD Ratings .......................................................... 5
   7.3 Recommended Operating Conditions ......................... 6
   7.4 Thermal Information .............................................. 6
   7.5 Electrical Characteristics ......................................... 7
   7.6 Timing Requirements ............................................ 10
   7.7 Typical Characteristics .......................................... 11
8 Detailed Description ..................................................... 16
   8.1 Overview ............................................................. 16
   8.2 Functional Block Diagram ....................................... 16
   8.3 Feature Description .............................................. 17
   8.4 Device Functional Modes ....................................... 18
   8.5 Programming ....................................................... 22
   8.6 Register Maps ..................................................... 24
9 Application and Implementation ..................................... 31
   9.1 Application Information ........................................ 31
   9.2 Typical Application .............................................. 33
10 Power Supply Recommendations ................................... 37
11 Layout ...................................................................... 38
   11.1 Layout Guidelines .............................................. 38
   11.2 Layout Example ................................................ 38
12 Device and Documentation Support ............................... 39
   12.1 Device Support .................................................. 39
   12.2 Documentation Support ....................................... 39
   12.3 Receiving Notification of Documentation Updates ....... 39
   12.4 Community Resources ....................................... 39
   12.5 Trademarks ....................................................... 39
   12.6 Electrostatic Discharge Caution .............................. 39
   12.7 Glossary ........................................................... 39
13 Mechanical, Packaging, and Orderable Information .......... 39

4 Revision History
NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision E (March 2016) to Revision F

<table>
<thead>
<tr>
<th>Changes</th>
<th>Page</th>
</tr>
</thead>
<tbody>
<tr>
<td>• Changed the title of the data sheet</td>
<td>1</td>
</tr>
<tr>
<td>• Changed all references of PowerPAD to thermal pad</td>
<td>4</td>
</tr>
<tr>
<td>• Changed the units of the current and peak current parameters from V to mA in the Absolute Maximum Ratings table</td>
<td>5</td>
</tr>
<tr>
<td>• Added the Receiving Notification of Documentation Updates section</td>
<td>39</td>
</tr>
</tbody>
</table>

Changes from Revision D (September 2011) to Revision E

<table>
<thead>
<tr>
<th>Changes</th>
<th>Page</th>
</tr>
</thead>
<tbody>
<tr>
<td>• Added Device Information table, Table of Contents, Revision History section, Pin Configuration and Functions section, Specifications section, ESD Ratings table, Detailed Description section, Application and Implementation section, Power Supply Recommendations section, Layout section, Device and Documentation Support section, and Mechanical, Packaging, and Orderable Information section</td>
<td>1</td>
</tr>
</tbody>
</table>
5 Description (continued)
The TPS65023-Q1 device also integrates two general-purpose 200-mA LDO voltage regulators, which are enabled with an external input pin. Each LDO operates with an input voltage range between 1.5 V and 6.5 V, allowing them to be supplied from one of the step-down converters or directly from the battery. The default output voltage of the LDOs can be digitally set to four different voltage combinations using the DEFLDO1 and DEFLDO2 pins. The serial interface can be used for dynamic voltage scaling, masking interrupts, or for disabling, enabling, and setting the LDO output voltages. The interface is compatible with the fast- or standard-mode I<sup>2</sup>C specifications, allowing transfers at up to 400 kHz. The TPS65023-Q1 device operates over a free-air temperature of –40°C to 125°C.

6 Pin Configuration and Functions
## Pin Functions

<table>
<thead>
<tr>
<th>PIN</th>
<th>I/O</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>SWITCHING REGULATOR</strong></td>
<td></td>
<td></td>
</tr>
<tr>
<td>AGND1</td>
<td>40</td>
<td>Analog ground. All analog ground pins are connected internally on the chip</td>
</tr>
<tr>
<td>AGND2</td>
<td>17</td>
<td>Analog ground. All analog ground pins are connected internally on the chip</td>
</tr>
<tr>
<td>DCDC1_EN</td>
<td>25</td>
<td>VDCDC1 enable pin. A logic high enables the regulator, a logic low disables the regulator</td>
</tr>
<tr>
<td>DCDC2_EN</td>
<td>24</td>
<td>VDCDC2 enable pin. A logic high enables the regulator, a logic low disables the regulator</td>
</tr>
<tr>
<td>DCDC3_EN</td>
<td>23</td>
<td>VDCDC3 enable pin. A logic high enables the regulator, a logic low disables the regulator</td>
</tr>
<tr>
<td>DEFDCDC1</td>
<td>10</td>
<td>Input for signal indicating default VDCDC1 voltage, 0 = 1.2 V, 1 = 1.6 V. DEFDCDC1 can also be connected to a resistor divider between VDCDC1 and GND, if the output voltage of the DCDC1 converter is set in a range from 0.8 V to VINDCDC1 V.</td>
</tr>
<tr>
<td>DEFDCDC2</td>
<td>32</td>
<td>Input for signal indicating default VDCDC2 voltage, 0 = 1.8 V, 1 = 3.3 V. DEFDCDC2 can also be connected to a resistor divider between VDCDC2 and GND, if the output voltage of the DCDC2 converter is set in a range from 0.8 V to VINDCDC2 V.</td>
</tr>
<tr>
<td>DEFDCDC3</td>
<td>1</td>
<td>Input for signal indicating default VDCDC3 voltage, 0 = 1.8 V, 1 = 3.3 V. DEFDCDC3 can also be connected to a resistor divider between VDCDC3 and GND, if the output voltage of the DCDC3 converter is set in a range from 0.8 V to VINDCDC3 V.</td>
</tr>
<tr>
<td>L1</td>
<td>7</td>
<td>Switch pin of VDCDC1 converter. The VDCDC1 inductor is connected here.</td>
</tr>
<tr>
<td>L2</td>
<td>35</td>
<td>Switch pin of VDCDC2 converter. The VDCDC2 inductor is connected here</td>
</tr>
<tr>
<td>L3</td>
<td>4</td>
<td>Switch pin of VDCDC3 converter. The VDCDC3 inductor is connected here</td>
</tr>
<tr>
<td>PGND1</td>
<td>8</td>
<td>Power ground for VDCDC1 converter</td>
</tr>
<tr>
<td>PGND2</td>
<td>34</td>
<td>Power ground for VDCDC2 converter</td>
</tr>
<tr>
<td>PGND3</td>
<td>3</td>
<td>Power ground for VDCDC3 converter</td>
</tr>
<tr>
<td>VCC</td>
<td>37</td>
<td>Power supply for digital and analog circuitry of VDCDC1, VDCDC2, and VDCDC3 DC-DC converters. VCC must be connected to the same voltage supply as VINDCDC1, VINDCDC2, and VINDCDC3. VCC also supplies serial interface block.</td>
</tr>
<tr>
<td>VDCDC1</td>
<td>9</td>
<td>VDCDC1 feedback voltage sense input. Connect directly to VDCDC1</td>
</tr>
<tr>
<td>VDCDC2</td>
<td>33</td>
<td>VDCDC2 feedback voltage sense input. Connect directly to VDCDC2</td>
</tr>
<tr>
<td>VDCDC3</td>
<td>2</td>
<td>VDCDC3 feedback voltage sense input. Connect directly to VDCDC3</td>
</tr>
<tr>
<td>VINDCDC1</td>
<td>6</td>
<td>Input for VDCDC1 step-down converter. VINDCDC1 must be connected to the same voltage supply as VINDCDC2, VINDCDC3, and VCC</td>
</tr>
<tr>
<td>VINDCDC2</td>
<td>36</td>
<td>Input for VDCDC2 step-down converter. VINDCDC2 must be connected to the same voltage supply as VINDCDC1, VINDCDC2, and VCC</td>
</tr>
<tr>
<td>VINDCDC3</td>
<td>5</td>
<td>Input for VDCDC3 step-down converter. VINDCDC3 must be connected to the same voltage supply as VINDCDC1, VINDCDC2, and VCC</td>
</tr>
<tr>
<td><strong>LDO REGULATOR</strong></td>
<td></td>
<td></td>
</tr>
<tr>
<td>DEFLD01</td>
<td>12</td>
<td>Digital input. DEFLD01 sets the default output voltage of LDO1 and LDO2</td>
</tr>
<tr>
<td>DEFLD02</td>
<td>13</td>
<td>Digital input. DEFLD02 sets the default output voltage of LDO1 and LDO2</td>
</tr>
<tr>
<td>LDO_EN</td>
<td>22</td>
<td>Enable input for LDO1 and LDO2. A logic high enables the LDOs, a logic low disables the LDOs</td>
</tr>
<tr>
<td>VBACKUP</td>
<td>15</td>
<td>Connect the backup battery to this input pin</td>
</tr>
<tr>
<td>VINLDO</td>
<td>19</td>
<td>Input for LDO1 and LDO2</td>
</tr>
<tr>
<td>VLOD1</td>
<td>20</td>
<td>Output of LDO1</td>
</tr>
<tr>
<td>VLOD2</td>
<td>18</td>
<td>Output of LDO2</td>
</tr>
<tr>
<td>VRTC</td>
<td>16</td>
<td>Output of the LDO/switch for the real time clock</td>
</tr>
<tr>
<td>VSYSEN</td>
<td>14</td>
<td>Input of system voltage for VRTC switch</td>
</tr>
<tr>
<td><strong>CONTROL AND I2C</strong></td>
<td></td>
<td></td>
</tr>
<tr>
<td>HOT_RESET</td>
<td>11</td>
<td>Push-button input that reboots or wakes up the processor through RESPWRON output pin</td>
</tr>
<tr>
<td>INT</td>
<td>28</td>
<td>Open drain output</td>
</tr>
<tr>
<td>LOW_BAT</td>
<td>21</td>
<td>Open-drain output of LOW_BAT comparator</td>
</tr>
<tr>
<td>LOWBAT_SNS</td>
<td>39</td>
<td>Input for the comparator driving the LOW_BAT output</td>
</tr>
<tr>
<td>PWRFAIL</td>
<td>31</td>
<td>Open-drain output. Active low when PWRFAIL comparator indicates low VBAT condition</td>
</tr>
</tbody>
</table>
Pin Functions (continued)

<table>
<thead>
<tr>
<th>PIN NAME</th>
<th>NO.</th>
<th>I/O</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>PWRFAIL_SNS</td>
<td>38</td>
<td>I</td>
<td>Input for the comparator driving the PWRFAIL output</td>
</tr>
<tr>
<td>RESPWRON</td>
<td>27</td>
<td>O</td>
<td>Open-drain system reset output</td>
</tr>
<tr>
<td>SCLK</td>
<td>30</td>
<td>I</td>
<td>Serial interface clock line</td>
</tr>
<tr>
<td>SDAT</td>
<td>29</td>
<td>I/O</td>
<td>Serial interface data/address</td>
</tr>
<tr>
<td>TRESPWRON</td>
<td>26</td>
<td>I</td>
<td>Connect the timing capacitor to TRESPWRON to set the reset delay time: 1 nF → 100 ms.</td>
</tr>
</tbody>
</table>

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)\(^{(1)}\)

<table>
<thead>
<tr>
<th></th>
<th>MIN</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>Input voltage(^{(2)}) All pins except AGND and PGND</td>
<td>–0.3</td>
<td>7</td>
<td>V</td>
</tr>
<tr>
<td>Current             L1, L2, L3, PGND1, PGND2, PGND3, VINDCDC1, VINDCDC2, VINDCDC3</td>
<td>2000</td>
<td>mA</td>
<td></td>
</tr>
<tr>
<td>Peak current        All pins except L1, L2, L3, PGND1, PGND2, PGND3, VINDCDC1, VINDCDC2, VINDCDC3</td>
<td>1000</td>
<td>mA</td>
<td></td>
</tr>
<tr>
<td>Operating free-air temperature</td>
<td>–40</td>
<td>125</td>
<td>°C</td>
</tr>
<tr>
<td>Maximum junction temperature, T(_{J(MAX)})</td>
<td>150</td>
<td>°C</td>
<td></td>
</tr>
<tr>
<td>Storage temperature, T(_{stg})</td>
<td>–65</td>
<td>150</td>
<td>°C</td>
</tr>
</tbody>
</table>

\(^{(1)}\) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

\(^{(2)}\) Voltages are in respect to AGND.

7.2 ESD Ratings

<table>
<thead>
<tr>
<th></th>
<th>VALUE</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>TPS65023-Q1 IN RHA PACKAGE</td>
<td></td>
<td></td>
</tr>
<tr>
<td>V(_{(ESD)}) Electrostatic discharge Human-body model (HBM), per AEC Q100-002(^{(1)})</td>
<td>±2000</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td>Charged-device model (CDM), per AEC Q100-011</td>
<td>±750</td>
</tr>
<tr>
<td></td>
<td>Machine model (MM)</td>
<td>±50</td>
</tr>
<tr>
<td>TPS65023-Q1 IN RSB PACKAGE</td>
<td></td>
<td></td>
</tr>
<tr>
<td>V(_{(ESD)}) Electrostatic discharge Human-body model (HBM), per AEC Q100-002(^{(1)})</td>
<td>±2000</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td>Charged-device model (CDM), per AEC Q100-011</td>
<td>±1000</td>
</tr>
<tr>
<td></td>
<td>Machine model (MM)</td>
<td>±100</td>
</tr>
</tbody>
</table>

\(^{(1)}\) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.
### 7.3 Recommended Operating Conditions

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Description</th>
<th>Minimum</th>
<th>Nominal</th>
<th>Maximum</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>( V_{CC} )</td>
<td>Input voltage range step-down converters</td>
<td>2.5</td>
<td>6</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>( V_{O} )</td>
<td>Output voltage range for VDCDC1 step-down converter(^{(1)})</td>
<td>0.6</td>
<td>( V_{CC} )</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>( V_{O} )</td>
<td>Output voltage range for VDCDC2 step-down converter(^{(1)})</td>
<td>0.6</td>
<td>( V_{CC} )</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>( V_{O} )</td>
<td>Output voltage range for VDCDC3 step-down converter(^{(1)})</td>
<td>0.6</td>
<td>( V_{CC} )</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>( V_{INLD0} )</td>
<td>Input voltage range for LDOs</td>
<td>1.5</td>
<td>6.5</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>( V_{O} )</td>
<td>Output voltage range for LDOs</td>
<td>1</td>
<td>( V_{CC} )</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>( I_{O(DCDC1)} )</td>
<td>Output current L1</td>
<td>1500 mA</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>( I_{O(DCDC2)} )</td>
<td>Output current L2</td>
<td>1200 mA</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>( I_{O(DCDC3)} )</td>
<td>Output current L3</td>
<td>1000 mA</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>( C_{L(DCDC1)} )</td>
<td>Inductor at L1(^{(2)})</td>
<td>1.5</td>
<td>2.2</td>
<td>( \mu )H</td>
<td></td>
</tr>
<tr>
<td>( C_{L(DCDC2)} )</td>
<td>Inductor at L2(^{(2)})</td>
<td>1.5</td>
<td>2.2</td>
<td>( \mu )H</td>
<td></td>
</tr>
<tr>
<td>( C_{L(DCDC3)} )</td>
<td>Inductor at L3(^{(2)})</td>
<td>1.5</td>
<td>2.2</td>
<td>( \mu )H</td>
<td></td>
</tr>
<tr>
<td>( C_{IN1} )</td>
<td>Input capacitor at VDCDC1(^{(3)})</td>
<td>10</td>
<td>( \mu )F</td>
<td></td>
<td></td>
</tr>
<tr>
<td>( C_{IN2} )</td>
<td>Input capacitor at VDCDC2(^{(3)})</td>
<td>10</td>
<td>( \mu )F</td>
<td></td>
<td></td>
</tr>
<tr>
<td>( C_{IN3} )</td>
<td>Input capacitor at VDCDC3(^{(3)})</td>
<td>10</td>
<td>( \mu )F</td>
<td></td>
<td></td>
</tr>
<tr>
<td>( C_{IN} )</td>
<td>Input capacitor at VCC(^{(3)})</td>
<td>10</td>
<td>22</td>
<td>( \mu )F</td>
<td></td>
</tr>
<tr>
<td>( C_{OUT1} )</td>
<td>Output capacitor at VDCDC1(^{(3)})</td>
<td>2.2</td>
<td>200 mA</td>
<td></td>
<td></td>
</tr>
<tr>
<td>( C_{OUT2} )</td>
<td>Output capacitor at VDCDC2(^{(3)})</td>
<td>2.2</td>
<td>200 mA</td>
<td></td>
<td></td>
</tr>
<tr>
<td>( C_{OUT3} )</td>
<td>Output capacitor at VDCDC3(^{(3)})</td>
<td>2.2</td>
<td>200 mA</td>
<td></td>
<td></td>
</tr>
<tr>
<td>( C_{OUT} )</td>
<td>Output capacitor at VLDO1, VLDO2(^{(3)})</td>
<td>2.2</td>
<td>200 mA</td>
<td></td>
<td></td>
</tr>
<tr>
<td>( T_{A} )</td>
<td>Operating ambient temperature</td>
<td>-40</td>
<td>125</td>
<td>°C</td>
<td></td>
</tr>
<tr>
<td>( T_{J} )</td>
<td>Operating junction temperature</td>
<td>-40</td>
<td>125</td>
<td>°C</td>
<td></td>
</tr>
<tr>
<td>( R )</td>
<td>Resistor from VINDCDC3, VINDCDC2, and VINDCDC1 to VCC used for filtering(^{(3)})</td>
<td>1</td>
<td>10</td>
<td>Ω</td>
<td></td>
</tr>
</tbody>
</table>

\(^{(1)}\) When using an external resistor divider at DEFDCDC3, DEFDCDC2, DEFDCDC1

\(^{(2)}\) See [Detailed Design Procedure](#) for more information.

\(^{(3)}\) Up to 3 mA can flow into VCC when all three converters are running in PWM. This resistor causes the UVLO threshold to be shifted accordingly.

### 7.4 Thermal Information

<table>
<thead>
<tr>
<th>THERMAL METRIC(^{(1)})</th>
<th>TPS65023-Q1</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>( R_{JA} )</td>
<td>Junction-to-ambient thermal resistance</td>
<td>31.6</td>
</tr>
<tr>
<td>( R_{JC(top)} )</td>
<td>Junction-to-case (top) thermal resistance</td>
<td>18.2</td>
</tr>
<tr>
<td>( R_{JB} )</td>
<td>Junction-to-board thermal resistance</td>
<td>6.6</td>
</tr>
<tr>
<td>( \psi_{JT} )</td>
<td>Junction-to-top characterization parameter</td>
<td>0.2</td>
</tr>
<tr>
<td>( \psi_{JB} )</td>
<td>Junction-to-board characterization parameter</td>
<td>6.5</td>
</tr>
<tr>
<td>( R_{JC(bot)} )</td>
<td>Junction-to-case (bottom) thermal resistance</td>
<td>1.7</td>
</tr>
</tbody>
</table>

\(^{(1)}\) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.
7.5 Electrical Characteristics

VINDCDC1 = VINDCDC2 = VINDCDC3 = VCC = V_INLDO = 3.6 V, V_BACKUP = 3 V, TA = −40°C to 125°C, typical values are at TA = 25°C (unless otherwise noted)

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>CONTROL SIGNALS: SCLK, SDAT (INPUT), DCDC1_EN, DCDC2_EN, DCDC3_EN, LDO_EN, DEFLDO1, DEFLDO2</td>
<td>VIH High-level input voltage</td>
<td>1.3</td>
<td>VCC</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td></td>
<td>VIL Low-level input voltage</td>
<td>0</td>
<td>0.4</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td></td>
<td>lIH Input bias current</td>
<td>0.01</td>
<td>0.1</td>
<td>μA</td>
<td></td>
</tr>
<tr>
<td>CONTROL SIGNALS: HOT_RESET</td>
<td>VIH High-level input voltage</td>
<td>1.3</td>
<td>VCC</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td></td>
<td>VIL Low-level input voltage</td>
<td>0</td>
<td>0.4</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td></td>
<td>lIH Input bias current</td>
<td>0.01</td>
<td>0.1</td>
<td>μA</td>
<td></td>
</tr>
<tr>
<td></td>
<td>tglitch Deglitch time at HOT_RESET</td>
<td>25</td>
<td>30</td>
<td>35</td>
<td>ms</td>
</tr>
<tr>
<td>CONTROL SIGNALS: LOWBAT, PWRFAIL, RESPWRON, INT, SDAT (OUTPUT)</td>
<td>VOH High-level output voltage</td>
<td>6</td>
<td>V</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>VOL Low-level output voltage</td>
<td>0</td>
<td>0.3</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td></td>
<td>lO Duration of low pulse at RESPWRON</td>
<td>100</td>
<td>ms</td>
<td></td>
<td></td>
</tr>
<tr>
<td>SUPPLY PINS: VCC, VINDCDC1, VINDCDC2, VINDCDC3</td>
<td>lO Operating quiescent current, PFM</td>
<td>85</td>
<td>100</td>
<td>μA</td>
<td></td>
</tr>
<tr>
<td></td>
<td>lI Current into VCC, PWM</td>
<td>2</td>
<td>3</td>
<td>mA</td>
<td></td>
</tr>
<tr>
<td></td>
<td>lQ Quiescent current</td>
<td>0.85</td>
<td>2</td>
<td></td>
<td></td>
</tr>
<tr>
<td>SUPPLY PINS: VBACKUP, V_SYSIN, VRTC</td>
<td>lO Operating quiescent current</td>
<td>20</td>
<td>33</td>
<td>μA</td>
<td></td>
</tr>
<tr>
<td></td>
<td>lQD Operating quiescent current</td>
<td>2</td>
<td>3</td>
<td>μA</td>
<td></td>
</tr>
<tr>
<td></td>
<td>lO Output current for VRTC</td>
<td>30</td>
<td>mA</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>lRTC Short-circuit current limit</td>
<td>100</td>
<td>mA</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>lO Output voltage accuracy for VRTC</td>
<td>−1%</td>
<td>1%</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
### Electrical Characteristics (continued)

\( V_{\text{INDCDC1}} = V_{\text{INDCDC2}} = V_{\text{INDCDC3}} = V_{\text{CC}} = V_{\text{INLDO}} = 3.6 \text{ V}, \ V_{\text{BACKUP}} = 3 \text{ V}, \ T_{\text{A}} = -40^\circ \text{C} \) to 125°C, typical values are at \( T_{\text{A}} = 25^\circ \text{C} \) (unless otherwise noted)

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>Line regulation for VRTC</td>
<td>( V_{\text{CC}} = V_{\text{RTC}} + 0.5 \text{ V} ) to 6.5 V, ( I_{\text{O}} = 5 \text{ mA} )</td>
<td>–1%</td>
<td>1%</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Load regulation VRTC</td>
<td>( I_{\text{O}} = 1 \text{ mA} ) to 30 mA, ( V_{\text{SYSIN}} = V_{\text{BACKUP}} = 0 \text{ V} )</td>
<td>–3%</td>
<td>1%</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Regulation time for VRTC</td>
<td>Load change from 10% to 90%</td>
<td>10</td>
<td>( \mu \text{s} )</td>
<td></td>
<td></td>
</tr>
<tr>
<td>( I_{\text{ST}} )</td>
<td>Input leakage current at VSYSIN</td>
<td>&lt; 2 ( \mu \text{A} )</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>( f_{\text{OFF(O)}} ) of VSYSIN switch</td>
<td>( V_{\text{SYSIN}} &lt; V_{\text{VSYSIN}} )</td>
<td>12.5</td>
<td>( \Omega )</td>
<td></td>
<td></td>
</tr>
<tr>
<td>( f_{\text{OFF(O)}} ) of VBACKUP switch</td>
<td></td>
<td>12.5</td>
<td>( \Omega )</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Input voltage range at VBACKUP(1)</td>
<td></td>
<td>2.73</td>
<td>3.75</td>
<td>( \text{V} )</td>
<td></td>
</tr>
<tr>
<td>Input voltage range at VSYSIN(1)</td>
<td></td>
<td>2.73</td>
<td>3.75</td>
<td>( \text{V} )</td>
<td></td>
</tr>
<tr>
<td>VSYSIN threshold</td>
<td>VSYSIN falling</td>
<td>–3%</td>
<td>2.55</td>
<td>3%</td>
<td>( \text{V} )</td>
</tr>
<tr>
<td>VSYSIN threshold</td>
<td>VSYSIN rising</td>
<td>–3%</td>
<td>2.65</td>
<td>3%</td>
<td>( \text{V} )</td>
</tr>
<tr>
<td>VBACKUP threshold</td>
<td>VBACKUP falling</td>
<td>–3%</td>
<td>2.55</td>
<td>3%</td>
<td>( \text{V} )</td>
</tr>
<tr>
<td>VBACKUP threshold</td>
<td>VBACKUP falling</td>
<td>–3%</td>
<td>2.65</td>
<td>3%</td>
<td>( \text{V} )</td>
</tr>
</tbody>
</table>

#### SUPPLY PIN: VINLDO

\( I_{\text{ID}} \) | Operating quiescent current | Current per LDO into VINLDO | 16 | 30 | \( \mu \text{A} \) |
| \( I_{\text{ID(O)}} \) | Shutdown current | Total current for both LDOs into VINLDO, \( V_{\text{INLDO}} = 0 \text{ V} \) | 0.1 | 1 | \( \mu \text{A} \) |

#### VDCDC1 STEP-DOWN CONVERTER

\( I_{\text{O}} \) | Maximum output current | 1500 | mA | | |
| \( I_{\text{ID(O)}} \) | Shutdown supply current in VINDC1 | DCDC1\_EN = GND | 0.1 | 1 | \( \mu \text{A} \) |
| \( f_{\text{DS(O)}} \) of P-channel MOSFET on-resistance | \( V_{\text{CC}} = V_{\text{GS(O)}} = 3.6 \text{ V} \) | 125 | 261 | m\( \Omega \) |
| \( I_{\text{ID}} \) | P-channel leakage current | \( V_{\text{CC}} = 6 \text{ V} \) | 2 | \( \mu \text{A} \) |
| \( f_{\text{DS(O)}} \) of N-channel MOSFET on-resistance | \( V_{\text{CC}} = V_{\text{GS(O)}} = 3.6 \text{ V} \) | 130 | 260 | m\( \Omega \) |
| \( I_{\text{ID}} \) | N-channel leakage current | \( V_{\text{GS(O)}} = 6 \text{ V} \) | 7 | 10 | \( \mu \text{A} \) |
| Forward current limit (P-channel and N-channel) | \( 2.5 \text{ V} + V_{\text{MAX}} < 6 \text{ V} \) | 1.9 | 2.19 | 2.6 | A |
| \( f_{\text{S}} \) | Oscillator frequency | 1.95 | 2.25 | 2.55 | MHz |

#### VDCDC2 STEP-DOWN CONVERTER

\( I_{\text{O}} \) | Maximum output current | \( V_{\text{CC}} = 3.6 \text{ V}, 3.3 \text{ V} – 1\% \leq V_{\text{DCDC2}} \leq 3.3 \text{ V} + 1\% \) | 1200 | mA | | |
| \( I_{\text{ID(O)}} \) | Shutdown supply current in VINDC2 | DCDC2\_EN = GND | 0.1 | 1 | \( \mu \text{A} \) |
| \( f_{\text{DS(O)}} \) of P-channel MOSFET on-resistance | \( V_{\text{DCDC2}} = V_{\text{GS(O)}} = 3.6 \text{ V} \) | 140 | 300 | m\( \Omega \) |
| \( I_{\text{ID}} \) | P-channel leakage current | \( V_{\text{CC}} = 6 \text{ V} \) | 2 | \( \mu \text{A} \) |
| \( f_{\text{DS(O)}} \) of N-channel MOSFET on-resistance | \( V_{\text{CC}} = V_{\text{GS(O)}} = 3.6 \text{ V} \) | 150 | 297 | m\( \Omega \) |
| \( I_{\text{ID}} \) | N-channel leakage current | \( V_{\text{GS(O)}} = 6 \text{ V} \) | 7 | 10 | \( \mu \text{A} \) |
| \( I_{\text{UF}} \) | Forward current limit (P-channel and N-channel) | \( 2.5 \text{ V} + V_{\text{CC}} < 6 \text{ V} \) | 1.7 | 1.94 | 2.2 | A |
| \( f_{\text{S}} \) | Oscillator frequency | 1.95 | 2.25 | 2.55 | MHz |

\( \text{(1)} \) Based on the requirements for the Intel PXA270 processor.

---

(1) Based on the requirements for the Intel PXA270 processor.
## Electrical Characteristics (continued)

VINDCDC1 = VINDCDC2 = VINDCDC3 = VCC = VINLDO = 3.6 V, VBACKUP = 3 V, T_A = –40°C to 125°C, typical values are at T_A = 25°C (unless otherwise noted).

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>Fixed output voltage</td>
<td>VDCDC2 = 1.8 V</td>
<td>VCC = 2.5 V to 6 V, 0 mA ≤ I_O ≤ 1.2 A</td>
<td>–2%</td>
<td>2%</td>
<td>mA</td>
</tr>
<tr>
<td>Adjustable output voltage with resistor divider at DEFDCDC2, FPWMDCDC2 = 0</td>
<td>VCC = VDCDC2 + 0.3 V (minimum 2.5 V) to 6 V, 0 mA ≤ I_O ≤ 1 A</td>
<td>–2%</td>
<td>2%</td>
<td>mA</td>
<td></td>
</tr>
<tr>
<td>Adjustable output voltage with resistor divider at DEFDCDC2, FPWMDCDC2 = 1</td>
<td>VCC = VDCDC2 + 0.3 V (minimum 2.5 V) to 6 V, 0 mA ≤ I_O ≤ 1 A</td>
<td>–1%</td>
<td>1%</td>
<td>mA</td>
<td></td>
</tr>
<tr>
<td>Line regulation</td>
<td>VCC = VDCDC2 + 0.3 V (minimum 2.5 V) to 6 V, I_O = 10 mA</td>
<td>0</td>
<td>%/V</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Load regulation</td>
<td>I_O = 10 mA to 1000 mA</td>
<td>0.25</td>
<td>%/A</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Soft-start ramp time</td>
<td>VDCDC2 ramping from 5% to 95% of target value</td>
<td>750</td>
<td>μs</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Internal resistance from L2 to GND</td>
<td></td>
<td>1</td>
<td>MO</td>
<td></td>
<td></td>
</tr>
<tr>
<td>VDCDC2 discharge resistance</td>
<td>DCDC2 discharge = 1</td>
<td>300</td>
<td>Ω</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**VDCDC3 STEP-DOWN CONVERTER**

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>I_O</td>
<td>Maximum output current</td>
<td>DEFDCDC3 = GND</td>
<td>1000</td>
<td>mA</td>
<td></td>
</tr>
<tr>
<td>I_GND</td>
<td>Shutdown supply current in VINDCDC3</td>
<td>DDCDC3_EN = GND</td>
<td>525</td>
<td>mA</td>
<td></td>
</tr>
<tr>
<td>I_GSD(max)</td>
<td>P-channel MOSFET on-resistance</td>
<td>VCC = V_GSD(max) = 3.6 V</td>
<td>310</td>
<td>mΩ</td>
<td></td>
</tr>
<tr>
<td>I_GS</td>
<td>P-channel leakage current</td>
<td>VCC = 6 V</td>
<td>0.1</td>
<td>μA</td>
<td></td>
</tr>
<tr>
<td>I_GSN(max)</td>
<td>N-channel MOSFET on-resistance</td>
<td>VCC = V_GSN(max) = 3.6 V</td>
<td>220</td>
<td>mΩ</td>
<td></td>
</tr>
<tr>
<td>I_GS</td>
<td>N-channel leakage current</td>
<td>V_GS(max) = 6 V</td>
<td>7</td>
<td>μA</td>
<td></td>
</tr>
<tr>
<td>Forward current limit (P-channel and N-channel)</td>
<td>2.5 V &lt; VCC &lt; 6 V</td>
<td>1.28</td>
<td>1.49</td>
<td>1.69</td>
<td>A</td>
</tr>
<tr>
<td>F_s</td>
<td>Oscillator frequency</td>
<td>1.95</td>
<td>2.25</td>
<td>2.55</td>
<td>MHz</td>
</tr>
</tbody>
</table>

**VLDO1 AND VLDO2 LOW DROPOUT REGULATORS**

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>V_I</td>
<td>Input voltage range for LDO1, 2</td>
<td></td>
<td>1.5</td>
<td>6.5</td>
<td>V</td>
</tr>
<tr>
<td>V_LDO</td>
<td>LDO1 output voltage range</td>
<td></td>
<td>1</td>
<td>3.15</td>
<td>V</td>
</tr>
<tr>
<td>V_LDD0</td>
<td>LDO2 output voltage range</td>
<td></td>
<td>1</td>
<td>3.3</td>
<td>V</td>
</tr>
<tr>
<td>I_O</td>
<td>Maximum output current for LDO1, LDO2</td>
<td>I_O = 50 mA, V_ILDO = 1.8 V</td>
<td>200</td>
<td>mA</td>
<td></td>
</tr>
<tr>
<td>I_GS</td>
<td>LDO1 and LDO2 short circuit current limit</td>
<td>V_NLD0 = GND, V_LDD0 = GND</td>
<td>400</td>
<td>mA</td>
<td></td>
</tr>
<tr>
<td>Minimum voltage drop at LDO1, LDO2</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Load regulation</td>
<td>I_O = 10 mA</td>
<td></td>
<td></td>
<td>1%</td>
<td></td>
</tr>
<tr>
<td>Line regulation</td>
<td>V_NLD0 = VLD0,2 + 0.5 V (minimum 2.5 V) to 6.5 V, I_O = 10 mA</td>
<td></td>
<td></td>
<td>1%</td>
<td></td>
</tr>
<tr>
<td>Load regulation</td>
<td>I_O = 0 mA to 50 mA</td>
<td></td>
<td></td>
<td>1%</td>
<td></td>
</tr>
<tr>
<td>Regulation time for LDO1, LDO2</td>
<td>Load change from 10% to 90%</td>
<td>10</td>
<td>μs</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
Electrical Characteristics (continued)

VIN\textsubscript{CDC1} = VIN\textsubscript{CDC2} = VIN\textsubscript{CDC3} = V\textsubscript{CC} = V\textsubscript{INLDO} = 3.6 V, V\textsubscript{BACKUP} = 3 V, T\textsubscript{A} = \textdegree40°C to 125°C, typical values are at T\textsubscript{A} = 25°C (unless otherwise noted)

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>ANALOG SIGNALS DEFDCDC1, DEFDCDC2, DEFDCDC3</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>V\textsubscript{HI}</td>
<td>High-level input voltage\textsuperscript{(2)}</td>
<td>1.3</td>
<td>V\textsubscript{CC}</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>V\textsubscript{IL}</td>
<td>Low-level input voltage</td>
<td>0</td>
<td>0.1</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>Input bias current</td>
<td></td>
<td>0.001</td>
<td>0.05</td>
<td>\mu A</td>
<td></td>
</tr>
<tr>
<td>THERMAL SHUTDOWN</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>T\textsubscript{(SD)}</td>
<td>Thermal shutdown</td>
<td>Increasing junction temperature</td>
<td>160</td>
<td>\degree C</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Thermal shutdown hysteresis</td>
<td>Decreasing junction temperature</td>
<td>20</td>
<td>\degree C</td>
<td></td>
</tr>
<tr>
<td>INTERNAL UNDervoltage LOCK OUT</td>
<td>VCC falling</td>
<td>V\textsubscript{UVLO}</td>
<td>2%</td>
<td>3.35</td>
<td>2%</td>
</tr>
<tr>
<td>V\textsubscript{UVLO_HYST}</td>
<td>Internal UVLO comparator hysteresis</td>
<td>120</td>
<td>mV</td>
<td></td>
<td></td>
</tr>
<tr>
<td>VOLTAGE DETECTOR COMPARATORS</td>
<td>Comparator threshold</td>
<td>Falling threshold</td>
<td>–2%</td>
<td>1</td>
<td>2%</td>
</tr>
<tr>
<td>Comparator threshold (PWRFAIL_SNS, LOWBAT_SNS)</td>
<td>Hysteresis</td>
<td>40</td>
<td>50</td>
<td>60</td>
<td>mV</td>
</tr>
<tr>
<td>Propagation delay</td>
<td>25-mV overdrive</td>
<td>10</td>
<td>\mu s</td>
<td></td>
<td></td>
</tr>
<tr>
<td>POWER GOOD</td>
<td>V\textsubscript{GOODF}</td>
<td>V\textsubscript{CDC1}, V\textsubscript{CDC2}, V\textsubscript{CDC3}, V\textsubscript{LDO1}, V\textsubscript{LDO2}, decreasing</td>
<td>–12%</td>
<td>–10%</td>
<td>–8%</td>
</tr>
<tr>
<td>V\textsubscript{GOODR}</td>
<td>V\textsubscript{CDC1}, V\textsubscript{CDC2}, V\textsubscript{CDC3}, V\textsubscript{LDO1}, V\textsubscript{LDO2}, increasing</td>
<td>–7%</td>
<td>–5%</td>
<td>–3%</td>
<td></td>
</tr>
</tbody>
</table>

\textsuperscript{(2)} The input voltage can go as high as 6 V. If the input voltage exceeds V\textsubscript{CC}, an input current of (V(PB_IN) - 0.7 V - V\textsubscript{CC}) / 10 k\Omega flows.

7.6 Timing Requirements

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>MIN</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>f\textsubscript{MAX}</td>
<td>Clock frequency</td>
<td>400</td>
<td>kHz</td>
<td></td>
</tr>
<tr>
<td>f\textsubscript{WH(HIGH)}</td>
<td>Clock high time</td>
<td>600</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>f\textsubscript{WL(LOW)}</td>
<td>Clock low time</td>
<td>1300</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>t\textsubscript{r}</td>
<td>DATA and CLK rise time</td>
<td>300</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>t\textsubscript{f}</td>
<td>DATA and CLK fall time</td>
<td>300</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>t\textsubscript{h(STA)}</td>
<td>Hold time (repeated) START condition (after this period the first clock pulse is generated)</td>
<td>600</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>t\textsubscript{h(DATA)}</td>
<td>Setup time for repeated START condition</td>
<td>600</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>t\textsubscript{h(DATA)}</td>
<td>Data input hold time</td>
<td>300</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>t\textsubscript{su(DATA)}</td>
<td>Data input setup time</td>
<td>300</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>t\textsubscript{su(STO)}</td>
<td>STOP condition setup time</td>
<td>600</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>t\textsubscript{(BUF)}</td>
<td>Bus free time</td>
<td>1300</td>
<td>ns</td>
<td></td>
</tr>
</tbody>
</table>

Figure 1. Serial Interface Timing Diagram

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7.7 Typical Characteristics

Table 1. EVM Parameters for Typical Characteristics Measurement

<table>
<thead>
<tr>
<th>CONVERTER</th>
<th>INDUCTOR</th>
<th>OUTPUT CAPACITOR</th>
<th>OUTPUT CAPACITOR VALUE</th>
</tr>
</thead>
<tbody>
<tr>
<td>VDCDC1</td>
<td>VLCF4020-2R2</td>
<td>C2012X5R0J106M</td>
<td>2 × 10 μF</td>
</tr>
<tr>
<td>VDCDC2</td>
<td>VLCF4020-2R2</td>
<td>C2012X5R0J106M</td>
<td>2 × 10 μF</td>
</tr>
<tr>
<td>VDCDC3</td>
<td>VLF4012AT-2R2M1R5</td>
<td>C2012X5R0J106M</td>
<td>2 × 10 μF</td>
</tr>
</tbody>
</table>

(1) Graphs were taken using the evaluation module (EVM), TPS65023EVM-205, with the inductor and output capacitor combinations in Table 1. See TPS65023EVM, User's Guide for more information.

Table 2. Table Of Graphs

<table>
<thead>
<tr>
<th>FIGURE</th>
</tr>
</thead>
<tbody>
<tr>
<td>Efficiency vs Output current</td>
</tr>
<tr>
<td>Output voltage vs Output current at 85°C</td>
</tr>
<tr>
<td>Line transient response</td>
</tr>
<tr>
<td>Load transient response</td>
</tr>
<tr>
<td>VDCDC2 PFM operation</td>
</tr>
<tr>
<td>VDCDC2 low ripple PFM operation</td>
</tr>
<tr>
<td>VDCDC2 PWM operation</td>
</tr>
<tr>
<td>Startup VDCDC1, VDCDC2 and VDCDC3</td>
</tr>
<tr>
<td>Startup LDO1 and LDO2</td>
</tr>
<tr>
<td>Line transient response</td>
</tr>
<tr>
<td>Load transient response</td>
</tr>
</tbody>
</table>

Figure 2. DCDC1: Efficiency vs Output Current

Figure 3. DCDC1: Efficiency vs Output Current
Figure 4. DCDC2: Efficiency vs Output Current

Figure 5. DCDC2: Efficiency vs Output Current

Figure 6. DCDC3: Efficiency vs Output Current

Figure 7. DCDC3: Efficiency vs Output Current

Figure 8. DCDC2: Output Voltage vs Output Current At 85°C

Figure 9. DCDC3: Output Voltage vs Output Current At 85°C
Figure 10. VDCDC1 Line Transient Response

Figure 11. VDCDC2 Line Transient Response

Figure 12. VDCDC3 Line Transient Response

Figure 13. VDCDC1 Load Transient Response

Figure 14. VDCDC2 Load Transient Response

Figure 15. VDCDC3 Load Transient Response
Figure 16. VDCDC2 Output Voltage Ripple

Figure 17. VDCDC2 Output Voltage Ripple

Figure 18. VDCDC2 Output Voltage Ripple

Figure 19. Startup VDCDC1, VDCDC2, and VDCDC3

Figure 20. Startup LDO1 and LDO2

Figure 21. LDO1 Line Transient Response
8 Detailed Description

8.1 Overview

The TPS65023-Q1 device has 5 regulator channels, 3 DCDCs, and 2 LDOs. DCDC3 has dynamic voltage scaling feature (DVS) that allows for power reduction to CORE supplies during idle operation or overvoltage during heavy-duty operation. With DVS and 2 more DCDCs plus 2 LDOs, the TPS65023-Q1 is ideal for CORE, Memory, IO, and peripheral power for the entire system of a wide range of suitable applications.

The device incorporates enables for the DCDCs and LDOs, I²C for device control, push button, and a reset interface that complete the system and allow the TPS65023-Q1 to be adapted for different kinds of processors or FPGAs.

For noise-sensitive circuits, the DCDCs can be synchronized out of phase from one another, reducing the peak noise at the switching frequency. Each converter can be forced to operate in PWM mode to ensure constant switching frequency across the entire load range. However, for low load efficiency performance the DCDCs automatically enter PSM mode which reduces the switching frequency when the load current is low, saving power at idle operation.

8.2 Functional Block Diagram
8.3 Feature Description

8.3.1 Step-Down Converters, VDCDC1, VDCDC2, and VDCDC3

The TPS65023-Q1 incorporates three synchronous step-down converters operating typically at 2.25 MHz fixed-frequency pulse-width modulation (PWM) at moderate to heavy load currents. At light load currents, the converters automatically enter the power-save mode (PSM), and operate with pulse-frequency modulation (PFM). The VDCDC1 converter is capable of delivering 1.5-A output current, the VDCDC2 converter is capable of delivering 1.2 A, and the VDCDC3 converter is capable of delivering up to 1 A.

The converter output voltages can be programmed through the DEFDCDC1, DEFDCDC2, and DEFDCDC3 pins. The pins can either be connected to GND, VCC, or to a resistor divider between the output voltage and GND. The VDCDC1 converter defaults to 1.2 V or 1.6 V, depending on the DEFDCDC1 configuration pin. If DEFDCDC1 is tied to ground, the default is 1.2 V. If it is tied to VCC, the default is 1.6 V. When the DEFDCDC1 pin is connected to a resistor divider, the output voltage can be set in the range of 0.6 V to VCC. See Application and Implementation for more details. The core voltage can be reprogrammed through the serial interface in the range of 0.8 V to 1.6 V with a programmable slew rate. The converter is forced into PWM operation while any programmed voltage change is underway, whether the voltage is being increased or decreased. The DEFCORE and DEFSLEW registers are used to program the output voltage and slew rate during voltage transitions.

The VDCDC2 converter defaults to 1.8 V or 3.3 V, depending on the DEFDCDC2 configuration pin. If DEFDCDC2 is tied to ground, the default is 1.8 V. If it is tied to VCC, the default is 3.3 V. When the DEFDCDC2 pin is connected to a resistor divider, the output voltage can be set in the range of 0.6 V to VCC.

The VDCDC3 converter defaults to 1.8 V or 3.3 V, depending on the DEFDCDC3 configuration pin. If DEFDCDC3 is tied to ground, the default is 1.8 V. If it is tied to VCC, the default is 3.3 V. When the DEFDCDC3 pin is connected to a resistor divider, the output voltage can be set in the range of 0.6 V to VCC.

The step-down converter outputs (when enabled) are monitored by power good (PG) comparators, the outputs of which are available through the serial interface. The outputs of the DC-DC converters can be optionally discharged through on-chip 300-Ω resistors when the DC-DC converters are disabled.

During PWM operation, the converters use a unique fast-response voltage-mode controller scheme with input-voltage feed-forward to achieve good line and load regulation, allowing the use of small ceramic input and output capacitors. At the beginning of each clock cycle initiated by the clock signal, the P-channel MOSFET switch is turned on. The inductor current ramps up until the comparator trips and the control logic turns off the switch. The current-limit comparator also turns off the switch if the current limit of the P-channel switch is exceeded. After the adaptive dead time used to prevent shoot-through current, the N-channel MOSFET rectifier is turned on, and the inductor current ramps down. The next cycle is initiated by the clock signal, again turning off the N-channel rectifier and turning on the P-channel switch.

The three DC-DC converters operate synchronized to each other with the VDCDC1 converter as the master. A 180° phase shift between the VDCDC1 switch turnon and the VDCDC2 and a further 90° shift to the VDCDC3 switch turnon decreases the input rms current, and smaller input capacitors can be used. This is optimized for a typical application where the VDCDC1 converter regulates a Li-Ion battery voltage of 3.7 V to 1.2 V, the VDCDC2 converter from 3.7 V to 1.8 V, and the VDCDC3 converter from 3.7 V to 3.3 V. The phase of the three converters can be changed using the CON_CTRL register.

8.3.2 Soft Start

Each of the three converters has an internal soft-start circuit that limits the inrush current during start-up. The soft start is realized by using a low initial current to charge the internal compensation capacitor. The soft-start time is typically 750 μs if the output voltage ramps from 5% to 95% of the final target value. If the output is already precharged to some voltage when the converter is enabled, then this time is reduced proportionally. There is a short delay of typically 170 μs between the converter being enabled and switching activity actually starting. This allows the converter to bias itself properly, to recognize if the output is precharged, and if so to prevent discharging of the output while the internal soft-start ramp catches up with the output voltage.
Feature Description (continued)

8.3.3 Active Discharge When Disabled
When the VDCDC1, VDCDC2, and VDCDC3 converters are disabled, due to an UVLO, DCDC_EN or OVERTEMP condition, it is possible to pull down the outputs actively. This feature is disabled per default and is individually enabled through the CON_CTRL2 register in the serial interface. When this feature is enabled, the VDCDC1, VDCDC2, and VDCDC3 outputs are discharged by a 300-Ω (typical) load which is active as long as the converters are disabled.

8.3.4 Power-Good Monitoring
All three step-down converters and both the LDO1 and LDO2 linear regulators have power-good comparators. Each comparator indicates when the relevant output voltage has dropped 10% below its target value with 5% hysteresis. The outputs of these comparators are available in the PGOODZ register through the serial interface. An interrupt is generated when any voltage rail drops below the 10% threshold. The comparators are disabled when the converters are disabled and the relevant PGOODZ register bits indicate that power is good.

8.3.5 Low-Dropout Voltage Regulators
The low-dropout voltage regulators are designed to operate well with low-value ceramic input and output capacitors. They operate with input voltages down to 1.5 V. The LDOs offer a maximum dropout voltage of 300 mV at rated output current. Each LDO supports a current-limit feature. Both LDOs are enabled by the LDO_EN pin, and both LDOs can be disabled or programmed through the serial interface using the REG_CTRL and LDO_CTRL registers. The LDOs also have reverse-conduction prevention. This allows the possibility to connect external regulators in parallel in systems with a backup battery. The TPS65023-Q1 step-down and LDO voltage regulators automatically power down when the Vcc voltage drops below the UVLO threshold or when the junction temperature rises above 160°C.

8.3.6 Undervoltage Lockout
The undervoltage-lockout circuit for the five regulators on the TPS65023-Q1 prevents the device from malfunctioning at low input voltages and from excessive discharge of the battery. It disables the converters and LDOs. The UVLO circuit monitors the Vcc pin, the threshold is set internally to 2.35 V with 5% (120 mV) hysteresis. Note that when any of the DC-DC converters are running, there is an input current at the Vcc pin, which is up to 3 mA when all three converters are running in PWM mode. This current must be considered if an external RC filter is used at the Vcc pin to remove switching noise from the TPS65023-Q1 internal analog circuitry supply.

8.4 Device Functional Modes

8.4.1 VRTC Output and Operation With or Without Backup Battery
The VRTC pin is an always-on output, intended to supply up to 30 mA to a permanently required rail (that is, for a real-time clock). The TPS65023-Q1 asserts the RESPWRON signal if VRTC drops below 2.4 V. VRTC is selected from a priority scheme based on the VSYSIN and VBACKUP inputs.

When the voltage at the VSYSIN pin exceeds 2.65 V, VRTC connects to the VSYSIN input through a PMOS switch and all other paths to VRTC are disabled. The PMOS switch drops a maximum of 375 mV at 30 mA, which should be considered when using VRTC. VSYSIN can be connected to any voltage source with the appropriate input voltage, including VCC or, if set to 3.3-V output, DCDC2 or DCDC3. When VSYSIN falls below 2.65 V or shorts to ground, the PMOS switch connecting VRTC and VSYSIN opens and VRTC then connects to either VBACKUP or the output of a dedicated 3-V, 30-mA LDO. TI recommends connecting VSYSIN to VCC or ground—VCC if a non-replaceable primary cell is connected to VBACKUP and ground if the VRTC output floats.

If the PMOS switch between VSYSIN and VRTC is open and VBACKUP exceeds 2.65 V, VRTC connects to VBACKUP through a PMOS switch. The PMOS switch drops a maximum of 375 mV at 30 mA, which should be considered if using VRTC. A typical application may connect VBACKUP to a primary Li button cell, but any battery that provides a voltage between 2.65 V and 6 V (that is, a single Li-Ion cell or a single boosted NiMH battery) is acceptable, to supply the VRTC output. In systems with no backup battery, the VBACKUP pin should be connected to GND.

If the switches between VRTC and VSYSIN or VBACKUP are open, the dedicated 3-V, 30-mA LDO, driven from VCC, connects to VRTC. This LDO is disabled if the voltage at the VSYSIN input exceeds 2.65 V.
Device Functional Modes (continued)

Inside TPS65023-Q1 there is a switch (\(V_{\text{MAX}}\) switch) which selects the higher voltage between \(V_{\text{CC}}\) and \(V_{\text{BACKUP}}\). This is used as the supply voltage for some basic functions. The functions powered from the output of the \(V_{\text{MAX}}\) switch are:

- INT output
- RESPWRON output
- HOT_RESET input
- LOW_BAT output
- PWRFAIL output
- Enable pins for DC-DC converters, LDO1 and LDO2
- Undervoltage lockout comparator (UVLO)
- Reference system with low-frequency timing oscillators
- LOW_BAT and PWRFAIL comparators

The main 2.25-MHz oscillator, and the \(I^2C\) interface are only powered from VCC.

A. \(V_{\text{VSYSIN}}, V_{\text{VBACKUP}}\) thresholds: falling = 2.55 V, rising = 2.65 V ±3%

B. RESPWRON thresholds: falling = 2.4 V, rising = 2.52 V ±3%

Figure 27. Power Switches Block Diagram
Device Functional Modes (continued)

8.4.2 Power-Save Mode Operation (PSM)

As the load current decreases, the converters enter the power-save mode of operation. During PSM, the converters operate in a burst mode (PFM mode) with a frequency between 750 kHz and 2.25 MHz, nominal, for one burst cycle. However, the frequency between different burst cycles depends on the actual load current and is typically far less than the switching frequency, with a minimum quiescent current to maintain high efficiency.

To optimize the converter efficiency at light load, the average current is monitored, and if in PWM mode the inductor current remains below a certain threshold, then PSM is entered. The typical threshold to enter PSM is calculated as follows:

\[
I_{\text{PFMDCDC1 enter}} = \frac{V_{\text{INDCDC1}}}{24 \Omega}
\]

\[
I_{\text{PFMDCDC2 enter}} = \frac{V_{\text{INDCDC2}}}{26 \Omega}
\]

\[
I_{\text{PFMDCDC3 enter}} = \frac{V_{\text{INDCDC3}}}{39 \Omega}
\]

(1)

During PSM, the output voltage is monitored with a comparator, and by maximum skip burst duration. As the output voltage falls below the threshold, set to the nominal \(V_O\), the P-channel switch turns on, and the converter effectively delivers a constant current defined as follows.

\[
I_{\text{PFMDCDC1 leave}} = \frac{V_{\text{INDCDC1}}}{18 \Omega}
\]

\[
I_{\text{PFMDCDC2 leave}} = \frac{V_{\text{INDCDC2}}}{20 \Omega}
\]

\[
I_{\text{PFMDCDC3 leave}} = \frac{V_{\text{INDCDC3}}}{29 \Omega}
\]

(2)

If the load is below the delivered current, then the output voltage rises until the same threshold is crossed in the other direction. All switching activity ceases, reducing the quiescent current to a minimum until the output voltage has again dropped below the threshold. The power-save mode is exited, and the converter returns to PWM mode if either of the following conditions is met:

- the output voltage drops 2% below the nominal \(V_O\) due to increasing load current
- the PFM burst time exceeds \(16 \times \frac{1}{f_S}\) (7.11 \(\mu\)s typical).

These control methods reduce the quiescent current to typically 14 \(\mu\)A per converter, and the switching activity to a minimum, thus achieving the highest converter efficiency. Setting the comparator thresholds at the nominal output voltage at light load current results in a low output-voltage ripple. The ripple depends on the comparator delay and the size of the output capacitor. Increasing capacitor values makes the output ripple tend to zero. The PSM is disabled through the I\(^2\)C interface to force the individual converters to stay in fixed-frequency PWM mode.

8.4.3 Low-Ripple Mode

Setting bit 3 in register CON-CTRL to 1 enables the low-ripple mode for all of the DC-DC converters if operated in PFM mode. For an output current less than approximately 10 mA, the output-voltage ripple in PFM mode is reduced, depending on the actual load current. The lower the actual output current on the converter, the lower the output ripple voltage. For an output current above 10 mA, there is only a minor difference in output-voltage ripple between PFM mode and low-ripple PFM mode. As this feature also increases switching frequency, it is used to keep the switching frequency above the audible range in PFM mode down to a low output current.
Device Functional Modes (continued)

8.4.4 100% Duty-Cycle Low-Dropout Operation

The TPS65023-Q1 converters offer a low input-to-output voltage difference while still maintaining operation with the use of the 100% duty-cycle mode. In this mode, the P-channel switch is constantly turned on. This is particularly useful in battery-powered applications to achieve longest operation time by taking full advantage of the whole battery voltage range. The minimum input voltage required to maintain DC regulation depends on the load current and output voltage. Use Equation 3 to calculate the minimum input voltage.

\[ V_{IN(min)} = V_{OUT(min)} + I_{OUT(max)} \times (r_{DS(on)}^\text{max} + R_L) \]

where

- \( I_{OUT(max)} \) = maximum load current (Note: ripple current in the inductor is zero under these conditions)
- \( r_{DS(on)}^\text{max} \) = maximum P-channel switch \( r_{DS(on)} \)
- \( R_L \) = DC resistance of the inductor
- \( V_{OUT(min)} \) = nominal output voltage minus 2% tolerance limit

8.4.5 System Reset and Control Signals

The \text{RESPWRON} signal can be used as a global reset for the application. It is an open-drain output. The \text{RESPWRON} signal is generated according to the power-good comparator of VRTC, and remains low for \( t_{\text{respwrn}} \) seconds after VRTC has risen above 2.52 V (falling threshold is 2.4 V, 5% hysteresis). \( t_{\text{respwrn}} \) is set by an external capacitor at the TRESPWRON pin. 1 nF gives typically 100 ms. \text{RESPWRON} is also triggered by the \text{HOT_RESET} input. This input is internally debounced, with a filter time of typically 30 ms.

The \text{PWRFAIL} and \text{LOW_BAT} signals are generated by two voltage detectors using the \text{PWRFAIL_SNS} and \text{LOWBAT_SNS} input signals. Each input signal is compared to a 1-V threshold (falling edge) with 5% (50 mV) hysteresis.

The DCDC1 converter is reset to its default output voltage defined by the \text{DEFDCDC1} input, when \text{HOT_RESET} is asserted. Other I^2C registers are not affected. Generally, the DCDC1 converter is set to its default voltage with one of these conditions: \text{HOT_RESET} active, VRTC lower than its threshold voltage, undervoltage lockout (UVLO) condition, or \text{RESPWRON} active.

8.4.5.1 \text{DEFLDO1} and \text{DEFLDO2}

These two pins are used to set the default output voltage of the two 200-mA LDOs. The digital value applied to the pins is latched during power up and determines the initial output voltage according to Table 3. The voltage of both LDOs can be changed during operation with the I^2C interface as described in the interface description.

<table>
<thead>
<tr>
<th>Table 3. VLDO1 and VLDO2 Voltage Options</th>
</tr>
</thead>
<tbody>
<tr>
<td>DEFLDO2</td>
</tr>
<tr>
<td>0</td>
</tr>
<tr>
<td>0</td>
</tr>
<tr>
<td>1</td>
</tr>
<tr>
<td>1</td>
</tr>
</tbody>
</table>

8.4.5.2 Interrupt Management and the \text{INT} Pin

The \text{INT} pin combines the outputs of the PGOOD comparators from each DC-DC converter and the LDOs. The \text{INT} pin is used as a \text{POWER_OK} pin to indicate when all enabled supplies are in regulation. The \text{INT} pin remains active (low state) during power up as long as all enabled power rails are below their regulation limit. Once the last enabled power rail is within regulation, the \text{INT} pin transitions to a high state.

During operation, if one of the enabled supplies goes out of regulation, \text{INT} transitions to a low state, and the corresponding bit in the PGOODZ register goes high. If the supply goes back to its regulation limits, \text{INT} transitions back to a high state.
While INT is in an active low state, reading the PGOODZ register through the I²C bus forces INT into a high-Z state. Because this pin requires an external pullup resistor, the INT pin transitions to a logic-high state even though the supply in question is still out of regulation. The corresponding bit in the PGOODZ register still indicates that the power rail is out of regulation.

Interrupts can be masked using the MASK register. The default operation is not to mask any DCDC or LDO interrupts, because these provide the POWER_OK function.

8.5 Programming

8.5.1 Power-Up Sequencing

The TPS65023-Q1 power-up sequencing is designed to be entirely flexible and customer driven. This is achieved by providing separate enable pins for each switch-mode converter and a common enable signal for the LDOs. The relevant control pins are described in Table 4.

<table>
<thead>
<tr>
<th>Table 4. Control Pins and Status Outputs For DC-DC Converters</th>
</tr>
</thead>
<tbody>
<tr>
<td>PIN NAME</td>
</tr>
<tr>
<td>----------</td>
</tr>
<tr>
<td>DEFDCDC3</td>
</tr>
<tr>
<td>DEFDCDC2</td>
</tr>
<tr>
<td>DEFDCDC1</td>
</tr>
<tr>
<td>DCDC3_EN</td>
</tr>
<tr>
<td>DCDC2_EN</td>
</tr>
<tr>
<td>DCDC1_EN</td>
</tr>
<tr>
<td>HOT_RESET</td>
</tr>
<tr>
<td>RESPWRON</td>
</tr>
<tr>
<td>TRESPWRON</td>
</tr>
</tbody>
</table>

8.5.2 Serial Interface

The serial interface is compatible with the standard- and fast-mode I²C specifications, allowing transfers at up to 400 kHz. The interface adds flexibility to the power-supply solution, enabling most functions to be programmed to new values, depending on the instantaneous application requirements and charger status to be monitored. Register contents remain intact as long as VCC remains above 2 V. The TPS65023-Q1 has a 7-bit address: 1001000; other addresses are available on contact with the factory. Attempting to read data from the register addresses not listed in this section results in FFh being read out.

For normal data transfer, DATA is allowed to change only when CLK is low. Changes when CLK is high are reserved for indicating the start and stop conditions. During data transfer, the data line must remain stable whenever the clock line is high. There is one clock pulse per bit of data. Each data transfer is initiated with a start condition and terminated with a stop condition. When addressed, the TPS65023-Q1 device generates an acknowledge bit after the reception of each byte. The master device (microprocessor) must generate an extra clock pulse that is associated with the acknowledge bit. The TPS65023-Q1 device must pull down the DATA line during the acknowledge clock pulse so that the DATA line is a stable low during the high period of the acknowledge clock pulse. The DATA line is a stable low during the high period of the acknowledge-related clock pulse. Setup and hold times must be taken into account. During read operations, a master must signal the end of data to the slave by not generating an acknowledge bit on the last byte that was clocked out of the slave. In this case, the slave TPS65023-Q1 device must leave the data line high to enable the master to generate the stop condition.
Figure 28. Bit Transfer on the Serial Interface

Figure 29. Start and Stop Conditions

Figure 30. Serial Interface Write to TPS65023-Q1 Device

Figure 31. Serial Interface Read from TPS65023-Q1: Protocol A
8.6 Register Maps

8.6.1 VERSION Register (address: 00h) Read-Only

Figure 33. VERSION Register Fields

<table>
<thead>
<tr>
<th>7</th>
<th>6</th>
<th>5</th>
<th>4</th>
<th>3</th>
<th>2</th>
<th>1</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>R-0</td>
<td>R-0</td>
<td>R-1</td>
<td>R-0</td>
<td>R-0</td>
<td>R-0</td>
<td>R-1</td>
<td>R-1</td>
</tr>
</tbody>
</table>

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Note: SLAVE = TPS65020

Figure 32. Serial Interface Read from TPS65023-Q1: Protocol B
8.6.2 **PGOODZ Register (address: 01h) Read-Only**

**Figure 34. PGOODZ Register Fields**

<table>
<thead>
<tr>
<th>Bit</th>
<th>Field</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>7</td>
<td>PWRFAILZ</td>
<td>R</td>
<td>0</td>
<td>Set by signal: PWRFAIL&lt;br&gt;0 = indicates that the PWRFAIL_SNS input voltage is above the 1-V threshold.&lt;br&gt;1 = indicates that the PWRFAIL_SNS input voltage is below the 1-V threshold.</td>
</tr>
<tr>
<td>6</td>
<td>LOWBATTZ</td>
<td>R</td>
<td>0</td>
<td>Set by signal: LOWBATT&lt;br&gt;0 = indicates that the LOWBATT_SNS input voltage is above the 1-V threshold.&lt;br&gt;1 = indicates that the LOWBATT_SNS input voltage is below the 1-V threshold.</td>
</tr>
<tr>
<td>5</td>
<td>PGOODZ VDCDC1</td>
<td>R</td>
<td>0</td>
<td>Set by signal: PGOODZ_VDCDC1&lt;br&gt;0 = indicates that the VDCDC1 converter output voltage is within its nominal range. This bit is zero if the VDCDC1 converter is disabled.&lt;br&gt;1 = indicates that the VDCDC1 converter output voltage is below its target regulation voltage.</td>
</tr>
<tr>
<td>4</td>
<td>PGOODZ VDCDC2</td>
<td>R</td>
<td>0</td>
<td>Set by signal: PGOODZ_VDCDC2&lt;br&gt;0 = indicates that the VDCDC2 converter output voltage is within its nominal range. This bit is zero if the VDCDC2 converter is disabled.&lt;br&gt;1 = indicates that the VDCDC2 converter output voltage is below its target regulation voltage.</td>
</tr>
<tr>
<td>3</td>
<td>PGOODZ VDCDC3</td>
<td>R</td>
<td>0</td>
<td>Set by signal: PGOODZ_VDCDC3&lt;br&gt;0 = indicates that the VDCDC3 converter output voltage is within its nominal range. This bit is zero if the VDCDC3 converter is disabled and during a DVM-controlled output-voltage transition.&lt;br&gt;1 = indicates that the VDCDC3 converter output voltage is below its target regulation voltage.</td>
</tr>
<tr>
<td>2</td>
<td>PGOODZ LDO2</td>
<td>R</td>
<td>0</td>
<td>Set by signal: PGOODZ_LDO2&lt;br&gt;0 = indicates that the LDO2 output voltage is within its nominal range. This bit is zero if LDO2 is disabled.&lt;br&gt;1 = indicates that LDO2 output voltage is below its target regulation voltage.</td>
</tr>
<tr>
<td>1</td>
<td>PGOODZ LDO1</td>
<td>R</td>
<td>0</td>
<td>Set by signal: PGOODZ_LDO1&lt;br&gt;0 = indicates that the LDO1 output voltage is within its nominal range. This bit is zero if LDO1 is disabled.&lt;br&gt;1 = indicates that the LDO1 output voltage is below its target regulation voltage.</td>
</tr>
</tbody>
</table>

**Table 5. PGOODZ Register Field Descriptions**

**LEGEND:** R/W = Read/Write; R = Read only; -n = value after reset
8.6.3 MASK Register (address: 02h)

The MASK register can be used to mask particular fault conditions from appearing at the INT pin. MASK<\text{n}> = 1 masks PGOODZ<\text{n}>.

8.6.4 REG_CTRL Register (address: 03h)

The REG_CTRL register is used to disable or enable the power supplies through the serial interface. The contents of the register are logically ANDed with the enable pins to determine the state of the supplies. A UVLO condition resets the REG_CTRL to 0xFF, so the state of the supplies defaults to the state of the enable pin. The REG_CTRL bits are automatically reset to default when the corresponding enable pin is low.
### 8.6.5 CON_CTRL Register (address: 04h)

The CON_CTRL register is used to force any or all of the converters into forced PWM operation when low output-voltage ripple is vital. It is also used to control the phase shift between the three converters to minimize the input rms current, hence reduce the required input blocking capacitance. The DCDC1 converter is taken as the reference and consequently has a fixed-zero phase shift.

#### Table 7. CON_CTRL Register Field Descriptions

<table>
<thead>
<tr>
<th>Bit</th>
<th>Field</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>7–6</td>
<td>DCDC2 PHASE1, PHASE0</td>
<td>R/W</td>
<td>10</td>
<td>DCDC2 Converter delay is set by these bits.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>00 = Zero</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>01 = 1/4 cycle</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>10 = 1/2 cycle</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>11 = 3/4 cycle</td>
</tr>
<tr>
<td>5–4</td>
<td>DCDC3 PHASE1, PHASE0</td>
<td>R/W</td>
<td>11</td>
<td>DCDC3 Converter delay is set by these bits.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>00 = Zero</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>01 = 1/4 cycle</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>10 = 1/2 cycle</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>11 = 3/4 cycle</td>
</tr>
<tr>
<td>3</td>
<td>LOW RIPPLE:</td>
<td>R/W</td>
<td>0</td>
<td>0 = PFM mode operation optimized for high efficiency for all converters</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1 = PFM mode operation optimized for low output-voltage ripple for all converters</td>
</tr>
<tr>
<td>2</td>
<td>FPWM DCDC2:</td>
<td>R/W</td>
<td>0</td>
<td>0 = DCDC2 converter operates in PWM or PFM mode</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1 = DCDC2 converter is forced into fixed-frequency PWM mode.</td>
</tr>
<tr>
<td>1</td>
<td>FPWM DCDC1:</td>
<td>R/W</td>
<td>0</td>
<td>0 = DCDC1 converter operates in PWM or PFM mode</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1 = DCDC1 converter is forced into fixed-frequency PWM mode.</td>
</tr>
<tr>
<td>0</td>
<td>FPWM DCDC3:</td>
<td>R/W</td>
<td>0</td>
<td>0 = DCDC3 converter operates in PWM or PFM mode</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1 = DCDC3 converter is forced into fixed-frequency PWM mode.</td>
</tr>
</tbody>
</table>
8.6.6 CON_CTRL2 Register (address: 05h)

The CON_CTRL2 register can be used to take control the inductive converters.

RESET(1): CON_CTRL2[6] is reset to its default value by one of these events:

- Undervoltage lockout (UVLO)
- HOT_RESET pulled low
- RESPWRON active
- VRTC below threshold

**Table 8. CON_CTRL2 Register Field Descriptions**

<table>
<thead>
<tr>
<th>Bit</th>
<th>Field</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>7</td>
<td>GO</td>
<td>R/W</td>
<td>0</td>
<td>0 = no change in the output voltage for the DCDC1 converter&lt;br&gt;1 = the output voltage of the DCDC1 converter is changed to the value defined in&lt;br&gt;DEFCORE with the slew rate defined in DEFSLEW. This bit is automatically&lt;br&gt;cleared when the DVM transition is complete. The transition is considered&lt;br&gt;complete in this case when the desired output voltage code has been reached,&lt;br&gt;not when the VDCDC3 output voltage is actually in regulation at the desired&lt;br&gt;voltage.</td>
</tr>
<tr>
<td>6</td>
<td>CORE ADJ allowed</td>
<td>R/W</td>
<td>1</td>
<td>0 = the output voltage is set with the I2C register&lt;br&gt;1 = DEFDCC1 is either connected to GND or VCC or an external voltage divider. When connected to GND or VCC, VDCDC1 defaults to 1.2 V or 1.6 V, respectively, at start-up.</td>
</tr>
<tr>
<td>2–0</td>
<td>DCDC2, DCDC1, DCDC3 discharge</td>
<td>R/W</td>
<td>000</td>
<td>0 = the output capacitor of the associated converter is not actively discharged when the converter is disabled.&lt;br&gt;1 = the output capacitor of the associated converter is actively discharged when the converter is disabled. This decreases the fall time of the output voltage at light load.</td>
</tr>
</tbody>
</table>
8.6.7 DEFCORE Register (address: 06h)

**Figure 39. DEFCORE Register Fields**

<table>
<thead>
<tr>
<th>Bit</th>
<th>Field</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>4–0</td>
<td>CORE4, CORE3, CORE2, CORE1, CORE0</td>
<td>R/W</td>
<td>10100</td>
<td>These bits set VDCDC1.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>00000 = 0.8 V</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>00001 = 0.825 V</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>00010 = 0.85 V</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>00011 = 0.875 V</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>00100 = 0.9 V</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>00101 = 0.925 V</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>00110 = 0.95 V</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>00111 = 0.975 V</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>01000 = 1 V</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>01001 = 1.025 V</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>01010 = 1.05 V</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>01011 = 1.075 V</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>01100 = 1.1 V</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>01101 = 1.125 V</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>01110 = 1.15 V</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>01111 = 1.175 V</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>10000 = 1.2 V</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>10001 = 1.225 V</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>10010 = 1.25 V</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>10011 = 1.275 V</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>10100 = 1.3 V</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>10101 = 1.325 V</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>10110 = 1.35 V</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>10111 = 1.375 V</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>11000 = 1.4 V</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>11001 = 1.425 V</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>11010 = 1.45 V</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>11011 = 1.475 V</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>11100 = 1.5 V</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>11101 = 1.525 V</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>11110 = 1.55 V</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>11111 = 1.6 V</td>
</tr>
</tbody>
</table>

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

**RESET(1): DEFCORE is reset to its default value by one of these events:**

- Undervoltage lockout (UVLO)
- HOT_RESET pulled low
- RESPWRON active
- VRTC below threshold

**Table 9. DEFCORE Register Field Descriptions**

<table>
<thead>
<tr>
<th>Bit</th>
<th>Field</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>4–0</td>
<td>CORE4, CORE3, CORE2, CORE1, CORE0</td>
<td>R/W</td>
<td>10100</td>
<td>These bits set VDCDC1.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>00000 = 0.8 V</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>00001 = 0.825 V</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>00010 = 0.85 V</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>00011 = 0.875 V</td>
</tr>
<tr>
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<td></td>
<td>00100 = 0.9 V</td>
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<tr>
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<td></td>
<td></td>
<td>00101 = 0.925 V</td>
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<tr>
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<td></td>
<td></td>
<td></td>
<td>00110 = 0.95 V</td>
</tr>
<tr>
<td></td>
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<td></td>
<td></td>
<td>00111 = 0.975 V</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>01000 = 1 V</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>01001 = 1.025 V</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>01010 = 1.05 V</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>01011 = 1.075 V</td>
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<tr>
<td></td>
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<td></td>
<td></td>
<td>01100 = 1.1 V</td>
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<td></td>
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<td></td>
<td>01101 = 1.125 V</td>
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<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>01110 = 1.15 V</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>01111 = 1.175 V</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>10000 = 1.2 V</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>10001 = 1.225 V</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>10010 = 1.25 V</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>10011 = 1.275 V</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>10100 = 1.3 V</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>10101 = 1.325 V</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>10110 = 1.35 V</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>10111 = 1.375 V</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>11000 = 1.4 V</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>11001 = 1.425 V</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>11010 = 1.45 V</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>11011 = 1.475 V</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>11100 = 1.5 V</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>11101 = 1.525 V</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>11110 = 1.55 V</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>11111 = 1.6 V</td>
</tr>
</tbody>
</table>
8.6.8 DEFSLEW Register (address: 07h)

**Figure 40. DEFSLEW Register Fields**

<table>
<thead>
<tr>
<th>Bit</th>
<th>Field</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0–2</td>
<td>SLEW2, SLEW1, SLEW0</td>
<td>R/W</td>
<td>110</td>
<td>These bits set the VDCDC1 SLEW RATE</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>000 = 0.225 mV/μs</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>001 = 0.45 mV/μs</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>010 = 0.9 mV/μs</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>011 = 1.8 mV/μs</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>100 = 3.6 mV/μs</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>101 = 7.2 mV/μs</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>110 = 14.4 mV/μs</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>111 = Immediate</td>
</tr>
</tbody>
</table>

**Table 10. DEFSLEW Register Field Descriptions**

<table>
<thead>
<tr>
<th>Bit</th>
<th>Field</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>6–4</td>
<td>LDO2_2, LDO2_1, LDO2_0</td>
<td>R/W</td>
<td>See (1)</td>
<td>000 = 1.05 V</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>001 = 1.2 V</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>010 = 1.3 V</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>011 = 1.8 V</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>100 = 2.5 V</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>101 = 2.8 V</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>110 = 3 V</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>111 = 3.3 V</td>
</tr>
</tbody>
</table>

**Table 11. LDO_CTRL Register Field Descriptions**

<table>
<thead>
<tr>
<th>Bit</th>
<th>Field</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>6–4</td>
<td>LDO2_2, LDO2_1, LDO2_0</td>
<td>R/W</td>
<td>See (1)</td>
<td>000 = 1 V</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>001 = 1.1 V</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>010 = 1.3 V</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>011 = 1.8 V</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>100 = 2.2 V</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>101 = 2.6 V</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>110 = 2.8 V</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>111 = 3.15 V</td>
</tr>
</tbody>
</table>

(1) Table 3 describes the default voltage options based on DEFLDO1 and DEFLDO2 pins.
9 Application and Implementation

NOTE
Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI’s customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

9.1.1 Reset Condition of DCDC1
If DEFDCDC1 is connected to ground and DCDC1_EN is pulled high after VINDCDC1 is applied, the output voltage of DCDC1 defaults to 1.225 V instead of 1.2 V (high by 2%). Figure 42 illustrates the problem.

![Figure 42. Default DCDC1](image)

Workaround 1: Tie DCDC1_EN to VINDCDC1 (Figure 43)

![Figure 43. Workaround 1](image)
Application Information (continued)

Workaround 2: Write the correct voltage to the DEF_CORE register through I²C. This can be done before or after the converter is enabled. If written before the enable, the only bit changed is DEF_CORE[0]. The voltage is 1.2 V, however, when the enable is pulled high (Figure 44).

![Figure 44. Workaround 2](image)

Workaround 3: Generate a HOT_RESET after enabling DCDC1 (Figure 45)

![Figure 45. Workaround 3](image)
9.2 Typical Application

Figure 46. Typical Configuration for the Texas Instruments TMS320DM644x DaVinci Processors

9.2.1 Design Requirements

The TPS65023-Q1 devices have only a few design requirements. Use the following parameters for the design examples:

- 1-μF bypass capacitor on VCC, located as close as possible to the VCC pin to ground.
- VCC and VINDCDCx must be connected to the same voltage supply with minimal voltage difference.
- Input capacitors must be present on the VINDCDCx and VIN_LDO supplies if used.
- Output inductor and capacitors must be used on the outputs of the DC-DC converters if used.
- Output capacitors must be used on the outputs of the LDOs if used.
Typical Application (continued)

9.2.2 Detailed Design Procedure

9.2.2.1 Inductor Selection for the DC-DC Converters

Each of the converters in the TPS65023-Q1 typically uses a 2.2-μH output inductor. Larger or smaller inductor values are used to optimize the performance of the device for specific operation conditions. The selected inductor must be rated for its DC resistance and saturation current. The DC resistance of the inductance influences directly the efficiency of the converter. Therefore, an inductor with lowest DC resistance should be selected for highest efficiency.

For a fast transient response, TI recommends a 2.2-μH inductor in combination with a 22-μF output capacitor.

**Equation 4** calculates the maximum inductor current under static load conditions. The saturation current of the inductor should be rated higher than the maximum inductor current as calculated with **Equation 4**. This is needed because during a heavy load transient the inductor current rises above the value calculated under **Equation 4**.

\[
\Delta I_L = V_{OUT} \times \frac{1 - \frac{V_{OUT}}{V_{IN}}}{L \times f} 
\]

\[
I_{L(max)} = I_{OUT(max)} + \frac{\Delta I_L}{2} 
\]

where
- \(f\) = Switching frequency (2.25 MHz typical)
- \(L\) = Inductor value
- \(\Delta I_L\) = Peak-to-peak inductor ripple current
- \(I_{LMAX}\) = Maximum inductor current

The highest inductor current occurs at maximum \(V_{IN}\).

Open-core inductors have a soft saturation characteristic, and they can usually handle higher inductor currents versus a comparable shielded inductor.

A more-conservative approach is to select the inductor current rating just for the maximum switch current of the TPS65023-Q1 (2 A for the VDCDC1 and VDCDC2 converters, and 1.5 A for the VDCDC3 converter). The core material from inductor to inductor differs and has an impact on the efficiency, especially at high switching frequencies.

See **Table 12** and the typical applications for possible inductors.

**Table 12. Tested Inductors**

<table>
<thead>
<tr>
<th>DEVICE</th>
<th>INDUCTOR VALUE</th>
<th>TYPE</th>
<th>COMPONENT SUPPLIER</th>
</tr>
</thead>
<tbody>
<tr>
<td>All converters</td>
<td>2.2 μH</td>
<td>LPS4012-222LMB</td>
<td>Coilcraft</td>
</tr>
<tr>
<td></td>
<td>2.2 μH</td>
<td>VLCF4020T-2R2N1R7</td>
<td>TDK</td>
</tr>
</tbody>
</table>

9.2.2.2 Output Capacitor Selection

The advanced fast-response voltage-mode control scheme of the inductive converters implemented in the TPS65023-Q1 allow the use of small ceramic capacitors with a typical value of 10 μF for each converter without having large output-voltage under- and overshoots during heavy load transients. Ceramic capacitors having low ESR values have the lowest output-voltage ripple and are recommended. See **Table 13** for recommended components.

If ceramic output capacitors are used, the capacitor rms ripple-current rating always meets the application requirements. Just for completeness, the rms ripple current is calculated as:

\[
I_{RMS\text{OUT}} = V_{OUT} \times \frac{1 - \frac{V_{OUT}}{V_{IN}}}{L \times f} \times \frac{1}{2 \sqrt{3}} 
\]

(6)
At nominal load current, the inductive converters operate in PWM mode. The overall output-voltage ripple is the sum of the voltage spike caused by the output capacitor ESR plus the voltage ripple caused by charging and discharging the output capacitor:

$$\Delta V_{OUT} = V_{OUT} \times \frac{1 - \frac{V_{OUT}}{V_{IN}}}{L \times f} \times \left( \frac{1}{8 \times C_{OUT} \times f} + ESR \right)$$

where

- the highest output-voltage ripple occurs at the highest input-voltage \( V_{IN} \) \( \text{(7)} \)

At light load currents, the converters operate in PSM and the output-voltage ripple is dependent on the output-capacitor value. The output-voltage ripple is set by the internal comparator delay and the external capacitor. The typical output-voltage ripple is less than 1% of the nominal output voltage.

### 9.2.2.3 Input Capacitor Selection

Because of the nature of the buck converter having a pulsating input current, a low-ESR input capacitor is required for best input-voltage filtering and minimizing the interference with other circuits caused by high input-voltage spikes. Each DC-DC converter requires a 10-μF ceramic input capacitor on its input pin VINDCDCx. The input capacitor is increased without any limit for better input-voltage filtering. The VCC pin is separated from the input for the DC-DC converters. A filter resistor of up to 10Ω and a 1-μF capacitor are used for decoupling the VCC pin from switching noise. Note that the filter resistor may affect the UVLO threshold, because up to 3 mA can flow through this resistor into the VCC pin when all converters are running in PWM mode.

#### Table 13. Possible Capacitors

<table>
<thead>
<tr>
<th>CAPACITOR VALUE</th>
<th>CASE SIZE</th>
<th>COMPONENT SUPPLIER</th>
<th>COMMENTS</th>
</tr>
</thead>
<tbody>
<tr>
<td>22 μF</td>
<td>1206</td>
<td>TDK C3216X5R0J226M</td>
<td>Ceramic</td>
</tr>
<tr>
<td>22 μF</td>
<td>1206</td>
<td>Taiyo Yuden JMK316BJ226ML</td>
<td>Ceramic</td>
</tr>
<tr>
<td>22 μF</td>
<td>0805</td>
<td>TDK C2012X5R0J226MT</td>
<td>Ceramic</td>
</tr>
<tr>
<td>22 μF</td>
<td>0805</td>
<td>Taiyo Yuden JMK212BJ226MG</td>
<td>Ceramic</td>
</tr>
<tr>
<td>10 μF</td>
<td>0805</td>
<td>Taiyo Yuden JMK212BJ106M</td>
<td>Ceramic</td>
</tr>
<tr>
<td>10 μF</td>
<td>0805</td>
<td>TDK C2012X5R0J106M</td>
<td>Ceramic</td>
</tr>
</tbody>
</table>

### 9.2.2.4 Output Voltage Selection

The DEFDCDC1, DEFDCDC2, and DEFDCDC3 pins are used to set the output voltage for each step-down converter. See Table 14 for the default voltages if the pins are pulled to GND or to VCC. If a different voltage is needed, an external resistor divider can be added to the DEFDCDCx pin as shown in Figure 47.

The output voltage of VDCDC1 is set with the \(^{2}\text{C}\) interface. If the voltage is changed from the default, using the DEFCORE register, the output voltage only depends on the register value. Any resistor divider at DEFDCDC1 does not change the voltage set with the register.

#### Table 14. DCDC1, DCDC2, and DCDC3 Default Voltage Levels

<table>
<thead>
<tr>
<th>PIN</th>
<th>LEVEL</th>
<th>DEFAULT OUTPUT VOLTAGE</th>
</tr>
</thead>
<tbody>
<tr>
<td>DEFDCDC1</td>
<td>VCC</td>
<td>1.6 V</td>
</tr>
<tr>
<td></td>
<td>GND</td>
<td>1.2 V</td>
</tr>
<tr>
<td>DEFDCDC2</td>
<td>VCC</td>
<td>3.3 V</td>
</tr>
<tr>
<td></td>
<td>GND</td>
<td>1.8 V</td>
</tr>
<tr>
<td>DEFDCDC3</td>
<td>VCC</td>
<td>3.3 V</td>
</tr>
<tr>
<td></td>
<td>GND</td>
<td>1.8 V</td>
</tr>
</tbody>
</table>
Using an external resistor divider at DEFDCDCx:

![Diagram](image-url)

**Figure 47. External Resistor Divider**

When a resistor divider is connected to DEFDCDCx, the output voltage can be set from 0.6 V up to the input voltage $V_{\text{bat}}$. The total resistance ($R_1 + R_2$) of the voltage divider should be kept in the 1-MR range to maintain a high efficiency at light load.

$$V_{\text{DEFDCDCx}} = 0.6 \text{ V}$$

$$V_{\text{OUT}} = V_{\text{DEFDCDCx}} \times \frac{R_1 + R_2}{R_2} \quad R_1 = R_2 \times \left( \frac{V_{\text{OUT}}}{V_{\text{DEFDCDCx}}} \right) - R_2$$

(8)

### 9.2.2.5 VRTC Output

TI recommends adding a 4.7-$\mu$F (minimum) capacitor to the VRTC pin.

### 9.2.2.6 LDO1 and LDO2

The LDOs in the TPS65023-Q1 are general-purpose LDOs which are stable using ceramic capacitors. The minimum output capacitor required is 2.2 $\mu$F. The LDO output voltages can be changed to different values between 1 V and 3.3 V using the I$^2$C interface. Therefore, they can also be used as general-purpose LDOs in applications powering processors different from DaVinci processors. The supply voltage for the LDOs must be connected to the VINLDO pin, giving the flexibility to connect the lowest voltage available in the system and providing the highest efficiency.

### 9.2.2.7 TRESPWRON

This is the input to a capacitor that defines the reset delay time after the voltage at VRTC rises above 2.52 V. The timing is generated by charging and discharging the capacitor with a current of 2 $\mu$A between a threshold of 0.25 V and 1 V for 128 cycles. A 1-nF capacitor gives a delay time of 100 ms.

$$t_{\text{reset}} = 2 \times 128 \times \left( \frac{1 \text{ V} - 0.25 \text{ V}}{2 \text{ \mu A}} \right)$$

where

- $t_{\text{reset}}$ is the reset delay time
- $C_{\text{reset}}$ is the capacitor connected to the TRESPWRON pin

(9)
### 9.2.2.8 \( V_{CC} \) Filter

An RC filter connected at the VCC input is used to keep noise from the internal supply for the band-gap and other analog circuitry. A typical value of 1 Ω and 1 μF is used to filter the switching spikes generated by the DC-DC converters. A larger resistor than 10 Ω should not be used, because the current into VCC of up to 3 mA causes a voltage drop at the resistor causing the undervoltage lockout circuitry connected at VCC internally to switch off too early.

### 9.2.3 Application Curves

Graphs were taken using the EVM with the inductor and output capacitor combinations found in Table 1.

![Figure 48. DCDC1 Efficiency](image1.png)

![Figure 49. DCDC2 Efficiency](image2.png)

![Figure 50. DCDC3 Efficiency](image3.png)

### 10 Power Supply Recommendations

For a supply voltage on pins VCC, VINDCDC1, VINDCDC2, and VINDCDC3 below 3 V, TI recommends enabling the DCDC1, DCDC2, and DCDC3 converters in sequence. If all 3 step-down converters are enabled at the same time while the supply voltage is close to the internal reset detection threshold, a reset may be generated during power up. Therefore TI recommends enabling the DC-DC converters in sequence. This can be done by driving one or two of the enable pins with a RC delay or by driving the enable pin by the output voltage of one of the other step-down converters. If a voltage above 3 V is applied on pin VBACKUP while VCC and VINDCDCx is below 3 V, there is no restriction in the power-up sequencing as VBACKUP is used to power the internal circuitry.
11 Layout

11.1 Layout Guidelines

As for all switching power supplies, the layout is an important step in the design. Proper function of the device demands careful attention to PCB layout. Take care in board layout to get the specified performance. If the layout is not carefully done, the regulators may show poor line, load regulation, or both, along with stability issues and EMI problems. It is critical to provide a low impedance ground path. Therefore, use wide and short traces for the main current paths. The input capacitors must be placed as close as possible to the IC pins as well as the inductor and output capacitor.

For the TPS65023-Q1 device, connect the PGND pins of the device to the thermal pad land of the PCB and connect the analog ground connections (AGND) to the PGND at the thermal pad. It is essential to provide a good thermal and electrical connection of all GND pins using multiple vias to the GND-plane. Keep the common path to the AGND pins, which returns the small signal components, and the high current of the output capacitors as short as possible to avoid ground noise. The VDCDCx line must be connected right to the output capacitor and routed away from noisy components and traces (for example, the L1, L2, and L3 traces).

11.2 Layout Example

Figure 51. Layout Example of a DC-DC Converter
12 Device and Documentation Support

12.1 Device Support

12.1.1 Third-Party Products Disclaimer
TI'S PUBLICATION OF INFORMATION REGARDING THIRD-PARTY PRODUCTS OR SERVICES DOES NOT CONSTITUTE AN ENDORSEMENT REGARDING THE SUITABILITY OF SUCH PRODUCTS OR SERVICES OR A WARRANTY, REPRESENTATION OR ENDORSEMENT OF SUCH PRODUCTS OR SERVICES, EITHER ALONE OR IN COMBINATION WITH ANY TI PRODUCT OR SERVICE.

12.2 Documentation Support

12.2.1 Related Documentation
For related documentation see the following:
- Texas Instruments, Choosing an Appropriate Pull-up/Pull-down Resistor for Open Drain Outputs application report
- Texas Instruments, Power Supply Design for NXP i.MX 7 Using the TPS65023 application report
- Texas Instruments, Power Supply Design for NXP i.MX 6 Using the TPS65023 application report
- Texas Instruments, TPS65023EVM User's Guide

12.3 Receiving Notification of Documentation Updates
To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on Alert me to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.4 Community Resources
The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community TI's Engineer-to-Engineer (E2E) Community. Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support TI's Design Support Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.5 Trademarks
DaVinci, E2E are trademarks of Texas Instruments.
All other trademarks are the property of their respective owners.

12.6 Electrostatic Discharge Caution
These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.7 Glossary
SLYZ022 — TI Glossary.
This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information
The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.
PACKAGING INFORMATION

<table>
<thead>
<tr>
<th>Orderable Device</th>
<th>Status (1)</th>
<th>Package Type</th>
<th>Package Drawing</th>
<th>Pins</th>
<th>Package Qty</th>
<th>Eco Plan (2)</th>
<th>Lead/Ball Finish (6)</th>
<th>MSL Peak Temp (3)</th>
<th>Op Temp (°C)</th>
<th>Device Marking (4/5)</th>
<th>Samples</th>
</tr>
</thead>
<tbody>
<tr>
<td>TPS65023QRHARQ1</td>
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<td>VQFN</td>
<td>RHA</td>
<td>40</td>
<td>3000</td>
<td>Green (RoHS &amp; no Sb/Br)</td>
<td>CU NIPDAU</td>
<td>Level-3-260C-168 HR</td>
<td>-40 to 125</td>
<td>65023Q RHA</td>
<td>Samples</td>
</tr>
<tr>
<td>TPS65023QRSBRQ1</td>
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<td>WQFN</td>
<td>RSB</td>
<td>40</td>
<td>3000</td>
<td>Green (RoHS &amp; no Sb/Br)</td>
<td>CU NIPDAU</td>
<td>Level-3-260C-168 HR</td>
<td>-40 to 125</td>
<td>TPS 65023Q</td>
<td>Samples</td>
</tr>
</tbody>
</table>

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBsolete: TI has discontinued the production of the device.

(2) RoHS: TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.
OTHER QUALIFIED VERSIONS OF TPS65023-Q1:

- Catalog: TPS65023

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
TAPE AND REEL INFORMATION

<table>
<thead>
<tr>
<th>Device</th>
<th>Package Type</th>
<th>Package Drawing</th>
<th>Pins</th>
<th>SPQ</th>
<th>Reel Diameter (mm)</th>
<th>Reel Width W1 (mm)</th>
<th>A0  (mm)</th>
<th>B0  (mm)</th>
<th>K0  (mm)</th>
<th>P1  (mm)</th>
<th>W   (mm)</th>
<th>Pin 1 Quadrant</th>
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</thead>
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<td>8.0</td>
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<td>Q2</td>
</tr>
</tbody>
</table>

*All dimensions are nominal.

**TAPE DIMENSIONS**

- **A0**: Dimension designed to accommodate the component width
- **B0**: Dimension designed to accommodate the component length
- **K0**: Dimension designed to accommodate the component thickness
- **W**: Overall width of the carrier tape
- **P1**: Pitch between successive cavity centers

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**

- **Q1**, **Q2**, **Q3**, **Q4**: Pocket Quadrants
- **Sprocket Holes**: Points where tape is folded
- **User Direction of Feed**: Direction in which tape is fed
## TAPE AND REEL BOX DIMENSIONS

<table>
<thead>
<tr>
<th>Device</th>
<th>Package Type</th>
<th>Package Drawing</th>
<th>Pins</th>
<th>SPQ</th>
<th>Length (mm)</th>
<th>Width (mm)</th>
<th>Height (mm)</th>
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<tr>
<td>TPS65023QRHARQ1</td>
<td>VQFN</td>
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<td>40</td>
<td>3000</td>
<td>367.0</td>
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<td>3000</td>
<td>367.0</td>
<td>367.0</td>
<td>35.0</td>
</tr>
</tbody>
</table>

*All dimensions are nominal*
MECHANICAL DATA

RHA (S-PVQFN-N40) PLASTIC QUAD FLATPACK NO-LEAD

Pin 1 Index Area
Top and Bottom

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
B. This drawing is subject to change without notice.
C. QFN (Quad Flatpack No-Lead) Package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Package complies to JEDEC MO-220 variation VJ1D-2.

4204276/E 06/11
THERMAL PAD MECHANICAL DATA

RHA (S-PVQFN-N40) PLASTIC QUAD FLATPACK NO-LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.

![Exposed Thermal Pad Dimensions](image-url)

**NOTES:**

A. All linear dimensions are in millimeters

B. The Pin 1 Identification mark is an optional feature that may be present on some devices

In addition, this Pin 1 feature if present is electrically connected to the center thermal pad and therefore should be considered when routing the board layout.
NOTES:  
A. All linear dimensions are in millimeters.  
B. This drawing is subject to change without notice.  
C. Publication IPC-7351 is recommended for alternate designs.  
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat-Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.  
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.  
F. Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for vias placed in the thermal pad.
Images above are just a representation of the package family, actual package may vary. Refer to the product data sheet for package details.
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).

5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC-7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat-Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com (http://www.ti.com).
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for recommended solder mask tolerances and via testing recommendations for vias placed in the thermal pad.
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