High Resolution, Fully Programmable LCD Bias IC for TV

1 FEATURES

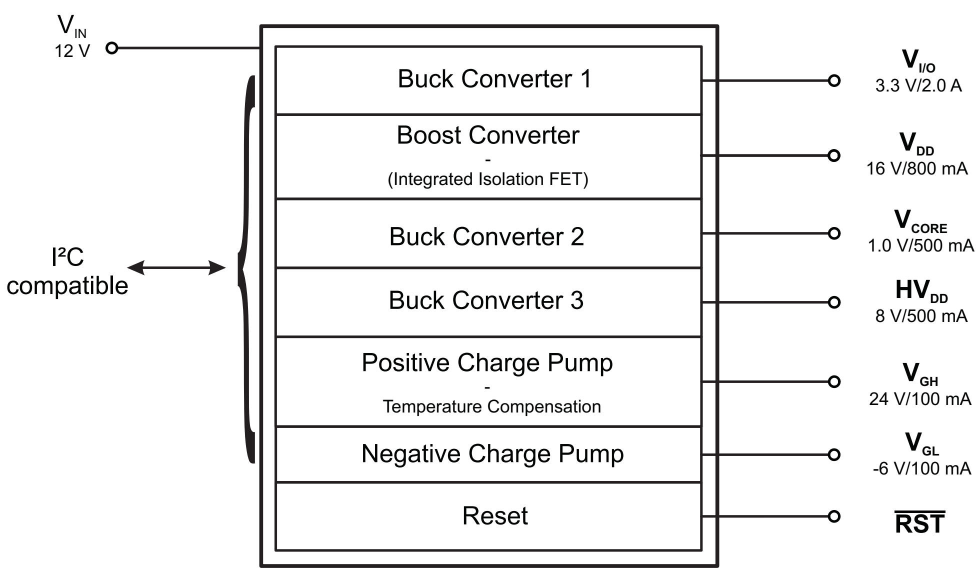
- 8.6 to 14.7V Input Voltage Range
- 6-Bit Boost Converter V_{DD}: 12.8V to 19V
  - 3.5A Switch Current Limit
- Integrated Input-to-Output Isolation Switch
- 6-Bit Buck Converter HV_{DD}: 6.4V to 9.55V
  - 0.8A Switch Current Limit
- 3-Bit Buck Converter $V_{I/O}$: 3V to 3.7V
  - 2.8A Switch Current Limit
- 4-Bit Buck Converter V_{CORE}: 0.9V to 2.4V
  - 1A Switch Current Limit
- 2 x 4-Bit Positive Charge Pump Controller V_{GH}:
  - Low Temperature Voltage: 19V to 34V
  - High Temperature Voltage: 17V to 32V
- Temperature Compensation for V_{GH}
- 6-Bit Negative Charge Pump Controller V_{GL}: –1.8V to –8.1V
- Reset Signal With Programmable Delay Time
- Programmable Delays For Flexible Sequencing (3 × 3 bits)
- Thermal Shutdown
- 40-Pin 5-mm × 5-mm QFN Package

2 APPLICATIONS

- LCD TVs
- LCD monitors

3 DESCRIPTION

The TPS65168 provides an economic power supply solution for a wide variety of LCD bias applications. The device provides all supply rails needed by a TFT-LCD panel. $V_{I/O}$, V_{CORE} and $\overline{RST}$ for the T-Con. V_{DD} and HV_{DD} for the Source Driver and the Gamma Buffer. V_{GH} and V_{GL} for the Gate Driver or the Level Shifter. The V_{GH} voltage can be compensated for low and high adjustable temperatures, if GIP technology is used. The transition from one programmed V_{GH} value to another is made using an external thermistor connected to the IC. All output rails and delay times are programmable by a Two-Wire interface: a single BOM can cover several panel types and sizes whose desired output levels can be programmed in production and stored in a non-volatile memory embedded into the TPS65168. Both V_{CORE} and HV_{DD} are generated by synchronous buck converters which support chip inductors for an optimized solution size. The solution is delivered in a small 5x5 mm QFN package.



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ORDERING INFORMATION

T_A	ORDERING	PACKAGE	PACKAGE MARKING
–40°C to 85°C	TPS65168RSB	40-Pin 5x5 QFN	TPS65168

4 ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted) (1)

	VALUE		UNIT
	MIN	MAX	
Input voltage range AVIN, PVINB1, PVINB3 (2)	–0.3	20	V
Voltage range on pin CTRLP, FBN, VGH (2)	–0.3	40	V
Voltage range on pins OUT3, SW, SWB1, SWB3, SWI, SWO (2)	–0.3	20	V
Voltage on pin A0, COMP, CTRLN, EN, OUT1, OUT2, $\overline{\text{RST}}$, SCL, SDA, SS, SWB2, TCOMP, VL (2)	–0.3	7	V
ESD rating HBM (Human Body Model)		2	kV
ESD rating MM (Machine Model)		200	V
ESD rating CDM (Charged Device Model)		700	V
Continuous power dissipation	See the Thermal Table		
Operating junction temperature range	–40	150	°C
Storage temperature range	–65	150	°C

(1) Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) With respect to the GND pin.

5 THERMAL INFORMATION

THERMAL METRIC (1)		TPS65168 RSB 40 PINS	UNITS
θ_{JA}	Junction-to-ambient thermal resistance	33.9	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance	18.5	
θ_{JB}	Junction-to-board thermal resistance	15.2	
ψ_{JT}	Junction-to-top characterization parameter	0.1	
ψ_{JB}	Junction-to-board characterization parameter	6.7	
θ_{JCbot}	Junction-to-case (bottom) thermal resistance	1.9	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

6 RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range (unless otherwise noted)

		MIN	TYP	MAX	UNIT
AV_{IN}	Input voltage range	8.6	12	14.7	V
C_{VL}	Input capacitor on internal regulator input pin VL		1		µF
BOOST CONVERTER					
V_{DD}	Boost output voltage range	12.8		19	V
L	Boost converter inductor	10		22	µH
C_{IN_BOOST}	Input capacitor on boost converter input	20			µF
C_{OUT_BOOST}	Output capacitor on boost converter output	30	40		µF
BUCK 1 CONVERTER					
$V_{I/O}$	Buck 1 converter output voltage range	3.0		3.7	V
L1	Buck 1 converter inductor	10		22	µF
C_{IN_BUCK1}	Input capacitor on buck 1 converter input pin PVINB1	10			µF
C_{OUT_BUCK1}	Output capacitor on buck 1 converter output	30	40		µF
BUCK 2 CONVERTER					
V_{CORE}	Buck 2 converter output voltage range	0.9		2.4	V
L2 (1)	Buck 2 converter inductor	1.0		2.2	µF
C_{IN_BUCK2}	Input capacitor on buck 2 converter input pin OUT1	1.0	4.7		µF
C_{OUT_BUCK2}	Output capacitor on buck 2 converter output	2.2	4.7	20	µF
BUCK 3 CONVERTER					
HV_{DD}	Buck 3 converter output voltage range	6.4		9.55	V
L3 (1)	Buck 3 converter inductor	4.7	6.8	10	µH
C_{IN_BUCK3}	Input capacitor on buck 3 converter input pin PVINB3		10		µF
C_{OUT_BUCK3}	Output capacitor on buck 3 converter output	4.7	10	20	µF
POSITIVE CHARGE PUMP CONTROLLER					
$V_{GH(COLD)}$	Positive charge pump output voltage range	19		34	V
$V_{GH(HOT)}$	Positive charge pump output voltage range	17		32	V
C_{FLY_CPP}	Positive charge pump flying capacitor		220		nF
C_{EM_CPP}	Positive charge pump emitter capacitor		1		µF
C_{OUT_CPP}	Positive charge pump output capacitor		4.7		µF
NEGATIVE CHARGE PUMP CONTROLLER					
V_{GL}	Negative charge pump output voltage range	–1.8		–8.1	V
C_{FLY_CPN}	Negative charge pump flying capacitor		470		nF
C_{COL_CPN}	Negative charge pump collector capacitor		100		nF
C_{OUT_CPN}	Negative charge pump output capacitor		4.7		µF
TEMPERATURE					
T_A	Operating ambient temperature	–40		85	°C
T_J	Operating junction temperature	–40		125	°C

(1) For buck 2 and 3, if possible it is recommended to use shielded wire wounded chip inductors because of their stable performance over temperature, current and frequency, and their good shielding preventing magnetic radiation.

7 ELECTRICAL CHARACTERISTICS

$AV_{IN} = PV_{INB1} = PV_{INB3}$ = 12V, EN = VL, V_{DD} = 16V, HV_{DD} = 8V , $V_{I/O}$ = 3.3V, V_{CORE} = 1V, $V_{GH(COLD)}$ = 28V, $V_{GH(HOT)}$ = 26V, V_{GL} = –5V, T_A = –40°C to 85°C, typical values are at T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER SUPPLY						
AV_{IN}	Input voltage range		8.6		14.7	V
I_{Q_AVIN}	Supply quiescent current AVIN	Device not switching		2		mA
I_{Q_PVINB1}	Supply quiescent current PVINB1	Device not switching		0.2		mA
I_{Q_PVINB3}	Supply quiescent current PVINB3	Device not switching		0.6		mA
I_{Q_OUT1}	Supply quiescent current OUT1	Device not switching		50		µA
I_{SD_AVIN}	Supply shutdown current AVIN	EN = GND		900		µA
I_{SD_PVINB1}	Supply shutdown current PVINB1	EN = GND		0.01		µA
I_{SD_PVINB3}	Supply shutdown current PVINB3	EN = GND		400		µA
UVLO	Undervoltage lockout	AV_{IN} rising	8.3	8.6	8.9	V
		Hysterisis, AV_{IN} falling	0.3	0.8	1.3	V
T_{SD}	Thermal shutdown	T_J rising		140		°C
T_{HYS}	Thermal shutdown hysteresis	T_J falling		8		°C
LOGIC SIGNAL A0, EN, SCL, SDA						
V_{IH}	High level input voltage A0, EN	AV_{IN} = 8.6 V to 14.7 V	1.5			V
	High level input voltage SCL, SDA		1.2			
V_{IL}	Low level input voltage	AV_{IN} = 8.6 V to 14.7 V			0.5	V
EN_pull_down	Internal pull-down resistor on EN pin			400		kΩ
INTERNAL OSCILLATOR						
f_{OSC}	Switching frequency of buck 1 and boost converters		600	750	900	kHz
INTERNAL REGULATOR						
V_L	Internal regulator	I_{VL} = 10 mA, EN = GND	4.8	5.0	5.2	V
BOOST CONVERTER [V_{DD}]						
V_{DD_ACC}	Output voltage accuracy	V_{DD} default value	–2%	16	2%	V
$r_{DS(on)}$	MOSFET on-resistance	I_{SW} = current limit		90	165	mΩ
I_{LIM}	MOSFET current limit		3.5	4.2	5	A
I_{SS}	Soft-start current	V_{SS} = 1.230 V		10		µA
	Line regulation	AV_{IN} = 8.6 V to 14.7 V, I_{OUT} = 700 mA		0.001		%/V
	Load regulation	I_{OUT} = 0 A to 1 A		0.087		%/A
ISOLATION SWITCH						
$r_{DS(on)}$	Isolation MOSFET on-resistance	I_{SWI} = 1 A		170		mΩ
I_{SC_ISO}	Short circuit current limit	V_{SWI} = 12 V, V_{SWO} = 0 V		350		mA
BUCK 1 CONVERTER [$V_{I/O}$]						
V_{I/O_ACC}	Output voltage accuracy	$V_{I/O}$ default value	–3%	3.3	3%	V
$r_{DS(on)}$	MOSFET on-resistance	I_{SWB1} = current limit		190	370	mΩ
I_{LIM}	MOSFET current limit		2.6	3.4	4.2	A
	Line regulation	$AV_{IN} = PV_{INB1}$ = 8.6 V to 14.7 V, $I_{I/O}$ = 200 mA		0.001		%/V
	Load regulation	$I_{I/O}$ = 200 mA to 800 mA		0.076		%/A

ELECTRICAL CHARACTERISTICS (continued)

AV_{IN} = PV_{INB1} = PV_{INB3} = 12V, EN = VL, V_{DD} = 16V, HV_{DD} = 8V , $V_{I/O}$ = 3.3V, V_{CORE} = 1V, $V_{GH(COLD)}$ = 28V, $V_{GH(HOT)}$ = 26V, V_{GL} = –5V, T_A = –40°C to 85°C, typical values are at T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
BUCK 2 CONVERTER [V_{CORE}]						
V_{CORE_ACC}	Output voltage accuracy	V_{CORE} default value	–3%	1.0	3%	V
$r_{DS(on)}$	MOSFET on-resistance	I_{SWB2} = current limit		250	450	mΩ
I_{LIM}	MOSFET current limit		1.1	1.4	1.8	A
f_{SWB2}	Switching frequency buck 2 converter		0.8		3.7	MHz
	Line regulation	V_{OUT1} = 3.0 V to 3.7 V I_{CORE} = 300 mA		0.004		%/V
	Load regulation	I_{CORE} = 0 A to 500 mA		0.470		%/A
BUCK 3 CONVERTER [HV_{DD}]						
HV_{DD_ACC}	Output voltage accuracy	HV_{DD} default value	–3%	8	3%	V
$r_{DS(on)}$	P-MOSFET on-resistance	I_{SWB3} = current limit		320	450	mΩ
I_{LIM}	MOSFET current limit – source		0.8	1.4	2	A
	MOSFET current limit – sink		-0.8	-1.4	-2	
f_{SWB3}	Switching frequency buck 3 converter		0.25		2	MHz
	Line regulation	AV_{IN} = PV_{INB3} = 8.6 V to 14.7 V, I_{OUT} = 300 mA		0.015		%/V
	Load regulation	I_{OUT} = –500 mA to 500 mA		0.006		%/A
POSITIVE CHARGE PUMP CONTROLLER [V_{GH}]						
$V_{GH(COLD)\_ACC}$	Output voltage accuracy	$V_{GH(COLD)}$ default value	–3.5%	28	3.5%	V
$V_{GH(HOT)\_ACC}$		$V_{GH(HOT)}$ default value	–3.5%	26	3.5%	V
I_{CTRLP_SC}	Base current during short circuit	VGH = GND	40		75	µA
I_{CTRLP}	Base current		1		2	mA
	Line regulation	AV_{IN} = 8.6 V to 14.7 V, I_{GH} = 50 mA		0.001		%/V
	Load regulation	I_{GH} = 0 A to 100 mA		2.32		%/A
NEGATIVE CHARGE PUMP CONTROLLER [V_{GL}]						
V_{GL}	Programmable output voltage range negative charge pump		-1.8		-8.1	V
V_{FBN}	Feedback regulation voltage		-4%	900	+4%	mV
I_{FBN}	Feedback input bias current	V_{FBN} = 0 V			0.1	µA
I_{CTRLN_SC}	Base current during short circuit	V_{CTRLN} = 0.6 V, V_{FBN} = 20 mV	200		440	µA
I_{CTRLN}	Base current	V_{CTRLN} = 0.6 V	5			mA
	Line regulation	AV_{IN} = 8.6 V to 14.7 V, I_{GL} = 50 mA		0.006		%/V
	Load regulation	I_{GL} = 0 A to 100 mA		1.83		%/A
RESET GENERATOR [$\overline{RST}$](1)						
$V_{\overline{RST}(ON)}$	Low voltage level	$I_{/RST(ON)}$ = 1 mA			0.5	V
$I_{LEAK\_\overline{RST}}$	Leakage current	$V_{/RST(ON)}$ = $V_{I/O}$ = 3.3 V			2	µA

(1) External pull-up resistor to be chosen so that the current flowing into /RST Pin when active ($V_{/RST}$ = 0 V) is below $I_{/RST(ON)}$ = 1 mA.

8 I²C INTERFACE TIMING CHARACTERISTICS (2)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{SCL}	SCL clock frequency	Standard mode			100	kHz
		Fast mode			400	kHz
t_{LOW}	LOW period of the SCL clock	Standard mode	4.7			µs
		Fast mode	1.3			µs
t_{HIGH}	HIGH period of the SCL clock	Standard mode	4.0			µs
		Fast mode	600			ns
t_{BUF}	Bus free time between a STOP and START condition	Standard mode	4.7			µs
		Fast mode	1.3			µs
$t_{hd;STA}$	Hold time for a repeated START condition	Standard mode	4.0			µs
		Fast mode	600			ns
$t_{su;STA}$	Setup time for a repeated START condition	Standard mode	4.7			µs
		Fast mode	600			ns
$t_{su;DAT}$	Data setup time	Standard mode	250			ns
		Fast mode	100			ns
$t_{hd;DAT}$	Data hold time	Standard mode	0.05		3.45	µs
		Fast mode	0.05		0.9	µs
t_{RCL1}	Rise time of SCL signal after a repeated START condition and after an acknowledge bit	Standard mode	$20 + 0.1C_B$		1000	ns
		Fast mode	$20 + 0.1C_B$		1000	ns
t_{RCL}	Rise time of SCL signal	Standard mode	$20 + 0.1C_B$		1000	ns
		Fast mode	$20 + 0.1C_B$		300	ns
t_{FCL}	Fall time of SCL signal	Standard mode	$20 + 0.1C_B$		300	ns
		Fast mode	$20 + 0.1C_B$		300	ns
t_{RDA}	Rise time of SDA signal	Standard mode	$20 + 0.1C_B$		1000	ns
		Fast mode	$20 + 0.1C_B$		300	ns
t_{FDA}	Fall time of SDA signal	Standard mode	$20 + 0.1C_B$		300	ns
		Fast mode	$20 + 0.1C_B$		300	ns
$t_{su;STO}$	Setup time for STOP condition	Standard mode	4.0			µs
		Fast mode	600			ns
C_B	Capacitive load for SDA and SCL				400	pF

(2) Industry standard I²C timing characteristics. Not tested in production.

8.1 I²C TIMING DIAGRAMS

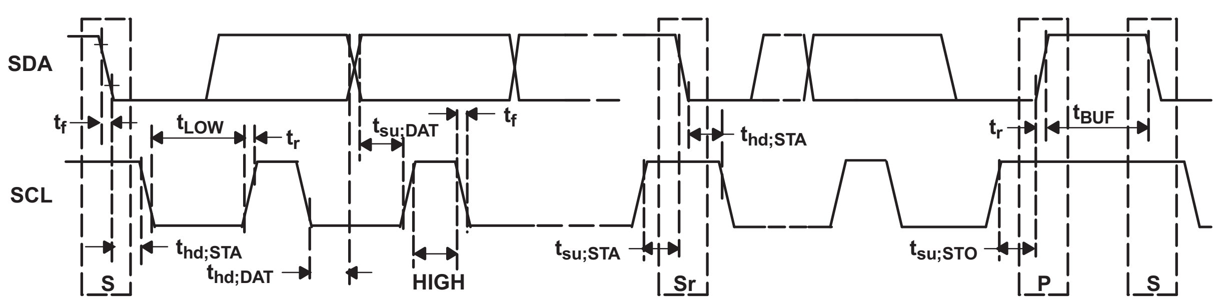
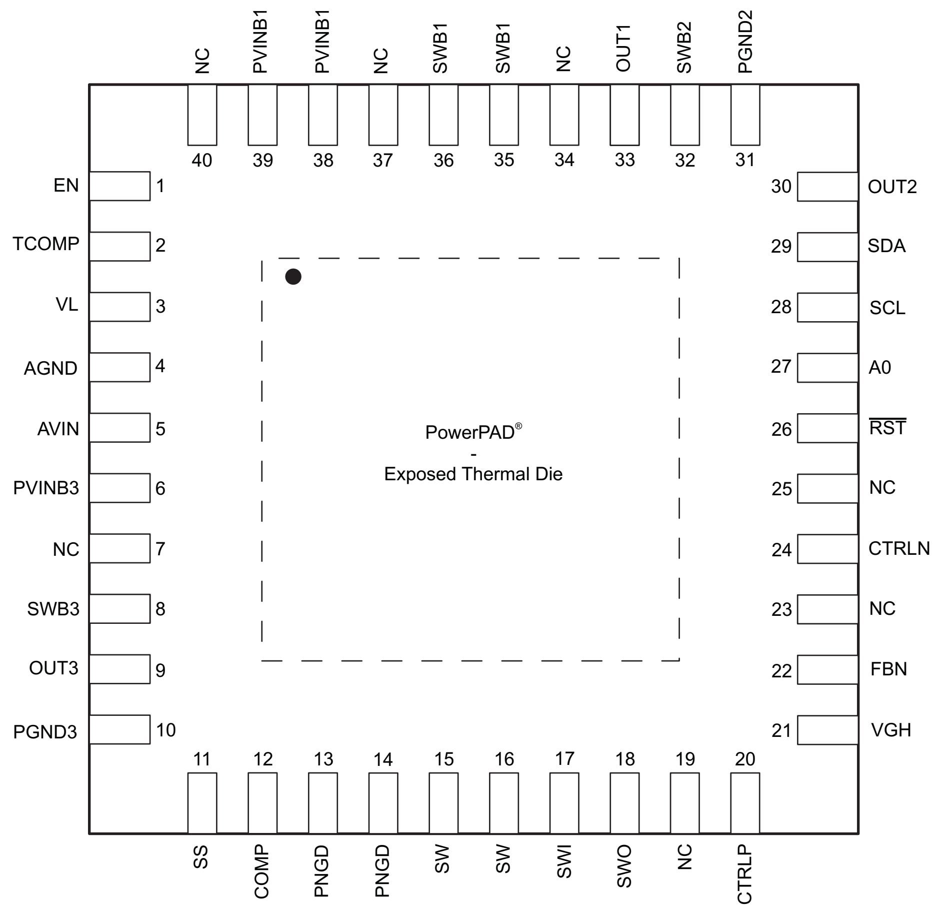


Figure 1. Serial Interface Timing for F/S-Mode

9 DEVICE INFORMATION

QFN 40 pin
5mm x 5mm
(TOP VIEW)



PIN FUNCTIONS

PIN		I/O	DESCRIPTION
NAME	NO.		
EN	1	I	Device enable pin. Set this pin high to enable the device. See the sequencing section for more information
TCOMP	2	I	Temperature compensation input pin. Connect the thermistor / resistors network to this pin
VL	3	O	Internal regulator output pin. Connect an output capacitor of 1 µF to this pin
AGND	4, exposed pad		Analog ground pin. Connect this pin to the PowerPAD™ The PowerPAD™ needs to be soldered onto the ground copper plane of the PCB board for proper power dissipation
AVIN	5	I	Internal regulator supply pin
PVINB3	6	I	Buck 3 converter (HVDD) power input pin
NC	7, 19, 23, 25, 34, 37, 40		Not connected
SWB3	8	I/O	Buck 3 converter (HV_{DD}) switch pin
OUT3	9	I	Buck 3 converter (HV_{DD}) output voltage sense pin
PGND3	10		Buck 3 converter (HV_{DD}) power ground pin
SS	11	O	Boost converter ($_{VDD}$) soft-start pin. Connect a capacitor to this pin if a soft-start is needed. Open = no soft-start
COMP	12	I/O	Boost converter (V_{DD}) compensation pin

PIN FUNCTIONS (continued)

PIN		I/O	DESCRIPTION
NAME	NO.		
PGND	13, 14		Boost converter (V_{DD}) power ground pin
SW	15, 16	I/O	Boost converter (V_{DD}) switch pin
SWI	17	I	Isolation switch input pin. The SWI pin is connected to the internal overvoltage protection comparator of the Boost converter
SWO	18	O	Isolation switch output pin (V_{DD})
CTRLP	20	O	Positive charge pump (V_{GH}) base drive signal pin
VGH	21	I	Positive charge pump (V_{GH}) output voltage sense pin
FBN	22	I	Negative charge pump (V_{GL}) feedback pin
CTRLN	24	O	Negative charge pump (V_{GL}) base drive signal pin
/RST	26	O	Reset generator open drain output pin
A0	27	I	I^2C slave address select pin
SCL	28	I/O	I^2C clock pin
SDA	29	I/O	I^2C data pin
OUT2	30	I	Buck 2 converter (V_{CORE}) output voltage sense pin
PGND2	31		Buck 2 converter ($V_{CORE)}$ power ground pin
SWB2	32	I/O	Buck 2 converter (V_{CORE}) switch pin
OUT1	33	I	Buck 1 converter ($V_{I/O)}$ output voltage sense
SWB1	35, 36	I/O	Buck 1 converter ($V_{I/O}$) switch pin
PVINB1	38, 39	I	Buck 1 converter ($V_{I/O}$) input supply pin

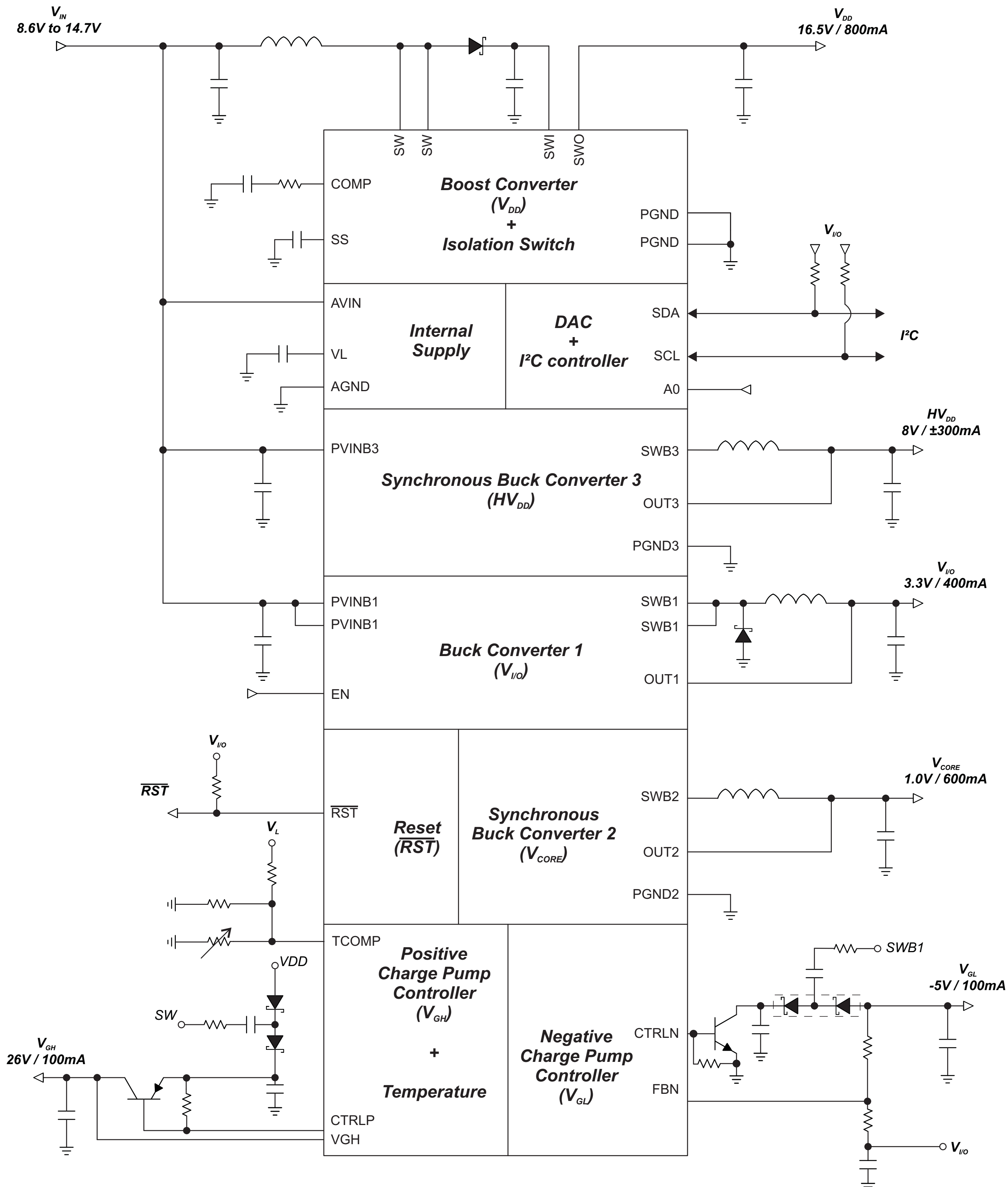


Figure 2. Simple Application Schematic

10 TYPICAL CHARACTERISTICS

Table 1. Table of Graphs

PARAMETER	Conditions	Figure
Buck 1 Converter		
Efficiency vs. Load Current	V_{IN} = 12 V, $V_{I/O}$ = 3.3 V L = 10 µH	Figure 3
PWM Switching – Light Load	V_{IN} = 12 V, $V_{I/O}$ = 3.3 V/50 mA L = 10 µH	Figure 4
PWM Switching – Heavy Load	V_{IN} = 12 V, $V_{I/O}$ = 3.3 V/ 500 mA L = 10 µH	Figure 5
Load Transient Response	V_{IN} = 12 V, $V_{I/O}$ = 3.3 V/100 ~ 500 mA L = 10 µH, C_{OUT} = 40 µF	Figure 6
Buck 2 Converter		
Efficiency vs. Load Current	V_{IN} = 12 V, V_{CORE} = 1.0 V, 1.2 V, 1.5 V, 1.8 V L = 2.2 µH	Figure 7
PWM Switching – Light Load	V_{IN} = 12 V, V_{CORE} = 1.0 V/0 A L = 2.2 µH	Figure 8
PWM Switching – Heavy Load	V_{IN} = 12 V, V_{CORE} = 1.0 V/500 mA L = 2.2 µH	Figure 9
Load Transient Response	V_{IN} = 12 V, V_{CORE} = 3.3 V/100~ 500 mA L = 2.2 µH, C_{OUT} = 10 µF	Figure 10
Buck 3 Converter		
Efficiency vs. Load Current	V_{IN} = 12 V, HV_{DD} = 8 V L = 6.8 µH	Figure 11
PWM Switching – Light Load	V_{IN} = 12 V, HV_{DD} = 8 V/0 A L = 6.8 µH	Figure 12
PWM Switching – Heavy Load (Source)	V_{IN} = 12 V, HV_{DD} = 8 V/500 mA L = 6.8 µH	Figure 13
PWM Switching – Heavy Load (Sink)	V_{IN} = 12 V, HV_{DD} = 8 V/–500 mA L = 6.8 µH	Figure 14
Load Transient Response	V_{IN} = 12 V, HV_{DD} = 3.3 V/–500 ~ +500 mA L = 6.8 µH, C_{OUT} = 10 µF	Figure 15
Boost Converter		
Efficiency vs. Load Current	V_{IN} = 12 V, V_{DD} = 16 V L = 10 µH	Figure 16
PWM Switching – Light Load	V_{IN} = 12 V, V_{DD} = 16 V/0 A L = 10 µH	Figure 17
PWM Switching – Heavy Load	V_{IN} = 12 V, V_{DD} = 16 V/ 700 mA L = 10 µH	Figure 18
Load Transient Response	V_{IN} = 12 V, V_{DD} = 16 V/ 50 ~ 500 mA L = 10 µH, C_{OUT} = 40 µF	Figure 19
Positive Charge Pump		
Load Transient Response	V_{IN} = 12 V, V_{GH} = 28 V/ 10 ~ 60 mA C_{OUT} = 10 µF	Figure 20
Negative Charge Pump		
Load Transient Response	V_{IN} = 12 V, V_{GL} = –5 V/ 10 ~ 50 mA C_{OUT} = 10 µF	Figure 21
Temperature Compensation		
Voltage Adjustment - [–2°C ~ 25°C)	$V_{GH(COLD)1}$ = 34 V, $V_{GH(HOT)1}$ = 17 V $V_{GH(COLD)2}$ = 27 V, $V_{GH(HOT)2}$ = 24 V	Figure 23
Temperature Adjustment - [$V_{GH(COLD)}$ = 28 V, $V_{GH(HOT)}$ = 22 V]	T°C Variation1: 2 °C ~ 18 °C T°C Variation: 16 °C ~ 32 °C	Figure 24
Sequencing		
Power On Sequencing	V_{IN} = 12 V, $V_{I/O}$ = 3.3 V, V_{CORE} = 1.0 V, V_{GL}= –5 V V_{DD}= 16 V, HV_{DD} = 8 V, V_{GH} = 26 V	Figure 22

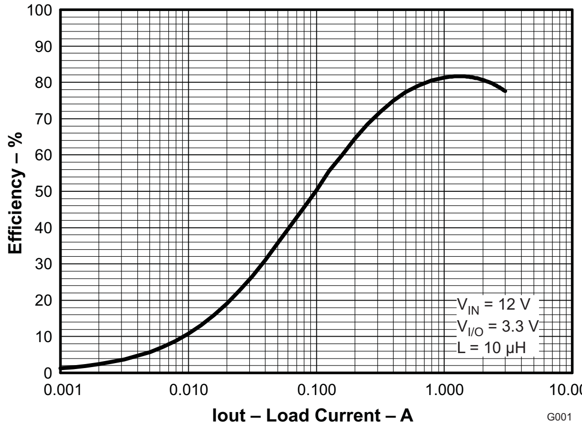


Figure 3. BUCK 1 ($V_{I/O}$) EFFICIENCY vs LOAD CURRENT

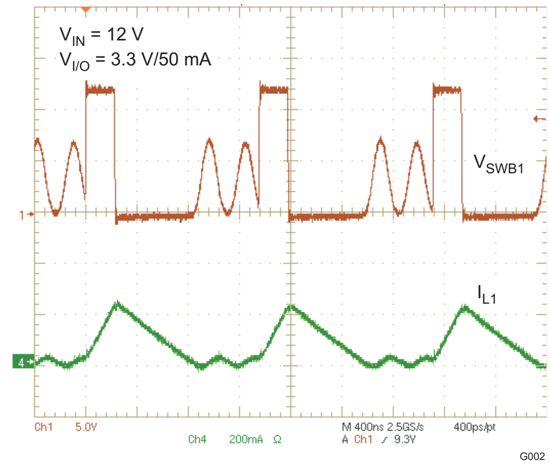


Figure 4. BUCK 1 ($V_{I/O}$) PWM SWITCHING – LIGHT LOAD

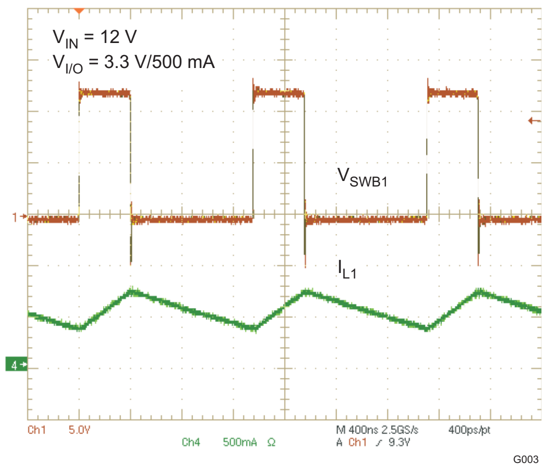


Figure 5. BUCK 1 ($V_{I/O}$) PWM SWITCHING – HEAVY LOAD

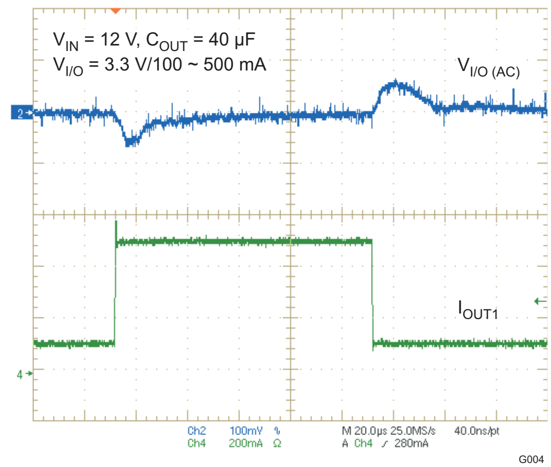


Figure 6. BUCK 1 ($V_{I/O}$) LOAD TRANSIENT RESPONSE

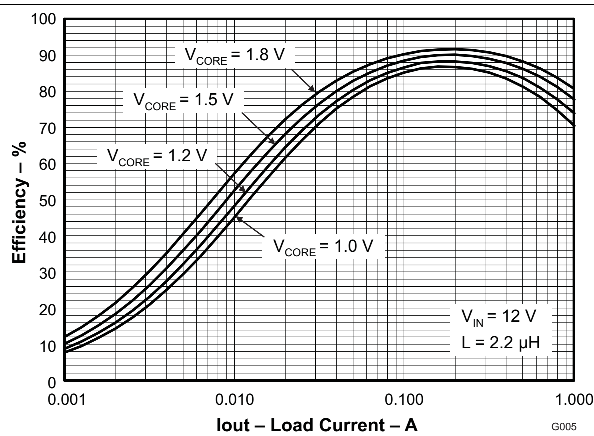


Figure 7. BUCK 2 (V_{CORE}) EFFICIENCY vs LOAD CURRENT

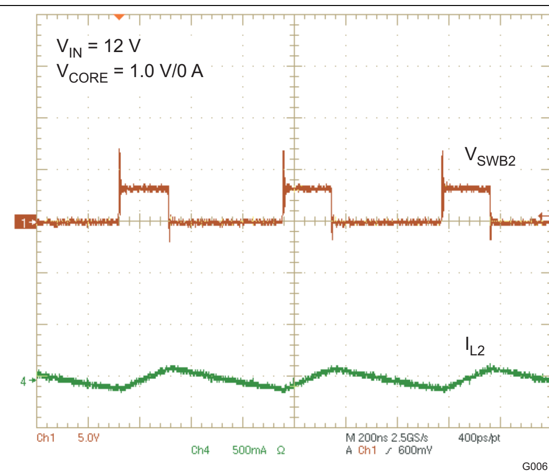


Figure 8. BUCK 2 (V_{CORE}) PWM SWITCHING – LIGHT LOAD

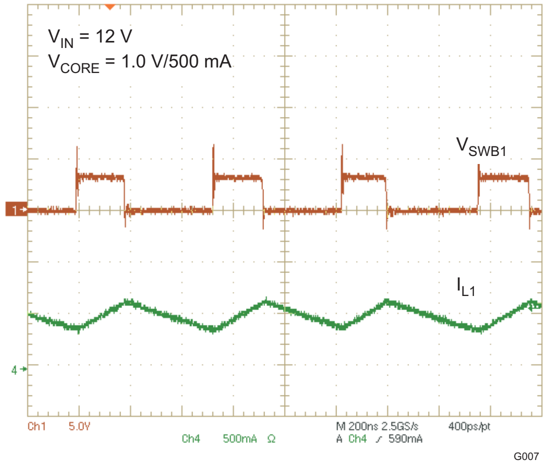


Figure 9. BUCK 2 (V_{CORE}) PWM SWITCHING – HEAVY LOAD

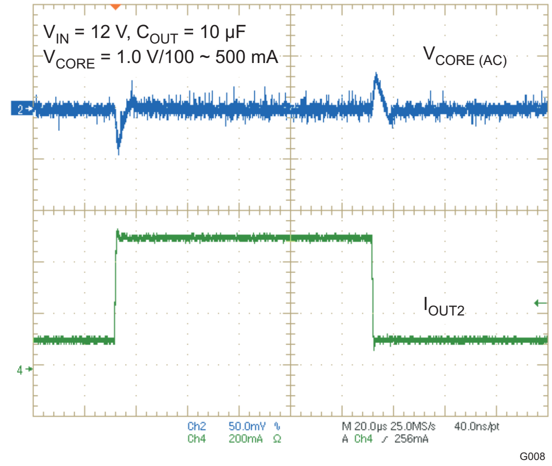


Figure 10. BUCK 2 (V_{CORE}) LOAD TRANSIENT RESPONSE

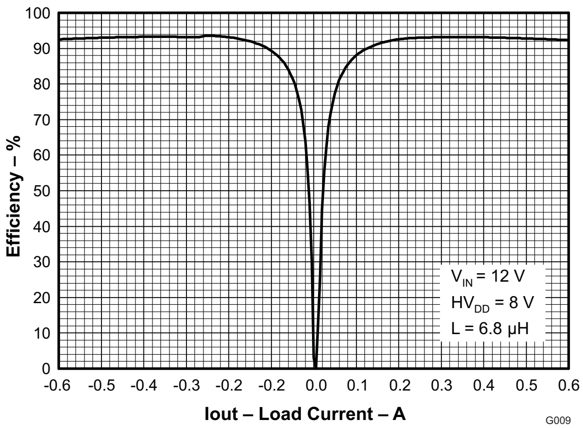


Figure 11. BUCK 3 (HV_{DD}) EFFICIENCY vs LOAD CURRENT

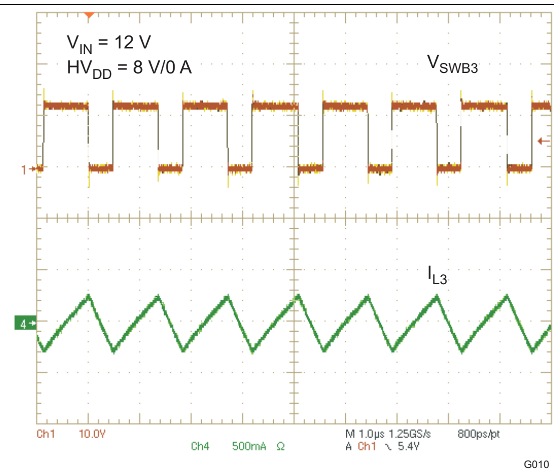


Figure 12. BUCK 3 (HV_{DD}) PWM SWITCHING - LIGHT LOAD

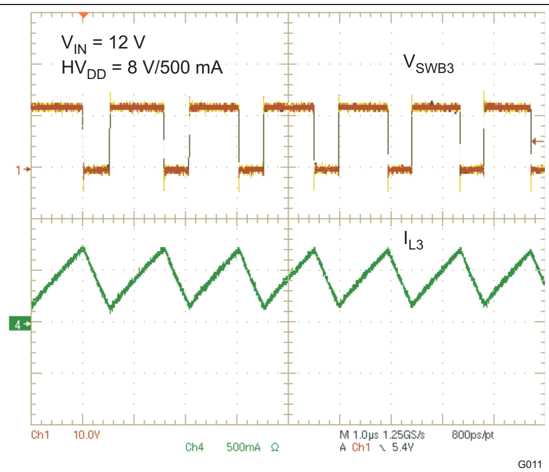


Figure 13. BUCK 3 (HV_{DD}) PWM SWITCHING – HEAVY LOAD (SOURCE)

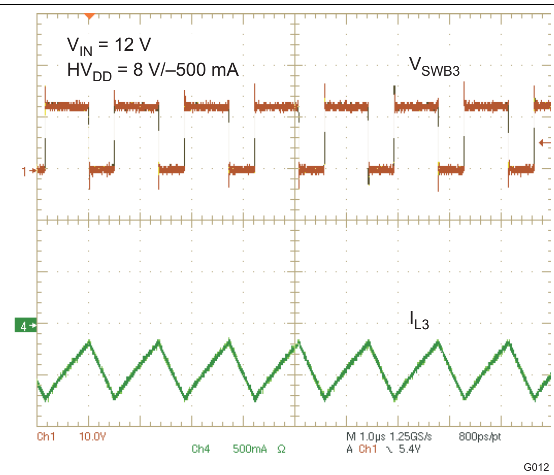


Figure 14. BUCK 3 (HV_{DD}) PWM SWITCHING – HEAVY LOAD (SINK)

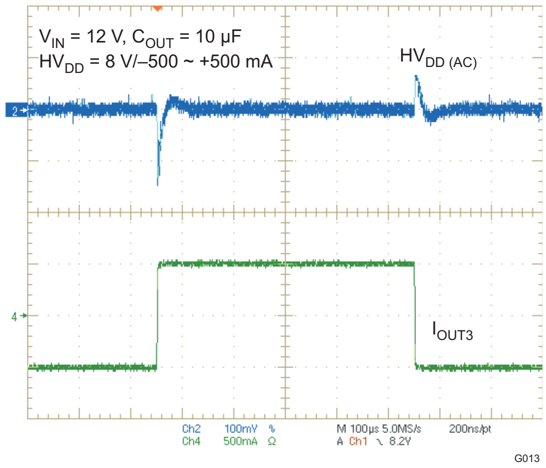


Figure 15. BUCK 3 (HV_{DD}) LOAD TRANSIENT RESPONSE

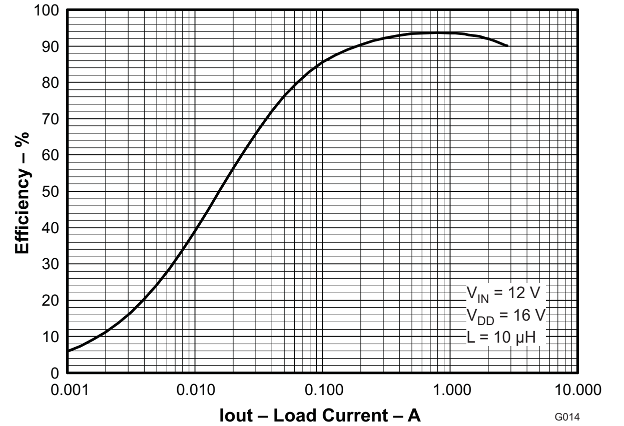


Figure 16. BOOST (V_{DD}) EFFICIENCY vs LOAD CURRENT

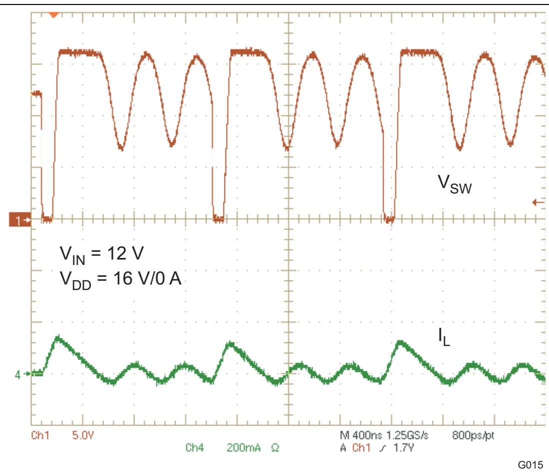


Figure 17. BOOST (V_{DD}) PWM SWITCHING – LIGHT LOAD

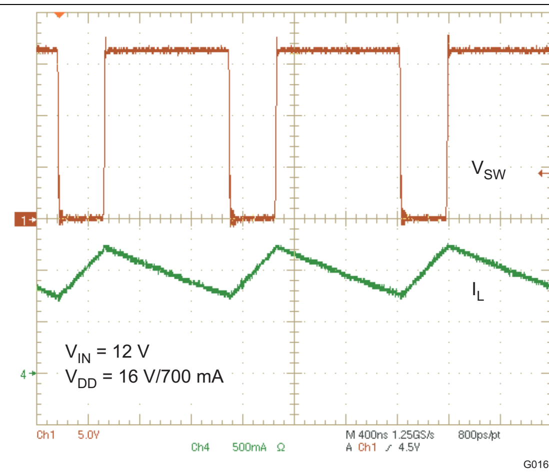


Figure 18. BOOST (V_{DD}) PWM SWITCHING – HEAVY LOAD

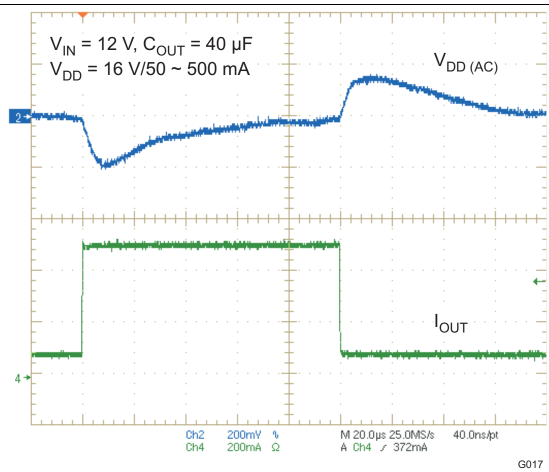


Figure 19. BOOST (V_{DD}) LOAD TRANSIENT RESPONSE

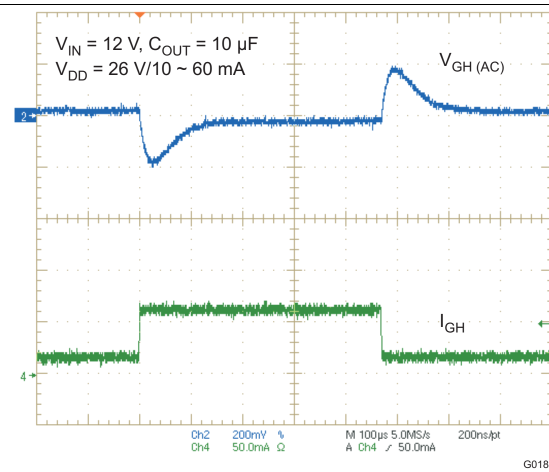


Figure 20. CPP (V_{GH}) LOAD TRANSIENT RESPONSE

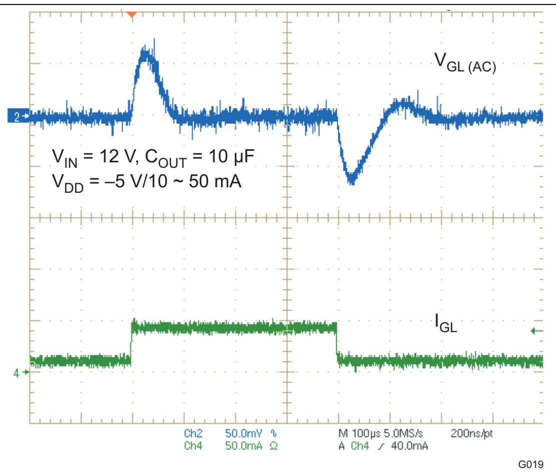


Figure 21. CPN (V_{GL}) LOAD TRANSIENT RESPONSE

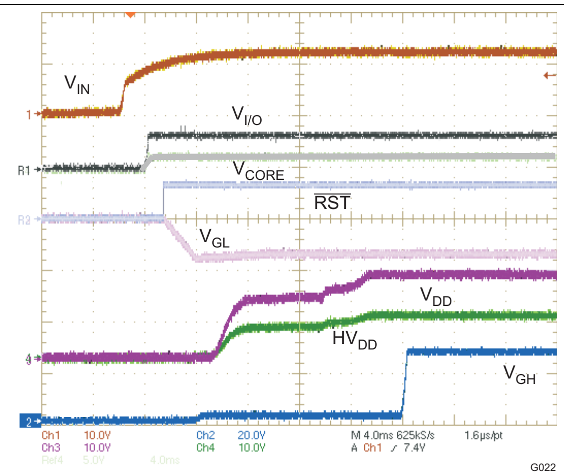


Figure 22. POWER ON SEQUENCE

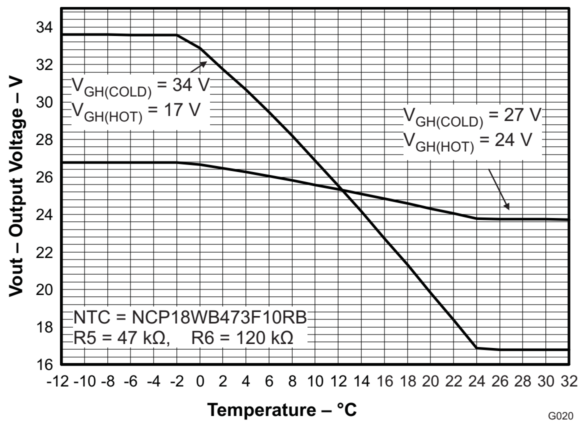


Figure 23. TEMPERATURE COMPENSATION VOLTAGE ADJUSTMENT

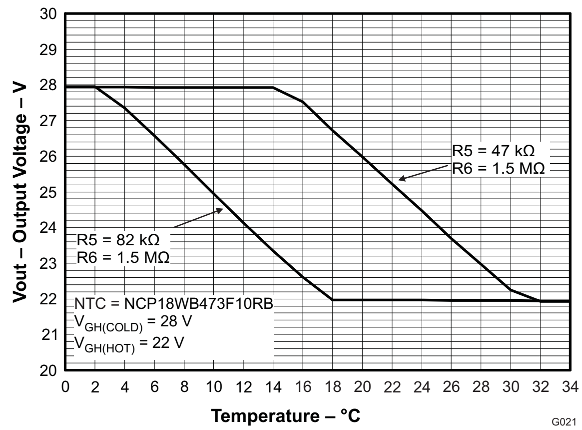


Figure 24. TEMPERATURE COMPENSATION TEMPERATURE ADJUSTMENT

11 OUTPUT VOLTAGE RANGE SUMMARY

All outputs are programmable using a Two-Wire interface.

Boost Converter (V_{DD})

Number of bit address: 6
Output voltage range: 12.8V…19V

Buck 1 Converter ($V_{I/O}$)

Number of bit address: 3
Output voltage range: 3.0V…3.7V

Buck 2 converter (V_{CORE})

Number of bit address: 4
Output voltage range: 0.9V…2.4V

Buck 3 converter (HV_{DD})

Number of bit address: 6
Output voltage range: 6.4V…9.55V

Positive Charge Pump Controller ($V_{GH(COLD)}$ – low temperature)

Number of bit address: 4
Output voltage range: 19V…34V

Positive Charge Pump Controller ($V_{GH(HOT)}$ – high temperature)

Number of bit address: 4
Output voltage range: 17V…32V

Negative Charge Pump (V_{GL})

Number of bit address: 6
Output voltage range: –1.8V…–8.1V

11.1 SEQUENCING

The power-up sequence delays are programmable with a Two-Wire interface. DLY1, DLY2 and DLY3 can be set per steps of 5 ms, up to 35 ms.

DLY1, 2, 3

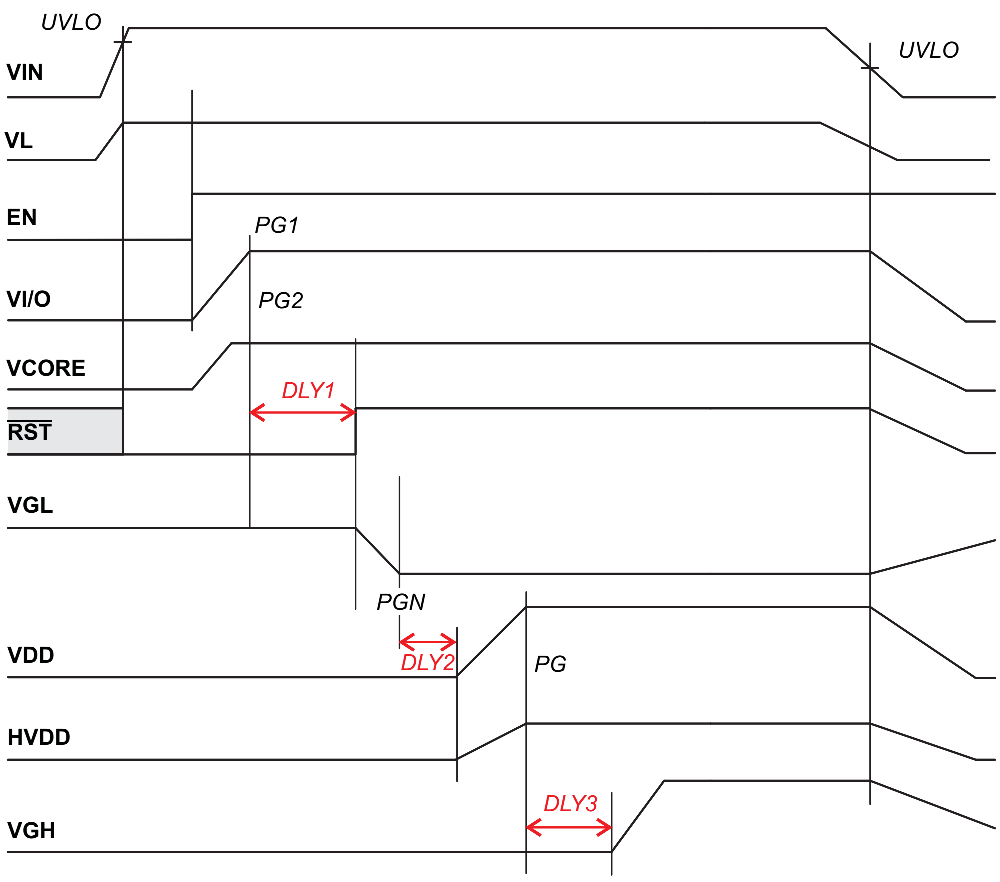
Number of bit address: 3
Timing delay range: 0ms…35ms

11.2 POWER-UP

1. When V_{IN} > 8.6 V the device is enabled and the $\overline{RST}$ signal is set 'low', and V_L goes into regulation.
2. When EN = 'high' the buck 1 ($V_{I/O}$) **and** buck 2 (V_{CORE}) converters start up.
3. When PG1 and PG2 are reached **and** DLY1 has passed, $\overline{RST}$ is released and the negative charge pump controller (V_{GL}) starts.
4. When PGN is reached **and** DLY2 has passed, the boost converter (V_{DD}) and the buck 3 converter (HV_{DD}) start.
5. When PG is reached **and** DLY3 has passed, the positive charge pump controller (V_{GH}) starts.

11.3 POWER-DOWN

1. When VIN falls down below the UVLO threshold, all blocks are disabled and discharge at a rate driven by the output load and the output capacitors mainly



12 DETAILED DESCRIPTION

12.1 BOOST CONVERTER (V_{DD})

The non-synchronous boost converter uses a current mode topology and operates at a fixed frequency of 750kHz. A typical application circuit is shown in Figure 27. The external compensation allows designers to optimize the performance for individual applications, and is easily implemented by connecting a suitable capacitor/resistor network between the COMP pin and AGND (see design procedure section for more details).

12.1.1 Enable Signal (DLY2)

The boost converter is enabled when the power good signal from the negative charge pump controller (V_{GL}) is asserted and the programmed DLY2 has passed (see the *Appendix* section to set DLY2 timing).

12.1.2 Startup (Boost Converter)

The startup of the boost converter block operates in two steps:

1. **Input-to-output isolation switch (Iso)**

   As soon as the internal enable signal of the boost converter is activated, the isolation switch is slowly turned on, ramping up smoothly the current flowing from V_{IN} into the output capacitors. The startup current is limited to 350 mA typically, increasing as the output voltage is getting higher. Once $V_{SWI} - V_{SWO} \leq 1.2$ V, the isolation switch is fully turned on and the boost converter starts switching. The soft-start function is also enabled.

2. **Soft-start (SS)**

   To minimize the inrush current during start-up an external capacitor connected to the soft-start pin SS is used to slowly ramp up the internal current limit of the boost converter. It is charged with a constant current of typically 10 µA. The inductor peak current limit is proportional to the SS voltage and the maximum load current is available after the soft-start is completed (V_{SS} = 0.8 V) or V_{DD} has reached its Power Good value (90% of its nominal voltage). The larger the SS capacitor, the slower the ramp of the current limit and the longer the soft-start time. A 100-nF capacitor is usually sufficient for most of the applications. When the EN pin is pulled low or the undervoltage lockout of the boost converter is reached, the soft-start capacitor is discharged to ground.

12.1.3 Protections (Boost Converter)

The boost converter is protected against potentially damaging conditions such as overvoltage and short circuits.

1. **Short-Circuit Protection**

   The boost converter integrates a short-circuit protection circuit to prevent the inductor or the rectifier diode from overheating when the output rail is shorted to GND. If the boost output is shorted to GND and the voltage difference between SWI and SWO exceeds the threshold voltage of 1.2 V typically, the boost converter shuts down and the input-to-output isolation switch limits the current to 350 mA typically.

2. **Overvoltage Protection**

   The boost converter integrates an overvoltage protection. If the output voltage V_{DD} exceeds the OVP threshold of 19.5 V typically, the boost converter stops switching. The output voltage will drop below the hysteresis and the boost converter will autonomously recover and switch again.

NOTE

Since the positive charge pump is driven from the boost converter's switch node as well as its output, an error condition on the boost converter's output will also cause the loss of V_{GH} until the circuit recovers.

The boost converter also stops switching while the positive charge pump is in a short circuit condition. This condition is not latched and the boost converter autonomously resumes normal operation once the short circuit condition has been removed from the positive charge pump.

BOOST CONVERTER (V_{DD}) (continued)

12.1.4 Setting the Output Voltage V_{DD}

The output voltage of the boost converter is programmable via a Two-Wire interface between 12.8 V and 19 V with a 6-bit resolution. See the *Appendix* section to set the V_{DD} voltage.

12.2 Boost Converter Design Procedure

The first step in the design procedure is to verify whether the maximum possible output current of the boost converter supports the specific application requirements. A simple approach is to estimate the converter efficiency, by taking the efficiency number from the provided efficiency curves at the application's maximum load or to use a worst case assumption for the expected efficiency, e.g., 85%.

1. Duty Cycle: $D = 1 - \frac{V_{IN\_min} \times \eta}{V_S}$
2. Inductor ripple current: $\Delta I_L = \frac{V_{IN\_min} \times D}{f_{OSC} \times L}$
3. Maximum output current: $I_{OUT\_max} = \left(I_{LIM\_min} - \frac{\Delta I_L}{2}\right) \times (1 - D)$
4. Peak switch current of the application: $I_{SWPEAK} = \frac{I_{OUT}}{1 - D} + \frac{\Delta I_L}{2}$

   η = Estimated boost converter efficiency (use the number from the efficiency plots or 85% as an estimation)
   f_{OSC} = Boost converter switching frequency (750 kHz)
   L = Selected inductor value for the boost converter (see the Inductor Selection section)
   I_{SWPEAK} = Boost converter switch current at the desired output current (must be < I_{LIM_min} = 3.5 A)
   ΔI_L = Inductor peak-to-peak ripple current

The peak switch current is the current that the integrated switch, the inductor and the external Schottky diode have to be able to handle. The calculation must be done for the minimum input voltage where the peak switch current is highest.

12.2.1 Inductor Selection (Boost Converter)

Saturation current: the inductor must handle the maximum peak current ($I_{L\_SAT} > I_{SWPEAK}$, or $I_{L\_SAT} > I_{LIM\_max}$ as conservative approach)

DC Resistance: the lower the DCR, the lower the losses

Inductor value: with a fixed frequency of 750 kHz, the recommended values are 10 µH ≤ L ≤ 22 µH. The boost converter is optimized to work with 10 µH. The higher the inductor value, the lower the inductor ripple and output voltage ripple but the slower the transient response.

Table 2. Inductor Selection Boost / Buck 1

L (µH)	SUPPLIER	COMPONENT CODE	SIZE (L x W x H mm)	DCR TYP (mΩ)	I_{SAT} (A)
10	Sumida	CDRH8D43	8.3 x 8.3 x 4.5	29	4
10	Murata	LQH6PPN100M43K	6.0 x 6.0 x 4.3	53	2.6
22	Sumida	CD105NP-100M	10.4 x 9.4 x 5.8	60	2.6
22	Sumida	CDRH129-220M	12.5 x 12.5 x 10	23	5

12.2.2 Rectifier Diode Selection (Boost Converter)

Diode type: Schottky type for better efficiency

Reverse voltage: V_R of the diode must block V_{OVP} voltage (20 V recommended)

Forward current: the diode's averaged rectified forward current I_F must handle the output current since $I_F = I_{OUT}$ (2A recommended as conservative approach, 1A sufficient for lower output current).

Thermal characteristics: the diode must be chosen so that it can dissipate the power ($P_D = I_F \times V_F$, 500 mW should be sufficient for most of the applications)

Table 3. Rectifier Diode Selection Boost / Buck 1

PART NUMBER	V_R / I_{AVG}	V_F	$R_{\theta JA}$	SIZE	COMPONENT SUPPLIER
MBRS320	20V / 3A	0.44V at 3A	46°C/W	SMC	International Rectifier
SL22	20V / 2A	0.44V at 2A	75°C/W	SMB	Vishay Semiconductor
SS22	20V / 2A	0.50V at 2A	75°C/W	SMB	Fairchild Semiconductor

12.2.3 Compensation (COMP)

The regulation loop can be compensated by adjusting the external components connected to the COMP pin. The COMP pin is the output of the internal transconductance error amplifier. The compensation capacitor will adjust the low frequency gain and the resistor value will adjust the high frequency gain. Lower output voltages require a higher gain and therefore a lower compensation capacitor value. A good start, that will work for the majority of the applications is R_{COMP} = 33 kΩ and C_{COMP} = 1 nF.

12.2.4 Input Capacitor Selection

For good input voltage filtering low ESR ceramic capacitors are recommended. TPS65168 has an analog input AVIN. A 1-µF bypass is required as close as possible from AVIN to GND.

Two 10-µF (or one 22-µF) ceramic input capacitor is sufficient for most of the applications. For better input voltage filtering this value can be increased. Refer to the *Recommended Operation Conditions* table, Table 4 and the *Typical Application* section for input capacitor recommendations.

12.2.5 Output Capacitor Selection

For best output voltage filtering a low ESR output capacitor is recommended. Typically, four 10-µF (or two 22-µF) ceramic output capacitors work for most of the applications. Higher capacitor values can be used to improve the load transient response. *A 10 µF capacitor is also required between the rectifier diode and the SWI pin* (Refer to the *Recommended Operation Conditions* table, Table 4 and the *Typical Application* section for output capacitor recommendations).

Table 4. Input and Output Capacitor Selection Boost / Buck 1

CAPACITOR	VOLTAGE RATING	COMPONENT SUPPLIER	COMPONENT CODE	COMMENTS
1µF/0603	16V	Taiyo Yuden	EMK107BJ105KA	AVIN bypass
10µF/1206	16V	Taiyo Yuden	EMK212BJ106KG	C_{IN}
10µF/1206	25V	Taiyo Yuden	TMK316BJ106KL	C_{OUT}
22µF/1210	25V	Murata	GRM32ER61E226KE15	C_{IN} / C_{OUT}

To calculate the output voltage ripple, the following equations can be used:

$$\Delta V_C = \frac{V_{DD} - V_{IN}}{V_{DD} \times f_{OSC}} \times \frac{I_{OUT}}{C_{OUT}} \qquad \Delta V_{C\_ESR} = I_{SWPEAK} \times R_{C\_ESR} \tag{1}$$

ΔV_{C_ESR} can be neglected in many cases since ceramic capacitors provide very low ESR.

12.3 BUCK 1 CONVERTER ($V_{I/O}$)

The buck 1 converter (step-down) used in TPS65168 is a non-synchronous type that runs at a fixed frequency of 750kHz. The converter features integrated soft-start, bootstrap, and compensation circuits to minimize external component count.

12.3.1 Enable Signal (UVLO – EN)

The buck 1 converter is enabled when the VIN voltage exceeds the UVLO threshold of 8.3 V typically and if the EN pin is pulled 'high'. If EN is pulled 'low', the entire IC shuts down.

12.3.2 Buck 1 Converter Operation

The buck 1 converter can operate in either continuous conduction mode (CCM) or discontinuous conduction mode (DCM), depending on the load current. At medium and high load currents, the inductor current is always greater than zero and the converter operates in CCM; at low load currents, the inductor current is zero during part of each switching cycle, and the converter operates in DCM. The switch node waveforms for CCM and DCM operation are shown in Figure 4 and Figure 5. Note that the ringing seen during DCM operation (at light load) occurs because of parasitic capacitance in the PCB layout and is normal for DCM operation. However, there is very little energy contained in the ringing waveform and it does not significantly affect EMI performance. Equation 2 can be used to calculate the load current below which the buck converter operates in DCM.

$$I_{DCM} = \frac{\left(V_{IN} - V_{LOGIC}\right)}{2 \times L \times f_{SW}} \times \frac{V_{LOGIC}}{V_{IN}} \tag{2}$$

The buck 1 converter uses a *skip* mode to regulate $V_{I/O}$ at very low load currents. This mode allows the converter to maintain its output at the required voltage while still meeting the requirement of a *minimum on time*. During skip mode, the buck 1 converter switches for a few cycles, then stops switching for a few cycles, and then starts switching again and so on, for as long as the output current is below the skip mode threshold. Output voltage ripple can be a little higher during skip mode.

12.3.3 Startup and Short Circuit Protection (Buck 1 Converter)

The buck 1 converter is limiting its switching frequency when its output voltage $V_{I/O}$ is below a certain threshold (f_{SWB1} = 1/4 × fosc for $V_{FB\_internal}$ < 400mV and f_{SWB1} = ½ × fosc for $V_{FB\_internal}$ < 800mV). This feature avoids run away of the inductor in case of short circuit and helps smoothing the buck converter startup as well.

12.3.4 Setting the Output Voltage $V_{I/O}$

The output voltage of the buck 1 converter is programmable via a Two-Wire interface between 3.0 V and 3.7 V with a 3-bit resolution. See the *Appendix* section to set the $V_{I/O}$ voltage.

12.4 Buck 1 Converter Design Procedure

1. Duty Cycle: $D = \frac{V_{I/O}}{V_{IN} \times \eta}$
2. Inductor ripple current: $\Delta I_L = \frac{(V_{IN\_max} - V_{I/O}) \times D}{f_{OSC} \times L}$
3. Maximum output current: $I_{I/O\_max} = I_{LIM\_min} - \frac{\Delta I_L}{2}$
4. Peak switch current: $I_{SWPEAK} = I_{I/O\_max} + \frac{\Delta I_L}{2}$

   η = Estimated buck 1 converter efficiency (use the number from the efficiency plots or 85% as an estimation)
   f_{OSC} = Buck 1 converter switching frequency (750 kHz)
   L = Selected inductor value for the boost converter (see the Inductor Selection section)
   I_{SWPEAK} = Buck 1 converter switch current (must be < I_{LIM_min} = 2.6 A)
   ΔI_L = Inductor peak-to-peak ripple current

Buck 1 Converter Design Procedure (continued)

Because the negative charge pump is driven from the buck 1 converter's switch node, ant the buck 2 converter is driven by the output rail of the buck 1 converter, the effective output current for design purposes is greater than II/O alone. For best performance, the effective current calculated using the following equation should be used during the design.

$$I_{I/O(EFFECTIVE)} = I_{I/O} + \frac{|V_{GL}| \times I_{GL}}{V_{I/O}} + I_{IN\_CORE} \tag{3}$$

12.4.1 Inductor Selection (Buck 1 Converter)

Refer to the boost converter *Inductor Selection*.

Inductor value: as for the boost converter, the buck 1 converter is designed to work with an inductor range as 10 µH ≤ L ≤ 22 µH. The buck 1 converter is optimized to work with 10 µH.

12.4.2 Rectifier Diode Selection (Buck 1 Converter)

Refer to the boost converter rectifier *Diode Rectifier Selection*.

12.4.3 Input Capacitor Selection (Buck 1 Converter)

Two 10-µF (or one 22-µF) ceramic input capacitor is sufficient for most of the applications. For better input voltage filtering this value can be increased. Refer to the *Recommended Operation Conditions* table, Table 4 and the *Typical Application* section for input capacitor recommendations.

12.4.4 Output Capacitor Selection (Buck 1 Converter)

For best output voltage filtering a low ESR output capacitor is recommended. Typically, four 10-µF (or two 22-µF) ceramic output capacitors work for most of the applications. Higher capacitor values can be used to improve the load transient response. Refer to the *Recommended Operation Conditions* table, Table 4 and the *Typical Application* section for input capacitor recommendations.

12.5 BUCK 2 CONVERTER (V_{CORE})

The TPS65168 integrates a synchronous buck 2 (step-down) converter that includes a unique hysteric PWM controller scheme which enables switch frequencies over 3MHz, excellent transient and ac load regulation as well as operation with tiny and cost competitive external components like chip inductors. The TPS65168's buck 2 converter offers adjustable output voltage down to 0.9 V, ideal to support the most recent timing controllers. The internal switch current limit of 1.1 A minimum supports output currents of up to 1 A.

12.5.1 Enable Signal (UVLO – EN)

The buck 2 converter is enabled together with the buck 1 converter when the VIN voltage exceeds the UVLO threshold of 8.3 V typically and if the EN pin is pulled 'high'. If EN is pulled 'low', the entire IC shuts down.

12.5.2 Buck 2 Converter Operation

The converter operates in a hysteretic mode. The high side transistor (PMOS) remains turned on until a minimum on time of $t_{ON\ min}$ expires and the output voltage trips the threshold of the error comparator or the inductor current reaches the high side switch current limit. Once the high side switch turns off, the low side switch rectifier is turned on and the inductor current ramps down. As the output voltage falls below the threshold of the error comparator, a switch pulse is initiated and the high side switch is turned on again. If the inductor current falls down to zero, will continue operating with $t_{ON\ min}$ and $t_{OFF\ min}$ in order to maintain the proper output voltage.

12.5.3 Startup and Short Circuit Protection (Buck 2 Converter)

The buck 2 converter tracks the buck 1 converter output voltage during startup until it has reached its programmed value. In the event of a short circuit, the converter will operate with maximum duty cycle and the ouput current will be limited by the internal current limit.

12.5.4 Setting the Output Voltage V_{CORE}

The output voltage of the buck 2 converter is programmable via a Two-Wire interface between 0.9 V and 2.4 V with a 4-bit resolution. See the *Appendix* section to set the V_{CORE} voltage.

12.6 Buck 2 Converter Design Procedure

1. Duty Cycle: $D = \dfrac{V_{CORE}}{V_{I/O} \times \eta}$
2. Inductor ripple current: $\Delta I_L = \dfrac{V_{I/O} - V_{CORE}}{L} \times t_{ON} = \dfrac{V_{I/O} - V_{CORE}}{L \times f} \times D$
3. Maximum output current: $I_{CORE\_max} = I_{LIM\_min} - \dfrac{\Delta I_L}{2}$
4. Peak switch current: $I_{SWPEAK} = I_{CORE\_max} + \dfrac{\Delta I_L}{2}$

   η = Estimated buck 2 converter efficiency (use the number from the efficiency plots or 80% as an estimation)
   f = Buck 2 converter switching frequency (use the frequency from the frequency plots)
   L = Selected inductor value for the buck 2 converter (see the Inductor Selection section)
   I_{SWPEAK} = Buck 2 converter switch current (must be < I_{LIM_min} = 1.1 A)
   ΔI_L = Inductor peak-to-peak ripple current

The peak switch current is the steady state current that the integrated switches and the inductor have to be able to handle.

12.6.1 Inductor Selection (Buck 2 Converter)

Refer to the boost converter inductor selection.

Inductor value: the buck 2 converter is designed to work with small inductors in the following range: 1.0 µH ≤ L ≤ 2.2 µH. The buck 2 converter is optimized to work with 2.2 µH.

Buck 2 Converter Design Procedure (continued)

Table 5. Inductor Selection Buck (Chip Inductors)

L (µH)	SUPPLIER	COMPONENT CODE	SIZE (LxWxH mm)	DCR TYP (mΩ)	I_{SAT} (A)
2.2	Murata	LQM21PN2R2	2 x 1.2 x 0.55	340	0.6
2.2	FDK	MPSZ2012D2R2	2 x 1.2 x 1	230	0.7
1.0	FDK	MIPSZ2012D1R0	2 x 1.2 x 1	90	1.1
2.2	Murata	LQM2HPN2R2MG0	2.5 x 2 x 1	80	1.3
1.0	Murata	LQM2HPN1R0MG0	2.5 x 2 x 1	90	1.5

12.6.2 Input Capacitor Selection

Because of the nature of the buck 2 converter having a pulsating input current, a low ESR input capacitor is required for best input voltage filtering and minimizing the interference with other circuits caused by high input voltage spikes. For most applications a minimum of 1 µF ceramic capacitor is recommended. The input capacitor connected as close as possible to the IC on OUT1 pin can be increased without any limit for better input voltage filtering. Refer to Table 6 for the selection of the filtering capacitors.

12.6.3 Output Capacitor Selection

The unique hysteric PWM control scheme of the TPS65168's buck 2 converter allows the use of tiny ceramic capacitors. Ceramic capacitors with low ESR values have the lowest output voltage ripple and are recommended. Refer to Table 6 for the selection of the output capacitors.

Table 6. Input and Output Capacitor Selection Buck 2

CAPACITOR	VOLTAGE RATING	COMPONENT SUPPLIER	COMPONENT CODE	COMMENTS
1µF/0603	16V	Taiyo Yuden	EMK107 BJ 105KA	C_{IN}
4.7µF/0603	10V	Taiyo Yuden	LMK107 BJ 475KA	C_{IN}
4.7µF/0603	6.3V	Taiyo Yuden	JMK107 BJ 475_A	C_{OUT}

Note: If the Buck 2 is not used, OUT2 (pin 30) must be connected to OUT1 (pin 33) for proper startup.

12.7 BUCK 3 CONVERTER (HV_{DD})

The TPS65168 integrates also a synchronous buck 3 (step-down) converter that includes a unique hysteric PWM able to sink and source current up to 500 mA. As the buck 2 converter, the buck 3 operates in a hysteretic mode.

A significant advantage of TPS65168's buck 3 converter compared to other hysteretic PWM controller topologies is its excellent AC load regulation capability providing superior transient response, ideal for output current loads switching from +500 mA to –500 mA in worst case LCD patterns.

12.7.1 Enable Signal (DLY2)

The buck 3 converter is enabled together with the boost converter when the power good of the negative charge pump (VGL) is asserted and that the DLY2 has passed. See the *Appendix* section to set the DLY2 timing.

12.7.2 Startup and Short Circuit Protection (Buck 3 Converter)

The buck 3 converter output voltage tracks the boost converter output voltage ratio metric pace value during startup. To prevent Source Driver damages, the TPS65168 implements a protection feature that disables both the boost (V_{DD}) and the buck 3 (HV_{DD}) converters when short-circuits or over voltages occur on one of the two converters. The converters will autonomously recover after the failure gone.

12.7.3 Setting the output voltage HVDD

The output voltage of the buck 3 converter is programmable via a Two-Wire interface between 6.4 V and 9.55 V with a 6-bit resolution. See the *Appendix* section to set the HV_{DD} voltage.

12.8 Buck 3 Converter Design Procedure

1. Duty Cycle: $D = \frac{HV_{DD}}{V_{IN} \times \eta}$
2. Inductor ripple current: $\Delta I_L = \frac{3.2 \times 10^{-6}}{L}$
3. Maximum output current: $I_{HVDD\_max} = I_{LIM\_min} - \frac{\Delta I_L}{2}$
4. Peak switch current: $I_{SWPEAK} = I_{HVDD\_max} + \frac{\Delta I_L}{2}$

   η = Estimated buck 3 converter efficiency (use the number from the efficiency plots or 80% as an estimation)
   f = Buck 3 converter switching frequency (use the frequency from the frequency plots)
   L = Selected inductor value for the buck 3 converter (in µH – for value see the *Inductor Selection* section)
   I_{SWPEAK} = Buck 3 converter switch current (must be < I_{LIM_min} = 0.8 A)
   ΔI_L = Inductor peak-to-peak ripple current

The peak switch current is the steady state current that the integrated switches and the inductor have to be able to handle.

12.8.1 Inductor Selection (Buck 3 Converter)

Refer to the boost converter *Inductor Selection* section, for more details.

Inductor value: the buck 3 converter is designed to work with small inductors in the following range: 4.7µH ≤ L ≤ 10 µH. The buck 3 converter is optimized to work with 6.8 µH.

NOTE

chip inductors (such as wounded type) work well with the converter providing a small solution size together with low magnetic radiations (because well shielded) and do not dissipate as much energy (do not get hot)as ferrite wire wounded types.

Buck 3 Converter Design Procedure (continued)

Table 7. Inductor Selection Buck 3 (Chip Inductors)

L (µH)	SUPPLIER	COMPONENT CODE	SIZE (LxWxH mm)	DCR TYP (mΩ)	I_{SAT} (A)
4.7, 6.8, 10	Taiyo Yuden	CBC2518T series	2.5 x 1.8 x 1.8	260 ~ 460	480 ~ 680
4.7, 6.8, 10	Taiyo Yuden	CBC3225T series	3.2 x 2.5 x 2.5	100 ~ 133	900 ~ 1250

For wire wounded inductors other than chip style, it is important to follow the layout recommendations in the section PCB Layout Recommendations to minimize frequency variations.

12.8.2 Input Capacitor Selection

Typically, one 10-µF ceramic capacitor on PVINB3 pin is recommended. For better input voltage filtering this value can be increased. Refer to the *Recommended Operation Conditions* table, Table 4 and the *Typical Application* section for input capacitor recommendations.

12.8.3 Output Capacitor Selection

Typically, one 10-µF ceramic output capacitor works for most of the applications. Refer to the *Recommended Operation Conditions* table, Table 4 and the *Typical Application* section for output capacitor recommendations.

12.9 POSITIVE CHARGE PUMP CONTROLLER (V_{GH}) and TEMPERATURE COMPENSATION

The positive charge pump is driven directly from the boost converter's switch node and regulated by controlling the current through an external PNP transistor. The TPS65168 also includes a temperature compensation feature that controls the output voltage depending on the temperature sense by an external Negative Thermistor (NTC).

12.9.1 Enable Signal (DLY3)

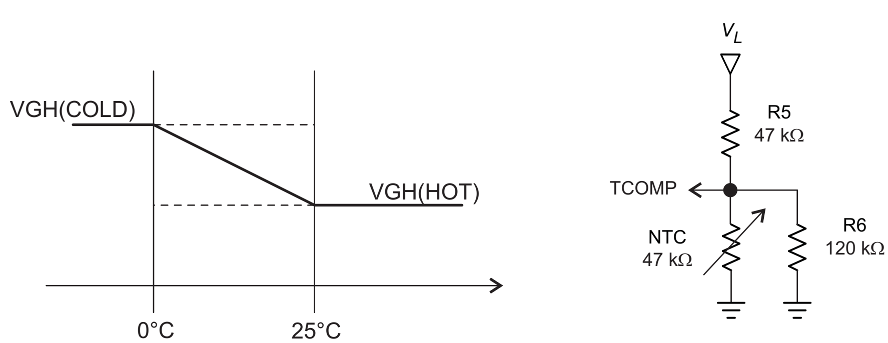
The positive charge pump controller is enabled when the boost and buck 3 converters' power good signals are asserted and that the DLY3 has passed. See the *Appendix* section to set the DLY3 timing.

12.9.2 Temperature Compensation

By connecting a fixed-value thermistor between [TCOMP and GND] and a fixed-value pull-up resistor between [VL and TCOMP], the V_{GH} voltage will vary from given $V_{GH(COLD)}$ voltage at a temperatures ≤ 0°C to a lower voltage defined by $V_{GH(HOT)}$ for temperatures greater than 25°C (and reversely). The user has to provide $V_{GH(COLD)}$ and $V_{GH(HOT)}$ and the temperatures can be adjusted using the external resistors.

NOTE

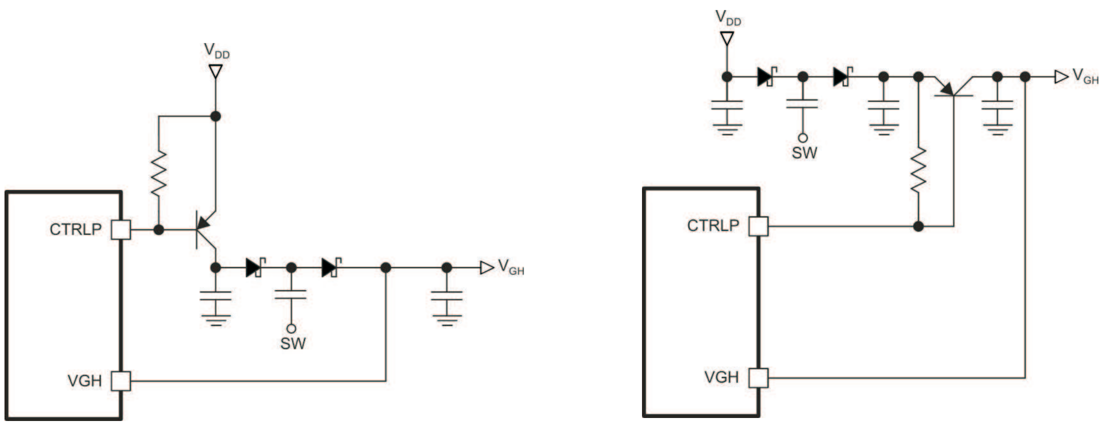
The internal temperature compensation system is made to work only with 47 kΩ NTC part number **NCP18WB473F10RB** (see Table 10 in *Appendix* section).



POSITIVE CHARGE PUMP CONTROLLER (V_{GH}) and TEMPERATURE COMPENSATION (continued)

12.9.3 Positive Charge Pump Controller Operation

During normal operation, the TPS65168 is able to provide up to 1.5 mA of base current typically and is designed to work best with transistors whose DC gain (hFE) is between 100 and 300. The charge pump is protected against short-circuits on its output, which are detected when the voltage on the charge pump's internal feedback is below 100 mV. During short-circuit mode, the base current available from the CTRLP pin is limited to 60 µA typically. Note that if a short-circuit is detected during normal operation, boost converter and buck 3 switching is also halted until the internal feedback voltage is above 100 mV. Typical application circuits are shown in Figure 25.



Input Regulation **Output Regulation**

Figure 25. Positive Charge Pump Application Circuits

12.9.4 Setting the output voltage $V_{GH(COLD)}$ and $V_{GH(HOT)}$

The output voltage of the positive charge pump is programmable via a Two-Wire interface between 19 V and 34 V with a 4-bit resolution for $V_{GH(COLD)}$, and between 17 V and 32 V with a 4-bit resolution for $V_{GH(HOT)}$. See the *Appendix* section to set the $V_{GH(COLD)}$ and $V_{GH(HOT)}$ voltage.

NOTE

In the case where $V_{GH(COLD)} \leq V_{GH(HOT)}$, whatever the temperature is, the output voltage will be $V_{GH(HOT)}$.

12.10 Positive Charge Pump Design Procedure

The regulation of the positive charge pump (CPP) can be done either on the input (transistor placed between VDD and the diode) or on the output. For better regulation and fewer interaction between the boost converter and the CPP controller, it is recommended to place the transistor on the output. However, during the boost converter's startup some high current spikes might appears on the flying capacitor until the V_{DD} voltage is doubled (if CPP configured in doubler mode) – time needed to charge up all the output capacitors.

12.10.1 Diodes selection (CPP)

Small-signal diodes can be used for most low current applications (<50mA) and higher rated diodes for higher power applications. The average current through the diode is equal to the output current, so that the power dissipated in the diode is given by: $P_D = I_{GH} \times V_F$

The peak current through the diode occurs during start-up and for a few cycles may be as high as a few amps. However, this condition typically lasts for <1ms and can be tolerated by many diodes whose repetitive current rating is much lower. The diodes' reverse voltage rating should be equal to $2 \times V_{DD}$.

Positive Charge Pump Design Procedure (continued)

Table 8. Positive Charge Pump Diode Selection

PART NUMBER	I_{AVG}	I_{PK}	V_R	V_F	COMPONENT SUPPLIER
BAV99W	150mA	1A for 1ms	75V	1V at 50mA	NXP
BAT54S	200mA	600mA for 1s	30V	0.8V at 100mA	Fairchild Semiconductor
MBR0540	500mA	5.5A for 8ms	40V	0.51 at 500mA	Fairchild Semiconductor

12.10.2 Capacitors Selection (CPP)

Flying capacitors

A flying capacitor in the range 100 nF to 1µF is suitable for most applications. Larger values experience a smaller voltage drop by the end of each switching cycle, and allow higher output voltages and/or currents to be achieved. Smaller values tend to be physically smaller and a bit cheaper. For best performance, it is recommended to include a resistor of a few ohms (1 Ω is a good value to start with) in series with the flying capacitor to limited peak currents occurring at the instant of switching.

Storage capacitors

For lowest output voltage ripple, low-ESR ceramic capacitors are recommended. The actual value is not critical and 1 µF to 10 µF is suitable for most applications. Larger capacitors provide better performance in applications where large load transient currents are present.

Transistor placed on the input (Figure 25)

A collector capacitor is required. A range of 100 nF to 1µF is suitable for most applications. Larger values are more suitable for high current applications but can affect stability if they are too big.

Transistor placed on the output (Figure 25)

An emitter capacitor is required. A range of 1µF to 10µF is suitable for most applications. A smaller ratio between the emitter capacitor and the output capacitor is better for startup reason. A combination of C_{OUT} = 4.7 µF, C_{FLY} = 220 nF, (and $C_{EMITTER}$ = 4.7 µF) is a good starting point for most applications (the final values can be optimized on a case-by-case basis if necessary).

12.10.3 Selecting the PNP Transistor (CPP)

The PNP transistor used to regulate VGH should have a DC gain (h_{FE}) of at least 100 when its collector current is equal to the charge pump's output current. The transistor should also be able to withstand voltages up to $2\times V_{DD}$ across its collector-emitter (V_{CE}) – in the case where the CPP operates in doubler mode.

The transistor must be able to dissipate this power without its junction becoming too hot. Note that the ability to dissipate power depends heavily on adequate PCB thermal design. The power dissipated in the transistor is given by the following equation:

The transistor must be able to dissipate this power without its junction becoming too hot. Note that the ability to dissipate power depends heavily on adequate PCB thermal design. The power dissipated in the transistor is given by the following equation:

$$P_Q = \left[(2 \times V_{DD}) - (2 \times V_F) - V_{GH} \right] \times I_{GH} \tag{4}$$

I_{GH} = Mean output current on V_{GH}
V_F = Diode forward voltage

A pull-up resistor is also required between the transistor's base and emitter. The value of this resistor is not critical, but it should be large enough not to divert significant current away from the base of the transistor. A value of 100 kΩ is suitable for most applications.

12.10.4 Positive Charge Pump Protection

The TPS65168 contains a circuit to protect the CPP against short circuits on its output. A short circuit condition is detected as long as the VGH voltage is below 1 V. The base current is then limited to 55 µA typically.

12.11 NEGATIVE CHARGE PUMP (V_{GL})

The negative charge pump (CPN) controller uses an external NPN transistor to regulate an external charge pump circuit. The IC is optimized for use with transistors having a DC gain (h_{FE}) in the range 100 to 300; however, it is possible to use transistors outside this range, depending on the application requirements. Regulation of the charge pump is achieved by using the external transistor as a controlled current source whose output depends on the voltage applied to the FBN pin: the higher the transistor current the greater the charge transferred to the output during each switching cycle and therefore the higher (i.e., the more negative) the output voltage. A typical application circuit is shown in Figure 26.

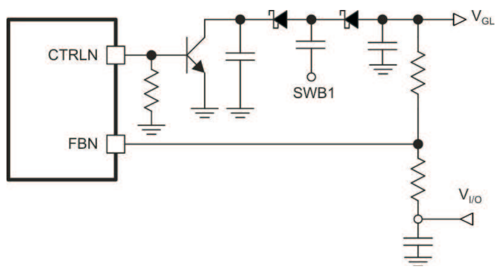


Figure 26. Negative Charge Pump Application Circuit

12.11.1 Enable Signal (DLY1)

The negative charge pump controller is enabled when the buck 1 and 2 converters' power good are asserted and that the DLY1 (3 bits DAC) has passed. See the *Appendix* section to set the DLY1 timing.

12.11.2 Setting the output voltage V_{GL}

The output voltage of the negative charge pump is programmable via a Two-Wire interface between –1.8 V and –8.1 V with a 6-bit resolution, and the external resistors need to be fixed with the following ratio: $\frac{R16}{R17} = 2.45$. See the *Appendix* section to set the V_{GL} voltage.

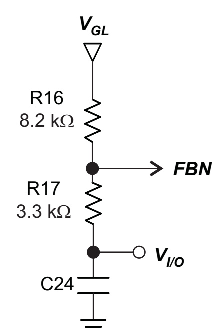
A current of the order of 1mA through the resistor network ensures good accuracy and increases the circuit's immunity to noise. It also ensures a minimum load on the charge pump, which reduces output voltage ripple under no-load. The positive reference voltage should be connected to $V_{I/O}$ to ensure proper short-circuit protection and easier PCB layout.

A 100-nF bypass capacitor C24 used on $V_{I/O}$ reference level is required. Note that the maximum voltage in an application is determined by the input voltage and the voltage drop across the diodes and NPN transistor. For a typical application in which the negative charge pump is configured as a voltage inverter, the maximum (i.e., most negative) output voltage is given by:

$$V_{GL(MAX)} = -V_{IN} + (2 \times V_F) + V_{CE} \tag{5}$$

V_F = Diode forward voltage

V_{CE} = Collector-emitter voltage of the transistor (recommended to be at least 1 V to avoid PNP saturation)



The TPS65168 contains a circuit to protect the CPN against short circuits on its output. A short circuit condition is detected as long as the FBN pin remains above 2.14 V (V_{GL} > –0.7 V), during which time the charge pump's output current is limited to 320 µA typically.

To ensure proper start-up under normal conditions, circuit designers should ensure that the full load current is not drawn by the load until the feedback voltage V_{FBN} is below the short circuit threshold voltage.

12.12 Negative Charge Pump Design Procedure

12.12.1 Diodes Selection (CPN)

As for the CPP, the CPN's diodes need to handle the following power: $P_D = I_{GL} \times V_F$. See Table 3 for diode selection.

12.12.2 Capacitors selection (CPN)

See the *Capacitors selection (CPP)* section for more detail.

A combination of C_{OUT} = 4.7 µF, C_{FLY} = 100 nF, and $C_{COLLECTOR}$ = 100 nF is a good starting point for most applications (the final values can be optimized on a case-by-case basis if necessary).

12.12.3 Selecting the NPN Transistor (CPN)

The NPN transistor used to regulate V_{GL} should have a DC gain (h_{FE}) of at least 100 when its collector current is equal to the charge pump's output current. The transistor should also be able to withstand voltages up to V_{IN} across its collector-emitter (V_{CE}).

The transistor must be able to dissipate this power without its junction becoming too hot. Note that the ability to dissipate power depends heavily on adequate PCB thermal design. The power dissipated in the transistor is given by the following equation:

$$P_Q = \left[V_{IN} - (2 \times V_F) - |V_{GL}|\right] \times I_{GL} \tag{6}$$

I_{GL} = Mean output current on V_{GL}
V_F = Diode forward voltage

A pull-down resistor is also required between the transistor's base and emitter. The value of this resistor is not critical, but it should be large enough not to divert significant current away from the base of the transistor. A value of 100 kΩ is suitable for most applications

12.12.4 Negative Charge Pump Protection

The TPS65168 contains a circuit to protect the CPN against short circuits on its output. A short circuit condition is detected as long as the FBN voltage is above 2.8 V. The base current is then limited to 320 µA typically.

12.13 TYPICAL APPLICATIONS

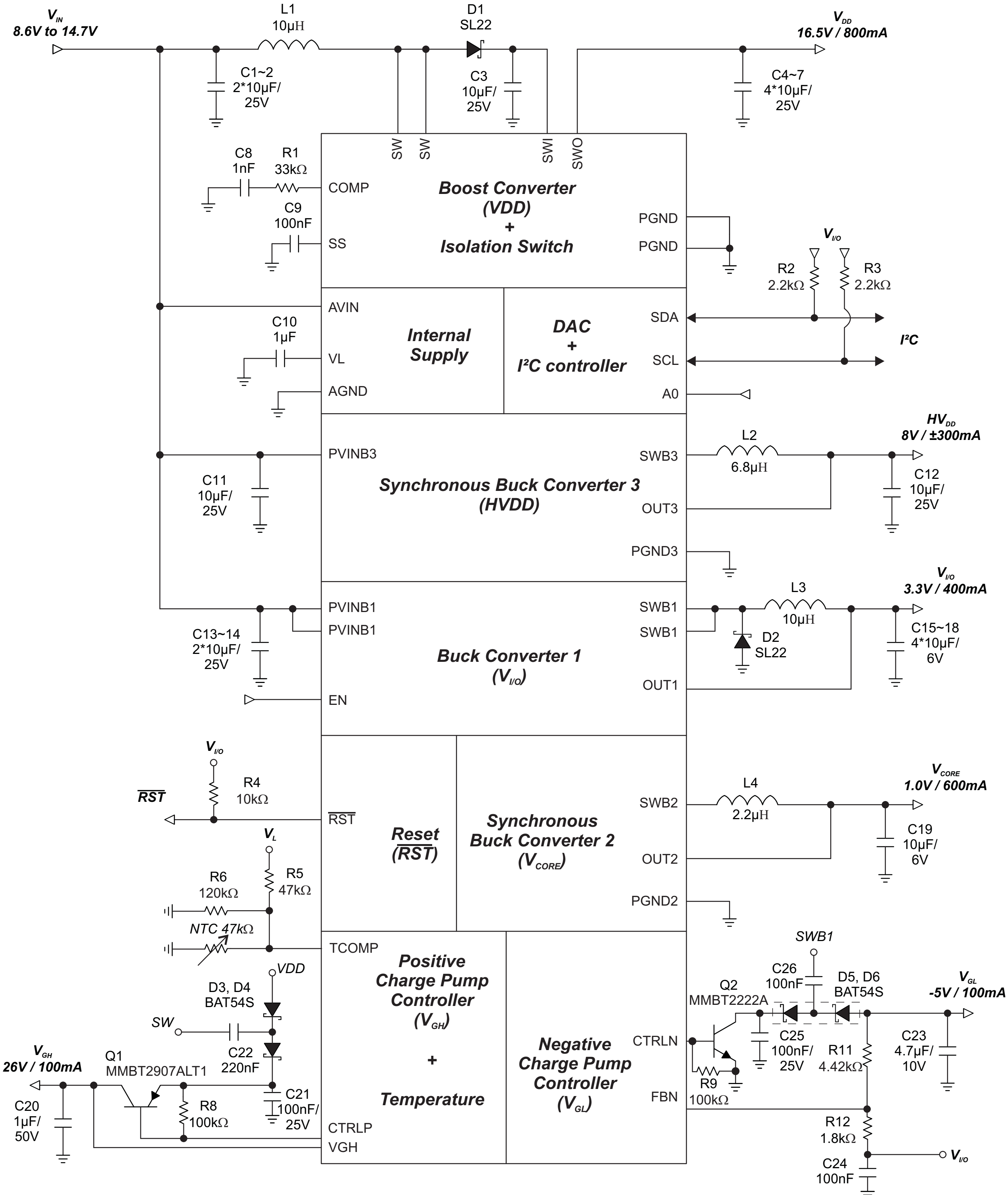


Figure 27.

12.14 PCB Layout Recommendations

NOTE

Special care must be taken for the Buck 2 and Buck 3 converters. Shielded chip inductors are highly recommended for reduced noise radiation. Keep the output sense line which act as feedback line (high ohmic and noise sensitive) away from inductor radiations and from switching lines. A bottom layer wiring is recommended to shield it from noise sources.

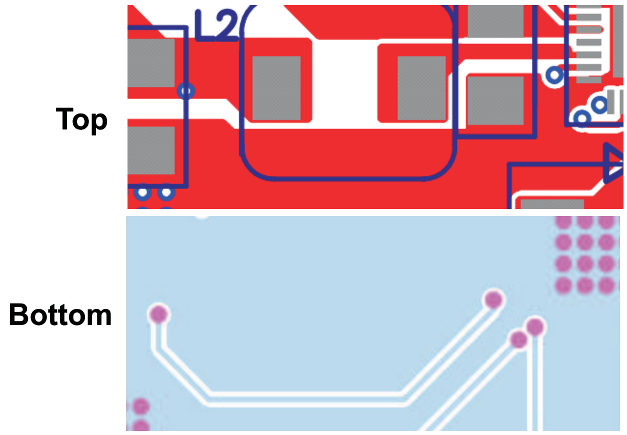


Figure 28. Recommended Layout for the sense line of Buck 3

If a wiring on the top layer is absolutely necessary and a conventional inductor is used, it is highly recommended to add a snubber circuit to the output sense line. For Buck 3 the recommended values are 150 Ω and 10 nF. See below Figure 29.

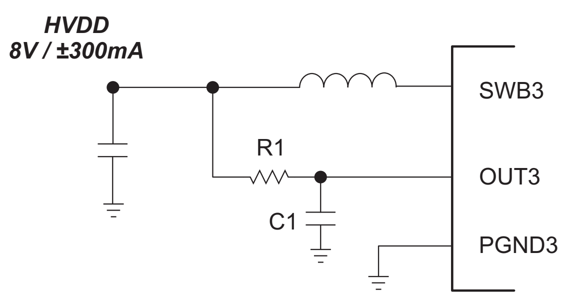


Figure 29. Connection of the snubber circuit for Buck 3

- For **high dv/dt** signals (switch pin traces): keep copper to a minimum to prevent making unintentional parallel plate capacitors with other traces or to a ground plane. Best to route signal and return on same layer.
- For **high di/dt** signals: keep traces short, wide and closely spaced. This will reduce stray inductance and decrease the current loop area to help prevent EMI.
- Always avoid vias when possible. They have high inductance and resistance. **If vias are necessary always use more than one in parallel to decrease parasitics especially for power lines.**
- Keep input capacitor close to the IC with low inductance traces.
- **Keep the copper trace between a switch node and a diode as short and wide as possible.**
- **Use single point grounding.**
- **All AGND and PGND pins must be connected to the Power Pad.**
- Isolate analog signal paths from power paths.
- Keep trace from switching node pin to inductor short: **it reduces EMI emissions and noise that may couple into other portions of the converter.**
- Output voltage feedback sampling must be taken right at output capacitor and shielded.

13 APPENDIX – I^{2}C INTERFACE

13.1 I^{2}C Serial Interface Description

TPS65168 communicates through an industry standard two-wire interface, I^{2}C, to receive data in slave mode.

I^{2}C is a 2-wire serial interface developed by Philips Semiconductor (see I2C-Bus Specification, Version 2.1, January 2000). The bus consists of a data line (SDA) and a clock line (SCL) with pull-up structures. When the bus is idle, both SDA and SCL lines are pulled high. All the I^{2}C compatible devices connect to the I^{2}C bus through open drain I/O pins, SDA and SCL. A master device, usually a microcontroller or a digital signal processor, controls the bus. The master is responsible for generating the SCL signal and device addresses. The master also generates specific conditions that indicate the START and STOP of data transfer. A slave device receives and/or transmits data on the bus under control of the master device.

The TPS65168 works as a slave and supports the following data transfer modes, as defined in the I^{2}C-Bus specification: standard mode (100 kbps) and fast mode (400 kbps). The data transfer protocol for standard and fast modes is exactly the same, therefore they are referred to as F/S-mode in this document. The TPS65168 supports 7-bit addressing. The device 7-bit address is defined as '010000X' (see Figure 30), where the bit X can be selected depending on the address pin configuration of A0 and the LSB enables the write or read function. Address pin A0 connected to GND results in a 0 in the corresponding bit position and connection to a logic high level results in a 1 in the corresponding bit positions

(MSB)	TPS65168 Address						(LSB)
0	1	0	0	0	0	A0	R/$\overline{W}$

NOTE: R/$\overline{W}$ = R/(W)

Figure 30. TPS65168 Slave Address Byte

The device that initiates the communication is called a master, and the devices controlled by the master are slaves. The master generates the serial clock on SCL, controls the bus access, and generates START and STOP conditions (see Figure 31). A START initiates a new data transfer to slave. Transitioning SDA from high to low while SCL remains high generates a START condition. A STOP condition ends a data transfer to slave. Transitioning SDA from low to high while SCL remains high generates a STOP condition.

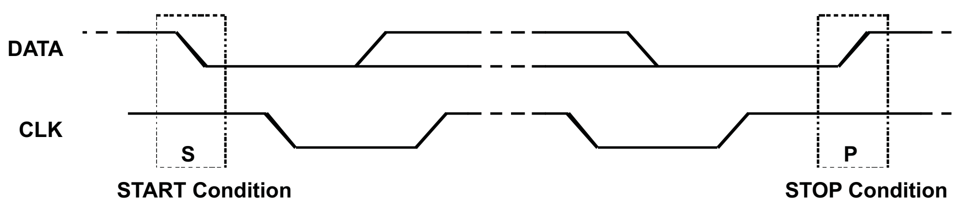


Figure 31. START and STOP Conditions

The master then generates the SCL pulses, and transmits the 7-bit address and the read/write direction bit R/(W) on the SDA line. During all transmissions, the master ensures that the data is valid. A valid data condition requires the SDA line to be stable during the entire high period of the clock pulse (see Figure 32). All devices recognize the address sent by the master and compare it to their internal fixed addresses. Only the slave device with a matching address generates an Acknowledgment, ACK, (see Figure 33) by pulling the SDA line low during the entire high period of the SCL cycle. Upon detecting this Acknowledgment, the master knows that communication link with a slave has been established.

I²C Serial Interface Description (continued)

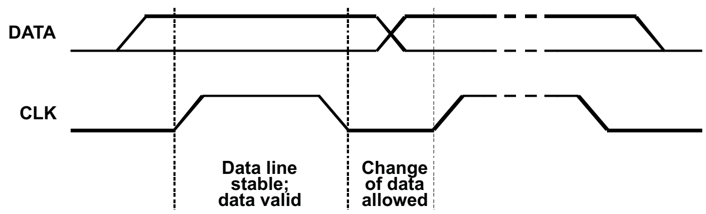


Figure 32. Bit Transfer on the Serial Interface

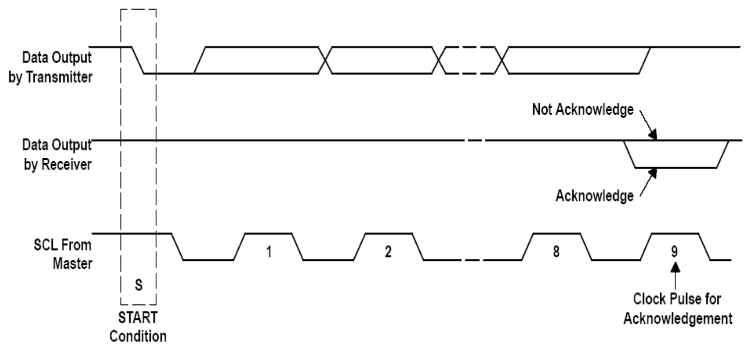


Figure 33. Acknowledge on the I²C Bus

The master generates further SCL cycles to either transmit data to the slave (R/(W) bit = 0) or receive data from the slave (R/(W) bit = 1). In either case, the receiver needs to acknowledge the data sent by the transmitter. So an acknowledge signal can either be generated by the master or by the slave, depending on which one is the receiver. 9-bit valid data sequences consisting of 8-bit data and 1-bit acknowledge can continue as long as necessary. To terminate the data transfer, the master generates STOP condition by pulling the SDA line from low to high while the SCL line is high (see Figure 34). This releases the bus and stops the communication link with the addressed slave. All I²C compatible devices must recognize the stop condition. Upon the receipt of a stop condition, all devices know that the bus is released, and they wait for a start condition followed by a matching address.

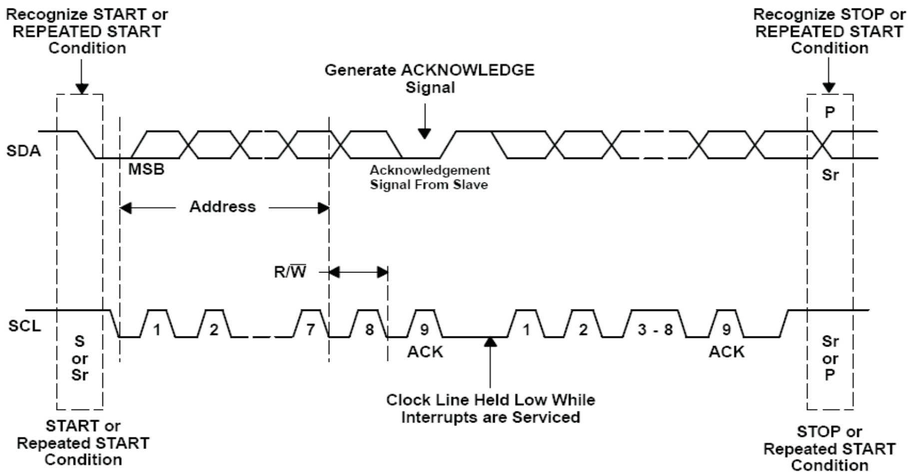


Figure 34. Bus Protocol

Attempting to read data from register addresses not listed in the following section will result in 00h being read out.

13.2 MEMORY DESCRIPTION

The TPS65168 has one non-volatile memory which contains the initial value of the DAC and one volatile memory which contains the DAC setting. The non-volatile memory is called the Initial Value Register (IVR) and the volatile memory is called DAC Register (DR). The non-volatile IVR and the volatile DR are accessed with the same address.

Startup option: At power-up, the value contained in the IVR is loaded into the volatile DR and IVR presets the DAC to the last stored setting. The factory programmed value of the IVR of each address is described on Table 3 and, at power-up, these data byte set the output voltage of each rail.

Write description: The user has to program all data registers first (00h ~ 09h), then set the WED (Write EEPROM Data) bit to 1 once all desired data are addressed. A dead time of 50 ms is then initiated during which all the register data (00h ~ 09h) are stored into the non volatile EEPROM cell. During that time, there should be no data flowing through the I^{2}C because the I^{2}C interface is momentarily not responding.

After the 50 ms have passed, the WED bit is automatically reset to 0, and the user is able to read the values or program again.

Table 9. Memory Map

REGISTER	NAME	ADDRESS	VOLATILE/NONVOLATILE	FACTORY (Power-Up Default)
VDD	Boost	00h	6Bit Nonvolatile	21h
HVDD	Buck 3	01h	6Bit Nonvolatile	20h
VI/O	Buck 1	02h	3Bit Nonvolatile	03h
VCORE	Buck 2	03h	4Bit Nonvolatile	01h
VGH(COLD)	Positive charge pump (Low temperature)	04h	4Bit Nonvolatile	09h
VGH(HOT)	Positive charge pump (High temperature)	05h	4Bit Nonvolatile	09h
VGL	Negative charge pump	06h	6Bit Nonvolatile	20h
DLY1	V_{GL} delay	07h	3Bit Nonvolatile	01h
DLY2	V_{DD} delay	08h	3Bit Nonvolatile	03h
DLY3	V_{GH} delay	09h	3Bit Nonvolatile	03h
CR	Control Register	FFh	Volatile	00h

13.3 DAC REGISTER (DR) AND INITIAL VALUE REGISTER (IVR)

VDD Register (with factory value) – 00h:

MSB			Address 00h				LSB
Reserved	Reserved	1	0	0	0	0	1

HVDD Register (with factory value) – 01h:

MSB			Address 01h				LSB
Reserved	Reserved	1	0	0	0	0	0

VI/O Register (with factory value) – 02h:

MSB			Address 02h				LSB
Reserved	Reserved	Reserved	Reserved	Reserved	0	1	1

VCORE Register (with factory value) – 03h:

MSB			Address 03h				LSB
Reserved	Reserved	Reserved	Reserved	0	0	0	1

VGH(COLD) Register (with factory value) – 04h:

MSB			Address 04h				LSB
Reserved	Reserved	Reserved	Reserved	1	0	0	1

VGH(HOT) Register (with factory value) – 05h:

MSB			Address 05h				LSB
Reserved	Reserved	Reserved	Reserved	1	0	0	1

VGL Register (with factory value) – 06h:

MSB			Address 06h				LSB
Reserved	Reserved	1	0	0	0	0	0

DLY1 Register (with factory value) – 07h:

MSB			Address 07h				LSB
Reserved	Reserved	Reserved	Reserved	Reserved	0	0	1

DLY2 Register (with factory value) – 08h:

MSB			Address 08h				LSB
Reserved	Reserved	Reserved	Reserved	Reserved	0	1	1

DLY3 Register (with factory value) – 09h:

MSB			Address 09h				LSB
Reserved	Reserved	Reserved	Reserved	Reserved	0	1	1

Control Register – FFh:

MSB			Address FFh				LSB
WED (Write EEPROM Data)	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	EE/(DR) (EEPROM or DR Read)

13.4 WRITING / READING PROTOCOL

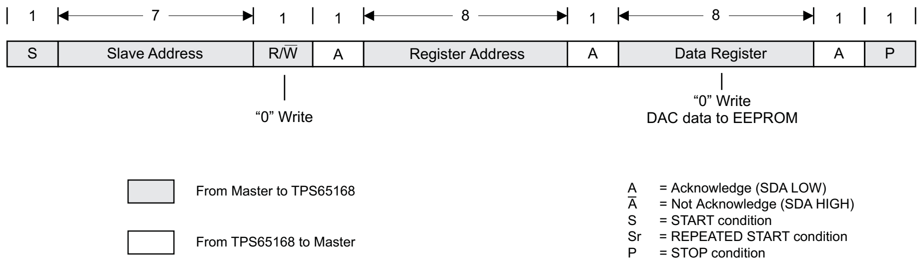


Figure 35. "Write" DAC Register Data Transfer Format

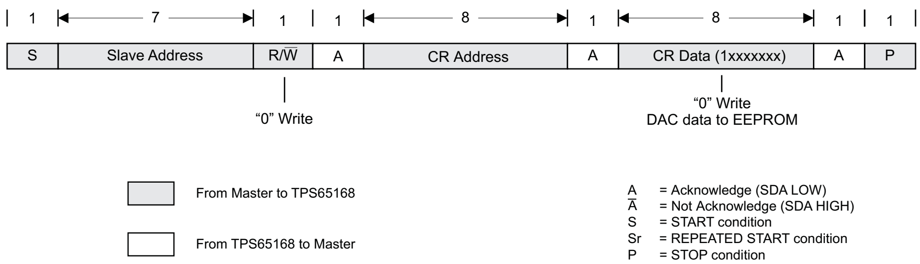


Figure 36. "Write" EEPROM Register Data Transfer Format

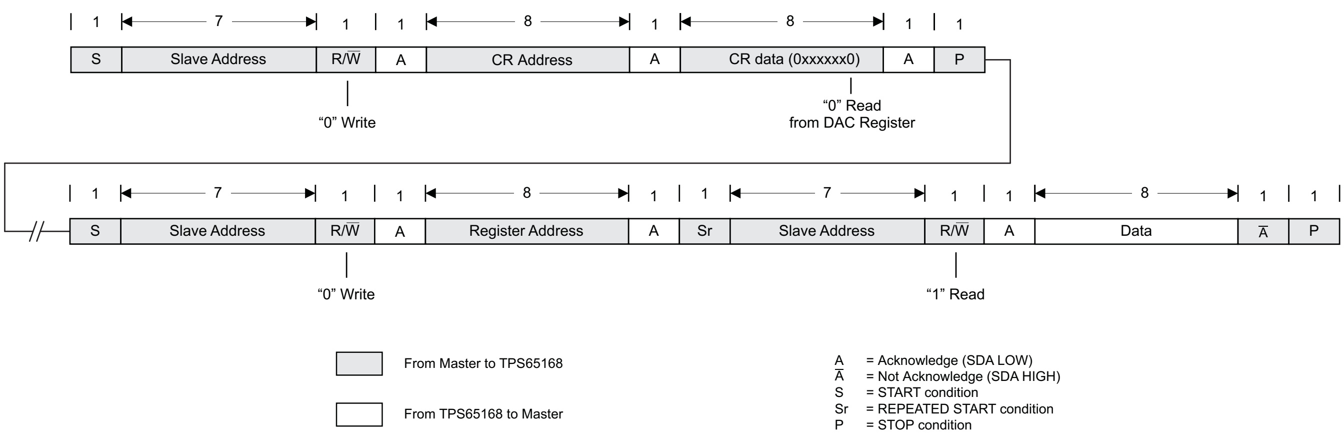


Figure 37. "Read" DAC Register Data Transfer Format

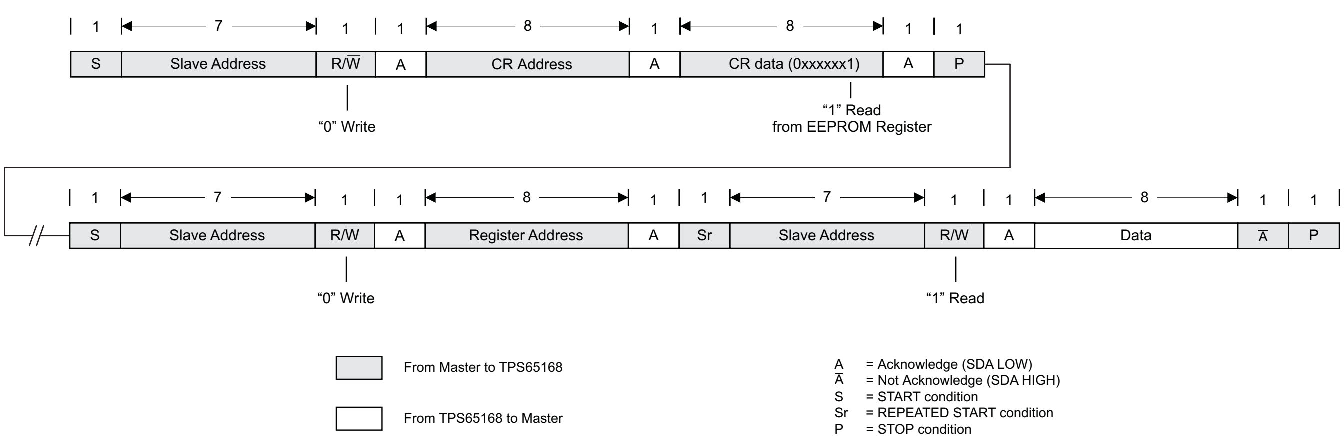


Figure 38. "Read" EEPROM Register Data Transfer Format

13.5 DAC SETTING

The following tables show the DAC values and the corresponding voltages of each block address.

VDD (00h)

DAC value	VDD	DAC value	VDD
00h	12.82 V	20h	15.95 V
01h	12.92 V	21h	16.05 V
02h	13.02 V	22h	16.14 V
03h	13.11 V	23h	16.24 V
04h	13.21 V	24h	16.34 V
05h	13.31 V	25h	16.44 V
06h	13.41 V	26h	16.54 V
07h	13.50 V	27h	16.63 V
08h	13.60 V	28h	16.73 V
09h	13.70 V	29h	16.83 V
0Ah	13.80 V	2Ah	16.93 V
0Bh	13.90 V	2Bh	17.02 V
0Ch	13.99 V	2Ch	17.12 V
0Dh	14.09 V	2Dh	17.22 V
0Eh	14.19 V	2Eh	17.32 V
0Fh	14.29 V	2Fh	17.42 V
10h	14.38 V	30h	17.51 V
11h	14.48 V	31h	17.61 V
12h	14.58 V	32h	17.71 V
13h	14.68 V	33h	17.81 V
14h	14.78 V	34h	17.90 V
15h	14.87 V	35h	18.00 V
16h	14.97 V	36h	18.10 V
17h	15.07 V	37h	18.20 V
18h	15.17 V	38h	18.30 V
19h	15.26 V	39h	18.39 V
1Ah	15.36 V	3Ah	18.49 V
1Bh	15.46 V	3Bh	18.59 V
1Ch	15.56 V	3Ch	18.69 V
1Dh	15.66 V	3Dh	18.78 V
1Eh	15.75 V	3Eh	18.88 V
1Fh	15.85 V	3Fh	18.98 V

HVDD (01h)

DAC value	HVDD	DAC value	HVDD
00h	6.40 V	20h	8.00 V
01h	6.45 V	21h	8.05 V
02h	6.50 V	22h	8.10 V
03h	6.55 V	23h	8.15 V
04h	6.60 V	24h	8.20 V
05h	6.65 V	25h	8.25 V
06h	6.70 V	26h	8.30 V
07h	6.75 V	27h	8.35 V
08h	6.80 V	28h	8.40 V
09h	6.85 V	29h	8.45 V
0Ah	6.90 V	2Ah	8.50 V
0Bh	6.95 V	2Bh	8.55 V
0Ch	7.00 V	2Ch	8.60 V
0Dh	7.05 V	2Dh	8.65 V
0Eh	7.10 V	2Eh	8.70 V
0Fh	7.15 V	2Fh	8.75 V
10h	7.20 V	30h	8.80 V
11h	7.25 V	31h	8.85 V
12h	7.30 V	32h	8.90 V
13h	7.35 V	33h	8.95 V
14h	7.40 V	34h	9.00 V
15h	7.45 V	35h	9.05 V
16h	7.50 V	36h	9.10 V
17h	7.55 V	37h	9.15 V
18h	7.60 V	38h	9.20 V
19h	7.65 V	39h	9.25 V
1Ah	7.70 V	3Ah	9.30 V
1Bh	7.75 V	3Bh	9.35 V
1Ch	7.80 V	3Ch	9.40 V
1Dh	7.85 V	3Dh	9.45 V
1Eh	7.90 V	3Eh	9.50 V
1Fh	7.95 V	3Fh	9.55 V

DAC SETTING (continued)

VGL (06h)

DAC value	VGL	DAC value	VGL
00h	-1.8 V	20h	-5.0 V
01h	-1.9 V	21h	-5.1 V
02h	-2.0 V	22h	-5.2 V
03h	-2.1 V	23h	-5.3 V
04h	-2.2 V	24h	-5.4 V
05h	-2.3 V	25h	-5.5 V
06h	-2.4 V	26h	-5.6 V
07h	-2.5 V	27h	-5.7 V
08h	-2.6 V	28h	-5.8 V
09h	-2.7 V	29h	-5.9 V
0Ah	-2.8 V	2Ah	-6.0 V
0Bh	-2.9 V	2Bh	-6.1 V
0Ch	-3.0 V	2Ch	-6.2 V
0Dh	-3.1 V	2Dh	-6.3 V
0Eh	-3.2 V	2Eh	-6.4 V
0Fh	-3.3 V	2Fh	-6.5 V
10h	-3.4 V	30h	-6.6 V
11h	-3.5 V	31h	-6.7 V
12h	-3.6 V	32h	-6.8 V
13h	-3.7 V	33h	-6.9 V
14h	-3.8 V	34h	-7.0 V
15h	-3.9 V	35h	-7.1 V
16h	-4.0 V	36h	-7.2 V
17h	-4.1 V	37h	-7.3 V
18h	-4.2 V	38h	-7.4 V
19h	-4.3 V	39h	-7.5 V
1Ah	-4.4 V	3Ah	-7.6 V
1Bh	-4.5 V	3Bh	-7.7 V
1Ch	-4.6 V	3Ch	-7.8 V
1Dh	-4.7 V	3Dh	-7.9 V
1Eh	-4.8 V	3Eh	-8.0 V
1Fh	-4.9 V	3Fh	-8.1 V

VGH (04h - COLD) (05h - HOT)

DAC value	VGH(COLD)
00h	19 V
01h	20 V
02h	21 V
03h	22 V
04h	23 V
05h	24 V
06h	25 V
07h	26 V
08h	27 V
09h	28 V
0Ah	29 V
0Bh	30 V
0Ch	31 V
0Dh	32 V
0Eh	33 V
0Fh	34 V

DAC value	VGH(HOT)
00h	17 V
01h	18 V
02h	19 V
03h	20 V
04h	21 V
05h	22 V
06h	23 V
07h	24 V
08h	25 V
09h	26 V
0Ah	27 V
0Bh	28 V
0Ch	29 V
0Dh	30 V
0Eh	31 V
0Fh	32 V

VI/O (02h)

DAC value	VCC
00h	3.0 V
01h	3.1 V
02h	3.2 V
03h	3.3 V
04h	3.4 V
05h	3.5 V
06h	3.6 V
07h	3.7 V

VCORE (03h)

DAC value	VCORE
00h	0.9 V
01h	1.0 V
02h	1.1 V
03h	1.2 V
04h	1.3 V
05h	1.4 V
06h	1.5 V
07h	1.6 V
08h	1.7 V
09h	1.8 V
0Ah	1.9 V
0Bh	2.0 V
0Ch	2.1 V
0Dh	2.2 V
0Eh	2.3 V
0Fh	2.4 V

DLYx

(07h - DLY1)
(08h - DLY2)
(09h - DLY3)

DAC value	DLY1	DAC value	DLY2	DAC value	DLY3
00h	0 ms	00h	0 ms	00h	0 ms
01h	5 ms	01h	5 ms	01h	5 ms
02h	10 ms	02h	10 ms	02h	10 ms
03h	15 ms	03h	15 ms	03h	15 ms
04h	20 ms	04h	20 ms	04h	20 ms
05h	25 ms	05h	25 ms	05h	25 ms
06h	30 ms	06h	30 ms	06h	30 ms
07h	35 ms	07h	35 ms	07h	35 ms

DAC SETTING (continued)

13.5.1 Write Operation

Writing to DAC Register (DR):

1. Master sends START condition on the bus.
2. Send the device address, 010000A_0, and R/(W) bit = Low.
   TPS65168 will acknowledge this byte.
3. Send DAC Register address of 00h (DR address 00h – VDD).
   TPS65168 will acknowledge this byte.
4. Send the data byte to be written to DR and to DAC.
   TPS65168 will acknowledge this byte.
5. Master sends STOP condition on the bus.
6. Repeat the above operations for DR addresses 01h ~ 09h

Example: Writing 29h to DR address 06h (VGL) and VGL DAC

START	0	1	0	0	0	0	A_0	0	Slave ACK	0	0	0	0	0	1	1	0	Slave ACK	0	0	1	0	1	0	0	1	Slave ACK	STOP

Writing to EEPROM:

1. Master sends START condition on the bus.
2. Send the device address, 010000A_0, and R/(W) bit = Low.
   TPS65168 will acknowledge this byte.
3. Send CR (Control register) address of FFh (WED bit).
   TPS65168 will acknowledge this byte.
4. Send data byte of 80h, to write data byte from DR 00h ~ 09h to EEPROM
   TPS65168 will acknowledge this byte.
5. Master sends STOP condition on the bus

Example: Writing DR data into EEPROM

START	0	1	0	0	0	0	A_0	0	Slave ACK	1	1	1	1	1	1	1	1	Slave ACK	1	0	0	0	0	0	0	0	Slave ACK	STOP

Note: *it is not possible to write data from a single DAC register into the EEPROM, all DR data from 00h to 09h will be written into the EEPROM at one time.*

13.5.2 Read Operation

Reading from DR:

1. Master sends START condition on the bus.
2. Send the device address, 010000A_0, and R/(W) bit = Low.
   TPS65168 will acknowledge this byte.
3. Send CR register address of FFh.
   TPS65168 will acknowledge this byte.
4. Send data byte of 00h (EE/(DR) bit), to specify that the data is read from DR.
   TPS65168 will acknowledge this byte.
5. Master sends STOP condition on the bus
6. Master sends START condition on the bus.
7. Send the device address, 010000A_0, and R/(W) bit =Low.
   TPS65168 will acknowledge this byte.
8. Send desired DAC Register address to be read (00h ~ 09h).
   TPS65168 will acknowledge this byte.
9. Master sends START condition on the bus again.
10. Send the device address, 010000A_0, and R/(W) bit = High.
    TPS65168 will acknowledge this byte.
11. Read data from DR.
    Master will not acknowledge this byte
12. Master sends STOP condition on the bus.

Example: Reading data from DR address 05h (VGH(HOT))

START	0	1	0	0	0	0	A_0	0	SACK	1	1	1	1	1	1	1	1	SACK	0	0	0	0	0	0	0	0	SACK	STOP
START	0	1	0	0	0	0	A_0	0	SACK	0	0	0	0	0	1	0	1	SACK										
START	0	1	0	0	0	0	A_0	1	SACK	0	0	0	0	x	x	x	x	MNACK	STOP									

Reading from EEPROM (IVR):

1. Master sends START condition on the bus.
2. Send the device address, 010000A_0, and R/(W) bit = Low.
   TPS65168 will acknowledge this byte.
3. Send CR register address of FFh.
   TPS65168 will acknowledge this byte.
4. Send data byte of 01h (EE/(DR) bit), to specify that the data is read from EEPROM.
   TPS65168 will acknowledge this byte.
5. Master sends STOP condition on the bus
6. Master sends START condition on the bus.
7. Send the device address, 010000A_0, and R/(W) bit =Low.
   TPS65168 will acknowledge this byte.
8. Send desired DR/IVR address to be read (00h ~ 09h).
   TPS65168 will acknowledge this byte.
9. Master sends START condition on the bus again.
10. Send the device address, 010000A_0, and R/(W) bit = High.
    TPS65168 will acknowledge this byte.
11. Read data from IVR.
    Master will not acknowledge this byte
12. Master sends STOP condition on the bus.

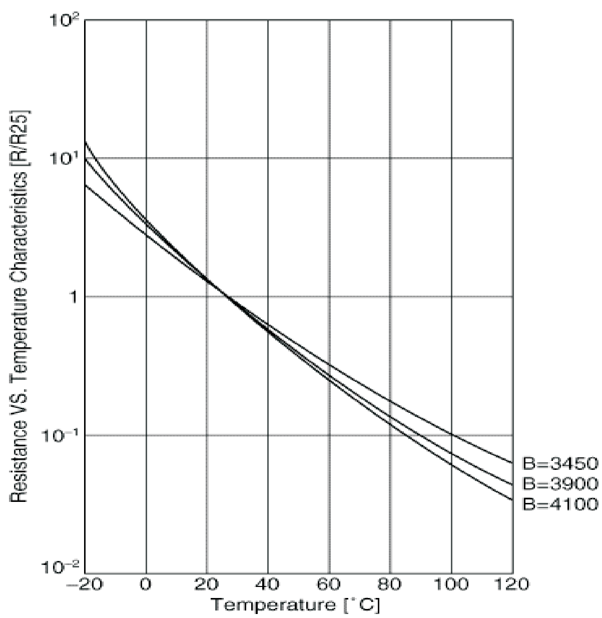
Example: Reading data from EEPROM address 09h (DLY3)

START	0	1	0	0	0	0	A_0	0	SACK	1	1	1	1	1	1	1	1	SACK	0	0	0	0	0	0	0	1	SACK	STOP
START	0	1	0	0	0	0	A_0	0	SACK	0	0	0	0	1	0	0	1	SACK										
START	0	1	0	0	0	0	A_0	1	SACK	0	0	0	0	0	x	x	x	MNACK	STOP									

13.6 TEMPERATURE COMPENSATION

Table 10. NTC 47 kΩ – NCP18WB473F10RB – Characteristics

Global Part Number	NCP18WB473F10RB
Resistance (25°C)	47 kΩ ±1%
B-Constant (25/50°C)	4050K ±1.5%
B-Constant (25/80°C)(Reference Value)	4101K
B-Constant (25/85°C)(Reference Value)	4108K
B-Constant (25/100°C)(Reference Value)	4131K
Permissive Operating Current (25°C)	0.14mA
Rated Electric Power (25°C)	100mW
Typical Dissipation Constant (25°C)	1mW/°C
Min. Operating Temp. Range	–40°C
Max. Operating Temp. Range	125°C



PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
TPS65168RSBR	ACTIVE	WQFN	RSB	40	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	TPS 65168	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

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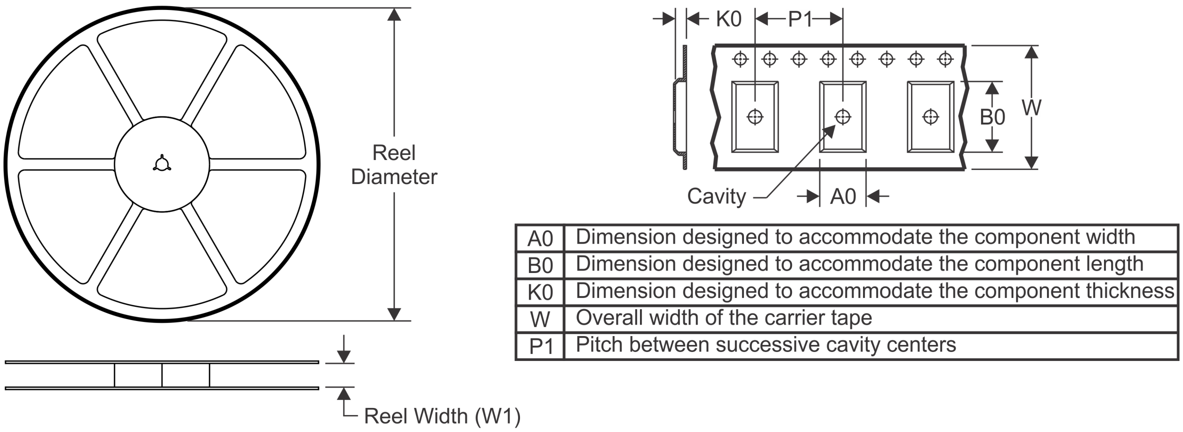
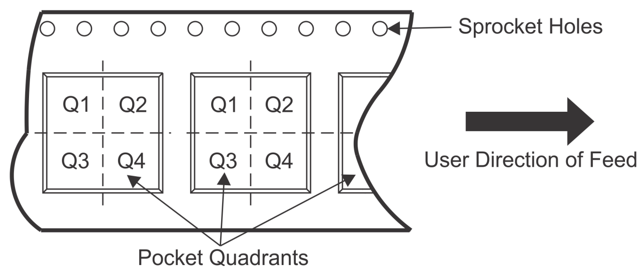
TAPE AND REEL INFORMATION



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

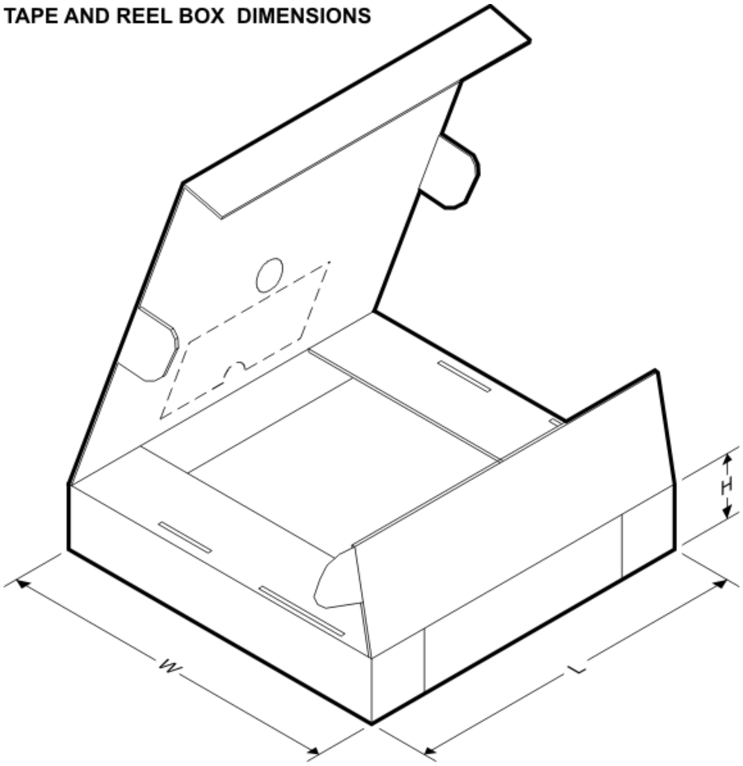
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS65168RSBR	WQFN	RSB	40	3000	330.0	12.4	5.3	5.3	1.5	8.0	12.0	Q2
TPS65168RSBR	WQFN	RSB	40	3000	330.0	12.4	5.3	5.3	1.5	8.0	12.0	Q2

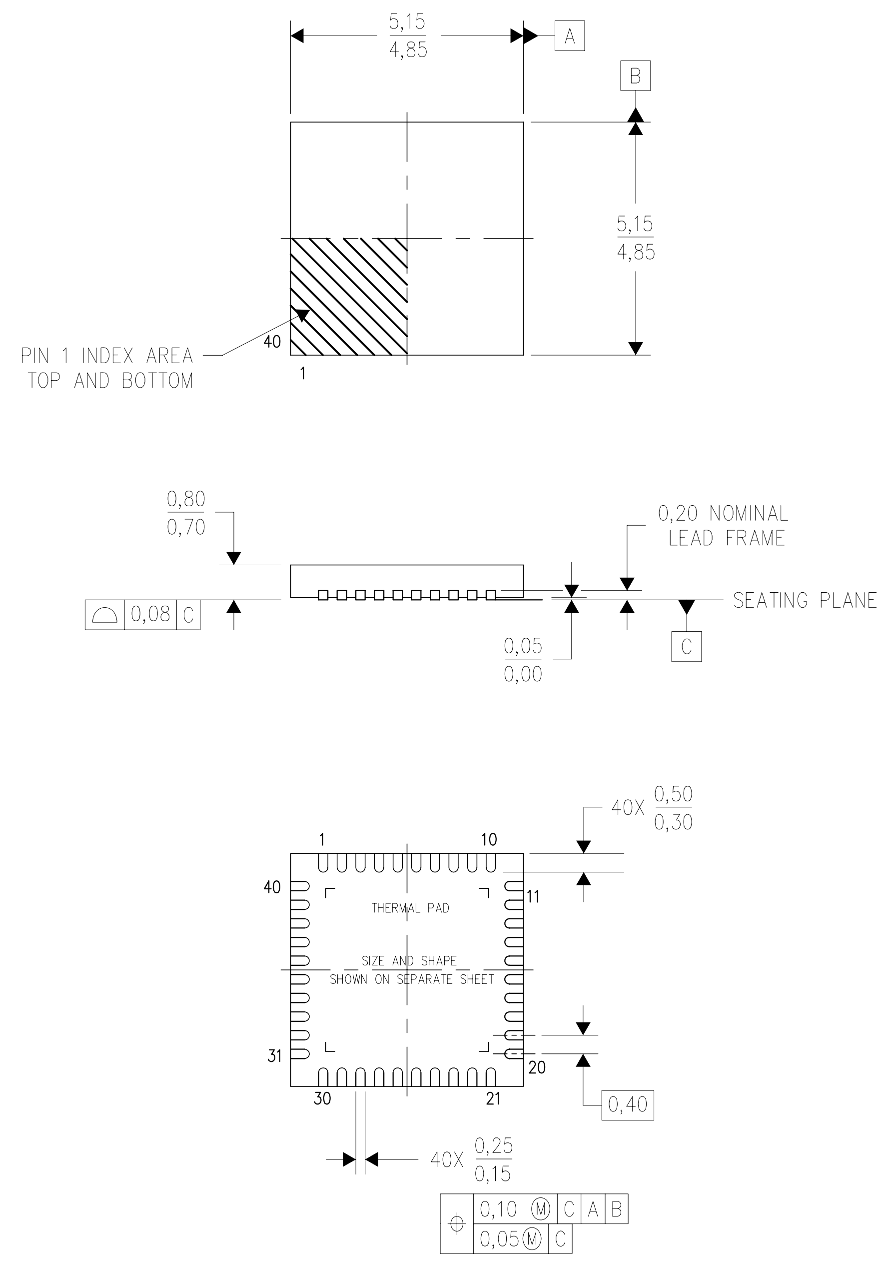
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS65168RSBR	WQFN	RSB	40	3000	367.0	367.0	35.0
TPS65168RSBR	WQFN	RSB	40	3000	367.0	367.0	35.0

RSB (S-PWQFN-N40) PLASTIC QUAD FLATPACK NO-LEAD



4207182/C 05/11

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
B. This drawing is subject to change without notice.
C. QFN (Quad Flatpack No-Lead) Package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.

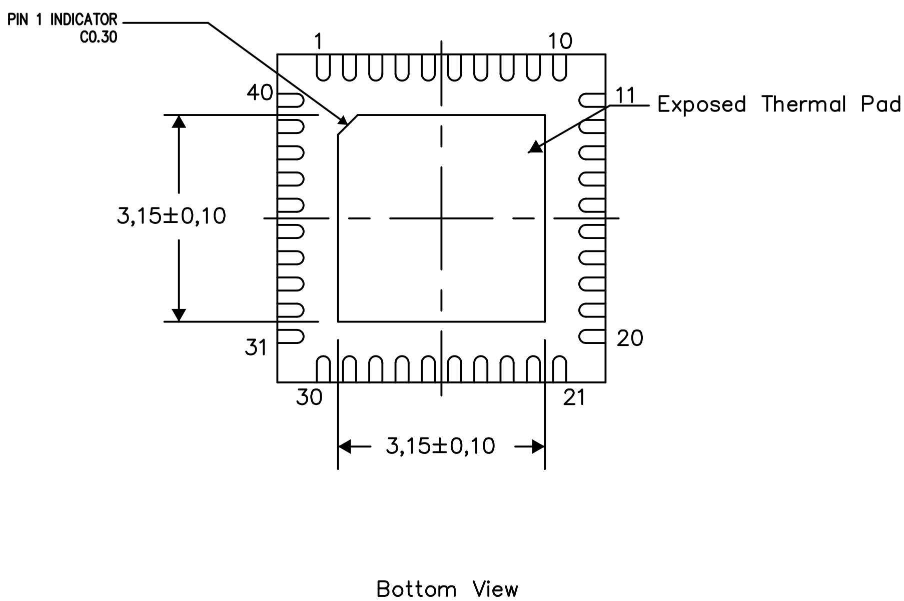
RSB (S–PWQFN–N40) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.

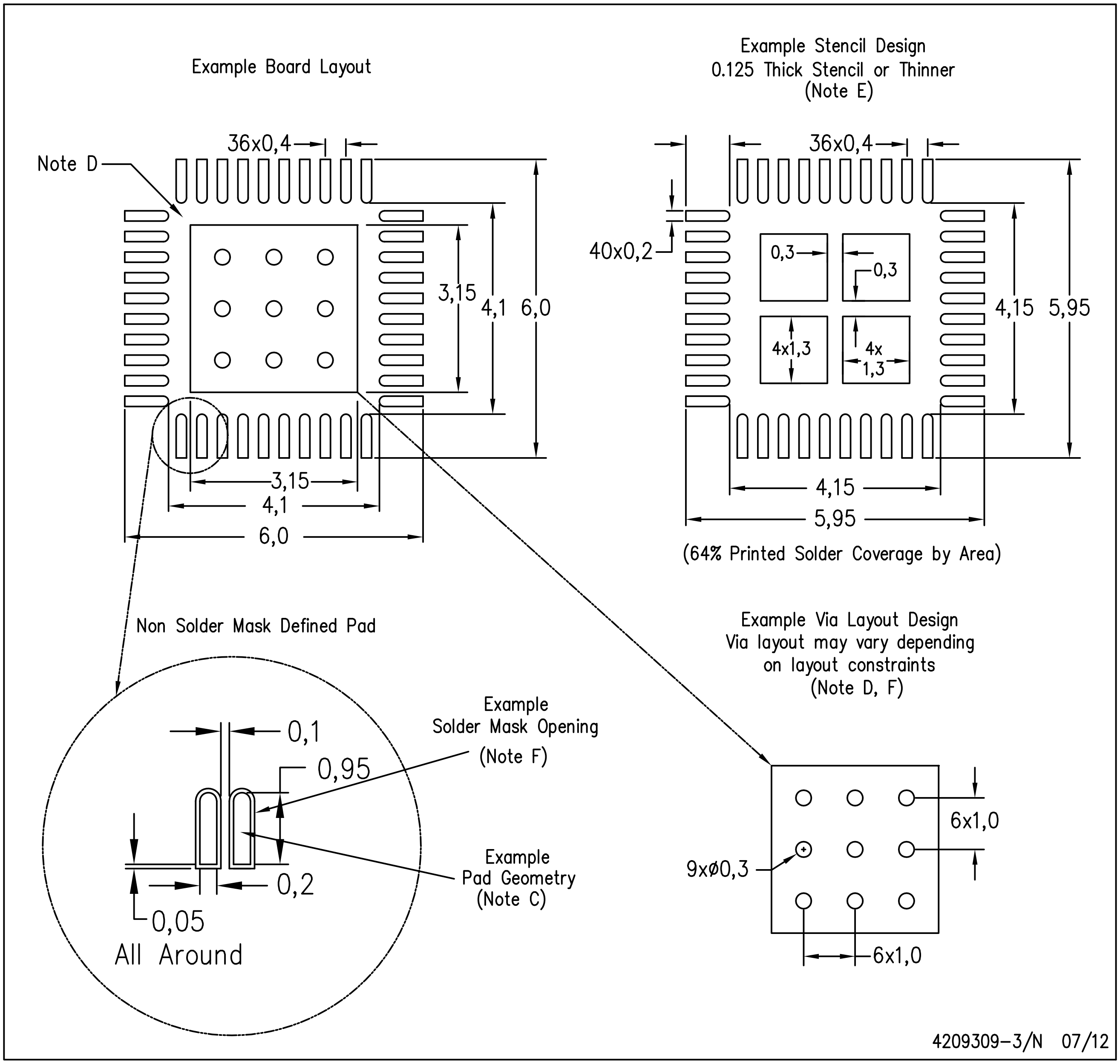


Exposed Thermal Pad Dimensions

4207183–3/P 06/12

NOTE: All linear dimensions are in millimeters

RSB (S-PWQFN-N40) PLASTIC QUAD FLATPACK NO-LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC-7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat-Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http: //www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for vias placed in the thermal pad.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS65168RSBR	ACTIVE	WQFN	RSB	40	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	TPS 65168	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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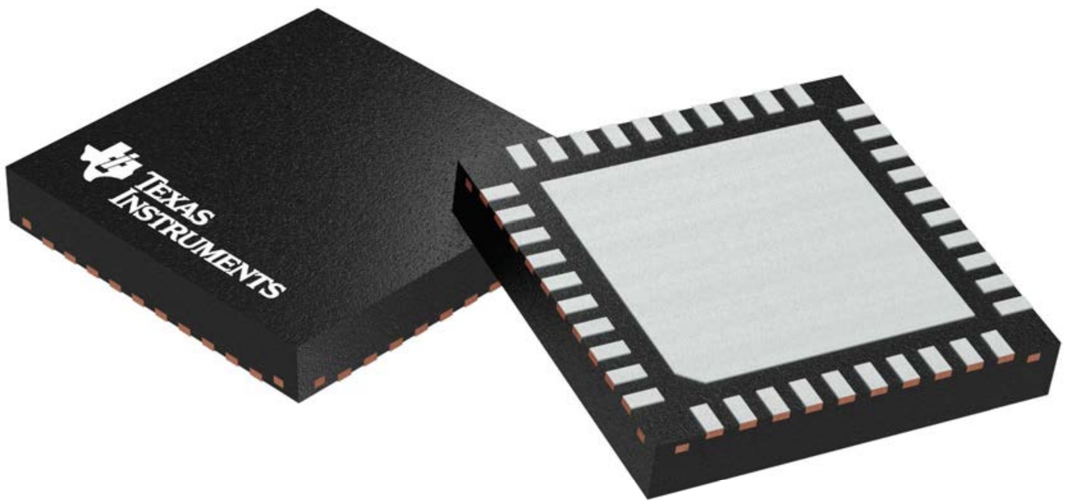
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

RSB 40

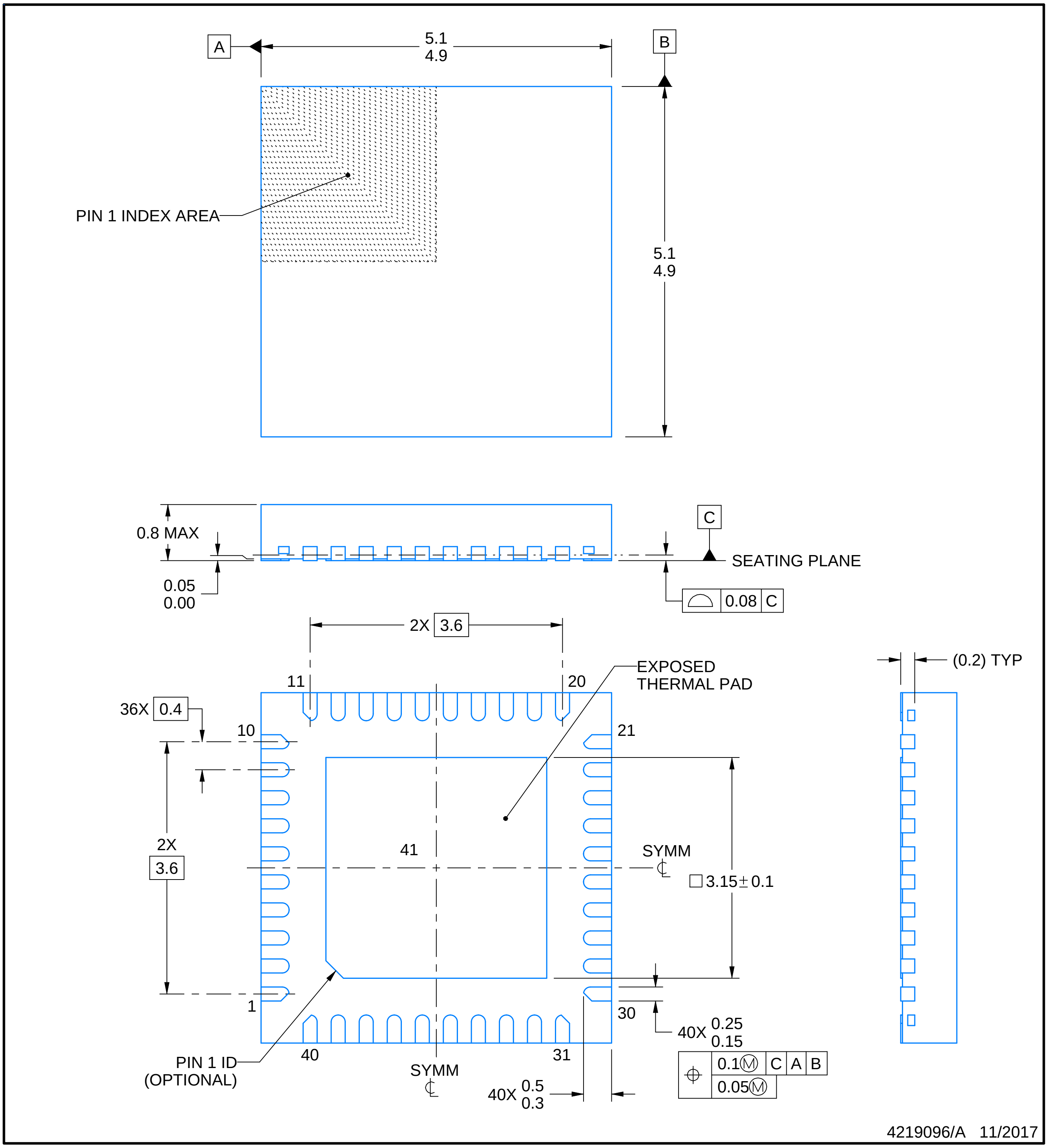
WQFN - 0.8 mm max height

5 x 5 mm, 0.4 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

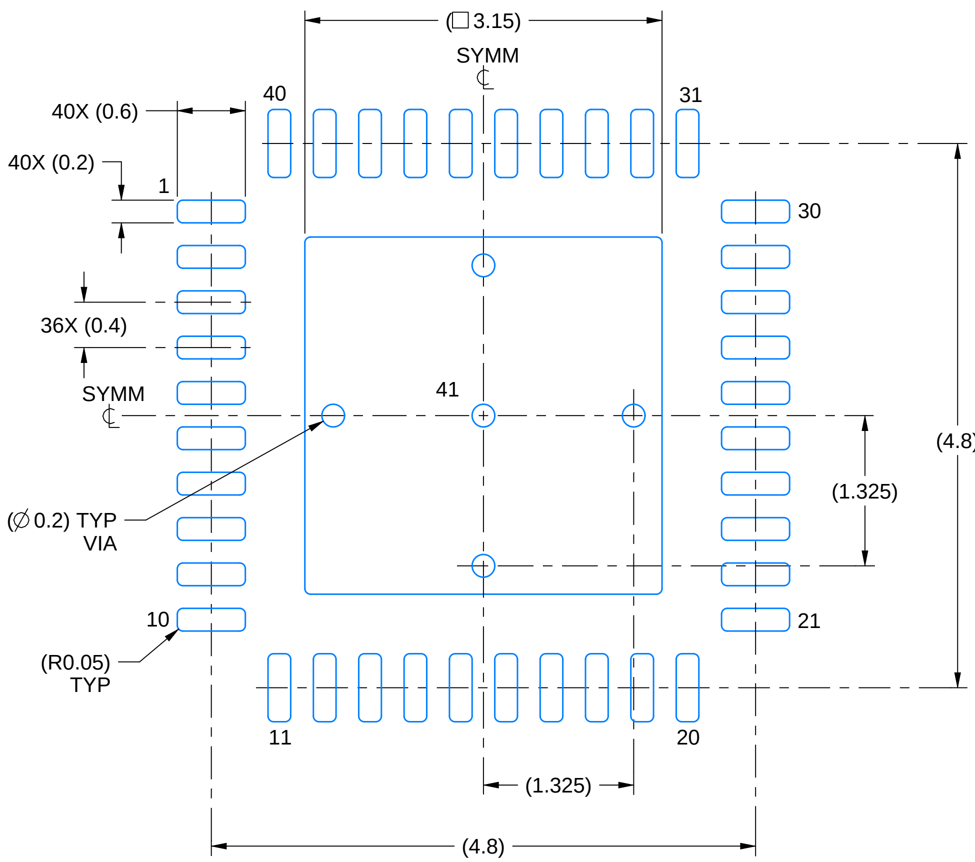


Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

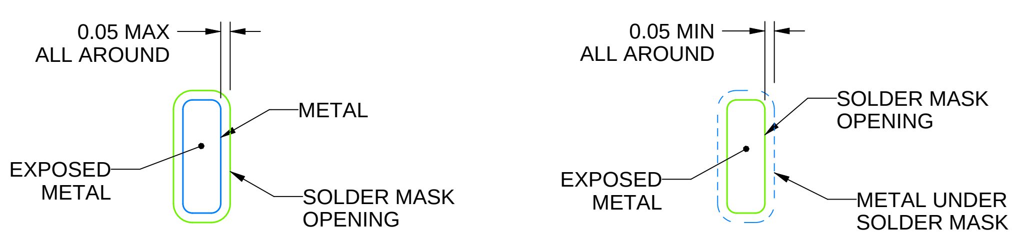


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



NON SOLDER MASK
DEFINED
(PREFERRED)

SOLDER MASK
DEFINED

SOLDER MASK DETAILS

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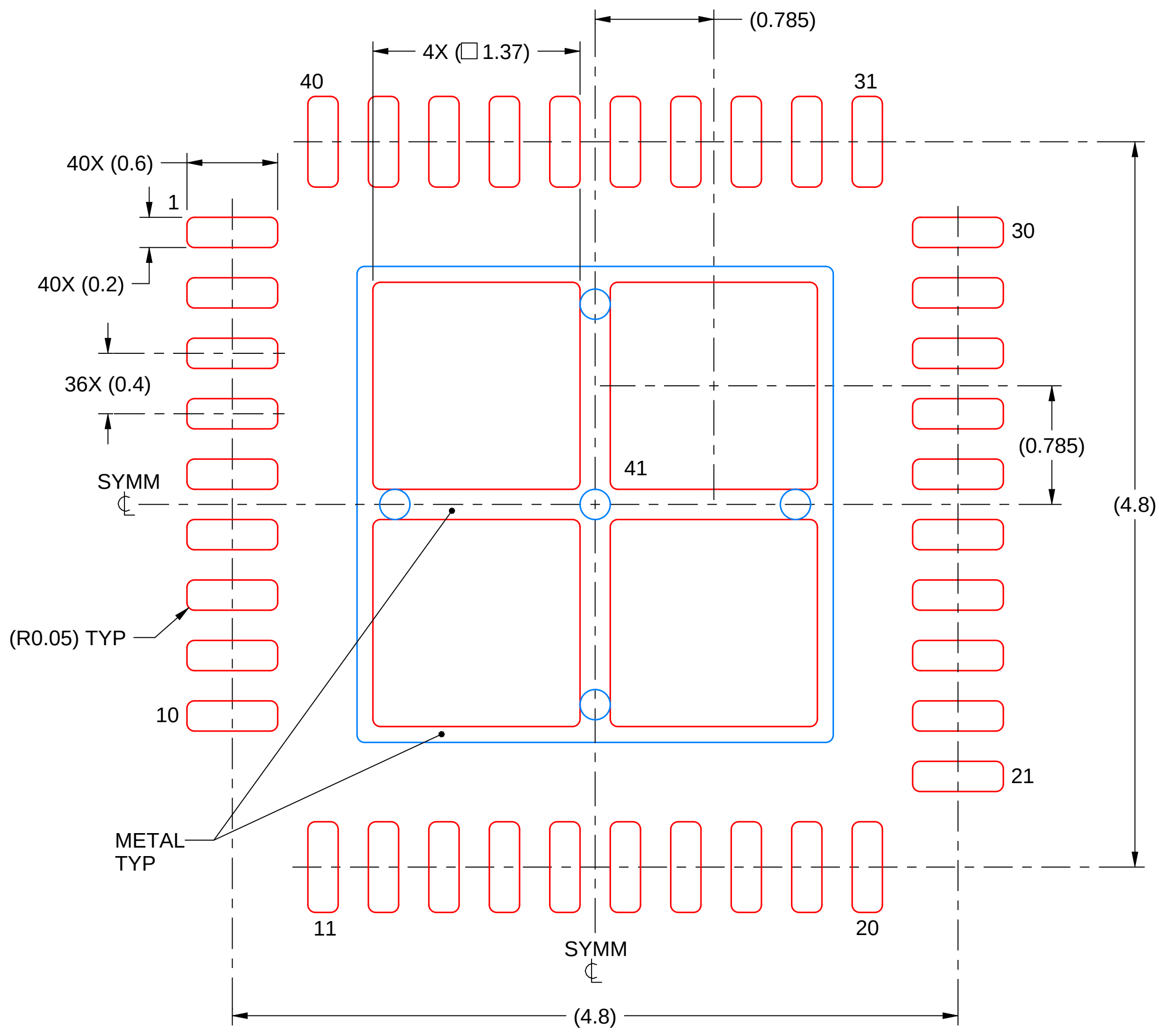
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL

EXPOSED PAD 41
75% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:20X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.