4.5-V TO 16-V INPUT, HIGH CURRENT, SYNCHRONOUS STEP DOWN DUAL BUCK CONVERTER WITH INTEGRATED FETS

Check for Samples: TPS65253

FEATURES

- Wide Input Supply Voltage Range: 4.5 V - 16 V
- Output Range: 0.8 V to ~V_{IN}-1 V
- Fully Integrated Dual Buck, 3.5-A/2.5-A Continuous Current (4-A/3-A Maximum Current)
- High Efficiency
- 300-kHz - 1.2-MHz Switching Frequency Set by External Resistor
- External Enable/Sequencing Pins
- Adjustable Cycle-by-Cycle Current Limit Set by External Resistor
- Soft-Start Pins
- Current-Mode Control With Simple Compensation Circuit
- Power Good and Reset Generator
- Low Power Mode Set By External Signal
- Supervisory Circuit
- QFN Package, 28-Pin 5 mm x 5 mm RHD

APPLICATIONS

- DTV
- DSL Modems
- Cable Modems
- Set Top Boxes
- Car DVD Players
- Home Gateway and Access Point Networks
- Wireless Routers

DESCRIPTION/ORDERING INFORMATION

The TPS65253 features two synchronous wide input range high efficiency buck converters. The converters are designed to simplify product application while giving designers the options to optimize their usage according to the target application.

The converters can operate in 5-, 9- and 12-V systems and have integrated power transistors. The output voltage can be set externally using a resistor divider to any value between 0.8 V and the input supply minus 1 V. Each converter features an enable pin that allows a delayed start-up for sequencing purposes, soft-start pin that allows adjustable soft-start time by choosing the soft-start capacitor, and a current limit (RLIMx) pin that enables designer to adjust current limit by selecting an external resistor and optimize the choice of inductor. The CMP pin allows optimizing transient versus dc accuracy response with a simple RC compensation.

The switching frequency of the converters is set by an external resistor connected to R_{OSC} pin. The switching regulators are designed to operate from 300 kHz to 1.2 MHz. The converters operate with 180° phase between then to minimize the input filter requirements.

TPS65253 also features a low power mode enabled by an external signal, which allows for a reduction on the input power supplied to the system when the host processor is in stand-by (low activity) mode.

TPS65253 features a supervisor circuit that monitors both converters and provides a PGOOD signal (End of Reset) with a 32-ms timer.

TPS65253 is packaged in a small, thermally efficient 28-pin QFN package.

ORDERING INFORMATION

<table>
<thead>
<tr>
<th>T_A</th>
<th>PACKAGE</th>
<th>PART NUMBER</th>
<th>TOP-SIDE MARKING</th>
</tr>
</thead>
<tbody>
<tr>
<td>-40°C to 85°C</td>
<td>28-Pin (QFN) - RHD</td>
<td>TPS65253RHD</td>
<td>TPS65253</td>
</tr>
</tbody>
</table>

(1) For the most current packaging and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.
(2) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.
This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

**FUNCTIONAL BLOCK DIAGRAM**
### TERMINAL FUNCTIONS

<table>
<thead>
<tr>
<th>NAME</th>
<th>NO.</th>
<th>I/O</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>OSC</td>
<td>1</td>
<td>I</td>
<td>Oscillator set. This resistor sets the frequency of the internal autonomous clock.</td>
</tr>
<tr>
<td>FB1</td>
<td>2</td>
<td>I</td>
<td>Feedback pin for Buck 1. Connect a divider set to 0.8 V from the output of the converter to ground.</td>
</tr>
<tr>
<td>CMP1</td>
<td>3</td>
<td>O</td>
<td>Compensation pin for Buck 1. Fit a series RC circuit to this pin to complete the compensation circuit of this converter.</td>
</tr>
<tr>
<td>SS1</td>
<td>4</td>
<td>I</td>
<td>Soft-start pin for Buck 1. Fit a small ceramic capacitor to this pin to set the converter soft-start time.</td>
</tr>
<tr>
<td>RLIM1</td>
<td>5</td>
<td>I</td>
<td>Current limit setting pin for Buck 1. Fit a resistor from this pin to ground to set the peak current limit on the output inductor.</td>
</tr>
<tr>
<td>EN1</td>
<td>6</td>
<td>I</td>
<td>Enable pin for Buck 1. A high signal on this pin enables the regulator Buck. For a delayed start-up add a small ceramic capacitor from this pin to ground.</td>
</tr>
<tr>
<td>BST1</td>
<td>7</td>
<td>I</td>
<td>Bootstrap capacitor for Buck 1. Fit a 47-nF ceramic capacitor from this pin to the switching node.</td>
</tr>
<tr>
<td>VIN1</td>
<td>8</td>
<td>I</td>
<td>Input supply for Buck 1. Fit a 10-µF ceramic capacitor close to this pin.</td>
</tr>
<tr>
<td>LX1</td>
<td>9, 10</td>
<td>O</td>
<td>Switching node for Buck 1</td>
</tr>
<tr>
<td>LX2</td>
<td>11, 12</td>
<td>O</td>
<td>Switching node for Buck 2</td>
</tr>
<tr>
<td>VIN2</td>
<td>13</td>
<td>I</td>
<td>Input supply for Buck 2. Fit a 10-µF ceramic capacitor close to this pin.</td>
</tr>
<tr>
<td>BST2</td>
<td>14</td>
<td>I</td>
<td>Bootstrap capacitor for Buck 1. Fit a 47-nF ceramic capacitor from this pin to the switching node.</td>
</tr>
<tr>
<td>EN2</td>
<td>15</td>
<td>I</td>
<td>Enable pin for Buck 2. A high signal on this pin enables the regulator Buck. For a delayed start-up add a small ceramic capacitor from this pin to ground.</td>
</tr>
<tr>
<td>RLIM2</td>
<td>16</td>
<td>I</td>
<td>Current limit setting pin for Buck 2. Fit a resistor from this pin to ground to set the peak current limit on the output inductor.</td>
</tr>
<tr>
<td>SS2</td>
<td>17</td>
<td>I</td>
<td>Soft-start pin for Buck 2. Fit a small ceramic capacitor to this pin to set the converter soft-start time.</td>
</tr>
<tr>
<td>CMP2</td>
<td>18</td>
<td>O</td>
<td>Compensation pin for Buck 2. Fit a series RC circuit to this pin to complete the compensation circuit of this converter.</td>
</tr>
<tr>
<td>FB2</td>
<td>19</td>
<td>I</td>
<td>Feedback pin for Buck 2. Connect a divider set to 0.8 V from the output of the converter to ground.</td>
</tr>
<tr>
<td>LOW_P</td>
<td>20</td>
<td>I</td>
<td>Low power operation mode (active high) input for TPS65253</td>
</tr>
<tr>
<td>V7V</td>
<td>21</td>
<td>O</td>
<td>Internal supply. Connect a 4.7-µF to 10-µF ceramic capacitor from this pin to ground.</td>
</tr>
<tr>
<td>V3V</td>
<td>22</td>
<td>O</td>
<td>Internal supply. Connect a 3.3-µF to 10-µF ceramic capacitor from this pin to ground.</td>
</tr>
<tr>
<td>GND</td>
<td>23, 25, 26, 27, 28</td>
<td>O</td>
<td>Ground</td>
</tr>
<tr>
<td>PGOOD</td>
<td>24</td>
<td>O</td>
<td>Open drain power good output</td>
</tr>
<tr>
<td>PowerPAD</td>
<td></td>
<td></td>
<td>PowerPAD. Connect to system ground for electrical and thermal connection.</td>
</tr>
</tbody>
</table>
ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)

| Voltage range at VIN1, VIN2, LX1, LX2 | –0.3 to 18 V |
| Voltage range at LX1, LX2 (maximum withstand voltage transient < 20 ns) | –3 to 18 V |
| Voltage at BST1, BST2, referenced to LX pin | –0.3 to 7 V |
| Voltage at V7V, CMP1, CMP2 | –0.3 to 7 V |
| Voltage at V3V, RLIM1, RLIM2, EN1, EN2, SS1, SS2, FB1, FB2, PGGOOD, ROSC, LOW_P | –0.3 to 3.6 V |
| Voltage at GND | –0.3 to 0.3 V |
| TJ | Operating virtual junction temperature range | –40 to 125 °C |
| TSTG | Storage temperature range | –55 to 150 °C |

(1) Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute–maximum–rated conditions for extended periods may affect device reliability.

(2) Excessive parasitic inductance may cause deeper negative voltage for less than 20 ns. To minimize this undershoot tight board layout is recommended.

RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range (unless otherwise noted)

<table>
<thead>
<tr>
<th>MIN</th>
<th>NOM</th>
<th>MAX</th>
</tr>
</thead>
<tbody>
<tr>
<td>VIN</td>
<td>Input operating voltage</td>
<td>4.5</td>
</tr>
<tr>
<td>TA</td>
<td>Junction temperature</td>
<td>–40</td>
</tr>
</tbody>
</table>

ELECTROSTATIC DISCHARGE (ESD) PROTECTION

<table>
<thead>
<tr>
<th>MIN</th>
<th>MAX</th>
</tr>
</thead>
<tbody>
<tr>
<td>Human body model (HBM)</td>
<td>2000 V</td>
</tr>
<tr>
<td>Charge device model (CDM)</td>
<td>500 V</td>
</tr>
</tbody>
</table>

PACKAGE DISSIPATION RATINGS

<table>
<thead>
<tr>
<th>PACKAGE</th>
<th>θJA (°C/W)</th>
<th>T_A = 25°C POWER RATING (W)</th>
<th>T_A = 55°C POWER RATING (W)</th>
</tr>
</thead>
<tbody>
<tr>
<td>RHD</td>
<td>34 (Simulated)</td>
<td>2.9</td>
<td>2</td>
</tr>
</tbody>
</table>

(1) Based on JEDEC 51.5 HIGH K environment measured on a 76.2 x 114 x 0.6-mm board with the following layer arrangement:
(a) Top layer: 2 Oz Cu, 6.7% coverage
(b) Layer 2: 1 Oz Cu, 90% coverage
(c) Layer 3: 1 Oz Cu, 90% coverage
(d) Bottom layer: 2 Oz Cu, 20% coverage

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### ELECTRICAL CHARACTERISTICS

\( T_A = -40°C \) to 85°C, \( V_{IN} = 12 \) V, \( L_O = 2.2 \ \mu\text{H} \), \( f_{SW} = 500 \) kHz (unless otherwise noted)

#### INPUT SUPPLY UVLO AND INTERNAL SUPPLY VOLTAGE

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>VIN</td>
<td>Input voltage range</td>
<td>4.5</td>
<td>16</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>IDD&lt;sub&gt;SDN&lt;/sub&gt;</td>
<td>Shutdown</td>
<td>0.4</td>
<td>mA</td>
<td></td>
<td></td>
</tr>
<tr>
<td>IDD&lt;sub&gt;Q&lt;/sub&gt;</td>
<td>Quiescent, low power disabled</td>
<td>40</td>
<td>mA</td>
<td></td>
<td></td>
</tr>
<tr>
<td>IDD&lt;sub&gt;Q_LOW_P&lt;/sub&gt;</td>
<td>Quiescent, low power enabled</td>
<td>0.6</td>
<td>mA</td>
<td></td>
<td></td>
</tr>
<tr>
<td>UVLO&lt;sub&gt;VIN&lt;/sub&gt;</td>
<td>( V_{IN} ) under voltage lockout</td>
<td>4.22</td>
<td>V</td>
<td></td>
<td></td>
</tr>
<tr>
<td>UVLO&lt;sub&gt;DEGLITCH&lt;/sub&gt;</td>
<td>Both edges</td>
<td>4.1</td>
<td>V</td>
<td></td>
<td></td>
</tr>
<tr>
<td>V3V</td>
<td>Internal supply output voltage</td>
<td>3.3</td>
<td>V</td>
<td></td>
<td></td>
</tr>
<tr>
<td>V7V</td>
<td>Internal supply output voltage</td>
<td>6.25</td>
<td>V</td>
<td></td>
<td></td>
</tr>
<tr>
<td>V7UVLO</td>
<td>UVLO for internal V7V rail</td>
<td>3.8</td>
<td>V</td>
<td></td>
<td></td>
</tr>
<tr>
<td>V7UVLO&lt;sub&gt;DEGLITCH&lt;/sub&gt;</td>
<td>Falling edge</td>
<td>3.6</td>
<td>V</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

#### BUCK CONVERTERS (ENABLE CIRCUIT, CURRENT LIMIT, SOFT-START, SWITCHING FREQUENCY AND LOW POWER MODE)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Cond.</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>( V_{IH.ENX} )</td>
<td>Enable threshold high</td>
<td>0.66xV&lt;sub&gt;3p3&lt;/sub&gt;</td>
<td>V</td>
<td></td>
<td></td>
</tr>
<tr>
<td>( V_{IL.ENX} )</td>
<td>Enable threshold Low</td>
<td>0.33xV&lt;sub&gt;3p3&lt;/sub&gt;</td>
<td>V</td>
<td></td>
<td></td>
</tr>
<tr>
<td>( I_{CH_EN} )</td>
<td>Pull up current enable pin</td>
<td>1.1</td>
<td>( \mu \text{A} )</td>
<td></td>
<td></td>
</tr>
<tr>
<td>( I_D )</td>
<td>Discharge time enable pins</td>
<td>10</td>
<td>ms</td>
<td></td>
<td></td>
</tr>
<tr>
<td>( I_{SS} )</td>
<td>Soft-start pin current source</td>
<td>5</td>
<td>( \mu \text{A} )</td>
<td></td>
<td></td>
</tr>
<tr>
<td>( f_{SW.BK} )</td>
<td>Converter switching frequency range</td>
<td>0.3</td>
<td>1.2</td>
<td>MHz</td>
<td></td>
</tr>
<tr>
<td>( R_{FSW} )</td>
<td>Frequency setting resistor</td>
<td>140</td>
<td>600</td>
<td>k( \Omega )</td>
<td></td>
</tr>
<tr>
<td>( f_{SW.TOL} )</td>
<td>Internal oscillator accuracy</td>
<td>-10</td>
<td>10</td>
<td>%</td>
<td></td>
</tr>
<tr>
<td>( V_{IH.LOW.P} )</td>
<td>Low power mode threshold high</td>
<td>0.66xV&lt;sub&gt;3p3&lt;/sub&gt;</td>
<td>V</td>
<td></td>
<td></td>
</tr>
<tr>
<td>( V_{IL.LOW.P} )</td>
<td>Low power mode threshold Low</td>
<td>0.33xV&lt;sub&gt;3p3&lt;/sub&gt;</td>
<td>V</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

#### FEEDBACK, REGULATION, OUTPUT STAGE

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Cond.</th>
<th>Min</th>
<th>TYP</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>( V_{FB} )</td>
<td>Feedback voltage</td>
<td>-1%</td>
<td>0.8</td>
<td>1%</td>
<td>V</td>
</tr>
<tr>
<td>( I_{ON_MIN} )</td>
<td>Minimum on time (current sense blanking)</td>
<td>100</td>
<td>135</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>( I_{LIMIT1} )</td>
<td>Peak inductor current limit range</td>
<td>-10%</td>
<td>5</td>
<td>10%</td>
<td>A</td>
</tr>
<tr>
<td>( I_{LIMIT2} )</td>
<td>Peak inductor current limit range</td>
<td>-15%</td>
<td>4.25</td>
<td>15%</td>
<td>A</td>
</tr>
</tbody>
</table>

#### MOSFET (BUCK 1)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Cond.</th>
<th>Min</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>H.S. Switch</td>
<td>On resistance of high side FET on CH1</td>
<td>25°C, BOOT = 6.5 V</td>
<td>90</td>
</tr>
<tr>
<td>L.S. Switch</td>
<td>On resistance of low side FET on CH1</td>
<td>25°C, VIN = 12 V</td>
<td>45</td>
</tr>
</tbody>
</table>
## ELECTRICAL CHARACTERISTICS (continued)

$T_A = -40^\circ C$ to $85^\circ C$, $V_IN = 12 \, V$, $L_O = 2.2 \, \mu H$, $f_{SW} = 500 \, kHz$ (unless otherwise noted)

### MOSFET (BUCK 2)

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>H.S. Switch</td>
<td>On resistance of high side FET on CH2</td>
<td>25°C, BOOT = 6.5 V</td>
<td>115</td>
<td>mΩ</td>
<td></td>
</tr>
<tr>
<td>L.S. Switch</td>
<td>On resistance of low side FET on CH2</td>
<td>25°C, $V_IN = 12 , V$</td>
<td>75</td>
<td>mΩ</td>
<td></td>
</tr>
</tbody>
</table>

### ERROR AMPLIFIER

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>Error amplifier</td>
<td>transconductance</td>
<td>$-2 , \mu A &lt; I_{COPM} &lt; 2 , \mu A$</td>
<td>130</td>
<td>μΩ</td>
<td></td>
</tr>
<tr>
<td>CMP to $I_LX , gm$</td>
<td>$I_LX = 0.5 , A$</td>
<td>12</td>
<td>A/V</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

### POWER GOOD RESET GENERATOR

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{UV _BUCKX}$</td>
<td>Threshold voltage for buck under voltage</td>
<td>Output falling</td>
<td>85</td>
<td>%</td>
<td></td>
</tr>
<tr>
<td>$t_{UV _deglitch}$</td>
<td>Deglitch time (both edges)</td>
<td>11</td>
<td>ms</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$t_{ON _HICCUP}$</td>
<td>Hiccup mode ON time</td>
<td>$V_{UV _BUCKX}$ asserted</td>
<td>12</td>
<td>ms</td>
<td></td>
</tr>
<tr>
<td>$t_{OFF _HICCUP}$</td>
<td>Hiccup mode OFF time</td>
<td>All converters disabled. Once $t_{OFF _HICCUP}$ elapses, all converters will go through sequencing again.</td>
<td>20</td>
<td>ms</td>
<td></td>
</tr>
<tr>
<td>$V_{OV _BUCKX}$</td>
<td>Threshold voltage for buck over voltage</td>
<td>Output rising (high side FET will be forced off). Output failing (high side FET will be allowed to switch )</td>
<td>109</td>
<td>%</td>
<td></td>
</tr>
<tr>
<td>$t_{RP}$</td>
<td>minimum reset period</td>
<td>Measured after the later of Buck 1 or Buck 2 power-up successfully</td>
<td>32</td>
<td>ms</td>
<td></td>
</tr>
</tbody>
</table>

### THERMAL SHUTDOWN

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>$T_{TRIP}$</td>
<td>Thermal shut down trip point</td>
<td>Rising temperature</td>
<td>160</td>
<td>°C</td>
<td></td>
</tr>
<tr>
<td>$T_{HYST}$</td>
<td>Thermal shut down hysteresis</td>
<td>Device re-starts</td>
<td>20</td>
<td>°C</td>
<td></td>
</tr>
<tr>
<td>$T_{TRIP _DEGLITCH}$</td>
<td>Thermal shut down deglitch</td>
<td>100</td>
<td>μs</td>
<td>120</td>
<td>μs</td>
</tr>
</tbody>
</table>

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TYPICAL CHARACTERISTICS

$V_{IN} = 12\, V$, $f_{SW} = 500\, kHz$, $L_{O} = 2.2\, \mu H$, $DCR = 15\, m\Omega$, $C_{O} = 44\, \mu F$ (unless otherwise specified)

**Buck 1 Efficiency vs $V_{OUT}$**

![Figure 1. Buck 1 Efficiency vs $V_{OUT}$](image)

**Buck 2 Efficiency vs $V_{OUT}$**

![Figure 2. Buck 2 Efficiency vs $V_{OUT}$](image)

**Buck 1 (1.8 V) Efficiency vs $V_{IN}$**

![Figure 3. Buck 1 (1.8 V) Efficiency vs $V_{IN}$](image)

**Buck 2 (3.3 V) Efficiency vs $V_{IN}$**

![Figure 4. Buck 2 (3.3 V) Efficiency vs $V_{IN}$](image)

**Buck 1 Load Regulation vs $V_{OUT}$**

![Figure 5. Buck 1 Load Regulation vs $V_{OUT}$](image)

**Buck 2 Load Regulation vs $V_{OUT}$**

![Figure 6. Buck 2 Load Regulation vs $V_{OUT}$](image)
Typical Characteristics (continued)

\[ V_{IN} = 12 \, \text{V}, \quad f_{SW} = 500 \, \text{kHz}, \quad L_O = 2.2 \, \mu\text{H}, \quad DCR = 15 \, \text{m\Omega}, \quad C_O = 44 \, \mu\text{F} \] (unless otherwise specified)

**Buck 1 Output Ripple**

\[ \text{Ripple (Vpp)} \]

- 0.01
- 0.02
- 0.03
- 0.04

Output Current (A)

0 1 2 3 4

**Figure 7.**

**Buck 2 Output Ripple**

\[ \text{Ripple (Vpp)} \]

- 0.01
- 0.02
- 0.03
- 0.04

Output Current (A)

0 1 2 3

**Figure 8.**

**Output Voltage (1.2 V)**

\[ V_{OUT} \]

\[ V_{OUT} \]

- 1.225
- 1.2
- 1.175

Output Current (A)

0 1 2 3 4

**Figure 9.**

**Output Voltage (1.8 V)**

\[ V_{OUT} \]

\[ V_{OUT} \]

- 1.82
- 1.8
- 1.78

Output Current (A)

0 1 2 3 4

**Figure 10.**

**Output Voltage (3.3 V)**

\[ V_{OUT} \]

\[ V_{OUT} \]

- 3.4
- 3.35
- 3.3

Output Current (A)

0 1 2 3 4

**Figure 11.**

**Output Voltage (5 V)**

\[ V_{OUT} \]

\[ V_{OUT} \]

- 5.1
- 5.05
- 4.95

Output Current (A)

0 1 2 3 4

**Figure 12.**
TYPICAL CHARACTERISTICS (continued)

\[ V_{\text{IN}} = 12 \text{ V}, f_{\text{SW}} = 500 \text{ kHz}, L_{\text{O}} = 2.2 \ \mu\text{H}, \text{DCR} = 15 \ \text{m}\Omega, C_{\text{O}} = 44 \ \mu\text{F} \] (unless otherwise specified)

Details on Soft-Start, 1 ms/div

Figure 13.

Buck 1 (1.2 V) Ripple at Output Load of 4 A, 20 mV/div

Figure 14.

Buck 2 (3.3 V) Ripple at Output Load of 3 A, 20 mV/div

Figure 15.

Buck 1 Transient Load Response (1-A to 3-A Step), 30 mV/div

Figure 16.

Buck 2 Transient Load Response (0.75-A to 2.25-A Step), 30 mV/div

Figure 17.

Ripple With LOW_P = 1, Each Buck is Loaded With 10 mA, 100 mV/div

Figure 18.
OVERVIEW

TPS65253 is a power management IC with two step-down buck converters. Both high-side and low-side MOSFETs are integrated to provide fully synchronous conversion with higher efficiency. TPS65253 can support 4.5-V to 16-V input supply, high load current, 300-kHz to 1.2-MHz clocking. The buck converters have an optional PFM mode, which can improve power dissipation at light loads. Alternatively, the device implements a constant frequency mode by connecting the LOW_P pin to ground. The wide switching frequency of 300 kHz to 1.2 MHz allows for efficiency and size optimization. The switching frequency is adjustable by selecting a resistor to ground on the ROSC pin. Input ripple is reduced by 180° out-of-phase operation between Buck 1 and Buck 2.

Both buck converters have peak current mode control which simplifies external frequency compensation. A traditional type II compensation network can stabilize the system and achieve fast transient response. Moreover, an optional capacitor in parallel with the upper resistor of the feedback divider provides one more zero and makes the crossover frequency over 100 kHz.

Each buck converter has an individual current limit, which can be set up by a resistor to ground from the RLIMx pin. The adjustable current limiting enables high efficiency design with smaller and less expensive inductors.

The device has two built-in LDO regulators. During a standby mode, the 3.3-V LDO and the 6.5-V LDO can be used to drive MCU and other active loads. By this, the system is able to turn of the two buck converters and improve the standby efficiency.

The device has a power good comparator monitoring the output voltage. Each converter has its own soft-start and enable pin, which provide independent control and programmable soft-start.

DETAILED DESCRIPTION

Adjustable Switching Frequency

To select the internal switching frequency, connect a resistor from ROSC to ground. Figure 19 shows the required resistance for a given switching frequency.

![Figure 19. ROSC vs Switching Frequency](image)

\[
R_{\text{OS}} (k\Omega) = 174 \cdot f_{\text{SW}}^{-1.122}
\]  

(1)
Out-of-Phase Operation
In order to reduce input ripple current, Buck 1 and Buck 2 operate 180° out-of-phase. This enables the system having less input ripple, then to lower component cost, save board space and reduce EMI.

Startup and Sequencing
If a delayed start-up is required on any of the buck converters fit a ceramic capacitor to the ENx pins. The delay added is ~1.7 ms per nF connected to the pin. Note that the EN pins have a weak 1-MΩ pull-up to the 3V3 rail. Figure 20 describes startup sequencing and PGOOD generation.

Soft-Start Time
The device has an internal pull-up current source of 5 µA that charges an external soft-start capacitor to implement a slow start time. Equation 2 shows how to select a soft-start capacitor based on an expected slow start time. The voltage reference (VREF) is 0.8 V and the soft-start charge current (Iss) is 5 µA. The soft-start circuit requires 1 nF per around 160 µs to be connected at the SS pin. A 0.8-ms soft-start time is implemented for all converters fitting 4.7 nF to the relevant SS pin.

\[ T_{ss}(ms) = V_{REF}(V) \cdot \left( \frac{C_{ss}(nF)}{I_{ss}(\mu A)} \right) \]  

(2)

The Power Good circuit for the bucks has a 10-ms watchdog. Therefore the soft-start time should be lower than this value. It is recommended not to exceed 5 ms.
Adjusting the Output Voltage

The output voltage is set with a resistor divider from the output node to the FB pin. It is recommended to use 1% tolerance or better divider resistors. In order to improve efficiency at light load, start with a value close to 40 kΩ for the R1 resistor and use Equation 3 to calculate R2.

\[ R_2 = R_1 \cdot \left( \frac{0.8V}{V_o - 0.8V} \right) \]

(3)

Figure 21. Voltage Divider Circuit
Loop Compensation

TPS65253 is a current mode control DC/DC converter. The error amplifier is a transconductance of 130 $\mu$A/V. A typical compensation circuit could be type II ($R_c$ and $C_c$) to have a phase margin above 45°, or type III ($R_c$ and $C_c$ and $C_{ff}$) to improve the converter transient response. Optional $C_{Roll}$ adds a high frequency pole to attenuate high-frequency noise when needed. It may also prevent noise coupling from other rails if there is possibility of cross coupling in between rails when layout is very compact.

![Figure 22. Loop Compensation Scheme](image)

To calculate the external compensation components follow the following steps:

<table>
<thead>
<tr>
<th>Select switching frequency that is appropriate for application depending on L, C sizes, output ripple, EMI concerns and etc. Switching frequencies around 500 kHz yield best trade off between performance and cost. When using smaller L and C, switching frequency can be increased. To optimize efficiency, switching frequency can be lowered.</th>
<th>TYPE II CIRCUIT</th>
<th>TYPE III CIRCUIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>Select cross over frequency ($f_c$) to be at least 1/5 to 1/10 of switching frequency ($f_s$).</td>
<td>$f_c = f_s/10$</td>
<td>Use type III circuit for switching frequencies higher than 500 kHz.</td>
</tr>
<tr>
<td>Set and calculate $R_c$.</td>
<td>$R_c = \frac{2\pi \cdot f_c \cdot Vo \cdot Co}{g_M \cdot Vref \cdot gm_{ps}}$</td>
<td>$R_c = \frac{2\pi \cdot f_c \cdot Vo \cdot Co}{g_M \cdot Vref \cdot gm_{ps}}$</td>
</tr>
<tr>
<td>Calculate $C_c$ by placing a compensation zero at or before the converter dominant pole</td>
<td>$C_c = \frac{R_L \cdot Co}{R_c}$</td>
<td>$C_c = \frac{R_L \cdot Co}{R_c}$</td>
</tr>
<tr>
<td>Add $C_{Roll}$ if needed to remove large signal coupling to high impedance CMP node. Make sure that $fp_{Roll} = \frac{1}{2 \cdot \pi \cdot R_c \cdot C_{Roll}}$ is at least twice the cross over frequency.</td>
<td>$C_{Roll} = \frac{Resr \cdot Co}{R_c}$</td>
<td>$C_{Roll} = \frac{Resr \cdot Co}{R_c}$</td>
</tr>
<tr>
<td>Calculate $C_{ff}$ compensation zero at low frequency to boost the phase margin at the crossover frequency. Make sure that the zero frequency ($f_{zff}$) is smaller than equivalent soft-start frequency ($1/T_{ss}$).</td>
<td>NA</td>
<td>$C_{ff} = \frac{1}{2 \cdot \pi \cdot f_{zff} \cdot R_i}$</td>
</tr>
</tbody>
</table>
Slope Compensation
The device has a built-in slope compensation ramp. The slope compensation can prevent sub harmonic oscillations in peak current mode control.

Input Capacitor
Use at least 10-μF X7R/X5R ceramic capacitors at the input of the converter inputs. These capacitors should be connected as close as physically possible to the input pins of the converters.

Bootstrap Capacitor
The device has two integrated boot regulators and requires a small ceramic capacitor between the BST and LX pins to provide the gate drive voltage for the high side MOSFET. The value of the ceramic capacitor should be 0.047 μF. A ceramic capacitor with an X7R or X5R grade dielectric is recommended because of the stable characteristics over temperature and voltage.

Power Good
The PGOOD pin is an open drain output. The PGOOD pin is pulled low when any buck converter is pulled below 85% of the nominal output voltage. The PGOOD is pulled up when both buck converters' outputs are more than 90% of its nominal output voltage.

The default reset time is 32 ms. The polarity of the PGOOD is active high.

Current Limit Protection
The TPS65253 current limit trip is set by the following formula for Buck 1:

\[ I_{\text{lim1}}(A) = \frac{252}{R_{\text{lim1}}(k\Omega)} + 0.6 \]  

and for Buck 2:

\[ I_{\text{lim2}}(A) = \frac{236}{R_{\text{lim2}}(k\Omega)} + 0.56 \]  

All converters operate in hiccup mode: Once an over-current lasting more than 12 ms is sensed in any of the converters, they will shut down for 20 ms and then the start-up sequencing will be tried again. If the overload has been removed, the converter will ramp up and operate normally. If this is not the case the converter will see another over-current event and shuts-down again repeating the cycle (hiccup) until the failure is cleared.

If an overload condition lasts for less than 12 ms, only the relevant converter affected will shut-down and re-start and no global hiccup mode will occur.

Overvoltage Transient Protection
The device incorporates an overvoltage transient protection (OVP) circuit to minimize voltage overshoot. The OVP feature minimizes the output overshoot by implementing a circuit to compare the FB pin voltage to OVTP threshold which is 109% of the internal voltage reference. If the FB pin voltage is greater than the OVTP threshold, the high side MOSFET is disabled preventing current from flowing to the output and minimizing output overshoot. When the FB voltage drops lower than the OVTP threshold which is 107%, the high side MOSFET is allowed to turn on the next clock cycle.

Low Power Mode Operation
By pulling high the Low_P pin all converters will operate in pulse-skipping mode, greatly reducing the overall power consumption at light and no load conditions. Although each buck converter has a skip comparator that makes sure regulation is not lost when a heavy load is applied and low power mode is enabled, system design needs to make sure that the LP pin is pulled low for continuous loading in excess of 100 mA.
When low power is implemented, the peak inductor current used to charge the output capacitor is:

\[
I_{LMPT} = 0.25 \cdot T_{SLEEP_CLK} \cdot \frac{V_{IN} - V_{OUT}}{L}
\]

(6)

Where \(T_{SLEEP_CLK}\) is half of the converter switching period, \(2/f_{SW}\).

The size of the additional ripple added to the output is:

\[
\Delta V_{OUT} = \frac{1}{C} \cdot \left(\frac{L \cdot I_{LMPT}^2}{2} \cdot \frac{V_{IN}}{V_{OUT} \cdot (V_{IN} - V_{OUT})} - \frac{I_{LOAD}}{f_{SLEEP_CLK}}\right)
\]

(7)

And the peak output voltage during low power operation is (see Figure 23):

\[
V_{OUT,PK} = V_{OUT} + \frac{\Delta V_{OUT}}{2}
\]

(8)

**Figure 23. Peak Output Voltage During Low Power Operation**

**Thermal Shutdown**

The device implements an internal thermal shutdown to protect itself if the junction temperature exceeds 160°C. The thermal shutdown forces the device to stop switching when the junction temperature exceeds thermal trip threshold. Once the die temperature decreases below 140°C, the device reinitiates the power up sequence. The thermal shutdown hysteresis is 20°C.

**3.3-V and 6.5 LDO Regulators**

The following ceramic capacitor (X7R/X5R) should be connected as close as possible to the described pins:

- 4.7 µF to 10 µF for V7V pin 21
- 3.3 µF or larger for V3V pin 229

**Layout Recommendation**

Layout is a critical portion of PMIC designs.

- Place tracing for output voltage and LX on the top layer and an inner power plane for VIN.
- For best thermal performance, pins 25, 26, 27, and 28 should be connected to GND on the top PCB layer as well as inner GND plane by through-hole connections.
- The top layer ground area should be connected to the internal ground layer(s) using vias at the input bypass capacitor, the output filter capacitor and directly under the TPS65253 device to provide a thermal path from the PowerPad land to ground.
- For operation at full rated load, the top side ground area together with the internal ground plane, must provide adequate heat dissipating area.
- There are several signals paths that conduct fast changing currents or voltages that can interact with stray inductance or parasitic capacitance to generate noise or degrade the power supplies performance. To help eliminate these problems, the VIN pin should be bypassed to ground with a low ESR ceramic bypass capacitor with X5R or X7R dielectric. Care should be taken to minimize the loop area formed by the bypass capacitor connections, the VIN pins, and the ground connections. Since the LX connection is the switching node, the output inductor should be located close to the LX pins, and the area of the PCB conductor minimized to prevent excessive capacitive coupling.
- The output filter capacitor ground should use the same power ground trace as the VIN input bypass capacitor. Try to minimize this conductor length while maintaining adequate width.
- The compensation should be as close as possible to the CMPx pins. The CMPx and ROSC pins are sensitive to noise so the components associated to these pins should be located as close as possible to the IC and routed with minimal lengths of trace.
## PACKAGING INFORMATION

<table>
<thead>
<tr>
<th>Orderable Device</th>
<th>Status</th>
<th>Package Type</th>
<th>Package Drawing</th>
<th>Pins</th>
<th>Package Qty</th>
<th>Eco Plan</th>
<th>Lead/Ball Finish</th>
<th>MSL Peak Temp</th>
<th>Op Temp (°C)</th>
<th>Device Marking</th>
<th>Samples</th>
</tr>
</thead>
<tbody>
<tr>
<td>TPS65253RHDR</td>
<td>ACTIVE</td>
<td>VQFN</td>
<td>RHD</td>
<td>28</td>
<td>3000</td>
<td>Green (RoHS &amp; no Sb/Br)</td>
<td>CU NIPDAU</td>
<td>Level-3-260C-168 HR</td>
<td>-40 to 85</td>
<td>TPS 65253</td>
<td></td>
</tr>
<tr>
<td>TPS65253RHDT</td>
<td>ACTIVE</td>
<td>VQFN</td>
<td>RHD</td>
<td>28</td>
<td>250</td>
<td>Green (RoHS &amp; no Sb/Br)</td>
<td>CU NIPDAU</td>
<td>Level-3-260C-168 HR</td>
<td>-40 to 85</td>
<td>TPS 65253</td>
<td></td>
</tr>
</tbody>
</table>

(1) The marketing status values are defined as follows:
- **ACTIVE:** Product device recommended for new designs.
- **LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
- **NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
- **PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
- **OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check [http://www.ti.com/productcontent](http://www.ti.com/productcontent) for the latest availability information and additional product content details.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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**TAPE AND REEL INFORMATION**

### REEL DIMENSIONS

![Reel Dimensions Diagram](image)

### TAPE DIMENSIONS

<table>
<thead>
<tr>
<th>Dimension</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>A0</td>
<td>Dimension designed to accommodate the component width</td>
</tr>
<tr>
<td>B0</td>
<td>Dimension designed to accommodate the component length</td>
</tr>
<tr>
<td>K0</td>
<td>Dimension designed to accommodate the component thickness</td>
</tr>
<tr>
<td>W</td>
<td>Overall width of the carrier tape</td>
</tr>
<tr>
<td>P1</td>
<td>Pitch between successive cavity centers</td>
</tr>
</tbody>
</table>

### PACKAGING INFORMATION

- **Device**: TPS65253RHDR
  - **Package**: VQFN
  - **Package Drawing**: RHD
  - **Pins**: 28
  - **SPQ**: 3000
  - **Reel Diameter (mm)**: 330.0
  - **Reel Width W1 (mm)**: 12.4
  - **A0 (mm)**: 5.3
  - **B0 (mm)**: 5.3
  - **K0 (mm)**: 1.1
  - **P1 (mm)**: 8.0
  - **W (mm)**: 12.0
  - **Pin1 Quadrant**: Q2

- **Device**: TPS65253RHDT
  - **Package**: VQFN
  - **Package Drawing**: RHD
  - **Pins**: 28
  - **SPQ**: 250
  - **Reel Diameter (mm)**: 180.0
  - **Reel Width W1 (mm)**: 12.4
  - **A0 (mm)**: 5.3
  - **B0 (mm)**: 5.3
  - **K0 (mm)**: 1.1
  - **P1 (mm)**: 8.0
  - **W (mm)**: 12.0
  - **Pin1 Quadrant**: Q2

*All dimensions are nominal.*
## TAPE AND REEL BOX DIMENSIONS

<table>
<thead>
<tr>
<th>Device</th>
<th>Package Type</th>
<th>Package Drawing</th>
<th>Pins</th>
<th>SPQ</th>
<th>Length (mm)</th>
<th>Width (mm)</th>
<th>Height (mm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>TPS65253RHDR</td>
<td>VQFN</td>
<td>RHD</td>
<td>28</td>
<td>3000</td>
<td>367.0</td>
<td>367.0</td>
<td>35.0</td>
</tr>
<tr>
<td>TPS65253RHDT</td>
<td>VQFN</td>
<td>RHD</td>
<td>28</td>
<td>250</td>
<td>210.0</td>
<td>185.0</td>
<td>35.0</td>
</tr>
</tbody>
</table>

*All dimensions are nominal*
Images above are just a representation of the package family, actual package may vary. Refer to the product data sheet for package details.
NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. QFN (Quad Flatpack No-Lead) Package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Falls within JEDEC MO-220.
THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.

NOTE: All linear dimensions are in millimeters
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com.<http://www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for vias placed in thermal pad.
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