DUAL-OUTPUT LOW-DROPOUT VOLTAGE REGULATORS
WITH POWER UP SEQUENCING FOR SPLIT VOLTAGE DSP SYSTEMS

FEATURES

- Dual Output Voltages for Split-Supply Applications
- Selectable Power Up Sequencing for DSP Applications
- –55°C to 125°C Operating Temperature
- Output Current Range of 1 A on Regulator 1 and 2 A on Regulator 2
- Fast Transient Response
- Voltage Options Are 3.3 V/2.5 V
- Open Drain Power-On Reset With 120-ms Delay
- Open Drain Power Good for Regulator 1
- Ultralow 185-µA (typical) Quiescent Current
- 2-µA Input Current During Standby
- Low Noise: 78-µVRMS Without Bypass Capacitor
- Quick Output Capacitor Discharge Feature
- Two Manual Reset Inputs
- 2% Accuracy Over Load and Temperature
- Undervoltage Lockout (UVLO) Feature
- 20-Pin Ceramic Flatpack Package
- Thermal Shutdown Protection

DESCRIPTION

The TPS70358 is designed to provide a complete power management solution for TI DSP, processor power, ASIC, FPGA, and digital applications where dual output voltage regulators are required. Easy programmability of the sequencing function makes this family ideal for any TI DSP applications with power sequencing requirement. Differentiated features, such as accuracy, fast transient response, SVS supervisory circuit (power on reset), manual reset inputs, and enable function, provide a complete system solution.

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DESCRIPTION (CONTINUED)

The TPS70358 regulator offers very low dropout voltage and dual outputs with power up sequence control, which is designed primarily for DSP applications. These devices have low noise output performance without using any added filter bypass capacitors and are designed to have a fast transient response and be stable with 47-µF low ESR capacitors.

The TPS70358 has a fixed 3.3-V/2.5-V voltage option. Regulator 1 can support up to 1 A, and regulator 2 can support up to 2 A. Separate voltage inputs allow the designer to configure the source power.

Because the PMOS pass element behaves as a low-value resistor, the dropout voltage is very low (typically 160 mV on regulator 1) and is directly proportional to the output current. Additionally, since the PMOS pass element is a voltage-driven device, the quiescent current is very low and independent of output loading (maximum of 250 µA over the full range of output current). This LDO family also features a sleep mode; applying a high signal to EN (enable) shuts down both regulators, reducing the input current to 1 µA at $T_J = 25^\circ$C.

The device is enabled when the EN pin is connected to a low-level input voltage. The output voltages of the two regulators are sensed at the $V_{\text{SENSE}1}$ and $V_{\text{SENSE}2}$ pins respectively.

The input signal at the SEQ pin controls the power-up sequence of the two regulators. When the device is enabled and the SEQ terminal is pulled up or left open, $V_{\text{OUT}2}$ turns on first and $V_{\text{OUT}1}$ remains off until $V_{\text{OUT}2}$ reaches approximately 83% of its regulated output voltage. At that time $V_{\text{OUT}1}$ is turned on. If $V_{\text{OUT}2}$ is pulled below 83% (i.e. overload condition) of its regulated voltage, $V_{\text{OUT}1}$ will be turned off. Pulling the SEQ terminal low reverses the power-up order and $V_{\text{OUT}1}$ is turned on first. The SEQ pin is connected to an internal pullup current source.

For each regulator, there is an internal discharge transistor to discharge the output capacitor when the regulator is turned off (disabled).

The PG1 pin reports the voltage conditions at $V_{\text{OUT}1}$. The PG1 pin can be used to implement a SVS (power on reset) for the circuitry supplied by regulator 1.

The TPS70358 features a RESET (SVS, POR, or power on reset). RESET is an active low, open drain output and requires a pullup resistor for normal operation. When pulled up, the PG1 goes to a high impedance state (i.e. logic high) after a 120-ms delay when all three of the following conditions are met. First, $V_{\text{IN}1}$ must be above the undervoltage condition. Second, the manual reset (MR) pin must be in a high impedance state. Third, $V_{\text{OUT}2}$ must be above approximately 95% of its regulated voltage. To monitor $V_{\text{OUT}1}$, the PG1 output pin can be connected to MR1 or MR2. RESET can be used to drive power on reset or a low-battery indicator. If RESET is not used, it can be left floating.

Internal bias voltages are powered by $V_{\text{IN}1}$ and require 2.7 V for full functionality. Each regulator input has an undervoltage lockout circuit that prevents each output from turning on until the respective input reaches 2.5 V.
TPS70358M

ORDERING INFORMATION

<table>
<thead>
<tr>
<th>PRODUCT</th>
<th>VOLTAGE (V)</th>
<th>PACKAGE-LEAD (DESIGNATOR)</th>
<th>T J</th>
<th>ORDERABLE PART NUMBER</th>
<th>TOP-SIDE MARKING</th>
</tr>
</thead>
<tbody>
<tr>
<td>TPS70358M</td>
<td>3.3 V</td>
<td>2.5 V</td>
<td>DFP-20 (HKH)</td>
<td>–55°C to 125°C</td>
<td>TPS70358MHKH</td>
</tr>
</tbody>
</table>

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.

DETAILED BLOCK DIAGRAM - FIXED VOLTAGE VERSION

NOTES: A. For most applications, V\text{IN1} and V\text{IN2} should be externally connected to V\text{OUT} as close as possible to the device. For other implementations, refer to SENSE terminal connection discussion in the Application Information section.

B. If the SEQ terminal is floating at the input, V\text{OUT} powers up first.
NOTES:

A. $V_{IN}$ is the minimum input voltage for a valid PG. The symbol $V_{IN}$ is not currently listed within EIA or JEDEC standards for semiconductor symbology.

B. $V_T$ - Trip voltage is typically 5% lower than the output voltage ($95\%V_o$) to $V_{OUT}$ is the hysteresis.

**Figure 1.** RESET Timing Diagram (With $V_{IN1}$ Powered Up and MR1 and MR2 at Logic High)

NOTES:

A. $V_{IN}$ is the minimum input voltage for a valid PG. The symbol $V_{IN}$ is not currently listed within EIA or JEDEC standards for semiconductor symbology.

B. $V_T$ - Trip voltage is typically 5% lower than the output voltage ($95\%V_o$) to $V_{OUT}$ is the hysteresis.

**Figure 2.** PG1 Timing Diagram
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2. Features
3. Pin Description
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5. Electrical Characteristics
6. Thermal Characteristics
7. Package Characteristics
8. Ordering Information
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SECTION 1: INTRODUCTION

The TPS703xx series of low dropout regulators are designed for use in applications requiring a high performance power management solution. These devices provide fast transient response and high accuracy, while drawing low quiescent current. Programmable sequencing provides a power solution for DSPs without any external component requirements. This reduces the component cost and board space while increasing total system reliability. TPS703xx family has an enable feature which puts the device in sleep mode reducing the input current to 1 μA. Other features are the integrated SVS (power on reset, RESET) and power good (PG1). These monitor output voltages and provide logic output to the system. These differentiated features provide a complete DSP power solution.

SECTION 2: FEATURES

- Low dropout regulator
- High performance power management solution
- Fast transient response and high accuracy
- Low quiescent current
- Programmable sequencing
- Integrated SVS (power on reset, RESET)
- Power good (PG1)
- Monitoring of output voltages
- Logic output to the system

SECTION 3: PIN DESCRIPTION

The following table provides a detailed description of each pin:

<table>
<thead>
<tr>
<th>TERMINAL</th>
<th>I/O</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>EN</td>
<td>I</td>
<td>Active low enable</td>
</tr>
<tr>
<td>GND</td>
<td></td>
<td>Regulator ground</td>
</tr>
<tr>
<td>MR1</td>
<td>I</td>
<td>Manual reset input 1, active low, pulled up internally</td>
</tr>
<tr>
<td>MR2</td>
<td>I</td>
<td>Manual reset input 2, active low, pulled up internally</td>
</tr>
<tr>
<td>NC</td>
<td></td>
<td>No connection</td>
</tr>
<tr>
<td>PG1</td>
<td>O</td>
<td>Open drain output, low when VOUT1 voltage is less than 95% of the nominal regulated voltage</td>
</tr>
<tr>
<td>RESET</td>
<td>O</td>
<td>Open drain output, SVS (power on reset) signal, active low</td>
</tr>
<tr>
<td>SEQ</td>
<td>I</td>
<td>Power up sequence control: SEQ=High, VOUT2 powers up first; SEQ=Low, VOUT1 powers up first, SEQ terminal pulled up internally</td>
</tr>
<tr>
<td>VIN1</td>
<td>I</td>
<td>Input voltage of regulator 1</td>
</tr>
<tr>
<td>VIN2</td>
<td>I</td>
<td>Input voltage of regulator 2</td>
</tr>
<tr>
<td>VOUT1</td>
<td>O</td>
<td>Output voltage of regulator 1</td>
</tr>
<tr>
<td>VOUT2</td>
<td>O</td>
<td>Output voltage of regulator 2</td>
</tr>
<tr>
<td>VSENSE2</td>
<td>I</td>
<td>Regulator 2 output voltage sense</td>
</tr>
<tr>
<td>VSENSE1</td>
<td>I</td>
<td>Regulator 1 output voltage sense</td>
</tr>
</tbody>
</table>

SECTION 4: APPLICATIONS

The TPS703xx series is ideal for use in battery-powered applications where minimizing power consumption is critical. This includes, but is not limited to, portable electronic devices, medical equipment, and industrial control systems.

SECTION 5: ELECTRICAL CHARACTERISTICS

- Input voltage range: 2.5 V to 5.5 V
- Output voltage range: 0.8 V to 5.5 V
- Dropout voltage: 75 mV (max)
- Quiescent current: 1 μA (max)
- Load regulation: ±2% (max)

SECTION 6: THERMAL CHARACTERISTICS

- Max ambient temperature: 125°C
- Max junction temperature: 150°C
- Thermal resistance: 63°C/W (Typ.)

SECTION 7: PACKAGE CHARACTERISTICS

The TPS703xx series is available in a 16-pin TSSOP package.

SECTION 8: ORDERING INFORMATION

TPS703xx [Voltage] [Output Current] [Series]

Example: TPS70358 [580 mA] [Series]

SECTION 9: REVISION HISTORY

- [Version]
- [Date]
- [Changes]

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Power Good (PG1)
The PG1 terminal is an open drain, active high output terminal which indicates the status of the \( V_{\text{OUT1}} \) regulator. When the \( V_{\text{OUT1}} \) reaches 95% of its regulated voltage, PG1 goes to a high impedance state. PG1 goes to a low impedance state when \( V_{\text{OUT1}} \) is pulled below 95% (i.e., over load condition) of its regulated voltage. The open drain output of the PG1 terminal requires a pullup resistor.

Manual Reset Pins (MR1 and MR2)
MR1 and MR2 are active low input terminals used to trigger a reset condition. When either MR1 or MR2 is pulled to logic low, a POR (RESET) occurs. These terminals have a 6-\( \mu \)A pullup current to \( V_{\text{IN1}} \). It is recommended that these pins be pulled high to \( V_{\text{IN}} \) when they are not used.

Sense (\( V_{\text{SENSE1}} \), \( V_{\text{SENSE2}} \))
The sense terminals of fixed-output options must be connected to the regulator output, and the connection should be as short as possible. Internally, the sense terminals connect to high-impedance wide-bandwidth amplifiers through resistor-divider networks and noise pickup feeds through to the regulator output. It is essential to route the sense connections in such a way to minimize/avoid noise pickup. Adding RC networks between the \( V_{\text{SENSE}} \) terminals and \( V_{\text{OUT}} \) terminals to filter noise is not recommended because it can cause the regulators to oscillate.

RESET Indicator
RESET is an active low, open drain output and requires a pullup resistor for normal operation. When pulled up, RESET goes to a high impedance state (i.e. logic high) after a 120-ms delay when all three of the following conditions are met. First, \( V_{\text{IN1}} \) must be above the undervoltage condition. Second, the manual reset (MR) pin must be in a high impedance state. Third, \( V_{\text{OUT2}} \) must be above approximately 95% of its regulated voltage. To monitor \( V_{\text{OUT1}} \), the PG1 output pin can be connected to MR1 or MR2.

\( V_{\text{IN1}} \) and \( V_{\text{IN2}} \)
\( V_{\text{IN1}} \) and \( V_{\text{IN2}} \) are inputs to the regulators.

\( V_{\text{OUT1}} \) and \( V_{\text{OUT2}} \)
\( V_{\text{OUT1}} \) and \( V_{\text{OUT2}} \) are output terminals of each regulator.
## ABSOLUTE MAXIMUM RATINGS\(^{(1)}\)

*over operating free-air temperature range (unless otherwise noted)*

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>(V_{IN1}, V_{IN2}) Input voltage range(^{(2)})</td>
<td>-0.3 to 7</td>
<td>V</td>
</tr>
<tr>
<td>Voltage range at (EN)</td>
<td>-0.3 to 7</td>
<td>V</td>
</tr>
<tr>
<td>(V_{OUT1}, V_{SENSE1}, V_{OUT2}, V_{SENSE2}) Output voltage range</td>
<td>5.5</td>
<td>V</td>
</tr>
<tr>
<td>Maximum (RESET, PG1) voltage</td>
<td>7</td>
<td>V</td>
</tr>
<tr>
<td>Maximum (MRT1, MRT2) and SEQ voltage</td>
<td>(V_{IN1})</td>
<td></td>
</tr>
<tr>
<td>Peak output current</td>
<td>Internally limited</td>
<td></td>
</tr>
<tr>
<td>(T_J) Operating virtual junction temperature range</td>
<td>-55 to 150</td>
<td>°C</td>
</tr>
<tr>
<td>Package thermal impedance</td>
<td>$\theta_{JC}$ (die to package top)</td>
<td>17.2</td>
</tr>
<tr>
<td></td>
<td>$\theta_{JC}$ (die to package bottom)</td>
<td>5.49</td>
</tr>
<tr>
<td></td>
<td>$\theta_{JE}$ (die to standard PCB trace)</td>
<td>38.4</td>
</tr>
<tr>
<td>(T_{stg}) Storage temperature range</td>
<td>-65 to 150</td>
<td>°C</td>
</tr>
<tr>
<td>ESD rating (HBM, human body model)</td>
<td>2</td>
<td>kV</td>
</tr>
</tbody>
</table>

\(^{(1)}\) Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

\(^{(2)}\) All voltages are tied to network ground.

## RECOMMENDED OPERATING CONDITIONS

*over operating free-air temperature range (unless otherwise noted)*

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Min</th>
<th>Nom</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>(V_I) Input voltage(^{(1)})</td>
<td>2.7</td>
<td>6</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>(I_O) Output current</td>
<td>Regulator 1</td>
<td>0</td>
<td>1</td>
<td>A</td>
</tr>
<tr>
<td></td>
<td>Regulator 2</td>
<td>0</td>
<td>2</td>
<td></td>
</tr>
<tr>
<td>(T_J) Operating virtual storage temperature</td>
<td>-55</td>
<td>125</td>
<td>°C</td>
<td></td>
</tr>
</tbody>
</table>

\(^{(1)}\) To calculate the minimum input voltage for maximum output current, use the following equation: \(V_{I(min)} = V_{O(max)} + V_{D0(max \, load)}\).

## ELECTRICAL CHARACTERISTICS

*over operating junction temperature range (\(T_J = -55^\circ C\) to 125°C) \(V_{IN1}\) or \(V_{IN2} = V_{OUTX(nom)} + V_I, I_{OUTX} = 1 mA, EN = 0, C_{OUT1} = 22 \mu F, C_{OUT2} = 47 \mu F\) (unless otherwise noted)*

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Test Conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>(V_O) Output voltage(^{(1)})(^{(2)})</td>
<td>2.5 V output ((V_{OUT2}))</td>
<td>3.5 V &lt; (V_I &lt; 6) V, (T_J = 25^\circ C)</td>
<td>2.5</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>3.5 V &lt; (V_I &lt; 6) V</td>
<td>2.45</td>
<td>2.55</td>
<td></td>
</tr>
<tr>
<td></td>
<td>3.3 V output ((V_{OUT1}))</td>
<td>4.3 V &lt; (V_I &lt; 6) V, (T_J = 25^\circ C)</td>
<td>3.3</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>4.3 V &lt; (V_I &lt; 6) V</td>
<td>3.234</td>
<td>3.366</td>
<td></td>
</tr>
<tr>
<td>Quiescent current (GND current) for regulator 1 and regulator 2, (EN = 0)(^{(3)})</td>
<td>(T_J = 25^\circ C)</td>
<td>185</td>
<td>250</td>
<td>μA</td>
<td></td>
</tr>
<tr>
<td>Load regulation for (V_{OUT1}) and (V_{OUT2})(^{(3)})</td>
<td>(T_J = 25^\circ C)</td>
<td>1</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Output voltage line regulation for regulator 1 and regulator 2(^{(1)})</td>
<td>(V_O + 1 V &lt; V_I &lt; 6 V, T_J = 25^\circ C)</td>
<td>0.01%</td>
<td>5.6</td>
<td>mV</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>(V_O + 1 V &lt; V_I &lt; 6 V)</td>
<td>6.25</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

\(^{(1)}\) Minimum input operating voltage is 2.7 V or \(V_{O(}\text{Typ}) + 1 V\), whichever is greater. Maximum input voltage is 6 V, minimum output current is 1 mA.

\(^{(2)}\) Input voltage\((\text{\(V_{IN1}\) or \(V_{IN2}\) = \(V_{O(}\text{Typ}) - 100 mV. For the 2.5-V regulators, the dropout voltage is limited by input voltage range. The 3.3-V regulator input voltage is set to 3.2 V to perform this test.\(}}\)

\(^{(3)}\) \(I_O = 1 mA\) to 1 A for regulator 1 and 1 mA to 2 A for regulator 2.
**ELECTRICAL CHARACTERISTICS (continued)**

over operating junction temperature range \((T_J = -55\degree C \text{ to } 125\degree C)\) \(V_{IN1} \text{ or } V_{IN2} = V_{OUTx(nom)} + V\), \(I_{OUTx} = 1 \text{ mA}\), \(EN = 0\), \(C_{OUT1} = 22 \mu\text{F}\), \(C_{OUT2} = 47 \mu\text{F}\) (unless otherwise noted)

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>Output current limit</td>
<td>Regulator 1 (V_O = 0 \text{ V})</td>
<td>1.75</td>
<td>2.2</td>
<td></td>
<td>A</td>
</tr>
<tr>
<td></td>
<td>Regulator 2 (V_O = 0 \text{ V})</td>
<td>3.8</td>
<td>4.5</td>
<td></td>
<td>°C</td>
</tr>
<tr>
<td>Thermal shutdown junction TEMP</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>(I_{(standby)}) Standby current</td>
<td>(EN = V_I), (T_J = 25\degree C)</td>
<td>1</td>
<td>2</td>
<td></td>
<td>µA</td>
</tr>
<tr>
<td></td>
<td>(EN = V_I)</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**RESET TERMINAL**

| Minimum input voltage for valid RESET | \(I\(_{(RESET)}\) = 300 \mu\text{A}\), \(V\(_{(RESET)}\) \leq 0.8 \text{ V}\) | 1   | 1.45 | V   |
| Trip threshold voltage             | \(V_O\) decreasing                                                                 | 92% | 95%  | 98%  | \(V_O\) |
| Hysteresis voltage                 | Measured at \(V_O\)                                                               | 0.5% |     |     |      |
| \(I\(_{(RESET)}\)\(_{(4)}\)\) Rising edge deglitch | \(V\(_{(RESET)}\)\(_{(4)}\)\) pulse duration \(T_J = 25\degree C\) | 80  | 160  | 160  | ms   |
| Output low voltage                 | \(V_I = 3.5 \text{ V}\), \(I\(_{(RESET)}\) = 1 \text{ mA}\)                    | 0.15 | 0.4  |     | V    |
| Leakage current                    | \(V\(_{(RESET)}\)\(_{(4)}\) = 6 \text{ V}\)                                    |     |     | 1    | µA   |

**PG TERMINAL**

| Minimum input voltage for valid PG | \(I\(_{(PG)}\) = 300 \mu\text{A}\), \(V\(_{(PG)}\) \leq 0.8 \text{ V}\) | 1   | 1.45 | V   |
| Trip threshold voltage             | \(V_O\) decreasing                                                                 | 92% | 95%  | 98%  | \(V_O\) |
| Hysteresis voltage                 | Measured at \(V_O\)                                                               | 0.5% |     |     |      |
| \(I\(_{(PG)}\)\(_{(4)}\)\) Rising edge deglitch | \(V\(_{(PG)}\)\(_{(4)}\)\) pulse duration \(T_J = 25\degree C\) | 30  |     |     | µs   |
| Output low voltage                 | \(V_I = 2.7 \text{ V}\), \(I\(_{(PG)}\) = 1 \text{ mA}\)                        | 0.15 | 0.4  |     | V    |
| Leakage current                    | \(V\(_{(PG)}\)\(_{(4)}\) = 6 \text{ V}\)                                    |     |     | 1    | µA   |

**EN TERMINAL**

| High–level EN input voltage        |                                                                 | 2   |     |     | V    |
| Low–level EN input voltage         |                                                                 | 0.7 |     |     | V    |
| Input current \(EN\)               | -1                                                                | 1   |     |     | µA   |

**SEQ TERMINAL**

| High–level SEQ input voltage       |                                                                 | 2   |     |     | V    |
| Low–level SEQ input voltage        |                                                                 | 0.7 |     |     | V    |
| SEQ pullup current source          |                                                                 | 6   |     |     | µA   |

**MR1 / MR2 TERMINAL**

| High–level input voltage           |                                                                 | 2   |     |     | V    |
| Low–level input voltage            |                                                                 | 0.7 |     |     | V    |
| Pullup current source              |                                                                 | 6   |     |     | µA   |

**V\(_{OUT2}\) TERMINAL**

| \(V\(_{OUT2}\)\) UV comparator - positive–going input threshold voltage of \(V\(_{OUT2}\)\) UV comparator | 80% \(V_O\) | 83% \(V_O\) | 86% \(V_O\) | V |
| \(V\(_{OUT2}\)\) UV comparator - hysteresis                                                        | 3% \(V_O\) |     |     | mV |
| \(V\(_{OUT2}\)\) UV comparator - falling edge deglitch \(_{(4)}\) \(V\(_{SENSE2}\)\) decreasing below threshold | 140 |     |     | µs |
| Peak output current                | 2-ms pulse width                                                  | 3   |     |     | A   |
| Discharge transistor current        | \(V\(_{OUT2}\) = 1.5 \text{ V}\)                                 | 7.5 |     |     | mA  |

**V\(_{OUT1}\) TERMINAL**

| \(V\(_{OUT1}\)\) UV comparator - positive–going input threshold voltage of \(V\(_{OUT1}\)\) UV comparator | 80% \(V_O\) | 83% \(V_O\) | 86% \(V_O\) | V |
| \(V\(_{OUT1}\)\) UV comparator - hysteresis                                                        | 3% \(V_O\) |     |     | mV |
| \(V\(_{OUT1}\)\) UV comparator - falling edge deglitch \(V\(_{SENSE1}\)\) decreasing below threshold | 140 |     |     | µs |

\(_{(4)}\) Not production tested. Specified by design.
ELECTRICAL CHARACTERISTICS (continued)

over operating junction temperature range (T_J = –55°C to 125°C) V_IN1 or V_IN2 = V_OUTx(nom) + V, I_OUTx = 1 mA, EN = 0, 
C_OUT1 = 22 µF, C_OUT2 = 47 µF (unless otherwise noted)

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>Dropout voltage&lt;sup&gt;(5)&lt;/sup&gt;</td>
<td>I_O = 1 A, V_IN1 = 3.2 V, T_J = 25°C</td>
<td>160</td>
<td></td>
<td></td>
<td>mV</td>
</tr>
<tr>
<td></td>
<td>I_O = 1 A, V_IN1 = 3.2 V</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Peak output current</td>
<td>2-ms pulse width</td>
<td>1.2</td>
<td></td>
<td></td>
<td>A</td>
</tr>
<tr>
<td>Discharge transistor current</td>
<td>V_OUT1 = 1.5 V</td>
<td>7.5</td>
<td></td>
<td></td>
<td>mA</td>
</tr>
</tbody>
</table>

VIN1 / VIN2 TERMINAL

<table>
<thead>
<tr>
<th></th>
<th>UVLO threshold</th>
<th>UVLO hysteresis</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>2.3</td>
<td>2.65</td>
</tr>
<tr>
<td></td>
<td>110</td>
<td>mV</td>
</tr>
</tbody>
</table>

<sup>(5)</sup> Input voltage(V_IN1 or V_IN2) = V_O(Typ) – 100 mV. For the 2.5-V regulators, the dropout voltage is limited by input voltage range. The 3.3-V regulator input voltage is set to 3.2 V to perform this test.
TYPICAL CHARACTERISTICS

Table 1. TPS70358M

<table>
<thead>
<tr>
<th>PRODUCT</th>
<th>VOLTAGE (V)</th>
<th>PACKAGE-LEAD (DESIGNATOR)</th>
<th>SPECIFIED TEMPERATURE RANGE (T_J)</th>
<th>ORDERING NUMBER</th>
<th>TOP-SIDE MARKING</th>
</tr>
</thead>
<tbody>
<tr>
<td>TPS70358M</td>
<td>3.3 V 2.5 V</td>
<td>DFP-20 (HKH)</td>
<td>–55°C to 125°C</td>
<td>TPS70358MHKH</td>
<td>TPS70358MHKH</td>
</tr>
</tbody>
</table>

Table 2. Table of Graphs

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Description</th>
<th>Figure</th>
</tr>
</thead>
<tbody>
<tr>
<td>V_O</td>
<td>Output voltage</td>
<td>Figure 3, Figure 4</td>
</tr>
<tr>
<td></td>
<td>vs Output current</td>
<td></td>
</tr>
<tr>
<td>Ground current</td>
<td>vs Junction temperature</td>
<td>Figure 5, Figure 6</td>
</tr>
<tr>
<td>PSRR</td>
<td>Power supply rejection ratio</td>
<td>Figure 7</td>
</tr>
<tr>
<td>Z_O</td>
<td>Output impedance</td>
<td>Figure 8 - Figure 11</td>
</tr>
<tr>
<td></td>
<td>vs Frequency</td>
<td></td>
</tr>
<tr>
<td>Dropout voltage</td>
<td>vs Temperature</td>
<td>Figure 12 - Figure 15</td>
</tr>
<tr>
<td></td>
<td>vs Frequency</td>
<td></td>
</tr>
<tr>
<td>Load transient response</td>
<td>vs Input voltage</td>
<td>Figure 16 - Figure 19</td>
</tr>
<tr>
<td>Line transient response</td>
<td>vs Junction temperature</td>
<td>Figure 20, Figure 21</td>
</tr>
<tr>
<td>V_O</td>
<td>Output voltage and enable voltage</td>
<td>Figure 22, Figure 23</td>
</tr>
<tr>
<td></td>
<td>vs Time (start–up)</td>
<td></td>
</tr>
<tr>
<td>Equivalent series resistance</td>
<td>vs Output current</td>
<td>Figure 24, Figure 25</td>
</tr>
</tbody>
</table>

Figure 3.

TPS70351 OUTPUT VOLTAGE vs OUTPUT CURRENT

Figure 4.

TPS70351 OUTPUT VOLTAGE vs OUTPUT CURRENT
TPS70351

OUTPUT VOLTAGE

VS

JUNCTION TEMPERATURE

Figure 5.

TPS70351

OUTPUT VOLTAGE

VS

JUNCTION TEMPERATURE

Figure 6.

TPS70351

GROUND CURRENT

VS

JUNCTION TEMPERATURE

Figure 7.
TPS70351
OUTPUT VOLTAGE
VS
JUNCTION TEMPERATURE (continued)

Figure 8.

Figure 9.

Figure 10.

Figure 11.
TPS70351
OUTPUT VOLTAGE
VS
JUNCTION TEMPERATURE (continued)

OUTPUT SPECTRAL NOISE DENSITY

\[ V_{\text{out}} = 4.3 \text{ V} \]
\[ V_{\text{in}} = 3.3 \text{ V} \]
\[ C_{\text{out}} = 22 \mu \text{F} \]
\[ I_{\text{o}} = 10 \text{ mA} \]
\[ T = 25 ^\circ \text{C} \]

OUTPUT SPECTRAL NOISE DENSITY vs FREQUENCY

\[ V_{\text{out}} = 2.8 \text{ V} \]
\[ V_{\text{in}} = 1.8 \text{ V} \]
\[ C_{\text{out}} = 47 \mu \text{F} \]
\[ I_{\text{o}} = 10 \text{ mA} \]
\[ T = 25 ^\circ \text{C} \]

Figure 12.

OUTPUT SPECTRAL NOISE DENSITY vs FREQUENCY

\[ V_{\text{out}} = 4.3 \text{ V} \]
\[ V_{\text{in}} = 3.3 \text{ V} \]
\[ C_{\text{out}} = 22 \mu \text{F} \]
\[ I_{\text{o}} = 1 \text{ A} \]
\[ T = 25 ^\circ \text{C} \]

Figure 13.

OUTPUT SPECTRAL NOISE DENSITY vs FREQUENCY

\[ V_{\text{out}} = 4.3 \text{ V} \]
\[ V_{\text{in}} = 3.3 \text{ V} \]
\[ C_{\text{out}} = 22 \mu \text{F} \]
\[ I_{\text{o}} = 1 \text{ A} \]
\[ T = 25 ^\circ \text{C} \]

Figure 14.

OUTPUT SPECTRAL NOISE DENSITY vs FREQUENCY

\[ V_{\text{out}} = 2.8 \text{ V} \]
\[ V_{\text{in}} = 1.8 \text{ V} \]
\[ C_{\text{out}} = 47 \mu \text{F} \]
\[ I_{\text{o}} = 2 \text{ A} \]
\[ T = 25 ^\circ \text{C} \]

Figure 15.
TPS70351
OUTPUT VOLTAGE
VS
JUNCTION TEMPERATURE (continued)

Figure 16.
OUTPUT IMPEDANCE
VS
FREQUENCY

Figure 17.
OUTPUT IMPEDANCE
VS
FREQUENCY

Figure 18.
OUTPUT IMPEDANCE
VS
FREQUENCY

Figure 19.
OUTPUT IMPEDANCE
VS
FREQUENCY
TPS70351
OUTPUT VOLTAGE
VS
JUNCTION TEMPERATURE (continued)

Figure 20.
TPS70302
DROPOUT VOLTAGE
VS
INPUT VOLTAGE

Figure 21.
TPS70302
DROPOUT VOLTAGE
VS
INPUT VOLTAGE

Figure 22.
TPS70302
DROPOUT VOLTAGE
VS
INPUT VOLTAGE

Figure 23.
TPS70351
OUTPUT VOLTAGE
VS
JUNCTION TEMPERATURE (continued)

Figure 24.

Figure 25.

Figure 26.

Figure 27.
TPS70351
OUTPUT VOLTAGE
VS
JUNCTION TEMPERATURE (continued)

OUTPUT VOLTAGE AND ENABLE VOLTAGE
VS
TIME (START-UP)

Output Voltage - VO
Enable Voltage - VOC

0 0.2 0.4 0.6 0.8 1 1.2 1.4 1.6 1.8 2 2

VOC = 22 µ F
VO = 3.3 V
I0 = 1 A

SEQ = Low

VOC = 47 µ F
VO = 1.8 V
I0 = 2 A

SEQ = High

Figure 28.

Figure 29.

Figure 30. Test Circuit for Typical Regions of Stability
Sequencing Timing Diagrams

The following figures provide a timing diagram of how this device functions in different configurations.

SEQ = Low

*Application Conditions Not Shown in Block Diagram:*

\( V_{IN1} \) and \( V_{IN2} \) are tied to the same fixed input voltage greater than the \( V_{UVLO} \); \( SEQ \) is tied to logic low; \( PG1 \) is tied to \( MR2 \); \( MR1 \) is not used and is connected to \( V_{IN} \).

**Explanation of Timing Diagram:**

\( EN \) is initially high; therefore, both regulators are off and \( PG1 \) and \( RESET \) are at logic low. With \( SEQ \) at logic low, when \( EN \) is taken to logic low, \( V_{OUT1} \) turns on. \( V_{OUT2} \) turns on after \( V_{OUT1} \) reaches 83\% of its regulated output voltage. When \( V_{OUT1} \) reaches 95\% of its regulated output voltage, \( PG1 \) (tied to \( MR2 \)) goes to logic high. When both \( V_{OUT1} \) and \( V_{OUT2} \) reach 95\% of their respective regulated output voltages and both \( MR1 \) and \( MR2 \) (tied to \( PG1 \)) are at logic high, \( RESET \) is pulled to logic high after a 120-ms delay. When \( EN \) is returned to logic high, both devices power down and both \( PG1 \) (tied to \( MR2 \)) and \( RESET \) return to logic low.
SEQ = High

Application Conditions Not Shown in Block Diagram:

V_{IN1} and V_{IN2} are tied to the same fixed input voltage greater than the V_{UVLO}; SEQ is tied to logic high; PG1 is tied to MR2; MRT is not used and is connected to V_{IN}.

Figure 35. Timing When SEQ = Low

NOTE A: t1 - Time at which both V_{out1} and V_{out2} are greater than the PG thresholds and MRT is logic high.
**Explanation of Timing Diagram:**

EN is initially high; therefore, both regulators are off and PG1 and RESET are at logic low. With SEQ at logic high, when EN is taken to logic low, \( V_{OUT2} \) turns on. \( V_{OUT1} \) turns on after \( V_{OUT2} \) reaches 83% of its regulated output voltage. When \( V_{OUT1} \) reaches 95% of its regulated output voltage, PG1 (tied to MR2) goes to logic high. When both \( V_{OUT1} \) and \( V_{OUT2} \) reach 95% of their respective regulated output voltages and both MRT and MR2 (tied to PG1) are at logic high, RESET is pulled to logic high after a 120-ms delay. When EN is returned to logic high, both devices turn off and both PG1 (tied to MR2) and RESET return to logic low.

**Figure 36. Timing When SEQ = High**
Toggled MR1

Application Conditions Not Shown in Block Diagram:

$V_{IN1}$ and $V_{IN2}$ are tied to the same fixed input voltage greater than the $V_{UVLO}$; SEQ is tied to logic high; PG1 is tied to MR2; MR1 is initially at logic high but is eventually toggled.

![Block Diagram of TPS70358M](image)

Explanation of Timing Diagram:

$EN$ is initially high; therefore, both regulators are off and PG1 and RESET are at logic low. With SEQ at logic high, when $EN$ is taken low, $V_{OUT2}$ turns on. $V_{OUT1}$ turns on after $V_{OUT2}$ reaches 83% of its regulated output voltage. When $V_{OUT1}$ reaches 95% of its regulated output voltage, PG1 (tied to MR2) goes to logic high. When both $V_{OUT1}$ and $V_{OUT2}$ reach 95% of their respective regulated output voltages and both MR1 and MR2 (tied to PG1) are at logic high, RESET is pulled to logic high after a 120-ms delay. When MR1 is taken low, RESET returns to logic low but the outputs remain in regulation. When MR1 is returned to logic high, since both $V_{OUT1}$ and $V_{OUT2}$ remain above 95% of their respective regulated output voltages and MR2 (tied to PG1) remains at logic high, RESET is pulled to logic high after a 120-ms delay.
NOTE A: t1 - Time at which both V_{out1} and V_{out2} are greater than the PG thresholds and M_{R1} is logic high.

**Figure 37. Timing When MR1 is Toggled**

V_{OUT1} FAULT

**Application Conditions Not Shown in Block Diagram:**

V_{IN1} and V_{IN2} are tied to the same fixed input voltage greater than the V_{UVLO}; SEQ is tied to logic high; PG1 is tied to MR2; M_{R1} is not used and is connected to V_{IN}.
**Explanation of Timing Diagram:**

EN is initially high; therefore, both regulators are off and PG1 and RESET are at logic low. With SEQ at logic high, when EN is taken low, V\text{OUT2} turns on. V\text{OUT1} turns on after V\text{OUT2} reaches 83% of its regulated output voltage. When V\text{OUT1} reaches 95% of its regulated output voltage, PG1 (tied to MR2) goes to logic high. When both V\text{OUT1} and V\text{OUT2} reach 95% of their respective regulated output voltages and both MRT and MR2 (tied to PG1) are at logic high, RESET is pulled to logic high after a 120-ms delay. When a fault on V\text{OUT1} causes it to fall below 95% of its regulated output voltage, PG1 (tied to MR2) goes to logic low.

![Timing Diagram](image)

**Figure 38. Timing When a Fault Occurs on V\text{OUT1}**

**NOTE A:** t1 - Time at which both V\text{OUT1} and V\text{OUT2} are greater than the PG thresholds and MRT is logic high.
**V\text{OUT2 FAULT}**

**Application Conditions Not Shown in Block Diagram:**

\(V_{\text{IN1}}\) and \(V_{\text{IN2}}\) are tied to the same fixed input voltage greater than the \(V_{\text{UVLO}}\); SEQ is tied to logic high; PG1 is tied to MR2; MR1 is not used and is connected to \(V_{\text{IN}}\).

![Block Diagram](image)

**Explanation of Timing Diagram:**

\(\text{EN}\) is initially high; therefore, both regulators are off and PG1 and \(\text{RESET}\) are at logic low. With SEQ at logic high, when \(\text{EN}\) is taken low, \(V_{\text{OUT2}}\) turns on. \(V_{\text{OUT1}}\) turns on after \(V_{\text{OUT2}}\) reaches 83% of its regulated output voltage. When \(V_{\text{OUT1}}\) reaches 95% of its regulated output voltage, PG1 (tied to MR2) goes to logic high. When both \(V_{\text{OUT1}}\) and \(V_{\text{OUT2}}\) reach 95% of their respective regulated output voltages and both MR1 and MR2 (tied to PG1) are at logic high, \(\text{RESET}\) is pulled to logic high after a 120-ms delay. When a fault on \(V_{\text{OUT2}}\) causes it to fall below 95% of its regulated output voltage, \(\text{RESET}\) returns to logic low and \(V_{\text{OUT1}}\) begins to power down because SEQ is high. When \(V_{\text{OUT1}}\) falls below 95% of its regulated output voltage, PG1 (tied to MR2) returns to logic low.
NOTE A: \( t_1 \) - Time at which both \( V_{\text{OUT1}} \) and \( V_{\text{OUT2}} \) are greater than the PG thresholds and \( \text{MRIT} \) is logic high.

Figure 39. Timing When a Fault Occurs on \( V_{\text{OUT2}} \)
Split Voltage DSP Application

Figure 40 shows a typical application where the TPS70358 is powering up a DSP. In this application, by grounding the SEQ pin, \( V_{\text{OUT1}} \) (I/O) is powered up first, and then \( V_{\text{OUT2}} \) (core).

Figure 40. Application Timing Diagram (SEQ = Low)

**NOTE A:** t1 - Time at which both \( V_{\text{OUT1}} \) and \( V_{\text{OUT2}} \) are greater than the PG1 thresholds and MRT is logic high.
Figure 41 shows a typical application where the TPS70358 is powering up a DSP. In this application, by pulling up the SEQ pin, V_{OUT2}(Core) is powered up first, and then V_{OUT1}(I/O).

Input Capacitor

For a typical application, a ceramic input bypass capacitor (0.22 μF – 1 μF) is recommended to ensure device stability. This capacitor should be as close as possible to the input pin. Due to the impedance of the input supply, large transient currents causes the input voltage to droop. If this droop causes the input voltage to drop below...
the UVLO threshold, the device turns off. Therefore, it is recommended that a larger capacitor be placed in parallel with the ceramic bypass capacitor at the regulator’s input. The size of this capacitor depends on the output current, response time of the main power supply, and the main power supply’s distance to the regulator. At a minimum, the capacitor should be sized to ensure that the input voltage does not drop below the minimum UVLO threshold voltage during normal operating conditions.

**Output Capacitor**

As with most LDO regulators, the TPS70358 requires an output capacitor connected between each OUT and GND to stabilize the internal control loop. The minimum recommended capacitance value for $V_{OUT1}$ is 22 µF and the ESR (equivalent series resistance) must be between 50 mΩ and 800 mΩ. The minimum recommended capacitance value for $V_{OUT2}$ is 47 µF and the ESR must be between 50 mΩ and 2 Ω. Solid tantalum electrolytic, aluminum electrolytic, and multilayer ceramic capacitors are all suitable, provided they meet the requirements described above. Larger capacitors provide a wider range of stability and better load transient response. Below is a partial listing of surface-mount capacitors usable with the TPS703xx for fast transient response application.

This information, along with the ESR graphs, is included to assist in selection of suitable capacitance for the user’s application. When necessary to achieve low height requirements along with high output current and/or high load capacitance, several higher ESR capacitors can be used in parallel to meet the guidelines above.

<table>
<thead>
<tr>
<th>VALUE</th>
<th>MANUFACTURER</th>
<th>PART NO.</th>
</tr>
</thead>
<tbody>
<tr>
<td>680 µF</td>
<td>Kemet</td>
<td>T510X6871004AS</td>
</tr>
<tr>
<td>470 µF</td>
<td>Sanyo</td>
<td>4TPB470M</td>
</tr>
<tr>
<td>150 µF</td>
<td>Sanyo</td>
<td>4TPC150M</td>
</tr>
<tr>
<td>220 µF</td>
<td>Sanyo</td>
<td>2R5TPC220M</td>
</tr>
<tr>
<td>100 µF</td>
<td>Sanyo</td>
<td>6TPC100M</td>
</tr>
<tr>
<td>68 µF</td>
<td>Sanyo</td>
<td>10TPC68M</td>
</tr>
<tr>
<td>68 µF</td>
<td>Kemet</td>
<td>T495D6861006AS</td>
</tr>
<tr>
<td>47 µF</td>
<td>Kemet</td>
<td>T495D4761010AS</td>
</tr>
<tr>
<td>33 µF</td>
<td>Kemet</td>
<td>T495C3361016AS</td>
</tr>
<tr>
<td>22 µF</td>
<td>Kemet</td>
<td>T495C2261010AS</td>
</tr>
</tbody>
</table>

**Regulator Protection**

Both TPS70358 PMOS-pass transistors have built-in back diodes that conduct reverse currents when the input voltage drops below the output voltage (e.g., during power down). Current is conducted from the output to the input and is not internally limited. When extended reverse voltage is anticipated, external limiting may be appropriate.

The TPS70358 also features internal current limiting and thermal protection. During normal operation, the TPS70358 regulator 1 limits output current to approximately 1.75 A (typ) and regulator 2 limits output current to approximately 3.8 A (typ). When current limiting engages, the output voltage scales back linearly until the overcurrent condition ends. While current limiting is designed to prevent gross device failure, care should be taken not to exceed the power dissipation ratings of the package. If the temperature of the device exceeds 150°C (typ), thermal-protection circuitry shuts it down. Once the device has cooled below 130°C (typ), regulator operation resumes.
## PACKAGING INFORMATION

<table>
<thead>
<tr>
<th>Orderable Device</th>
<th>Status (1)</th>
<th>Package Type</th>
<th>Package Drawing</th>
<th>Pins</th>
<th>Package Qty</th>
<th>Eco Plan (2)</th>
<th>Lead/Ball Finish</th>
<th>MSL Peak Temp (3)</th>
</tr>
</thead>
<tbody>
<tr>
<td>TPS70358MHKH</td>
<td>ACTIVE</td>
<td>CFP</td>
<td>HKH</td>
<td>20</td>
<td>25</td>
<td>TBD</td>
<td>Call TI</td>
<td>N/A for Pkg Type</td>
</tr>
</tbody>
</table>

(1) The marketing status values are defined as follows:
- **ACTIVE**: Product device recommended for new designs.
- **LIFEBUY**: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
- **NRND**: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
- **PREVIEW**: Device has been announced but is not in production. Samples may or may not be available.
- **OBSOLETE**: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check [http://www.ti.com/productcontent](http://www.ti.com/productcontent) for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material).

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

---

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**OTHER QUALIFIED VERSIONS OF TPS70358M:**

- Catalog: TPS70358

**NOTE:** Qualified Version Definitions:
- **Catalog**: TI's standard catalog product
HKH (R-CDFP-F20)  CERAMIC DUAL FLATPACK

NOTES:  A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a metal lid.
D. The terminals will be gold plated.
E. Falls within MIL STD 1835 CDFP-F20.

4209648/A 07/08

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<th>Applications</th>
</tr>
</thead>
<tbody>
<tr>
<td>Amplifiers</td>
<td>amplifier.ti.com</td>
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<tr>
<td>Data Converters</td>
<td>dataconverter.ti.com</td>
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<td>DLP® Products</td>
<td><a href="http://www.dlp.com">www.dlp.com</a></td>
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<td>DSP</td>
<td>dsp.ti.com</td>
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<td>Clocks and Timers</td>
<td><a href="http://www.ti.com/clocks">www.ti.com/clocks</a></td>
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<td>Interface</td>
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