TPS730 Low-Noise, High PSRR, RF, 200-mA Low-Dropout Linear Regulators

1 Features

- 200-mA RF Low-Dropout Regulator With Enable
- Available in Fixed Voltages from 1.8 V to 3.3 V and Adjustable Voltages (1.22 V to 5.5 V)
- High PSRR (68 dB at 100 Hz)
- Low Noise (33 μV_{RMS}, TPS73018)
- Fast Start-Up Time (50 µs)
- Stable With a 2.2-µF Ceramic Capacitor
- Excellent Load/Line Transient Response
- Very Low Dropout Voltage (120 mV at 200 mA)
- 5- and 6-Pin SOT-23 (DBV), and Wafer Chip Scale (YZQ) Packages

2 Applications

- RF: VCOs, Receivers, ADCs
- Audio
- Cellular and Cordless Telephones
- Bluetooth®, Wireless LAN
- Handheld Organizers, PDAs

3 Description

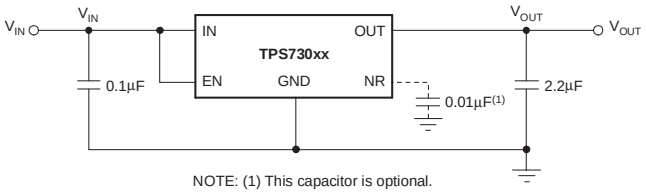
The TPS730 family of low-dropout (LDO) low-power linear voltage regulators features high power-supply rejection ratio (PSRR), low noise, fast start-up, and excellent line and load transient responses in a small SOT-23 package. NanoStar™ packaging gives an ultrasmall footprint as well as an ultralow profile and package weight, making it ideal for portable applications such as handsets and PDAs. Each device in the family is stable, with a small, 2.2-µF ceramic capacitor on the output. The TPS730 family uses an advanced, proprietary BiCMOS fabrication process to yield low dropout voltages (for example, 120 mV at 200 mA, TPS73030). Each device achieves fast start-up times (approximately 50 µs with a 0.001-µF bypass capacitor) while consuming low quiescent current (170 µA typical). Moreover, when the device is placed in standby mode, the supply current is reduced to less than 1 µA. The TPS73018 exhibits approximately 33 μV_{RMS} of output voltage noise at 1.8 V output with a 0.01-µF bypass capacitor. Applications with analog components that are noise-sensitive, such as portable RF electronics, benefit from the high PSRR and low-noise features as well as the fast response time.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPS730	SOT-23 (5)	2.90 mm × 1.60 mm
	SOT-23 (6)	2.90 mm × 1.60 mm
	DSBGA (5)	1.35 mm × 1.00 mm

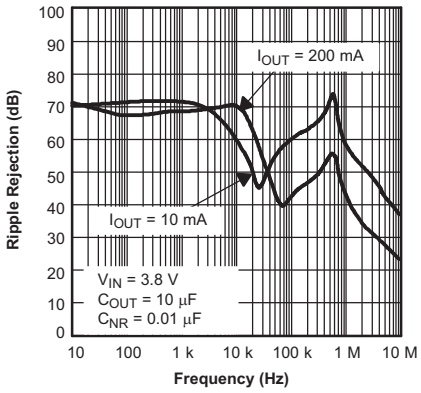
(1) For all available packages, see the orderable addendum at the end of the data sheet.

Simplified Schematic



NOTE: (1) This capacitor is optional.

Ripple Rejection vs Frequency



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision I (February, 2011) to Revision J **Page**

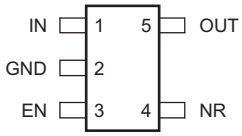
- Added *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section ... 1
- Changed fourth bullet of *Features* list to *low noise* ... 1
- Changed front-page figure ... 1
- Added *Pin Configuration and Functions* section ... 3
- Changed "free-air temperature" to "junction temperature" in *Absolute Maximum Ratings* condition statement ... 4
- Deleted *Dissipation Ratings* table; added *Thermal Information* table ... 4
- Added condition statement to *Typical Characteristics* ... 6
- Moved *Ordering Information* to *Device Nomenclature* section ... 18

Changes from Revision H (October, 2007) to Revision I **Page**

- Corrected units in y-axis of Figure 5 ... 6

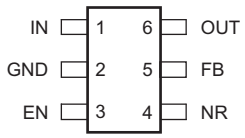
5 Pin Configuration and Functions

DBV Package
5-Pin SOT-23
Top View



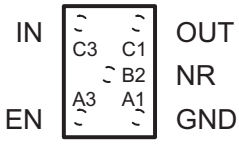
Fixed Voltage Versions

DBV Package
6-Pin SOT-23
Top View



Adjustable Voltage Version

YZQ Package
5-Pin DSBGA
Top View



Pin Functions

PIN			I/O	DESCRIPTION
NAME	NO.			
	SOT-23	DSBGA		
EN	3	A3	I	Enable pin. Driving the enable pin (EN) high turns on the regulator. Driving this pin low puts the regulator into shutdown mode. EN can be connected to IN if not used.
FB	5	N/A	I	Feedback pin. This terminal is the feedback input pin for the adjustable device. Fixed-voltage versions in the DBV package do not have this pin.
GND	2	A1	—	Regulator ground.
IN	1	C3	I	Input to the device.
OUT	6	C1	O	Output of the regulator.
NR	4	B2	—	Noise Reduction pin. Connecting an external capacitor to this pin filters noise generated by the internal bandgap. This configuration improves power-supply rejection and reduces output noise.

6 Specifications

6.1 Absolute Maximum Ratings

over operating junction temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
Voltage	Input range, V_{IN}		–0.3	6	V
	Enable range, V_{EN}		–0.3	6	
	Output range, V_{OUT}		–0.3	6	
Current	Peak output, $I_{OUT(max)}$		Internally limited		
Continuous total power dissipation			See *Thermal Information*		
Temperature	Junction, T_J	DBV package	–40	150	°C
		YZQ package	–40	125	
	Storage, T_{stg}		–65	150	

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

		VALUE	UNIT
$V_{(ESD)}$ Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	±2000	V
	Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating junction temperature range (unless otherwise noted).

		MIN	NOM	MAX	UNIT
V_{IN}	Input supply voltage	2.7		5.5	V
V_{EN}	Enable supply voltage	0		V_{IN}	V
V_{OUT}	Output voltage	V_{FB}		5	V
I_{OUT}	Output current	0		200	mA
T_J	Operating junction temperature	–40		125	°C
C_{IN}	Input capacitor	0.1	1		µF
C_{OUT}	Output capacitor	2.2(1)	10		µF
C_{NR}	Noise reduction capacitor	0	10		nF
C_{FF}	Feed-forward capacitor		15		pF
R_2	Lower feedback resistor		30.1		kΩ

(1) If C_{FF} is not used or $V_{OUT(nom)}$ < 1.8 V, the minimum recommended C_{OUT} = 4.7 µF.

6.4 Thermal Information

THERMAL METRIC(1)		TPS73001		UNIT
		DBV (SOT-23)	YZQ (DSBGA)	
		6 PINS	5 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	225.1	178.5	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	78.4	1.4	
$R_{\theta JB}$	Junction-to-board thermal resistance	54.7	62.1	
ψ_{JT}	Junction-to-top characterization parameter	3.3	0.9	
ψ_{JB}	Junction-to-board characterization parameter	53.8	62.1	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics

Over recommended operating temperature range T_J = –40 to +125°C, $V_{EN} = V_{IN}$, $V_{IN} = V_{OUT(nom)}$ + 1 V(1), I_{OUT} = 1 mA, C_{OUT} = 10 µF, C_{NR} = 0.01 µF (unless otherwise noted). Typical values are at 25°C.

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IN}	Input voltage range(1)			2.7		5.5	V
I_{OUT}	Continuous output current			0		200	mA
V_{FB}	Internal reference (TPS73001)			1.201	1.225	1.25	V
V_{OUT}	Output voltage range	TPS73001		V_{FB}		5.5 – V_{DO}	V
	Output voltage accuracy		0 µA ≤ I_{OUT} ≤ 200 mA, 2.75 V ≤ V_{IN} ≤ 5.5 V	–2%	$V_{OUT(nom)}$	2%	V
$\Delta V_{OUT(\Delta VIN)}$	Line regulation(1)		V_{OUT} + 1 V ≤ V_{IN} ≤ 5.5 V		0.05		%/V
$\Delta V_{OUT(\Delta IOUT)}$	Load regulation		0 µA ≤ I_{OUT} ≤ 200 mA, T_J = 25°C		5		mV
V_{DO}	Dropout voltage(2) ($V_{IN} = V_{OUT(nom)} – 0.1$ V)		I_{OUT} = 200 mA		120	210	mV
I_{CL}	Output current limit		V_{OUT} = 0 V	285		600	mA
I_{GND}	Ground pin current		0 µA < I_{OUT} < 200 mA		170	250	µA
$I_{SHUTDOWN}$	Shutdown current(3)		V_{EN} = 0 V, 2.7 V ≤ V_{IN} ≤ 5.5 V		0.07	1	µA
I_{FB}	FB pin current		V_{FB} = 1.8 V			1	µA
PSRR	Power-supply rejection ratio	TPS73028	f = 100 Hz, I_{OUT} = 200 mA, T_J = 25°C		68		dB
V_n	Output noise voltage	TPS73018	BW = 200 Hz to 100 kHz, I_{OUT} = 200 mA, C_{NR} = 0.01 µF		33		μV_{RMS}
t_{STR}	Start-up time	TPS73018	R_L = 14 Ω, C_{OUT} = 1 µF, C_{NR} = 0.001 µF		50		µs
$V_{EN(high)}$	High-level enable input voltage		2.7 V ≤ V_{IN} ≤ 5.5 V	1.7		V_{IN}	V
$V_{EN(low)}$	Low-level enable input voltage		2.7 V ≤ V_{IN} ≤ 5.5 V	0		0.7	V
I_{EN}	EN pin current		V_{EN} = 0 V	–1		1	µA
	UVLO		Threshold, V_{CC} rising	2.25		2.65	V
			Hysteresis		100		mV

(1) Minimum V_{IN} is 2.7 V or V_{OUT} + V_{DO}, whichever is greater.
(2) Dropout is not measured for the TPS73018 and TPS73025 since minimum V_{IN} = 2.7 V.
(3) For adjustable versions, this applies only after V_{IN} is applied; then V_{EN} transitions high to low.

6.6 Typical Characteristics

Over recommended operating temperature range T_J = –40°C to +125°C, $V_{EN} = V_{IN}$, $V_{IN} = V_{OUT(nom)}$ + 1 V, I_{OUT} = 1 mA, C_{OUT} = 10 µF, C_{NR} = 0.01 µF, $V_{OUT(nom)}$ = 2.8 V (unless otherwise noted). Typical values are at T_J = 25°C.

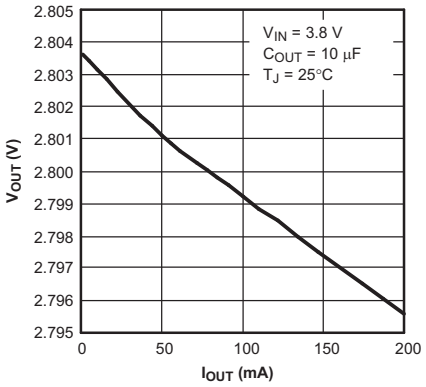


Figure 1. TPS73028 Output Voltage vs Output Current

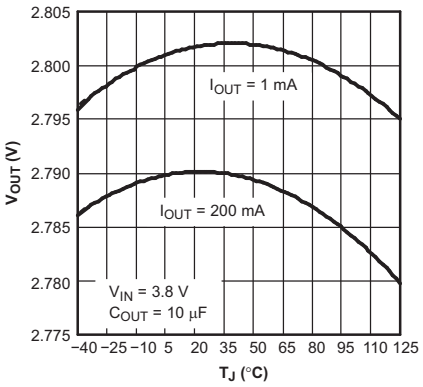


Figure 2. TPS73028 Output Voltage vs Junction Temperature

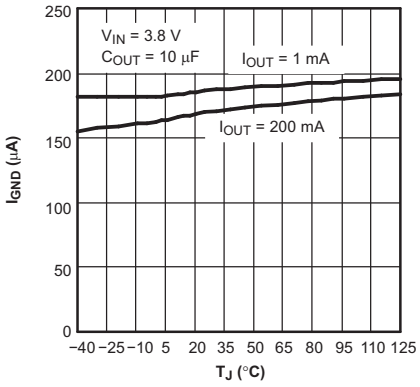


Figure 3. TPS73028 Ground Current vs Junction Temperature

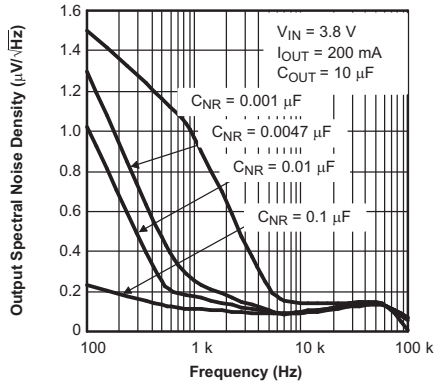


Figure 4. TPS73028 Output Spectral Noise Density vs Frequency

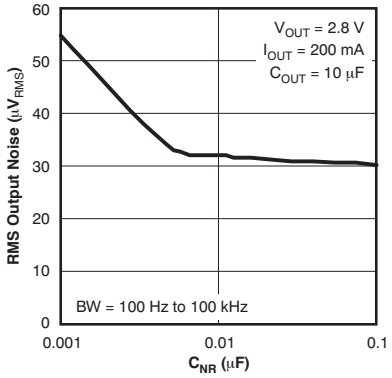


Figure 5. Root Mean Square Output Noise vs C_{NR}

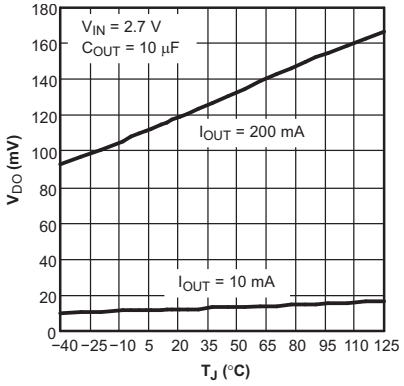


Figure 6. TPS73028 Dropout Voltage vs Junction Temperature

Typical Characteristics (continued)

Over recommended operating temperature range T_J = –40°C to +125°C, V_{EN} = V_{IN}, V_{IN} = $V_{OUT(nom)}$ + 1 V, I_{OUT} = 1 mA, C_{OUT} = 10 µF, C_{NR} = 0.01 µF, $V_{OUT(nom)}$ = 2.8 V (unless otherwise noted). Typical values are at T_J = 25°C.

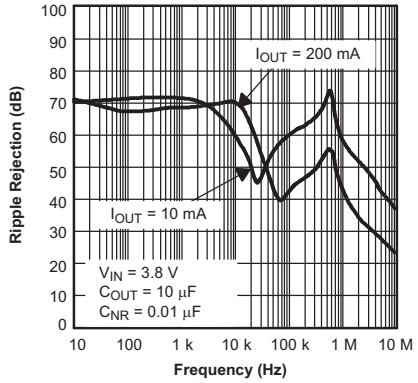


Figure 7. TPS73028 Ripple Rejection vs Frequency

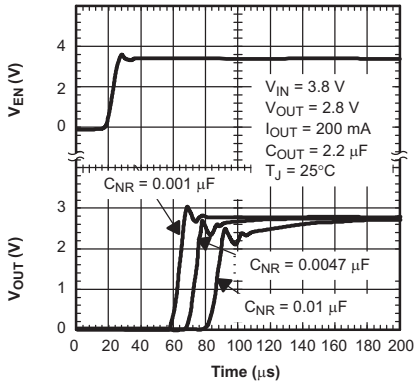


Figure 8. TPS73028 Output Voltage, Enable Voltage vs Time (Start-Up)

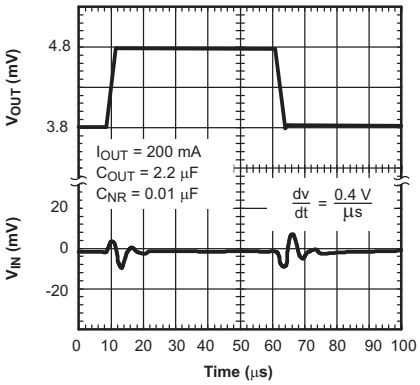


Figure 9. TPS73028 Line Transient Response

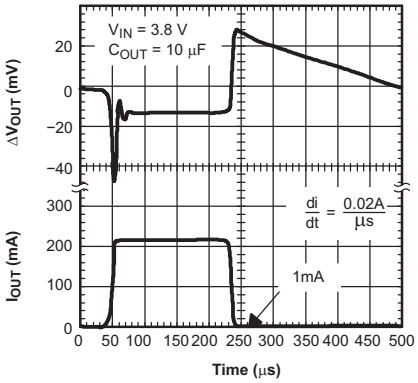


Figure 10. TPS73028 Load Transient Response

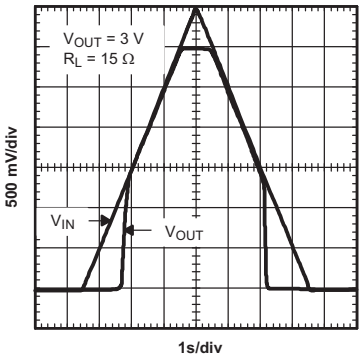


Figure 11. Power Up and Power Down

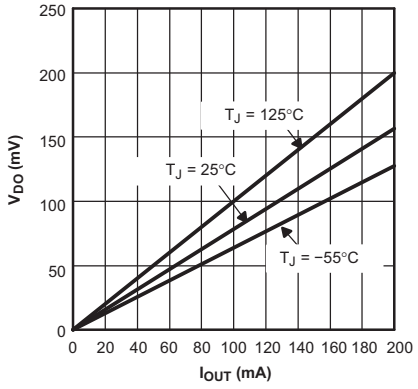


Figure 12. Dropout Voltage vs Output Current

Typical Characteristics (continued)

Over recommended operating temperature range T_J = –40°C to +125°C, $V_{EN} = V_{IN}$, $V_{IN} = V_{OUT(nom)}$ + 1 V, I_{OUT} = 1 mA, C_{OUT} = 10 µF, C_{NR} = 0.01 µF, $V_{OUT(nom)}$ = 2.8 V (unless otherwise noted). Typical values are at T_J = 25°C.

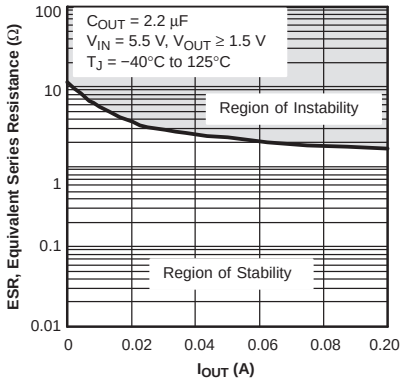


Figure 13. Typical Regions of Stability Equivalent Series Resistance (ESR) vs Output Current

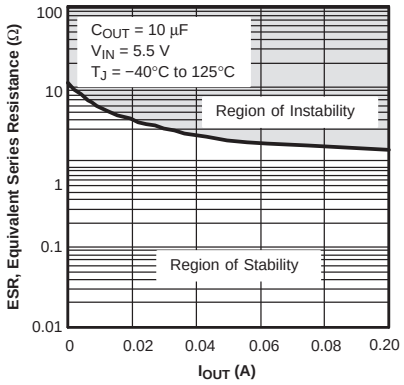


Figure 14. Typical Regions of Stability Equivalent Series Resistance (ESR) vs Output Current

7 Detailed Description

7.1 Overview

The TPS730 family of low-dropout (LDO) regulators has been optimized for use in noise-sensitive, battery-operated equipment. The device features extremely low dropout voltages, high PSRR, ultra-low output noise, low quiescent current (170 µA typically), and enable-input to reduce supply currents to less than 1 µA when the regulator is turned off.

7.2 Functional Block Diagrams

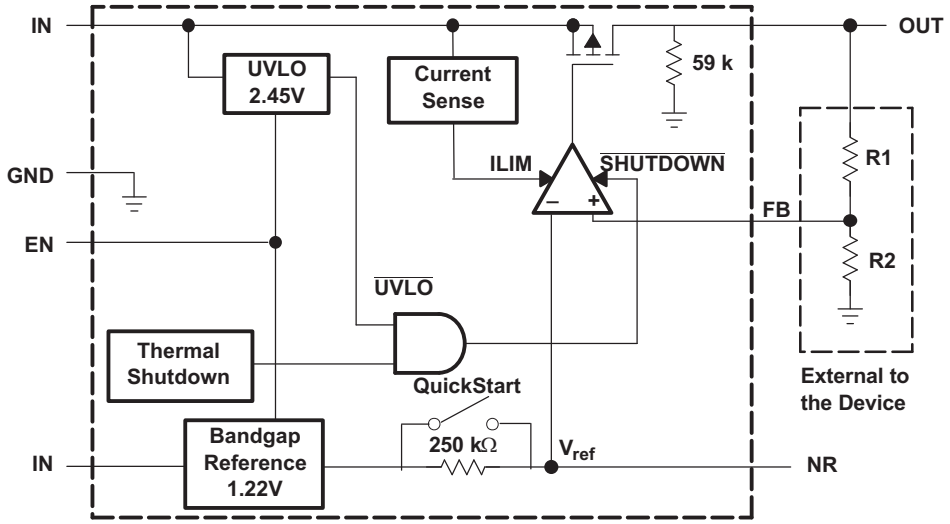


Figure 15. TPS730 Block Diagram (Adjustable-Voltage Version)

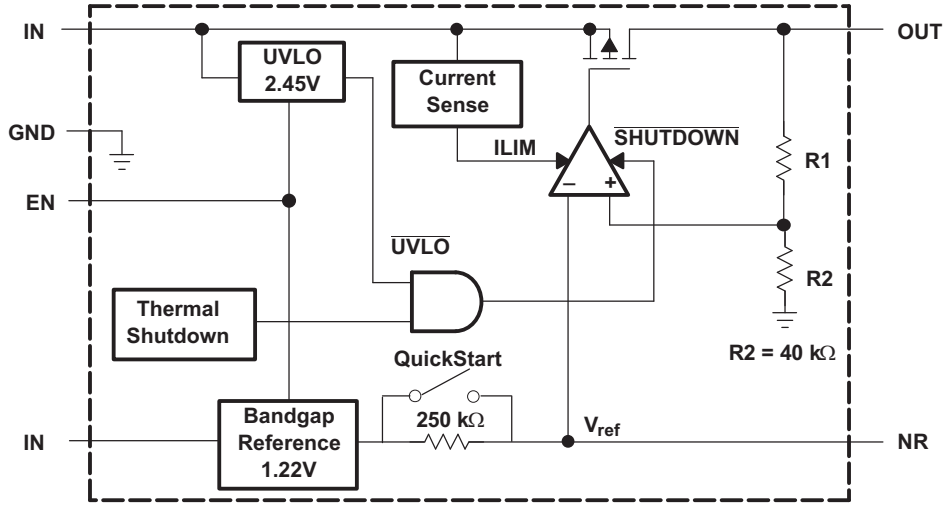


Figure 16. TPS730 Block Diagram (Fixed-Voltage Versions)

7.3 Feature Description

7.3.1 Undervoltage Lockout (UVLO)

The TPS730 uses an undervoltage lockout (UVLO) circuit that disables the output until the input voltage is greater than the rising UVLO voltage. This circuit ensures that the device does not exhibit any unpredictable behavior when the supply voltage is lower than the operational range of the internal circuitry, $V_{IN(min)}$.

7.3.2 Shutdown

The enable pin (EN) is active high. Enable the device by forcing the EN pin to exceed $V_{EN(high)}$ (1.7 V, minimum). Turn off the device by forcing the EN pin to drop below 0.7 V. If shutdown capability is not required, connect EN to IN.

7.3.3 Foldback Current Limit

The TPS730 features internal current limiting and thermal protection. During normal operation, the TPS730 limits output current to approximately 400 mA. When current limiting engages, the output voltage scales back linearly until the overcurrent condition ends. While current limiting is designed to prevent gross device failure, do not exceed the power dissipation ratings of the package or the absolute maximum voltage ratings of the device.

7.4 Device Functional Modes

7.4.1 Normal Operation

The device regulates to the nominal output voltage under the following conditions:

- The input voltage is at least as high as $V_{IN(min)}$.
- The input voltage is greater than the nominal output voltage added to the dropout voltage.
- The enable voltage is greater than $V_{EN(min)}$.
- The output current is less than the current limit.
- The device junction temperature is less than the maximum specified junction temperature.

7.4.2 Dropout Operation

If the input voltage is lower than the nominal output voltage plus the specified dropout voltage, but all other conditions are met for normal operation, the device operates in dropout mode. In this mode of operation, the output voltage is the same as the input voltage minus the dropout voltage. The transient performance of the device is significantly degraded because the pass device is in the linear region and no longer controls the current through the LDO. Line or load transients in dropout can result in large output voltage deviations.

7.4.3 Disabled

The device is disabled under the following conditions:

- The enable voltage is less than the enable falling threshold voltage or has not yet exceeded the enable rising threshold.
- The device junction temperature is greater than the thermal shutdown temperature.
- The input voltage is less than $UVLO_{falling}$.

Table 1 shows the conditions that lead to the different modes of operation.

Table 1. Device Functional Mode Comparison

OPERATING MODE	PARAMETER			
	V_{IN}	V_{EN}	I_{OUT}	T_J
Normal mode	$V_{IN} > V_{OUT(nom)} + V_{DO}$ and $V_{IN} > V_{IN(min)}$	$V_{EN} > V_{EN(high)}$	$I_{OUT} < I_{LIM}$	$T_J < 125°C$
Dropout mode	$V_{IN(min)} < V_{IN} < V_{OUT(nom)} + V_{DO}$	$V_{EN} > V_{EN(high)}$	—	$T_J < 125°C$
Disabled mode (any true condition disables the device)	$V_{IN} < UVLO_{falling}$	$V_{EN} < V_{EN(low)}$	—	$T_J > 165°C$ (1)

(1) Approximate value for thermal shutdown.

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The TPS730 family of low-dropout (LDO) regulators has been optimized for use in noise-sensitive battery-operated equipment. The device features extremely low dropout voltages, high PSRR, ultra-low output noise, low quiescent current (170 µA typically), and enable-input to reduce supply currents to less than 1 µA when the regulator is turned off.

8.1.1 Adjustable Operation

The output voltage of the TPS73001 adjustable regulator is programmed using an external resistor divider as shown in Figure 17. The output voltage is calculated using Equation 1:

$$V_{OUT} = V_{REF} \times \left(1 + \frac{R_1}{R_2}\right) \quad (1)$$

Where:

- V_{REF} = 1.225 V typical (the internal reference voltage)

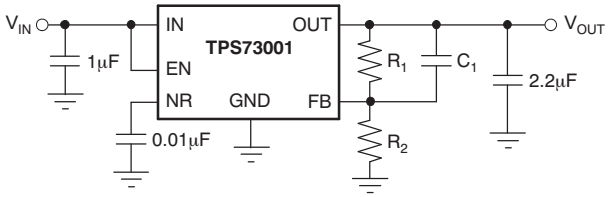
Resistors R_1 and R_2 should be chosen for approximately 50-µA divider current. Lower value resistors can be used for improved noise performance, but the solution consumes more power. Higher resistors values can cause accuracy issues and other problems. The recommended design procedure is to choose R_2 = 30.1 kΩ to set the divider current at 50 µA, C_1 = 15 pF for stability, and then calculate R_1 using Equation 2:

$$R_1 = \left(\frac{V_{OUT}}{V_{REF}} - 1\right) \times R_2 \quad (2)$$

To improve the stability of the adjustable version, TI suggests placing a small compensation capacitor between OUT and FB. For output voltages < 1.8 V, the value of this capacitor should be 100 pF. For output voltages > 1.8 V, use Equation 3 to calculate the approximate value of this capacitor.

$$C_1 = \frac{(3 \times 10^{-7}) \times (R_1 + R_2)}{(R_1 \times R_2)} \quad (3)$$

Figure 17 shows the suggested value of this capacitor for several resistor ratios. If this capacitor is not used (such as in a unity-gain configuration) or if an output voltage < 1.8 V is chosen, then the minimum recommended output capacitor is 4.7 µF instead of 2.2 µF.



OUTPUT VOLTAGE PROGRAMMING GUIDE

OUTPUT VOLTAGE	R_1	R_2	C_1
1.22V	short	open	0pF
2.5V	31.6kΩ	30.1kΩ	22pF
3.3V	51kΩ	30.1kΩ	15pF
3.6V	59kΩ	30.1kΩ	15pF

Figure 17. TPS73001 Adjustable LDO Regulator Programming

Application Information (continued)

8.1.2 Capacitor Recommendations

Low equivalent series resistance (ESR) capacitors should be used for the input, output, noise reduction, and bypass capacitors. Ceramic capacitors with X7R and X5R dielectrics are preferred. These dielectrics offer more stable characteristics. Ceramic X7R capacitors offer improved overtemperature performance, while ceramic X5R capacitors are more cost-effective and are available in higher values.

8.1.3 Input and Output Capacitor Requirements

A 0.1-µF or larger ceramic input bypass capacitor, connected between IN and GND and located close to the TPS730, is required for stability and improves transient response, noise rejection, and ripple rejection. A higher-value input capacitor may be necessary if large, fast-rise-time load transients are anticipated or the device is located several inches from the power source.

Like most low-dropout regulators, the TPS730 requires an output capacitor connected between OUT and GND to stabilize the internal control loop. The minimum recommended capacitance is 2.2 µF. Any 2.2-µF or larger ceramic capacitor is suitable, provided the capacitance does not vary significantly over temperature. If load current is not expected to exceed 100 mA, a 1-µF ceramic capacitor can be used. If a feed-forward capacitor is not used (such as in a unity-gain configuration) or if an output voltage less than 1.8 V is chosen, then the minimum recommended output capacitor is 4.7 µF instead of 2.2 µF. Table 2 lists the recommended output capacitor sizes for several common configurations.

Table 2. Output Capacitor Sizing

CONDITION	C_{OUT} (µF)
V_{OUT} < 1.8 V or C_{FF} = 0 nF	4.7
V_{OUT} > 1.8 V, I_{OUT} > 100 mA	2.2
V_{OUT} > 1.8 V, I_{OUT} < 100 mA	1

8.1.4 Noise Reduction and Feed-Forward Capacitor Requirements

The internal voltage reference is a key source of noise in an LDO regulator. The TPS730 has an NR pin which is connected to the voltage reference through a 250-kΩ internal resistor. The 250-kΩ internal resistor, in conjunction with an external bypass capacitor connected to the NR pin, creates a low-pass filter to reduce the voltage reference noise and, therefore, the noise at the regulator output. In order for the regulator to operate properly, the current flow out of the NR pin must be at a minimum, because any leakage current creates an IR drop across the internal resistor thus creating an output error. Therefore, the bypass capacitor must have minimal leakage current. The bypass capacitor should be no more than 0.1 µF to ensure that it is fully charged during the quick-start time provided by the internal switch shown in the *Functional Block Diagram* section.

As an example, the TPS73018 exhibits only 33 μV_{RMS} of output voltage noise using a 0.01-µF ceramic bypass capacitor and a 2.2-µF ceramic output capacitor. Note that the output starts up slower as the bypass capacitance increases due to the RC time constant at the NR pin that is created by the internal 250-kΩ resistor and external capacitor.

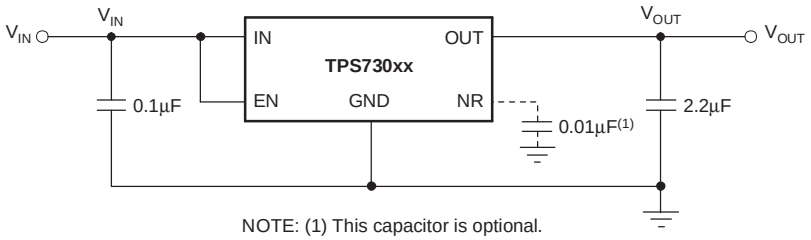
A feed-forward capacitor is recommended to improve the stability of the device. If R_2 = 30.1 kΩ, set C_1 to 15 pF for optimal performance. For voltages less than 1.8 V, the value of this capacitor should be 100 pF. For voltages greater than 1.8 V, the approximate value of this capacitor can be calculated as shown in Equation 3.

8.1.5 Reverse Current Operation

The TPS730 PMOS-pass transistor has a built-in back diode that conducts reverse current when the input voltage drops below the output voltage (for example, during power-down). Current is conducted from the output to the input and is not internally limited. If extended reverse voltage operation is anticipated, external limiting might be appropriate. If extended reverse voltage operation in anticipated, external limiting to 5% of the rated output current is recommended.

8.2 Typical Application

A typical application circuit is shown in Figure 18.



NOTE: (1) This capacitor is optional.

Figure 18. Typical Application Circuit

8.2.1 Design Requirements

Table 3 lists the design requirements.

Table 3. Design Parameters

PARAMETER	DESIGN REQUIREMENT
Input voltage	4.2 V to 3 V (Lithium Ion battery)
Output voltage	1.8 V, ±1%
DC output current	10 mA
Peak output current	75 mA
Maximum ambient temperature	65°C

8.2.2 Detailed Design Procedure

Pick the desired output voltage option. An input capacitor of 0.1 µF is used as the battery is connected to the input through a via and a short 10-mil (0.01-in) trace. An output capacitor of 10 µF is used to provide optimal response time for the load transient. Verify that the maximum junction temperature is not exceed by referring to Figure 24.

8.2.3 Application Curves

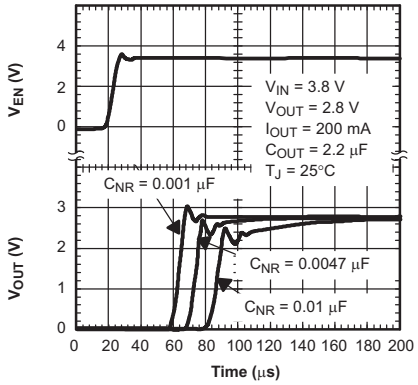


Figure 19. TPS73028 Output Voltage, Enable Voltage vs Time (Start-Up)

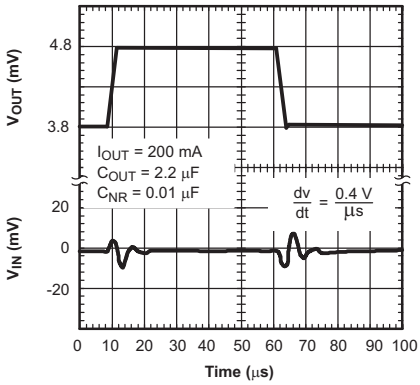


Figure 20. TPS73028 Line Transient Response

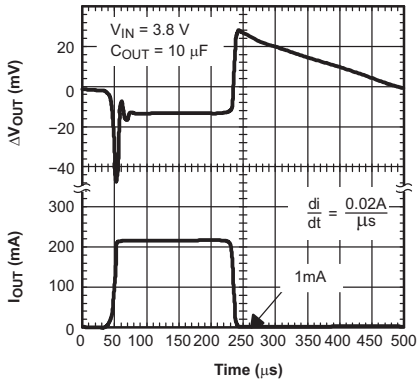


Figure 21. TPS73028 Load Transient Response

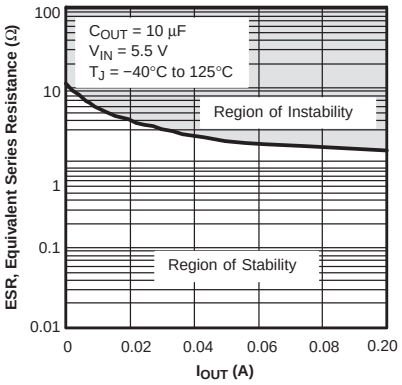


Figure 22. Typical Regions of Stability Equivalent Series Resistance (ESR) vs Output Current

8.3 Do's and Don'ts

Do place at least one, low-ESR, 2.2-µF capacitor as close as possible between the OUT pin of the regulator and the GND pin.

Do place at least one, low-ESR, 0.1-µF capacitor as close as possible between the IN pin of the regulator and the GND pin.

Do provide adequate thermal paths away from the device.

Do not place the input or output capacitor more than 10 mm away from the regulator.

Do not exceed the absolute maximum ratings.

Do not float the Enable (EN) pin.

Do not resistively or inductively load the NR pin.

Do not let the output voltage get more than 0.3 V above the input voltage.

9 Power Supply Recommendations

These devices are designed to operate from an input voltage supply range from 2.7 V to 5.5 V. The input voltage range must provide adequate headroom in order for the device to have a regulated output. This input supply must be well-regulated and stable. A 0.1-µF input capacitor is required for stability; if the input supply is noisy, additional input capacitors with low ESR can help improve the output noise performance.

10 Layout

10.1 Layout Guidelines

Layout is a critical part of good power-supply design. There are several signal paths that conduct fast-changing currents or voltages that can interact with stray inductance or parasitic capacitance to generate noise or degrade the power-supply performance. To help eliminate these problems, the IN pin should be bypassed to ground with a low ESR ceramic bypass capacitor with an X5R or X7R dielectric.

Equivalent series inductance (ESL) and equivalent series resistance (ESR) must be minimized to maximize performance and ensure stability. Every capacitor (C_{IN}, C_{OUT}, $C_{NR/SS}$, C_{FF}) must be placed as close as possible to the device and on the same side of the PCB as the regulator itself.

Do not place any of the capacitors on the opposite side of the PCB from where the regulator is installed. The use of vias and long traces is strongly discouraged because these circuits may impact system performance negatively, and even cause instability.

10.1.1 Board Layout Recommendations to Improve PSRR and Noise Performance

To improve AC measurements like PSRR, output noise, and transient response, TI recommends designing the board with separate ground planes for V_{IN} and V_{OUT}, with each ground plane connected only at the GND pin of the device. In addition, the ground connection for the bypass capacitor should connect directly to the GND pin of the device.

10.2 Layout Example

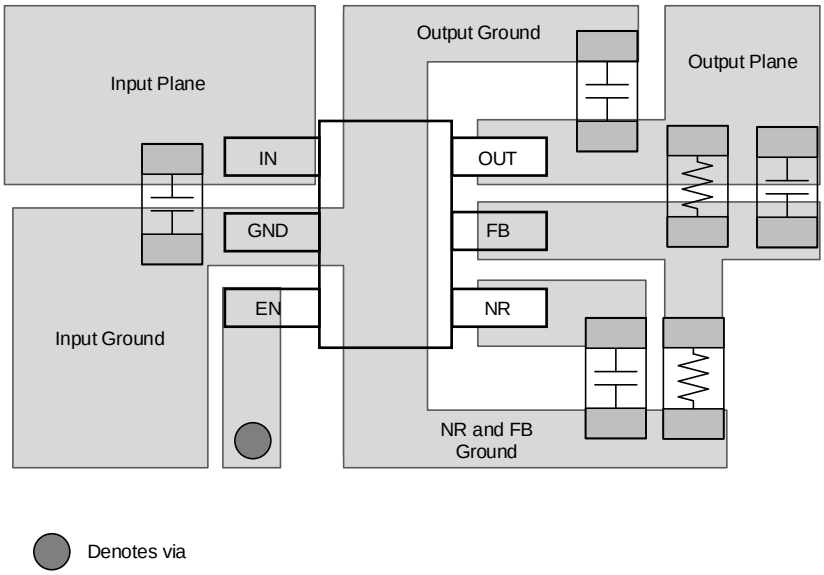


Figure 23. Layout Example (DBV Package)

10.3 Thermal Considerations

Thermal protection disables the output when the junction temperature rises to approximately 165°C, allowing the device to cool. When the junction temperature cools to approximately 140°C, the output circuitry is again enabled. Depending on power dissipation, thermal resistance, and ambient temperature, the thermal protection circuit may cycle on and off. This cycling limits regulator dissipation, protecting the device from damage as a result of overheating.

Any tendency to activate the thermal protection circuit indicates excessive power dissipation or an inadequate heatsink. For reliable operation, junction temperature must be limited to 125°C maximum. To estimate the margin of safety in a complete design (including heatsink), increase the ambient temperature until the thermal protection is triggered; use worst-case loads and signal conditions.

The TPS730 internal protection circuitry is designed to protect against overload conditions. This circuitry is not intended to replace proper heatsinking. Continuously running the TPS730 into thermal shutdown degrades device reliability.

10.4 Power Dissipation

Specified regulator operation is assured to a junction temperature of +125°C; the maximum junction temperature should be restricted to +125°C under normal operating conditions. This restriction limits the power dissipation the regulator can handle in any given application. To ensure the junction temperature is within acceptable limits, calculate the maximum allowable dissipation, $P_{D(max)}$, and the actual dissipation, P_D, which must be less than or equal to $P_{D(max)}$.

The maximum power dissipation limit is determined using Equation 4:

$$P_{D(max)} = \frac{T_J max - T_A}{R_{\Theta JA}} \quad (4)$$

Where:

- $T_J$max is the maximum allowable junction temperature.
- $R_{\theta JA}$ is the thermal resistance junction-to-ambient for the package (see the *Thermal Information* table).
- T_A is the ambient temperature.

The regulator dissipation is calculated using Equation 5:

$$P_D = (V_{IN} - V_{OUT}) \times I_{OUT} \quad (5)$$

Power dissipation resulting from quiescent current is negligible. Excessive power dissipation triggers the thermal protection circuit.

Figure 24 shows the maximum ambient temperature versus the power dissipation of the TPS730. This figure assumes the device is soldered on a JEDEC standard, high-K layout with no airflow over the board. Actual board thermal impedances vary widely. If the application requires high power dissipation, having a thorough understanding of the board temperature and thermal impedances is helpful to ensure the TPS730 does not operate above a junction temperature of 125°C.

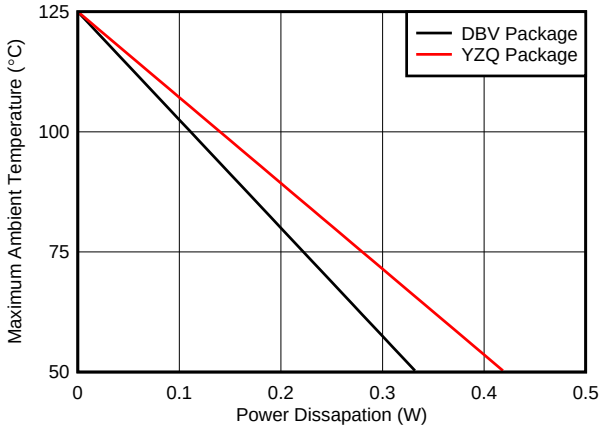


Figure 24. Maximum Ambient Temperature vs Power Dissipation

Power Dissipation (continued)

Estimating the junction temperature can be done by using the thermal metrics Ψ_{JT} and Ψ_{JB}, shown in the *Thermal Information* table. These metrics are a more accurate representation of the heat transfer characteristics of the die and the package than $R_{\theta JA}$. The junction temperature can be estimated with Equation 6.

$$\Psi_{JT}: \quad T_J = T_T + \Psi_{JT} \bullet P_D$$

$$\Psi_{JB}: \quad T_J = T_B + \Psi_{JB} \bullet P_D \tag{6}$$

where

- P_D is the power dissipation shown by Equation 5,
- T_T is the temperature at the center-top of the IC package,
- T_B is the PCB temperature measured 1 mm away from the IC package *on the PCB surface*.

NOTE

Both T_T and T_B can be measured on actual application boards using a thermo-gun (an infrared thermometer).

For more information about measuring T_T and T_B, see the application note *Using New Thermal Metrics* (SBVA025), available for download at www.ti.com.

11 Device and Documentation Support

11.1 Device Support

11.1.1 Development Support

11.1.1.1 Spice Models

Computer simulation of circuit performance using SPICE is often useful when analyzing the performance of analog circuits and systems. A SPICE model for the TPS730 is available through the product folders under *Tools & Software*.

11.1.2 Device Nomenclature

Table 4. Ordering Information(1)(2)

PRODUCT	V_{OUT}
TPS730**xxyyy***z*	**XX(X)** is the nominal output voltage (for example, 28 = 2.8 V; 285 = 2.85 V; 01 = adjustable version). **YYY** is the package designator. **Z** is the package quantity. R is for reel (3000 pieces), T is for tape (250 pieces).

(1) For the most current package and ordering information see the Package Option Addendum at the end of this document, or visit the device product folder on www.ti.com.
(2) Output voltages from 1.2 V to 4.8 V in 50-mV increments are available. Contact the factory for details and availability.

11.2 Documentation Support

11.2.1 Related Documentation

- *Using New Thermal Metrics*, SBVA025
- *Pros and Cons of Using a Feedforward Capacitor with a Low-Dropout Regulator*, SBVA042

11.3 Trademarks

NanoStar is a trademark of Texas Instruments.
Bluetooth is a registered trademark of Bluetooth Sig, Inc.
All other trademarks are the property of their respective owners.

11.4 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.5 Glossary

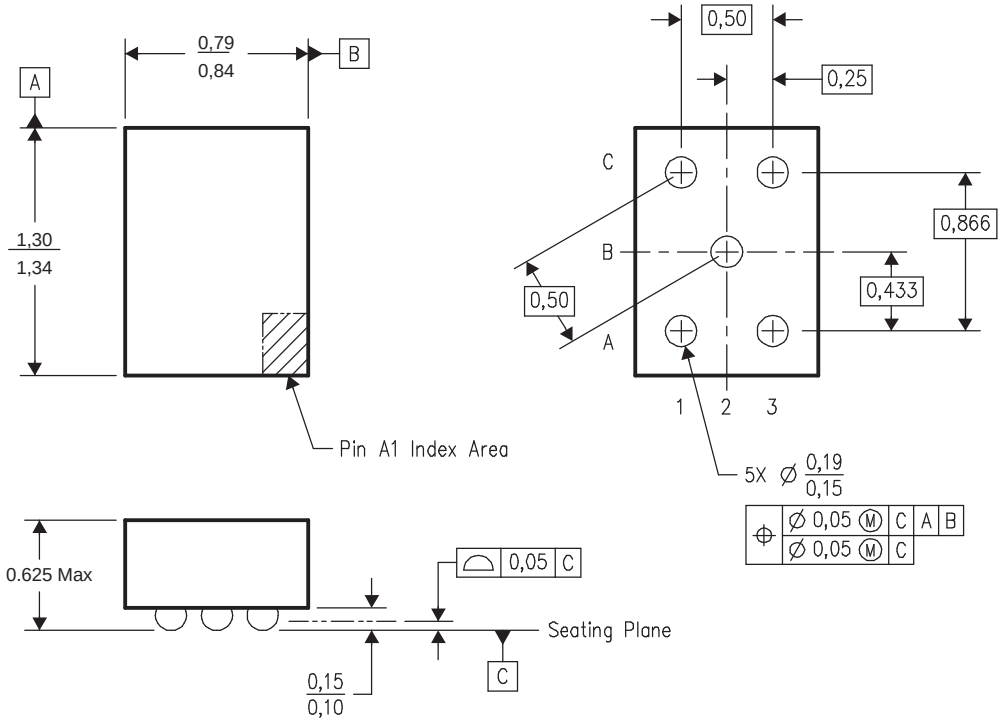
SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

12.1 TPS730YZQ Nanostar™ Wafer Chip Scale Information



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. NanoStar™ package configuration.
D. This package is tin-lead (SnPb); consult the factory for availability of lead-free material.

NanoStar is a trademark of Texas Instruments.

Figure 25. Nanostar™ Wafer Chip Scale Package

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS73001DBVR	ACTIVE	SOT-23	DBV	6	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	PGVI	Samples
TPS73001DBVRG4	ACTIVE	SOT-23	DBV	6	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	PGVI	Samples
TPS73001DBVT	ACTIVE	SOT-23	DBV	6	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	PGVI	Samples
TPS73001DBVTG4	ACTIVE	SOT-23	DBV	6	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	PGVI	Samples
TPS73018DBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	PHHI	Samples
TPS73018DBVRG4	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	PHHI	Samples
TPS73018DBVT	ACTIVE	SOT-23	DBV	5	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	PHHI	Samples
TPS73018DBVTG4	ACTIVE	SOT-23	DBV	5	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	PHHI	Samples
TPS73025DBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	PGWI	Samples
TPS73025DBVRG4	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	PGWI	Samples
TPS73025DBVT	LIFEBUY	SOT-23	DBV	5	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	PGWI	
TPS73025DBVTG4	LIFEBUY	SOT-23	DBV	5	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	PGWI	
TPS730285DBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	PHII	Samples
TPS730285DBVT	LIFEBUY	SOT-23	DBV	5	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	PHII	
TPS73028DBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	PGXI	Samples
TPS73028DBVRG4	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	PGXI	Samples
TPS73028DBVT	LIFEBUY	SOT-23	DBV	5	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	PGXI	
TPS73028DBVTG4	LIFEBUY	SOT-23	DBV	5	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	PGXI	
TPS73028YZQT	LIFEBUY	DSBGA	YZQ	5	250	TBD	Call TI	Call TI	-40 to 125	E2	
TPS73030DBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	PGYI	Samples
TPS73033DBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	PHUI	Samples
TPS73033DBVRG4	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	PHUI	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS73033DBVT	ACTIVE	SOT-23	DBV	5	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	PHUI	Samples
TPS73033DBVTG4	ACTIVE	SOT-23	DBV	5	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	PHUI	Samples
TPS73047DBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	PETI	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

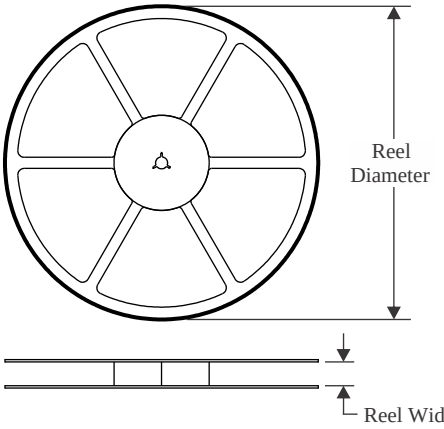
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

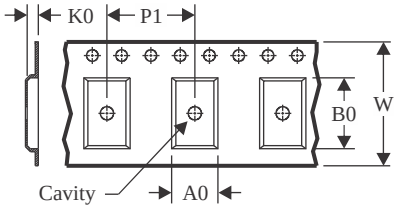
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

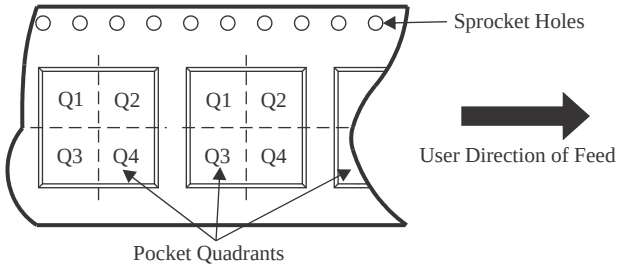


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

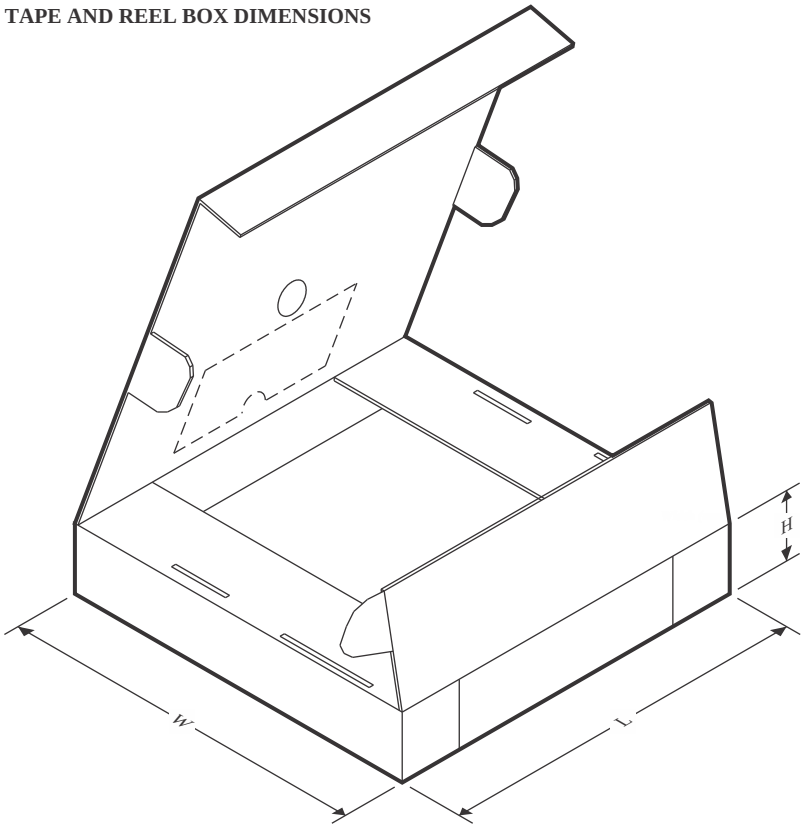
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS73001DBVR	SOT-23	DBV	6	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS73001DBVR	SOT-23	DBV	6	3000	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS73001DBVT	SOT-23	DBV	6	250	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS73018DBVR	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS73018DBVT	SOT-23	DBV	5	250	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS73025DBVR	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS73025DBVT	SOT-23	DBV	5	250	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS730285DBVR	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS730285DBVT	SOT-23	DBV	5	250	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS73028DBVR	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS73028DBVT	SOT-23	DBV	5	250	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS73030DBVR	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS73033DBVR	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS73047DBVR	SOT-23	DBV	5	3000	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3

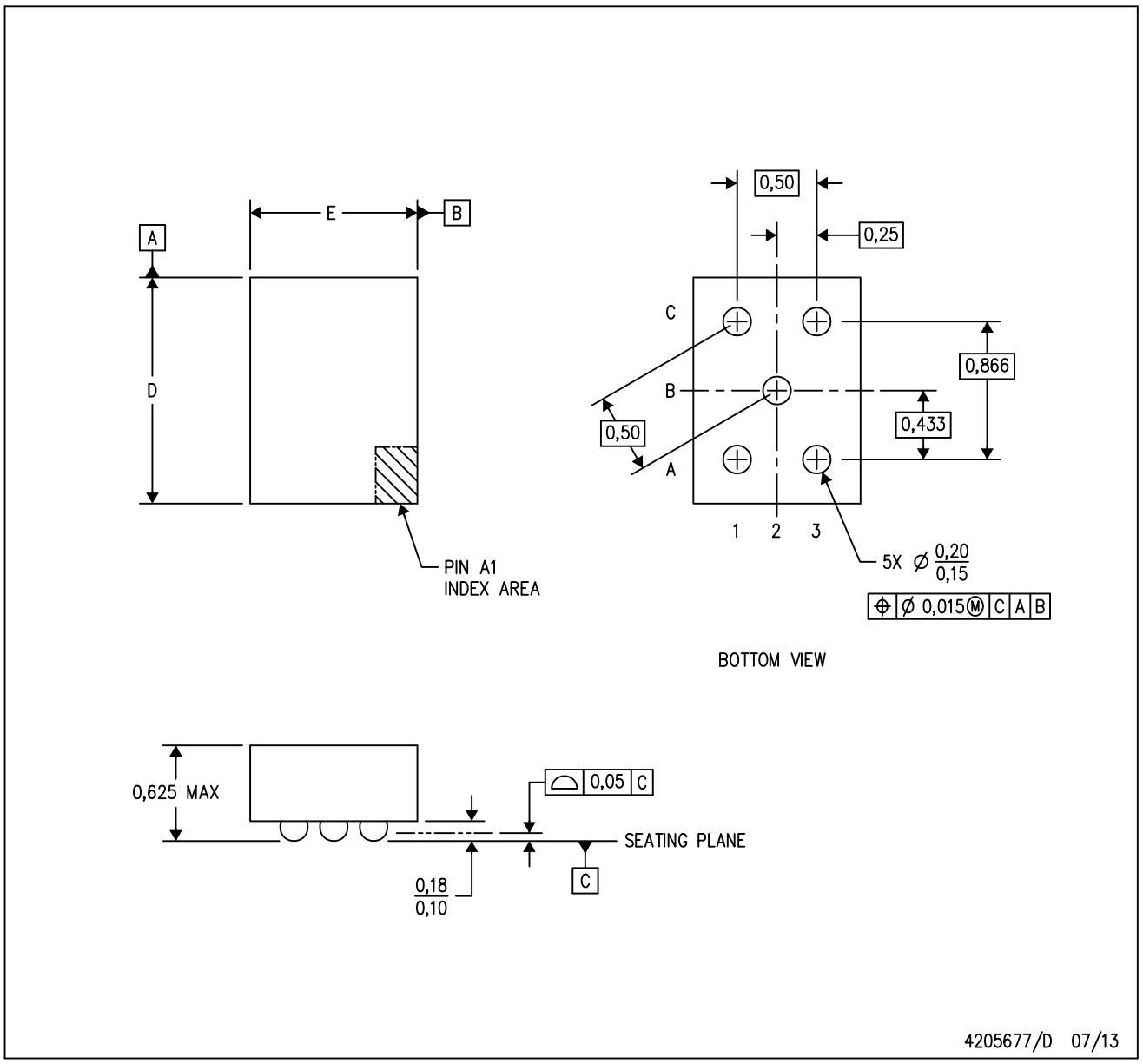
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS73001DBVR	SOT-23	DBV	6	3000	180.0	180.0	18.0
TPS73001DBVR	SOT-23	DBV	6	3000	200.0	183.0	25.0
TPS73001DBVT	SOT-23	DBV	6	250	180.0	180.0	18.0
TPS73018DBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
TPS73018DBVT	SOT-23	DBV	5	250	180.0	180.0	18.0
TPS73025DBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
TPS73025DBVT	SOT-23	DBV	5	250	180.0	180.0	18.0
TPS730285DBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
TPS730285DBVT	SOT-23	DBV	5	250	180.0	180.0	18.0
TPS73028DBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
TPS73028DBVT	SOT-23	DBV	5	250	180.0	180.0	18.0
TPS73030DBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
TPS73033DBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
TPS73047DBVR	SOT-23	DBV	5	3000	200.0	183.0	25.0

YZQ (R–XBGA–N5) DIE–SIZE BALL GRID ARRAY



Notes: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. NanoFree ™ package configuration.

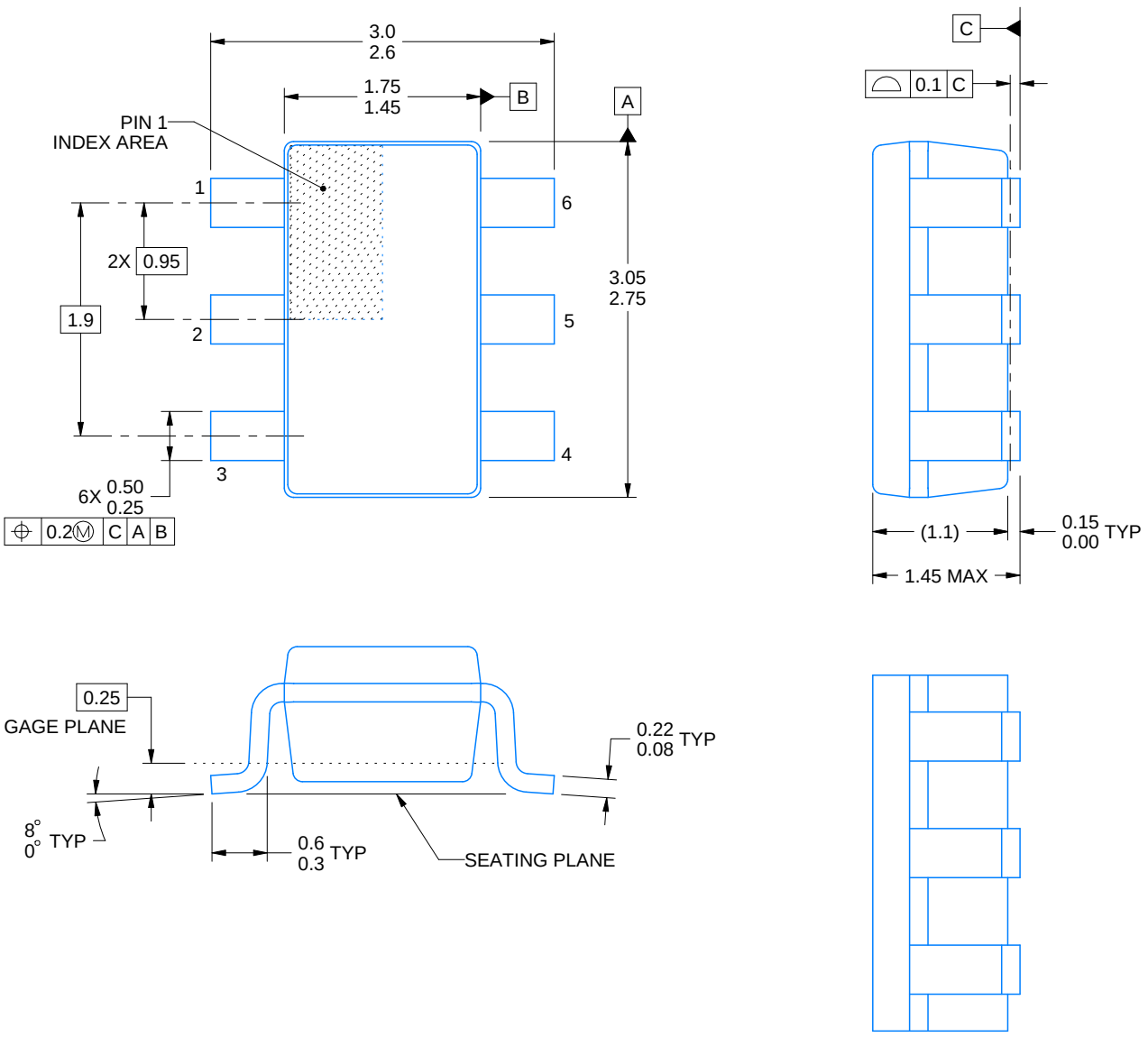
NanoFree is a trademark of Texas Instruments.

PACKAGE OUTLINE

DBV0006A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR

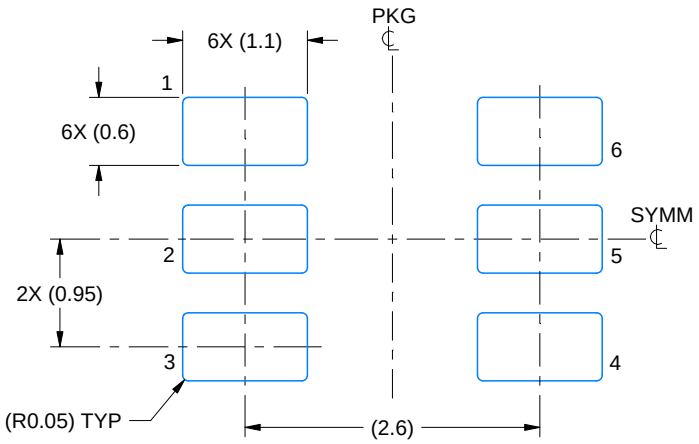


ALTERNATIVE PACKAGE SINGULATION VIEW

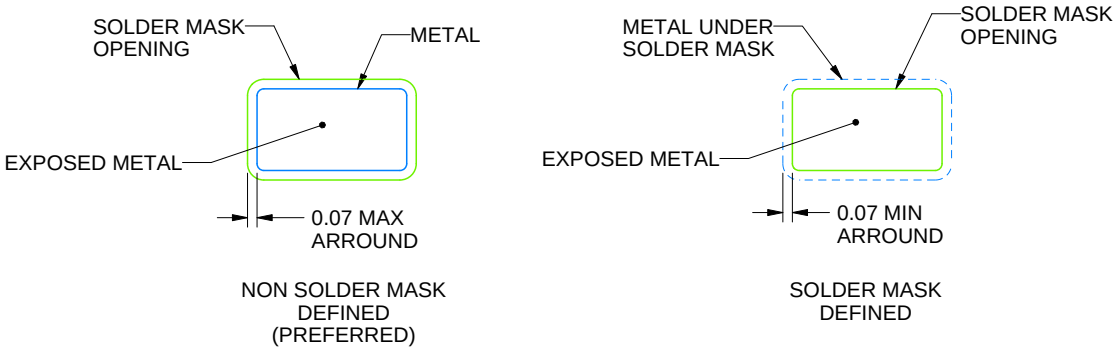
4214840/E 02/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.25 per side.
4. Leads 1,2,3 may be wider than leads 4,5,6 for package orientation.
5. Refernce JEDEC MO-178.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

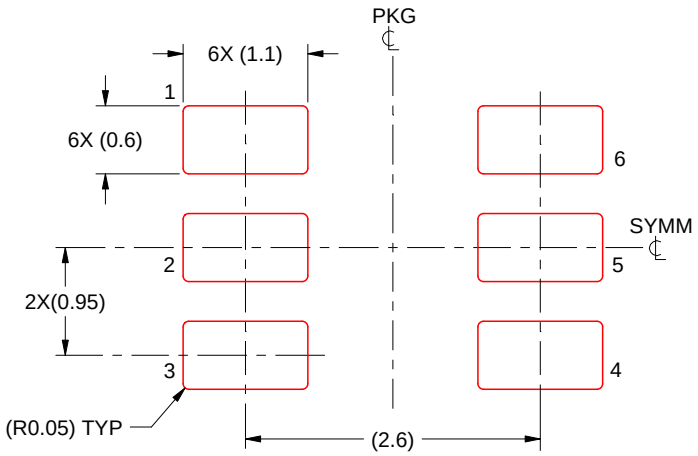


SOLDER MASK DETAILS

4214840/E 02/2024

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214840/E 02/2024

NOTES: (continued)

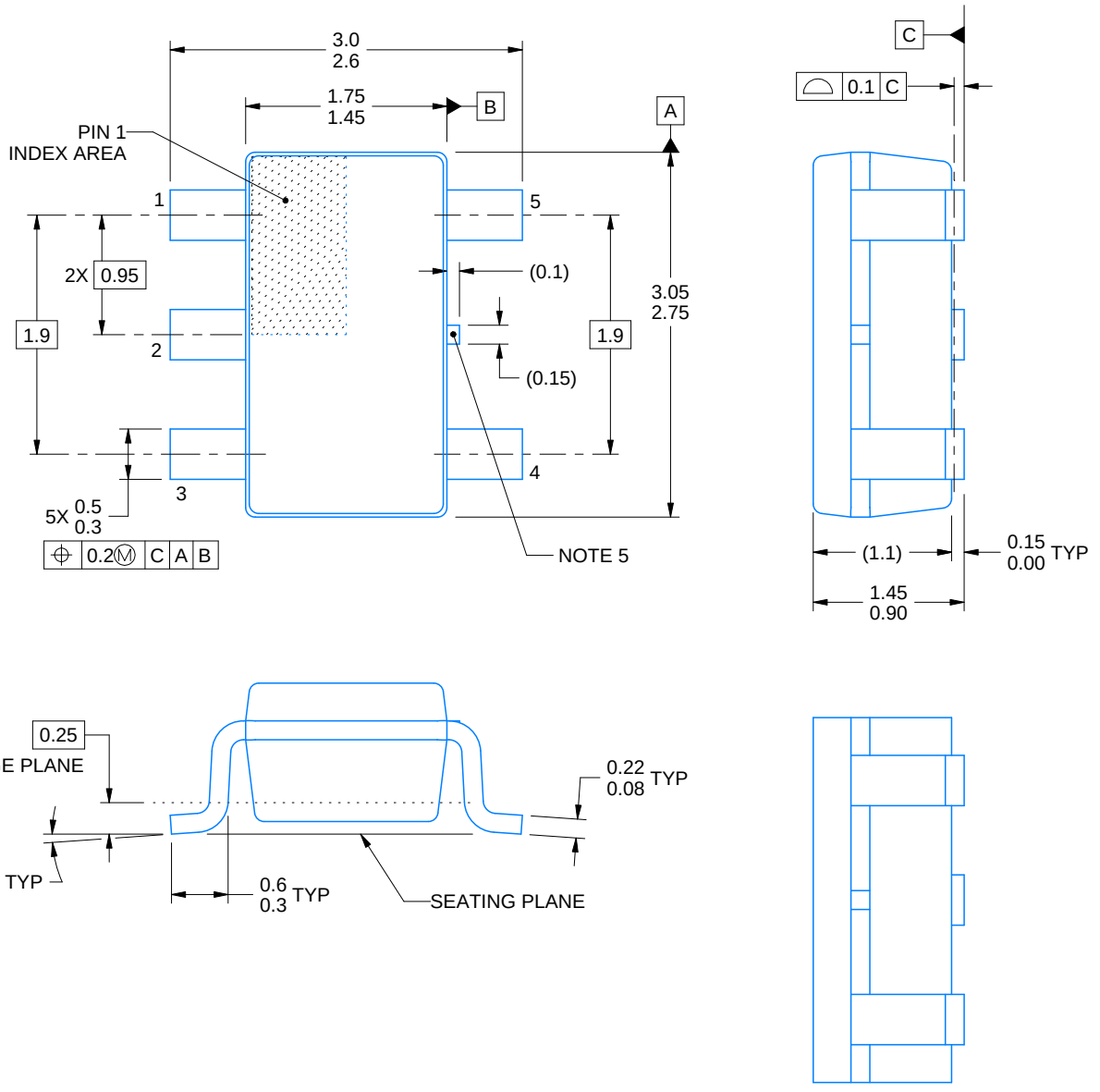
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR

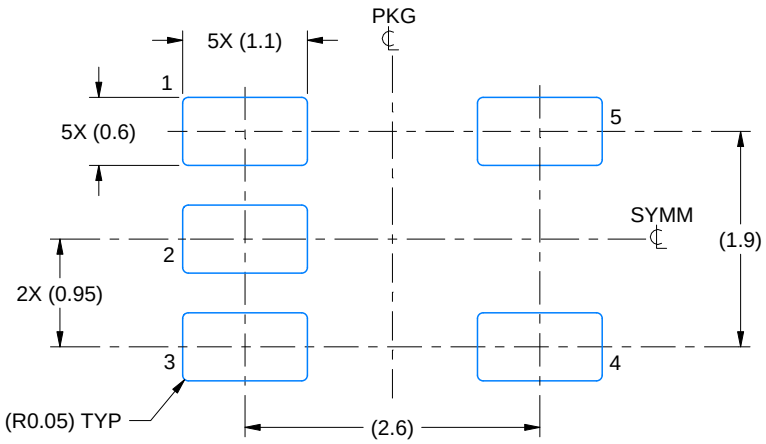


ALTERNATIVE PACKAGE SINGULATION VIEW

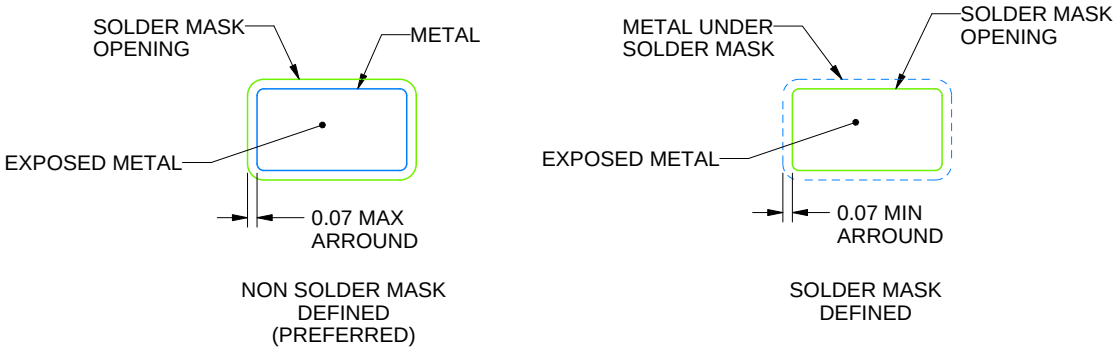
4214839/J 02/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.
5. Support pin may differ or may not be present.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

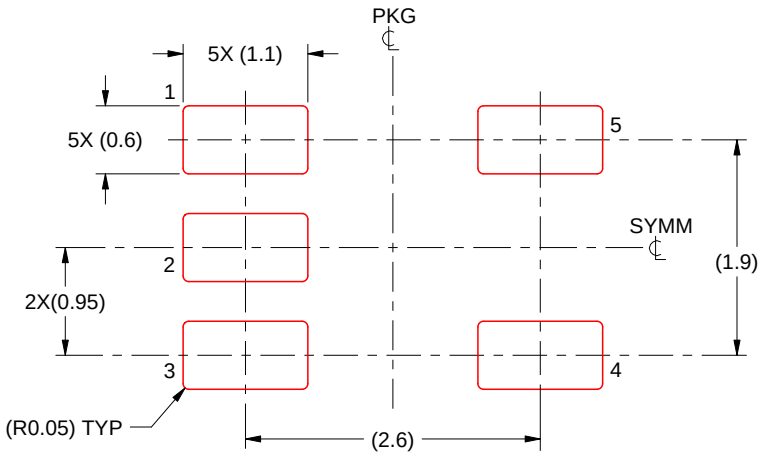


SOLDER MASK DETAILS

4214839/J 02/2024

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/J 02/2024

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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