250mA, Low Quiescent Current, Ultra-Low Noise, High PSRR
Low-Dropout Linear Regulator

FEATURES
- 250mA Low Dropout Regulator with EN
- Low \( I_0 \): 44\( \mu \)A
- Multiple Output Voltage Versions Available:
  - Fixed Outputs of 1.0V to 4.3V Using
    Innovative Factory EEPROM Programming
  - Adjustable Outputs from 1.25V to 6.2V
- High PSRR: 60dB at 1kHz
- Ultra-low Noise: 28\( \mu \)VRMS
- Fast Start-Up Time: 45\( \mu \)s
- Stable with a Low-ESR, 2.0\( \mu \)F Typical Output Capacitance
- Excellent Load/Line Transient Response
- 2% Overall Accuracy (Load/Line/Temp)
- Very Low Dropout: 125mV at 250mA
- ThinSOT-23, 2mm × 2mm SON-6, and 3mm × 3mm SON-8 Packages

APPLICATIONS
- WiFi, WiMax
- Printers
- Cellular Phones, SmartPhones
- Handheld Organizers, PDAs

DESCRIPTION
The TPS734xx family of low-dropout (LDO), low-power linear regulators offers excellent ac performance with very low ground current. High power-supply rejection ratio (PSRR), low noise, fast start-up, and excellent line and load transient response are provided while consuming a very low 44\( \mu \)A (typical) ground current. The TPS734xx is stable with ceramic capacitors and uses an advanced BiCMOS fabrication process to yield a typical dropout voltage of 125mV at 250mA output. The TPS734xx uses a precision voltage reference and feedback loop to achieve overall accuracy of 2% over all load, line, process, and temperature variations. It is fully specified from \( T_J = -40^\circ C \) to \(+125^\circ C \) and is offered in low-profile ThinSOT-23, 2mm × 2mm SON, and 3mm × 3mm SON packages that are ideal for wireless handsets, printers, and WLAN cards.

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

All trademarks are the property of their respective owners.
This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

### ORDERING INFORMATION\(^{(1)}\)

<table>
<thead>
<tr>
<th>PRODUCT</th>
<th>V(_{\text{OUT}})(^{(2)})</th>
</tr>
</thead>
<tbody>
<tr>
<td>TPS734xxxyyz</td>
<td>XXX is nominal output voltage (for example, 28 = 2.8V, 285 = 2.85V, 01 = Adjustable). YYY is package designator. Z is package quantity.</td>
</tr>
</tbody>
</table>

\(^{(1)}\) For the most current package and ordering information see the Package Option Addendum at the end of this document, or see the TI website at [www.ti.com](http://www.ti.com).

\(^{(2)}\) Output voltages from 1.0V to 3.6V in 50mV increments are available through the use of innovative factory EEPROM programming; minimum order quantities may apply. Contact factory for details and availability.

### ABSOLUTE MAXIMUM RATINGS\(^{(1)}\)

Over operating temperature range (unless otherwise noted).

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TPS734xx</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>V(_{\text{IN}}) range</td>
<td>(-0.3) to (+7.0)</td>
<td>V</td>
</tr>
<tr>
<td>V(_{\text{EN}}) range</td>
<td>(-0.3) to V(_{\text{IN}}) +0.3</td>
<td>V</td>
</tr>
<tr>
<td>V(_{\text{OUT}}) range</td>
<td>(-0.3) to V(_{\text{IN}}) +0.3</td>
<td>V</td>
</tr>
<tr>
<td>V(_{\text{FB}}) range</td>
<td>(-0.3) to V(_{\text{FB}}) (TYP) +0.3</td>
<td>V</td>
</tr>
<tr>
<td>Peak output current</td>
<td>Internally limited</td>
<td></td>
</tr>
<tr>
<td>Continuous total power dissipation</td>
<td>See Dissipation Ratings Table</td>
<td></td>
</tr>
<tr>
<td>Junction temperature range, T(_{\text{J}})</td>
<td>(-55) to (+150)</td>
<td>°C</td>
</tr>
<tr>
<td>Storage junction temperature range, T(_{\text{STG}})</td>
<td>(-55) to (+150)</td>
<td>°C</td>
</tr>
<tr>
<td>ESD rating, HBM</td>
<td>2</td>
<td>kV</td>
</tr>
<tr>
<td>ESD rating, CDM</td>
<td>500</td>
<td>V</td>
</tr>
</tbody>
</table>

\(^{(1)}\) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not implied.

### DISSIPATION RATINGS

<table>
<thead>
<tr>
<th>BOARD</th>
<th>PACKAGE</th>
<th>(R(_{\text{HJC}}))</th>
<th>(R(_{\text{HJA}}))</th>
<th>DERATING FACTOR ABOVE (T(_{\text{A}}) = +25°C)</th>
<th>(T(_{\text{A}}) = +25°C)</th>
<th>(T(_{\text{A}}) = +70°C)</th>
<th>(T(_{\text{A}}) = +85°C)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Low-K(^{(1)})</td>
<td>DDC</td>
<td>90°C/W</td>
<td>280°C/W</td>
<td>3.6mW/°C</td>
<td>360mW</td>
<td>200mW</td>
<td>145mW</td>
</tr>
<tr>
<td>High-K(^{(2)})</td>
<td>DDC</td>
<td>90°C/W</td>
<td>200°C/W</td>
<td>5.0mW/°C</td>
<td>500mW</td>
<td>275mW</td>
<td>200mW</td>
</tr>
<tr>
<td>Low-K(^{(1)})</td>
<td>DRV</td>
<td>20°C/W</td>
<td>140°C/W</td>
<td>7.1mW/°C</td>
<td>715mW</td>
<td>395mW</td>
<td>285mW</td>
</tr>
<tr>
<td>High-K(^{(2)})</td>
<td>DRV</td>
<td>20°C/W</td>
<td>65°C/W</td>
<td>15.4mW/°C</td>
<td>1.54W</td>
<td>845mW</td>
<td>615mW</td>
</tr>
</tbody>
</table>

\(^{(1)}\) The JEDEC low-K (1s) board used to derive this data was a 3in \(\times\) 3in (7.62cm \(\times\) 7.62cm), two-layer board with 2-ounce (56,699g) copper traces on top of the board.

\(^{(2)}\) The JEDEC high-K (2s2p) board used to derive this data was a 3in \(\times\) 3in (7.62cm \(\times\) 7.62cm), multilayer board with 1-ounce (28,35g) internal power and ground planes and 2-ounce (56,699g) copper traces on top and bottom of the board.
ELECTRICAL CHARACTERISTICS

Over operating temperature range (\(T_J = -40^\circ\text{C}\) to \(+125^\circ\text{C}\)), \(V_{IN} = V_{OUT} + 0.3\) or \(2.7\) V, whichever is greater; \(I_{OUT} = 1\) mA, \(V_{EN} = V_{IN}\), \(C_{OUT} = 2.2\mu F\), \(C_{NR} = 0.01\mu F\), unless otherwise noted. For TPS73401, \(V_{OUT} = 3.0\) V.

Typical values are at \(T_J = +25^\circ\text{C}\).

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>(V_{IN})</td>
<td>Input voltage range(^{(1)})</td>
<td>2.7</td>
<td>6.5</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>(V_{FB})</td>
<td>Internal reference (TPS73401)</td>
<td>1.184</td>
<td>1.208</td>
<td>1.232</td>
<td>V</td>
</tr>
<tr>
<td>(V_{OUT})</td>
<td>Output voltage range (TPS73401)</td>
<td>(V_{FB})</td>
<td>6.3</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>(V_{OUT})</td>
<td>Output accuracy Nominal</td>
<td>(T_J = +25^\circ\text{C})</td>
<td>(-1.0)</td>
<td>(+1.0)</td>
<td>%</td>
</tr>
<tr>
<td>(V_{OUT})</td>
<td>Output accuracy(^{(1)}) Over (V_{IN}, I_{OUT}), Temp</td>
<td>(V_{OUT} + 0.3) V (\leq V_{IN} \leq 6.5) V (1) mA (\leq I_{OUT} \leq 250) mA</td>
<td>(-2.0)</td>
<td>(\pm 1.0)</td>
<td>(\pm 2.0)</td>
</tr>
<tr>
<td>(\Delta V_{OUT}/\Delta V_{IN})</td>
<td>Line regulation(^{(1)}) (V_{OUT} + 0.3) V (\leq V_{IN} \leq 6.5) V</td>
<td>0.02</td>
<td>%/V</td>
<td></td>
<td></td>
</tr>
<tr>
<td>(\Delta V_{OUT}/\Delta I_{OUT})</td>
<td>Load regulation (500\mu\text{A} \leq I_{OUT} \leq 250) mA</td>
<td>0.005</td>
<td>%/mA</td>
<td></td>
<td></td>
</tr>
<tr>
<td>(V_{DO})</td>
<td>Dropout voltage(^{(2)}) (V_{IN} = V_{OUT} + 0.1) V (I_{OUT} = 250) mA</td>
<td>125</td>
<td>219</td>
<td>mV</td>
<td></td>
</tr>
<tr>
<td>(I_{CL})</td>
<td>Output current limit (V_{OUT} = 0.9 \times V_{OUT(NOM)})</td>
<td>300</td>
<td>580</td>
<td>900</td>
<td>mA</td>
</tr>
<tr>
<td>(I_{GND})</td>
<td>Ground pin current (500\mu\text{A} \leq I_{GND} \leq 250) mA</td>
<td>45</td>
<td>65</td>
<td>(\mu\text{A})</td>
<td></td>
</tr>
<tr>
<td>(I_{SHDN})</td>
<td>Shutdown current (I_{GND}) (V_{EN} \leq 0.4) V</td>
<td>0.15</td>
<td>1.0</td>
<td>(\mu\text{A})</td>
<td></td>
</tr>
<tr>
<td>(I_{FB})</td>
<td>Feedback pin current (TPS73401)</td>
<td>(-0.5)</td>
<td>0.5</td>
<td>(\mu\text{A})</td>
<td></td>
</tr>
<tr>
<td>(PSRR)</td>
<td>Power-supply rejection ratio (V_{IN} = 3.85) V, (V_{OUT} = 2.85) V, (C_{NR} = 0.01\mu F), (I_{OUT} = 100) mA (f = 100) Hz (60)</td>
<td>dB</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>(V_{N})</td>
<td>Output noise voltage BW from 10 Hz to 100 kHz, (V_{OUT} = 2.8) V (C_{NR} = 0.01\mu F), (C_{NR} = 11 \times V_{OUT}) (\mu V_{RMS})</td>
<td>(95 \times V_{OUT}) (\mu V_{RMS})</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>(T_{STR})</td>
<td>Startup time, (V_{OUT} = 0) to (90%), (V_{OUT} = 2.85) V, (R_{IN} = 14\Omega), (C_{OUT} = 2.2\mu F) (C_{NR} = 0)</td>
<td>45</td>
<td>(\mu s)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>(V_{EN(HI)})</td>
<td>Enable high (enabled)</td>
<td>1.2</td>
<td>(V_{IN})</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>(V_{EN(LO)})</td>
<td>Enable low (shutdown)</td>
<td>0</td>
<td>0.4</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>(I_{EN(HI)})</td>
<td>Enable pin current, enabled</td>
<td>(V_{EN} = V_{IN} = 6.5) V</td>
<td>0.03</td>
<td>1.0</td>
<td>(\mu\text{A})</td>
</tr>
<tr>
<td>(T_{SD})</td>
<td>Thermal shutdown temperature (165) °C</td>
<td>(145) °C</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>(T_{J})</td>
<td>Operating junction temperature</td>
<td>(-40)</td>
<td>(+125)</td>
<td>°C</td>
<td></td>
</tr>
<tr>
<td>UVLO</td>
<td>Undervoltage lock-out (V_{IN}) rising (1.90)</td>
<td>(2.20)</td>
<td>(2.65)</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Hysteresis (V_{IN}) falling</td>
<td>70</td>
<td>mV</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

\(^{(1)}\) Minimum \(V_{IN} = V_{OUT} + V_{DO}\) or \(2.7\) V, whichever is greater.

\(^{(2)}\) \(V_{DO}\) is not measured for devices with \(V_{OUT(NOM)} < 2.8\) V because minimum \(V_{IN} = 2.7\) V.
### DEVICE INFORMATION

#### FUNCTIONAL BLOCK DIAGRAMS

**Thermal Shutdown**

**UVLO**

**Current Limit**

**Overshoot Detect**

**500k/c87**

**1.208V Bandgap**

**IN**

**EN**

**FB**

**OUT**

**GND**

**400/c87**

---

**NOTE (1):** Fixed voltage versions between 1.0V to 1.2V have a 1.0V bandgap circuit instead of a 1.208V bandgap circuit.

---

#### PIN CONFIGURATIONS

**TPS734xx**

**TPS73401**

**DDC**

**TSOT23-5**

**TOP VIEW**

<table>
<thead>
<tr>
<th>PIN</th>
<th>1</th>
<th>2</th>
<th>3</th>
<th>4</th>
<th>5</th>
<th>6</th>
<th>7</th>
<th>8</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>IN</strong></td>
<td>EN</td>
<td>GND</td>
<td>NR</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>OUT</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**TPS734xx**

**TPS73401**

**DRV**

**2mm x 2mm SON-6**

**TOP VIEW**

<table>
<thead>
<tr>
<th>PIN</th>
<th>1</th>
<th>2</th>
<th>3</th>
<th>4</th>
<th>5</th>
<th>6</th>
<th>7</th>
<th>8</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>IN</strong></td>
<td>EN</td>
<td>GND</td>
<td>NR</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>FB</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>OUT</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

### PIN DESCRIPTIONS

<table>
<thead>
<tr>
<th>NAME</th>
<th>TPS734xx</th>
<th>TPS73401DDC</th>
<th>TPS73401DRV</th>
</tr>
</thead>
<tbody>
<tr>
<td>NAME</td>
<td>DDC</td>
<td>DRV</td>
<td>DRB</td>
</tr>
<tr>
<td>IN</td>
<td>1</td>
<td>6</td>
<td>8</td>
</tr>
<tr>
<td>GND</td>
<td>2</td>
<td>3, Pad</td>
<td>4</td>
</tr>
<tr>
<td>EN</td>
<td>3</td>
<td>4</td>
<td>5</td>
</tr>
<tr>
<td>NR</td>
<td>4</td>
<td>2</td>
<td>3</td>
</tr>
<tr>
<td>FB</td>
<td>4</td>
<td>2</td>
<td>3</td>
</tr>
<tr>
<td>OUT</td>
<td>5</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>N/C</td>
<td>—</td>
<td>5</td>
<td>2, 6, 7</td>
</tr>
</tbody>
</table>
TYPICAL CHARACTERISTICS

Over operating temperature range (TJ = −40°C to +125°C); VIN = VOUT(TYP) + 0.3V or 2.7V, whichever is greater; IOUT = 1mA, VEN = VIN, COUT = 2.2µF, CRM = 0.01µF, unless otherwise noted. For TPS73401, VOUT = 3.0V. Typical values are at TJ = +25°C.

---

**TPS73401 LINE REGULATION**

![Graph](image1)

**TPS73401 LOAD REGULATION**

![Graph](image2)

**TPS73425 LINE REGULATION**

![Graph](image3)

**TPS73425 LOAD REGULATION**

![Graph](image4)

**TPS73425 GROUND PIN CURRENT vs OUTPUT CURRENT**

![Graph](image5)

**TPS73425 GROUND PIN CURRENT (DISABLE) vs TEMPERATURE**

![Graph](image6)
TYPICAL CHARACTERISTICS (continued)

Over operating temperature range (T_J = –40°C to +125°C); V_IN = V_OUT(TYP) + 0.3V or 2.7V, whichever is greater; I_OUT = 1mA, V_EN = V_IN, C_OUT = 2.2µF, C_NR = 0.01µF, unless otherwise noted. For TPS73401, V_OUT = 3.0V. Typical values are at T_J = +25°C.

TPS73401 DROPOUT VOLTAGE vs OUTPUT CURRENT

![Figure 9.](image)

POWER-SUPPLY RIPPLE REJECTION vs FREQUENCY
(V_IN – V_OUT = 1.0V)

![Figure 10.](image)

POWER-SUPPLY RIPPLE REJECTION vs FREQUENCY
(V_IN – V_OUT = 0.5V)

![Figure 11.](image)

POWER-SUPPLY RIPPLE REJECTION vs FREQUENCY
(V_IN – V_OUT = 0.3V)

![Figure 12.](image)

TPS73425 TOTAL NOISE vs C_NR

![Figure 13.](image)

TPS73425 TOTAL NOISE vs C_OUT

![Figure 14.](image)
TYPICAL CHARACTERISTICS (continued)

Over operating temperature range ($T_J = -40^\circ C$ to $+125^\circ C$); $V_{IN} = V_{OUT(TYP)} + 0.3$V or 2.7V, whichever is greater; $I_{OUT} = 1mA, V_{EN} = V_{IN}, C_{OUT} = 2.2\mu F, C_{NR} = 0.01\mu F$, unless otherwise noted. For TPS73401, $V_{OUT} = 3.0V$. Typical values are at $T_J = +25^\circ C$.

TPS73425
TURN-ON RESPONSE
($V_{IN} = V_{EN}$)

TPS73425
ENABLE RESPONSE OVER STABLE $V_{IN}$

TPS73410
POWER-UP/POWER-DOWN

TPS73410
LOAD TRANSIENT RESPONSE

TPS73410
LINE TRANSIENT RESPONSE

Figure 15.

Figure 16.

Figure 17.

Figure 18.

Figure 19.
APPLICATION INFORMATION

The TPS734xx family of LDO regulators combines the high performance required of many RF and precision analog applications with ultra-low current consumption. High PSRR is provided by a high gain, high bandwidth error loop with good supply rejection at very low headroom (VIN – VOUT). Fixed voltage versions provide a noise reduction pin to bypass noise generated by the bandgap reference and to improve PSRR while a quick-start circuit fast-charges this capacitor at startup. The combination of high performance and low ground current also make the TPS734xx an excellent choice for portable applications. All versions have thermal and over-current protection and are fully specified from –40°C to +125°C.

Figure 20 shows the basic circuit connections for fixed voltage models. Figure 21 gives the connections for the adjustable output version (TPS73401). R1 and R2 can be calculated for any output voltage using the formula in Figure 21.

![Figure 20. Typical Application Circuit for Fixed Voltage Versions](image)

Input and Output Capacitor Requirements

Although an input capacitor is not required for stability, it is good analog design practice to connect a 0.1µF to 1µF low equivalent series resistance (ESR) capacitor across the input supply near the regulator. The ground of this capacitor should be connected as close as the ground of output capacitor; a capacitor value of 0.1µF is enough in this condition. When it is difficult to place these two ground points close together, a 1µF capacitor is recommended. This capacitor counteracts reactive input sources and improves transient response, noise rejection, and ripple rejection. A higher-value capacitor may be necessary if large, fast rise-time load transients are anticipated, or if the device is located several inches from the power source. If source impedance is not sufficiently low, a 0.1µF input capacitor may be necessary to ensure stability.

The TPS734xx is designed to be stable with standard ceramic output capacitors of values 2.2µF or larger. X5R and X7R type capacitors are best because they have minimal variation in value and ESR over temperature. Maximum ESR of the output capacitor should be < 1.0Ω, so output capacitor type should be either ceramic or conductive polymer electrolytic.

Feedback Capacitor Requirements (TPS73401 only)

The feedback capacitor, CFB, shown in Figure 21 is required for stability. For a parallel combination of R1 and R2 equal to 250kΩ, any value from 3pF to 1nF can be used. Fixed voltage versions have an internal 30pF feedback capacitor that is quick-charged at start-up. The adjustable version does not have this quick-charge circuit, so values below 5pF should be used to ensure fast startup; values above 47pF can be used to implement an output voltage soft-start. Larger value capacitors also improve noise slightly. The TPS73401 is stable in unity-gain configuration (OUT tied to FB) without CFB.

Output Noise

In most LDOs, the bandgap is the dominant noise source. If a noise reduction capacitor (CNR) is used with the TPS734xx, the bandgap does not contribute significantly to noise. Instead, noise is dominated by the output resistor divider and the error amplifier input. To minimize noise in a given application, use a 0.01µF noise reduction capacitor; for the adjustable version, smaller value resistors in the output resistor divider reduce noise. A parallel combination that gives 2µA of divider current has the same noise performance as a fixed voltage version. To further
optimize noise, equivalent series resistance of the output capacitor can be set to approximately 0.2Ω. This configuration maximizes phase margin in the control loop, reducing total output noise by up to 10%.

Noise can be referred to the feedback point (FB pin) such that with \( C_{NR} = 0.01\mu F \), total noise is given approximately by Equation 1:

\[
V_n = \frac{11\mu V_{RMS}}{V} \times V_{OUT}
\]  

(1)

The TPS73401 adjustable version does not have the noise-reduction pin available, so ultra-low noise operation is not possible. Noise can be minimized according to the above recommendations.

**Board Layout Recommendations to Improve PSRR and Noise Performance**

To improve ac performance such as PSRR, output noise, and transient response, it is recommended that the board be designed with separate ground planes for \( V_{IN} \) and \( V_{OUT} \), with each ground plane connected only at the GND pin of the device. In addition, the ground connection for the bypass capacitor should connect directly to the GND pin of the device.

**Internal Current Limit**

The TPS734xx internal current limit helps protect the regulator during fault conditions. During current limit, the output sources a fixed amount of current that is largely independent of output voltage. For reliable operation, the device should not be operated in current limit for extended periods of time.

The PMOS pass element in the TPS734xx has a built-in body diode that conducts current when the voltage at OUT exceeds the voltage at IN. This current is not limited, so if extended reverse voltage operation is anticipated, external limiting may be appropriate.

**Shutdown**

The enable pin (EN) is active high and is compatible with standard and low voltage TTL-CMOS levels. When shutdown capability is not required, EN can be connected to IN.

**Dropout Voltage**

The TPS734xx uses a PMOS pass transistor to achieve low dropout. When \( V_{IN} - V_{OUT} \) is less than the dropout voltage \( V_{DO} \), the PMOS pass device is in its linear region of operation and the input-to-output resistance is the \( R_{DS_{ON}} \) of the PMOS pass element. Because the PMOS device behaves like a resistor in dropout, \( V_{DO} \) approximately scales with output current.

As with any linear regulator, PSRR and transient response are degraded as \( (V_{IN} - V_{OUT}) \) approaches dropout. This effect is shown in the Typical Characteristics section.

**Startup and Noise Reduction Capacitor**

Fixed voltage versions of the TPS734xx use a quick-start circuit to fast-charge the noise reduction capacitor, \( C_{NR} \), if present (see the Functional Block Diagrams). This architecture allows the combination of very low output noise and fast start-up times. The NR pin is high impedance so a low leakage \( C_{NR} \) capacitor must be used; most ceramic capacitors are appropriate in this configuration.

Note that for fastest startup, \( V_{IN} \) should be applied first, then the enable pin (EN) driven high. If EN is tied to IN, startup is somewhat slower. Refer to the Typical Characteristics section. The quick-start switch is closed for approximately 135\( \mu \)s. To ensure that \( C_{NR} \) is fully charged during the quick-start time, a 0.01\( \mu \)F or smaller capacitor should be used.

**Transient Response**

As with any regulator, increasing the size of the output capacitor reduces over/undershoot magnitude but increases duration of the transient response. In the adjustable version, adding \( C_{FB} \) between OUT and FB improves stability and transient response. The transient response of the TPS734xx is enhanced by an active pull-down that engages when the output overshoots by approximately 5% or more when the device is enabled. When enabled, the pull-down device behaves like a 400\( \Omega \) resistor to ground.

**Undervoltage Lock-Out (UVLO)**

The TPS734xx utilizes an undervoltage lock-out circuit to keep the output shut off until internal circuitry is operating properly. The UVLO circuit has a de-glitch feature so that it typically ignores undershoot transients on the input if they are less than 50\( \mu \)s duration.

**Minimum Load**

The TPS734xx is stable and well-behaved with no output load. To meet the specified accuracy, a minimum load of 1mA is required. Below 1mA at junction temperatures near +125°C, the output can drift up enough to cause the output pull-down to turn on. The output pull-down limits voltage drift to 5% typically but ground current could increase by approximately 50\( \mu \)A. In typical applications, the junction cannot reach high temperatures at light loads because there is no appreciable dissipated power. The specified ground current would then be valid at no load conditions in most applications.
Thermal Information

Thermal Protection
Thermal protection disables the output when the junction temperature rises to approximately +165°C, allowing the device to cool. When the junction temperature cools to approximately +145°C the output circuitry is again enabled. Depending on power dissipation, thermal resistance, and ambient temperature, the thermal protection circuit may cycle on and off. This cycling limits the dissipation of the regulator, protecting it from damage as a result of overheating.

Any tendency to activate the thermal protection circuit indicates excessive power dissipation or an inadequate heatsink. For reliable operation, junction temperature should be limited to +125°C maximum. To estimate the margin of safety in a complete design (including heatsink), increase the ambient temperature until the thermal protection is triggered; use worst-case loads and signal conditions. For good reliability, thermal protection should trigger at least +35°C above the maximum expected ambient condition of your particular application. This configuration produces a worst-case junction temperature of +125°C at the highest expected ambient temperature and worst-case load.

The internal protection circuitry of the TPS734xx has been designed to protect against overload conditions. It was not intended to replace proper heatsinking. Continuously running the TPS734xx into thermal shutdown degrades device reliability.

Power Dissipation
The ability to remove heat from the die is different for each package type, presenting different considerations in the PCB layout. The PCB area around the device that is free of other components moves the heat from the device to the ambient air. Performance data for JEDEC low- and high-K boards are given in the Dissipation Ratings table. Using heavier copper increases the effectiveness in removing heat from the device. The addition of plated through-holes to heat-dissipating layers also improves the heatsink effectiveness.

Power dissipation depends on input voltage and load conditions. Power dissipation is equal to the product of the output current time the voltage drop across the output pass element, as shown in Equation 2:

\[ P_D = (V_{IN} - V_{OUT}) \cdot I_{OUT} \]  

(2)

Package Mounting
Solder pad footprint recommendations for the TPS734xx are available from the Texas Instruments web site at www.ti.com.
## PACKAGING INFORMATION

<table>
<thead>
<tr>
<th>Orderable Device</th>
<th>Status (1)</th>
<th>Package Type</th>
<th>Package Drawing</th>
<th>Pins</th>
<th>Package Qty</th>
<th>Eco Plan (2)</th>
<th>Lead/Ball Finish</th>
<th>MSL Peak Temp (3)</th>
<th>Op Temp (°C)</th>
<th>Device Marking (4/5)</th>
<th>Samples</th>
</tr>
</thead>
<tbody>
<tr>
<td>TPS73401DDCR</td>
<td>ACTIVE</td>
<td>SOT-23-THIN</td>
<td>DDC</td>
<td>5</td>
<td>3000</td>
<td>Green (RoHS &amp; no Sn/Pb)</td>
<td>CU NIPDAU</td>
<td>Level-2-260C-1 YEAR</td>
<td>-40 to 125</td>
<td>OCW</td>
<td></td>
</tr>
<tr>
<td>TPS73401DDCT</td>
<td>ACTIVE</td>
<td>SOT-23-THIN</td>
<td>DDC</td>
<td>5</td>
<td>250</td>
<td>Green (RoHS &amp; no Sn/Pb)</td>
<td>CU NIPDAU</td>
<td>Level-2-260C-1 YEAR</td>
<td>-40 to 125</td>
<td>OCW</td>
<td></td>
</tr>
<tr>
<td>TPS73401DRVR</td>
<td>ACTIVE</td>
<td>WSON</td>
<td>DRV</td>
<td>6</td>
<td>3000</td>
<td>Green (RoHS &amp; no Sn/Pb)</td>
<td>CU NIPDAU</td>
<td>Level-1-260C-UNLIM</td>
<td>-40 to 125</td>
<td>CBG</td>
<td></td>
</tr>
<tr>
<td>TPS73401DRVT</td>
<td>ACTIVE</td>
<td>WSON</td>
<td>DRV</td>
<td>6</td>
<td>250</td>
<td>Green (RoHS &amp; no Sn/Pb)</td>
<td>CU NIPDAU</td>
<td>Level-1-260C-UNLIM</td>
<td>-40 to 125</td>
<td>CBG</td>
<td></td>
</tr>
<tr>
<td>TPS73418DRVR</td>
<td>ACTIVE</td>
<td>WSON</td>
<td>DRV</td>
<td>6</td>
<td>3000</td>
<td>Green (RoHS &amp; no Sn/Pb)</td>
<td>CU NIPDAU</td>
<td>Level-1-260C-UNLIM</td>
<td>-40 to 125</td>
<td>CBI</td>
<td></td>
</tr>
<tr>
<td>TPS73418DRVT</td>
<td>ACTIVE</td>
<td>WSON</td>
<td>DRV</td>
<td>6</td>
<td>250</td>
<td>Green (RoHS &amp; no Sn/Pb)</td>
<td>CU NIPDAU</td>
<td>Level-1-260C-UNLIM</td>
<td>-40 to 125</td>
<td>CBI</td>
<td></td>
</tr>
<tr>
<td>TPS73430DRVT</td>
<td>ACTIVE</td>
<td>WSON</td>
<td>DRV</td>
<td>6</td>
<td>250</td>
<td>Green (RoHS &amp; no Sn/Pb)</td>
<td>CU NIPDAU</td>
<td>Level-1-260C-UNLIM</td>
<td>-40 to 125</td>
<td>CVW</td>
<td></td>
</tr>
<tr>
<td>TPS73430DRVT</td>
<td>ACTIVE</td>
<td>WSON</td>
<td>DRV</td>
<td>6</td>
<td>250</td>
<td>Green (RoHS &amp; no Sn/Pb)</td>
<td>CU NIPDAU</td>
<td>Level-1-260C-UNLIM</td>
<td>-40 to 125</td>
<td>CVW</td>
<td></td>
</tr>
<tr>
<td>TPS73433DDCR</td>
<td>ACTIVE</td>
<td>SOT-23-THIN</td>
<td>DDC</td>
<td>5</td>
<td>3000</td>
<td>Green (RoHS &amp; no Sn/Pb)</td>
<td>CU NIPDAU</td>
<td>Level-2-260C-1 YEAR</td>
<td>-40 to 125</td>
<td>OEV</td>
<td></td>
</tr>
<tr>
<td>TPS73433DDCT</td>
<td>ACTIVE</td>
<td>SOT-23-THIN</td>
<td>DDC</td>
<td>5</td>
<td>250</td>
<td>Green (RoHS &amp; no Sn/Pb)</td>
<td>CU NIPDAU</td>
<td>Level-2-260C-1 YEAR</td>
<td>-40 to 125</td>
<td>OEV</td>
<td></td>
</tr>
<tr>
<td>TPS73433DRVR</td>
<td>ACTIVE</td>
<td>WSON</td>
<td>DRV</td>
<td>6</td>
<td>3000</td>
<td>Green (RoHS &amp; no Sn/Pb)</td>
<td>CU NIPDAU</td>
<td>Level-1-260C-UNLIM</td>
<td>-40 to 125</td>
<td>CVX</td>
<td></td>
</tr>
<tr>
<td>TPS73433DRVT</td>
<td>ACTIVE</td>
<td>WSON</td>
<td>DRV</td>
<td>6</td>
<td>250</td>
<td>Green (RoHS &amp; no Sn/Pb)</td>
<td>CU NIPDAU</td>
<td>Level-1-260C-UNLIM</td>
<td>-40 to 125</td>
<td>CVX</td>
<td></td>
</tr>
</tbody>
</table>

(1) The marketing status values are defined as follows:
- **ACTIVE**: Product device recommended for new designs.
- **LIFEBUY**: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
- **NRND**: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
- **PREVIEW**: Device has been announced but is not in production. Samples may or may not be available.
- **OBSOLETE**: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sn/Pb) - please check [http://www.ti.com/productcontent](http://www.ti.com/productcontent) for the latest availability information and additional product content details.
- **TBD**: The Pb-Free/Green conversion plan has not been defined.
**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

**Important Information and Disclaimer:** The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.
TAPE AND REEL INFORMATION

**Dimensions**

- **Device**: TPS73401DDCR
  - **Package Type**: SOT-23-THIN
  - **Package Drawing**: DDC
  - **Pins**: 5
  - **SPQ**: 3000
  - **Reel Diameter (mm)**: 180.0
  - **Reel Width W1 (mm)**: 8.4
  - **A0 (mm)**: 3.2
  - **B0 (mm)**: 3.2
  - **K0 (mm)**: 1.4
  - **P1 (mm)**: 4.0
  - **W (mm)**: 8.0
  - **Pin1 Quadrant**: Q3

- **Device**: TPS73401DDCT
  - **Package Type**: SOT-23-THIN
  - **Package Drawing**: DDC
  - **Pins**: 5
  - **SPQ**: 250
  - **Reel Diameter (mm)**: 179.0
  - **Reel Width W1 (mm)**: 8.4
  - **A0 (mm)**: 3.2
  - **B0 (mm)**: 3.2
  - **K0 (mm)**: 1.4
  - **P1 (mm)**: 4.0
  - **W (mm)**: 8.0
  - **Pin1 Quadrant**: Q3

- **Device**: TPS73401DRVR
  - **Package Type**: WSON
  - **Package Drawing**: DRV
  - **Pins**: 6
  - **SPQ**: 3000
  - **Reel Diameter (mm)**: 179.0
  - **Reel Width W1 (mm)**: 8.4
  - **A0 (mm)**: 2.2
  - **B0 (mm)**: 2.2
  - **K0 (mm)**: 1.2
  - **P1 (mm)**: 4.0
  - **W (mm)**: 8.0
  - **Pin1 Quadrant**: Q2

- **Device**: TPS73430DRVR
  - **Package Type**: WSON
  - **Package Drawing**: DRV
  - **Pins**: 6
  - **SPQ**: 3000
  - **Reel Diameter (mm)**: 179.0
  - **Reel Width W1 (mm)**: 8.4
  - **A0 (mm)**: 2.25
  - **B0 (mm)**: 2.25
  - **K0 (mm)**: 1.0
  - **P1 (mm)**: 4.0
  - **W (mm)**: 8.0
  - **Pin1 Quadrant**: Q2

- **Device**: TPS73430DRVT
  - **Package Type**: WSON
  - **Package Drawing**: DRV
  - **Pins**: 6
  - **SPQ**: 250
  - **Reel Diameter (mm)**: 178.0
  - **Reel Width W1 (mm)**: 8.4
  - **A0 (mm)**: 2.25
  - **B0 (mm)**: 2.25
  - **K0 (mm)**: 1.0
  - **P1 (mm)**: 4.0
  - **W (mm)**: 8.0
  - **Pin1 Quadrant**: Q2

- **Device**: TPS73433DDCR
  - **Package Type**: SOT-23-THIN
  - **Package Drawing**: DDC
  - **Pins**: 5
  - **SPQ**: 3000
  - **Reel Diameter (mm)**: 180.0
  - **Reel Width W1 (mm)**: 8.4
  - **A0 (mm)**: 3.2
  - **B0 (mm)**: 3.2
  - **K0 (mm)**: 1.4
  - **P1 (mm)**: 4.0
  - **W (mm)**: 8.0
  - **Pin1 Quadrant**: Q3

- **Device**: TPS73433DDCT
  - **Package Type**: SOT-23-THIN
  - **Package Drawing**: DDC
  - **Pins**: 5
  - **SPQ**: 250
  - **Reel Diameter (mm)**: 179.0
  - **Reel Width W1 (mm)**: 8.4
  - **A0 (mm)**: 3.2
  - **B0 (mm)**: 3.2
  - **K0 (mm)**: 1.4
  - **P1 (mm)**: 4.0
  - **W (mm)**: 8.0
  - **Pin1 Quadrant**: Q3

- **Device**: TPS73433DRVR
  - **Package Type**: WSON
  - **Package Drawing**: DRV
  - **Pins**: 6
  - **SPQ**: 3000
  - **Reel Diameter (mm)**: 179.0
  - **Reel Width W1 (mm)**: 8.4
  - **A0 (mm)**: 2.2
  - **B0 (mm)**: 2.2
  - **K0 (mm)**: 1.2
  - **P1 (mm)**: 4.0
  - **W (mm)**: 8.0
  - **Pin1 Quadrant**: Q2

- **Device**: TPS73433DRVT
  - **Package Type**: WSON
  - **Package Drawing**: DRV
  - **Pins**: 6
  - **SPQ**: 250
  - **Reel Diameter (mm)**: 179.0
  - **Reel Width W1 (mm)**: 8.4
  - **A0 (mm)**: 2.2
  - **B0 (mm)**: 2.2
  - **K0 (mm)**: 1.2
  - **P1 (mm)**: 4.0
  - **W (mm)**: 8.0
  - **Pin1 Quadrant**: Q2

*All dimensions are nominal.

---

Pack Materials-Page 1
<table>
<thead>
<tr>
<th>Device</th>
<th>Package Type</th>
<th>Package Drawing</th>
<th>Pins</th>
<th>SPQ</th>
<th>Length (mm)</th>
<th>Width (mm)</th>
<th>Height (mm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>TPS73401DDCR</td>
<td>SOT-23-THIN</td>
<td>DDC</td>
<td>5</td>
<td>3000</td>
<td>195.0</td>
<td>200.0</td>
<td>45.0</td>
</tr>
<tr>
<td>TPS73401DDCT</td>
<td>SOT-23-THIN</td>
<td>DDC</td>
<td>5</td>
<td>250</td>
<td>195.0</td>
<td>200.0</td>
<td>45.0</td>
</tr>
<tr>
<td>TPS73401DRVR</td>
<td>WSON</td>
<td>DRV</td>
<td>6</td>
<td>3000</td>
<td>203.0</td>
<td>203.0</td>
<td>35.0</td>
</tr>
<tr>
<td>TPS73401DRVT</td>
<td>WSON</td>
<td>DRV</td>
<td>6</td>
<td>250</td>
<td>203.0</td>
<td>203.0</td>
<td>35.0</td>
</tr>
<tr>
<td>TPS73418DRVR</td>
<td>WSON</td>
<td>DRV</td>
<td>6</td>
<td>3000</td>
<td>203.0</td>
<td>203.0</td>
<td>35.0</td>
</tr>
<tr>
<td>TPS73418DRVT</td>
<td>WSON</td>
<td>DRV</td>
<td>6</td>
<td>250</td>
<td>203.0</td>
<td>203.0</td>
<td>35.0</td>
</tr>
<tr>
<td>TPS73430DRVR</td>
<td>WSON</td>
<td>DRV</td>
<td>6</td>
<td>3000</td>
<td>205.0</td>
<td>200.0</td>
<td>33.0</td>
</tr>
<tr>
<td>TPS73430DRVT</td>
<td>WSON</td>
<td>DRV</td>
<td>6</td>
<td>250</td>
<td>203.0</td>
<td>203.0</td>
<td>35.0</td>
</tr>
<tr>
<td>TPS73433DDCR</td>
<td>SOT-23-THIN</td>
<td>DDC</td>
<td>5</td>
<td>3000</td>
<td>195.0</td>
<td>200.0</td>
<td>45.0</td>
</tr>
<tr>
<td>TPS73433DDCT</td>
<td>SOT-23-THIN</td>
<td>DDC</td>
<td>5</td>
<td>250</td>
<td>195.0</td>
<td>200.0</td>
<td>45.0</td>
</tr>
<tr>
<td>TPS73433DRVR</td>
<td>WSON</td>
<td>DRV</td>
<td>6</td>
<td>3000</td>
<td>203.0</td>
<td>203.0</td>
<td>35.0</td>
</tr>
<tr>
<td>TPS73433DRVT</td>
<td>WSON</td>
<td>DRV</td>
<td>6</td>
<td>250</td>
<td>203.0</td>
<td>203.0</td>
<td>35.0</td>
</tr>
</tbody>
</table>

*All dimensions are nominal*
Images above are just a representation of the package family, actual package may vary. Refer to the product data sheet for package details.
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.
EXAMPLE BOARD LAYOUT

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).

5. Vias are optional depending on application, refer to device data sheet. If some or all are implemented, recommended via locations are shown.
6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion.
D. Falls within JEDEC MO-193 variation AB (5 pin).
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC-7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.
Texas Instruments Incorporated (TI) reserves the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete.

TI's published terms of sale for semiconductor products (http://www.ti.com/sc/docs/stdterms.htm) apply to the sale of packaged integrated circuit products that TI has qualified and released to market. Additional terms may apply to the use or sale of other types of TI products and services.

Reproduction of significant portions of TI information in TI data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such reproduced documentation. Information of third parties may be subject to additional restrictions. Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyers and others who are developing systems that incorporate TI products (collectively, “Designers”) understand and agree that Designers remain responsible for using their independent analysis, evaluation and judgment in designing their applications and that Designers have full and exclusive responsibility to assure the safety of Designers’ applications and compliance of their applications (and of all TI products used in or for Designers’ applications) with all applicable regulations, laws and other applicable requirements. Designer represents that, with respect to their applications, Designer has all the necessary expertise to create and implement safeguards that (1) anticipate dangerous consequences of failures, (2) monitor failures and their consequences, and (3) lessen the likelihood of failures that might cause harm and take appropriate actions. Designer agrees that prior to using or distributing any applications that include TI products, Designer will thoroughly test such applications and the functionality of such TI products as used in such applications.

TI’s provision of technical, application or other design advice, quality characterization, reliability data or other services or information, including, but not limited to, reference designs and materials relating to evaluation modules, (collectively, “TI Resources”) are intended to assist designers who are developing applications that incorporate TI products; by downloading, accessing or using TI Resources in any way, Designer (individually or, if Designer is acting on behalf of a company, Designer’s company) agrees to use any particular TI Resource solely for this purpose and subject to the terms of this Notice.

TI’s provision of TI Resources does not expand or otherwise alter TI’s applicable published warranties or warranty disclaimers for TI products, and no additional obligations or liabilities arise from TI providing such TI Resources. TI reserves the right to make corrections, enhancements, improvements and other changes to its TI Resources. TI has not conducted any testing other than that specifically described in the published documentation for a particular TI Resource.

Designer is authorized to use, copy and modify any individual TI Resource only in connection with the development of applications that include the TI product(s) identified in such TI Resource. NO OTHER LICENSE, EXPRESS OR IMPLIED, BY ESTOPPEL OR OTHERWISE TO OWN OR INFRINGE UPON ANY TECHNICAL, PATENT, COPYRIGHT, TRADE SECRET, TRADE NAME, PROPERTY RIGHT OF TI OR ANY THIRD PARTY IS GRANTED HEREIN, including but not limited to any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information regarding or referencing third-party products or services does not constitute a license to use such products or services, or a warranty or endorsement thereof. Use of TI Resources may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

TI RESOURCES ARE PROVIDED “AS IS” AND WITH ALL FAULTS. TI DISCLAIMS ALL OTHER WARRANTIES OR REPRESENTATIONS, EXPRESS OR IMPLIED, REGARDING RESOURCES OR USE THEREOF, INCLUDING BUT NOT LIMITED TO ACCURACY OR COMPLETENESS, TITLE, ANY EPIDEMIC FAILURE WARRANTY AND ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, AND NON-INFRINGEMENT OF ANY THIRD PARTY INTELLECTUAL PROPERTY RIGHTS. TI SHALL NOT BE LIABLE FOR AND SHALL NOT DEFEND OR INDEMNIFY DESIGNER AGAINST ANY CLAIM, INCLUDING BUT NOT LIMITED TO ANY INFRINGEMENT CLAIM THAT RELATES TO OR IS BASED ON ANY COMBINATION OF PRODUCTS EVEN IF DESCRIBED IN TI RESOURCES OR OTHERWISE. IN NO EVENT SHALL TI BE LIABLE FOR ANY ACTUAL, DIRECT, SPECIAL, COLLATERAL, INDIRECT, PUNITIVE, INCIDENTAL, CONSEQUENTIAL OR EXEMPLARY DAMAGES IN CONNECTION WITH OR ARISING OUT OF TI RESOURCES OR USE THEREOF, AND REGARDLESS OF WHETHER TI HAS BEEN ADVISED OF THE POSSIBILITY OF SUCH DAMAGES.

Unless TI has explicitly designated an individual product as meeting the requirements of a particular industry standard (e.g., ISO/TS 16949 and ISO 26262), TI is not responsible for any failure to meet such industry standard requirements.

Where TI specifically promotes products as facilitating functional safety or as compliant with industry functional safety standards, such products are intended to help enable customers to design and create their own applications that meet applicable functional safety standards and requirements. Using products in an application does not by itself establish any safety features in the application. Designers must ensure compliance with safety-related requirements and standards applicable to their applications. Designers may not use any TI products in life-critical medical equipment unless authorized officers of the parties have executed a special contract specifically governing such use. Life-critical medical equipment is medical equipment where failure of such equipment would cause serious bodily injury or death (e.g., life support, pacemakers, defibrillators, heart pumps, neurostimulators, and implantables). Such equipment includes, without limitation, all medical devices identified by the U.S. Food and Drug Administration as Class III devices and equivalent classifications outside the U.S.

TI may expressly designate certain products as completing a particular qualification (e.g., Q100, Military Grade, or Enhanced Product). Designers agree that it has the necessary expertise to select the product with the appropriate qualification designation for their applications and that proper product selection is at Designers’ own risk. Designers are solely responsible for compliance with all legal and regulatory requirements in connection with such selection.

Designer will fully indemnify TI and its representatives against any damages, costs, losses, and/or liabilities arising out of Designer’s non-compliance with the terms and provisions of this Notice.