1 Features

- 500-mA Low-Dropout Regulator With Enable
- Available in Fixed and Adjustable (1.2-V to 5.5-V) Versions
- High PSRR (50 dB at 10 kHz)
- Ultralow Noise (33 \(\mu\text{V}_{\text{RMS}}\), TPS79530)
- Fast Start-Up Time (50 \(\mu\text{s}\))
- Stable With a 1-\(\mu\text{F}\) Ceramic Capacitor
- Excellent Load and Line Transient Response
- Low Dropout Voltage (110 mV at Full Load, TPS79530)
- 6-Pin SOT-223 and 3-mm \(\times\) 3-mm WSON Packages

2 Applications

- RF: VCOs, Receivers, ADCs
- Audio
- Bluetooth\(^\text{®}\), Wireless LAN
- Cellular and Cordless Telephones
- Handheld Organizers, PDAs

3 Description

The TPS795 family of low-dropout (LDO), low-power linear voltage regulators features high power-supply rejection ratio (PSRR), ultralow noise, fast start-up, and excellent line and load transient responses in small outline, 6-pin SOT-223 and 3-mm \(\times\) 3-mm WSON packages. Each device in the family is stable with a small 1-\(\mu\text{F}\) ceramic capacitor on the output. The family uses an advanced, proprietary BiCMOS fabrication process to yield extremely low dropout voltages (for example, 110 mV at 500 mA). Each device achieves fast start-up times (approximately 50 \(\mu\text{s}\) with a 0.001-\(\mu\text{F}\) bypass capacitor) while consuming very low quiescent current (265 \(\mu\text{A}\), typical). Moreover, when the device is placed in standby mode, the supply current is reduced to less than 1 \(\mu\text{A}\). The TPS79530 device exhibits approximately 33 \(\mu\text{V}_{\text{RMS}}\) of output voltage noise at 3-V output with a 0.1-\(\mu\text{F}\) bypass capacitor. Applications with analog components that are noise-sensitive, such as portable RF electronics, benefit from the high-PSRR and low-noise features, as well as from the fast response time.

Device Information\(^{(1)}\)

<table>
<thead>
<tr>
<th>PART NUMBER</th>
<th>PACKAGE</th>
<th>BODY SIZE (NOM)</th>
</tr>
</thead>
<tbody>
<tr>
<td>TPS795</td>
<td>SOT-223 (6)</td>
<td>6.50 mm (\times) 3.50 mm</td>
</tr>
<tr>
<td></td>
<td>WSON (8)</td>
<td>3.00 mm (\times) 3.00 mm</td>
</tr>
</tbody>
</table>

\(^{(1)}\) For all available packages, see the orderable addendum at the end of the data sheet.
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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision H (August 2010) to Revision I Page

• Added ESD Ratings table, Feature Description section, Device Functional Modes, Application and Implementation
  section, Power Supply Recommendations section, Layout section, Device and Documentation Support section, and
  Mechanical, Packaging, and Orderable Information section ......................................................... 1

• Changed front-page graphic .................................................................................................................. 1

• Changed Pin Configuration and Functions section; updated table format and added pinout drawings........... 3

• Changed “free-air” to “junction” temperature in condition statement for Absolute Maximum Ratings ....... 4

• Deleted Start-up time symbol ........................................................................................................... 5

• Corrected min value for EN(HI) parameter ...................................................................................... 5

• Added Thermal shutdown temperature specification to Electrical Characteristics ............................ 5

• Added Operating junction temperature specification to Electrical Characteristics .......................... 5

• Added condition statement to Typical Characteristics section .......................................................... 6

• Changed title for Thermal Protection section .................................................................................. 18

Changes from Revision G (July, 2006) to Revision H Page

• Replaced the Dissipation Ratings table with the Thermal Information table .................................. 4

• Updated the Thermal Protection section .......................................................................................... 18
5 Pin Configuration and Functions

### Pin Functions

<table>
<thead>
<tr>
<th>PIN</th>
<th>I/O</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>NAME</td>
<td>SOT-223</td>
<td>WSON</td>
</tr>
<tr>
<td>IN</td>
<td>2</td>
<td>1, 2</td>
</tr>
<tr>
<td>GND</td>
<td>3, 6</td>
<td>6</td>
</tr>
<tr>
<td>EN</td>
<td>1</td>
<td>8</td>
</tr>
<tr>
<td>NR</td>
<td>5</td>
<td>5</td>
</tr>
<tr>
<td>FB</td>
<td>5</td>
<td>5</td>
</tr>
<tr>
<td>OUT</td>
<td>4</td>
<td>3, 4</td>
</tr>
<tr>
<td>N/C</td>
<td>–</td>
<td>7</td>
</tr>
</tbody>
</table>
# 6 Specifications

## 6.1 Absolute Maximum Ratings

over operating junction temperature range (unless otherwise noted) \(^{(1)}\)

<table>
<thead>
<tr>
<th>MIN</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>(V_{\text{IN}})</td>
<td>(-0.3)</td>
<td>6</td>
</tr>
<tr>
<td>(V_{\text{EN}})</td>
<td>(-0.3)</td>
<td>(V_{\text{IN}} + 0.3)</td>
</tr>
<tr>
<td>(\text{Peak output})</td>
<td></td>
<td>(\text{Internally limited})</td>
</tr>
</tbody>
</table>

**Power dissipation**

- Junction, \(T_J\)
- Storage, \(T_{\text{stg}}\)

<table>
<thead>
<tr>
<th>MIN</th>
<th>NOM</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>(-40)</td>
<td>150</td>
<td>(-65)</td>
<td>150</td>
</tr>
</tbody>
</table>

\(^{(1)}\) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

## 6.2 ESD Ratings

<table>
<thead>
<tr>
<th>(V_{\text{ESD}})</th>
<th>Electrostatic discharge</th>
<th>VALUE</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins (^{(1)})</td>
<td>(\pm2000)</td>
<td>(V)</td>
<td></td>
</tr>
<tr>
<td>Charged device model (CDM), per JEDEC specification JESD22-C101, all pins (^{(2)})</td>
<td>(\pm500)</td>
<td>(V)</td>
<td></td>
</tr>
</tbody>
</table>

\(^{(1)}\) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

\(^{(2)}\) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

## 6.3 Recommended Operating Conditions

over operating junction temperature range (unless otherwise noted)

<table>
<thead>
<tr>
<th>(V_{\text{IN}})</th>
<th>Input voltage</th>
<th>MIN</th>
<th>NOM</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>(I_{\text{OUT}})</td>
<td>Output current</td>
<td>0</td>
<td>0.5</td>
<td>(A)</td>
<td></td>
</tr>
<tr>
<td>(T_J)</td>
<td>Operating junction temperature</td>
<td>(-40)</td>
<td>125</td>
<td>(^{\circ C})</td>
<td></td>
</tr>
</tbody>
</table>

## 6.4 Thermal Information

over operating free-air temperature range (unless otherwise noted)

<table>
<thead>
<tr>
<th>THERMAL METRIC (^{(1)}(2))</th>
<th>(r_{\text{JA}})</th>
<th>Junction-to-ambient thermal resistance</th>
<th>(R_{\text{JA}})</th>
<th>(47.8)</th>
<th>70.4</th>
</tr>
</thead>
<tbody>
<tr>
<td>(R_{\text{JC}(\text{top})})</td>
<td>Junction-to-case (top) thermal resistance</td>
<td>83</td>
<td>70</td>
<td></td>
<td></td>
</tr>
<tr>
<td>(\psi_{\text{JT}})</td>
<td>Junction-to-top characterization parameter</td>
<td>2.1</td>
<td>6.8</td>
<td></td>
<td></td>
</tr>
<tr>
<td>(\psi_{\text{JB}})</td>
<td>Junction-to-board characterization parameter</td>
<td>17.8</td>
<td>30.1</td>
<td></td>
<td></td>
</tr>
<tr>
<td>(R_{\text{JC}(\text{bot})})</td>
<td>Junction-to-case (bottom) thermal resistance</td>
<td>12.1</td>
<td>6.3</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

\(^{(1)}\) For more information about traditional and new thermal metrics, see the IC Package Thermal Metrics application report, SPRA953.

\(^{(2)}\) For thermal estimates of this device based on PCB copper area, see the TI PCB Thermal Calculator.

\(^{(3)}\) Thermal data for the DRB and DCQ packages are derived by thermal simulations based on JEDEC-standard methodology as specified in the JESD51 series. The following assumptions are used in the simulations:

- i. DRB: The exposed pad is connected to the PCB ground layer through a 2-mm x 2-mm thermal via array.
- ii. DCQ: Each of top and bottom copper layers has a dedicated pattern for 20% copper coverage.

- b. DRB: The top and bottom copper layers are assumed to have a 20% thermal conductivity of copper representing 20% copper coverage.
- ii. DCQ: Each of top and bottom copper layers has a dedicated pattern for 20% copper coverage.

- c. These data were generated with only a single device at the center of a JEDEC high-K (2s2p) board with 3in x 3in copper area. To understand the effects of the copper area on thermal performance, see Thermal Considerations and Estimating Junction Temperature of this data sheet.
### 6.5 Electrical Characteristics

Over recommended operating temperature range ($T_J = -40°C$ to $125°C$), $V_{EN} = V_{IN}$, $V_{IN} = V_{OUT(nom)} + 1$ V $(1)$, $I_{OUT} = 1$ mA, $C_{OUT} = 10 \mu F$, $C_{NR} = 0.01 \mu F$, unless otherwise noted. Typical values are at $25°C$.

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{IN}$</td>
<td>Input voltage</td>
<td>2.7</td>
<td>5.5</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>$V_{FB}$</td>
<td>Internal reference (TPS79501)</td>
<td>1.200</td>
<td>1.225</td>
<td>1.25</td>
<td>V</td>
</tr>
<tr>
<td>$I_{OUT}$</td>
<td>Continuous output current</td>
<td>0</td>
<td>500</td>
<td>mA</td>
<td></td>
</tr>
<tr>
<td>$V_{OUT}$</td>
<td>Output voltage range</td>
<td>TPS79501</td>
<td>0 µA $\leq I_{OUT} \leq 500$ mA, $V_{OUT(nom)} + 1$ V $\leq V_{IN} \leq$ $5.5$ V $(1)$</td>
<td>0.98$V_{OUT(nom)}$</td>
<td>$V_{OUT(nom)}$</td>
</tr>
<tr>
<td></td>
<td>Accuracy</td>
<td>Fixed $V_{OUT} &lt; 5$ V</td>
<td>0 µA $\leq I_{OUT} \leq 500$ mA, $V_{OUT(nom)} + 1$ V $\leq V_{IN} \leq$ $5.5$ V $(1)$</td>
<td>$-2%$</td>
<td>$%$</td>
</tr>
<tr>
<td>$\Delta V_{O(VI)}$</td>
<td>Line regulation</td>
<td>$V_{OUT} + 1$ V $\leq V_{IN} \leq 5.5$ V</td>
<td>0.05</td>
<td>0.12</td>
<td>$%$</td>
</tr>
<tr>
<td>$\Delta V_{O(IO)}$</td>
<td>Load regulation</td>
<td>$0 \mu A \leq I_{OUT} \leq 500$ mA</td>
<td>3</td>
<td>mV</td>
<td></td>
</tr>
<tr>
<td>$V_{DO}$</td>
<td>Dropout voltage $(3)$</td>
<td>TPS9530</td>
<td>$I_{OUT} = 500$ mA</td>
<td>110</td>
<td>170</td>
</tr>
<tr>
<td></td>
<td></td>
<td>TPS9533</td>
<td>$I_{OUT} = 500$ mA</td>
<td>105</td>
<td>160</td>
</tr>
<tr>
<td>$I_{CL}$</td>
<td>Output current limit</td>
<td>$V_{OUT} = 0$ V</td>
<td>2.4</td>
<td>2.8</td>
<td>A</td>
</tr>
<tr>
<td>$I_{GND}$</td>
<td>Ground pin current</td>
<td>$0 \mu A \leq I_{GND} \leq 500$ mA</td>
<td>265</td>
<td>385</td>
<td>$\mu A$</td>
</tr>
<tr>
<td>$I_{SHDN}$</td>
<td>Shutdown current $(4)$</td>
<td>$V_{EN} = 0$ V, $2.7$ V $\leq V_{IN} \leq 5.5$ V</td>
<td>0.07</td>
<td>1</td>
<td>$\mu A$</td>
</tr>
<tr>
<td>$I_{FB}$</td>
<td>Feedback pin current</td>
<td>$V_{FB} = 1.225$ V</td>
<td>1</td>
<td>$\mu A$</td>
<td></td>
</tr>
<tr>
<td>PSRR</td>
<td>Power-supply rejection ratio (TPS9530)</td>
<td>$f = 100$ Hz, $I_{OUT} = 10$ mA</td>
<td>59</td>
<td></td>
<td>dB</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$f = 100$ Hz, $I_{OUT} = 500$ mA</td>
<td>58</td>
<td></td>
<td>dB</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$f = 10$ kHz, $I_{OUT} = 500$ mA</td>
<td>50</td>
<td></td>
<td>dB</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$f = 100$ kHz, $I_{OUT} = 500$ mA</td>
<td>39</td>
<td></td>
<td>dB</td>
</tr>
<tr>
<td>$V_{n}$</td>
<td>Output noise voltage (TPS9530)</td>
<td>$BW = 100$ Hz to $100$ kHz, $I_{OUT} = 500$ mA</td>
<td>$C_{NR} = 0.001$ $\mu F$</td>
<td>$C_{NR} = 0.0047$ $\mu F$</td>
<td>$C_{NR} = 0.01$ $\mu F$</td>
</tr>
<tr>
<td></td>
<td>Start-up time (TPS9530)</td>
<td>$R_{L} = 6$ $\Omega$, $C_{OUT} = 1$ $\mu F$</td>
<td>$C_{HR} = 0.001$ $\mu F$</td>
<td>$C_{HR} = 0.0047$ $\mu F$</td>
<td>$C_{HR} = 0.01$ $\mu F$</td>
</tr>
<tr>
<td>$V_{EN(HI)}$</td>
<td>Enable high (enabled)</td>
<td>$2.7$ V $\leq V_{IN} \leq 5.5$ V</td>
<td>1.7</td>
<td>$V_{IN}$</td>
<td>V</td>
</tr>
<tr>
<td>$V_{EN(LO)}$</td>
<td>Enable low (shutdown)</td>
<td>$2.7$ V $\leq V_{IN} \leq 5.5$ V</td>
<td>0.7</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>$I_{EN(HI)}$</td>
<td>Enable pin current, enabled</td>
<td>$V_{EN} = 0$ V</td>
<td>$-1$</td>
<td>1</td>
<td>$\mu A$</td>
</tr>
<tr>
<td>UVLO</td>
<td>Undervoltage lockout</td>
<td>$V_{CC}$ rising</td>
<td>2.25</td>
<td>2.65</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td>Hysteresis</td>
<td>$100$</td>
<td>mV</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$T_{sd}$</td>
<td>Thermal shutdown temperature</td>
<td>Shutdown, temperature increasing</td>
<td>165</td>
<td>°C</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Reset, temperature decreasing</td>
<td>140</td>
<td>°C</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$T_J$</td>
<td>Operating junction temperature</td>
<td>$-40$</td>
<td>125</td>
<td>°C</td>
<td></td>
</tr>
</tbody>
</table>

(1) Minimum $V_{IN}$ is $2.7$ V or $V_{OUT} + V_{DO}$, whichever is greater.
(2) Tolerance of external resistors not included in this specification.
(3) Dropout is not measured for the TPS79501 and TPS79525 because minimum $V_{IN} = 2.7$ V.
(4) For adjustable version, this applies only after $V_{IN}$ is applied; then $V_{EN}$ transitions high to low.
6.6 Typical Characteristics

At $V_{EN} = V_{IN}$, $V_{IN} = V_{OUT(nom)} + 1$ V, $I_{OUT} = 1$ mA, $C_{OUT} = 10$ μF, $C_{NR} = 0.01$ μF, $C_{IN} = 2.2$ μF, and $T_J = 25^\circ$C, unless otherwise noted.

**Figure 1. TPS79530 Output Voltage vs Output Current**

**Figure 2. TPS79530 Output Voltage vs Junction Temperature**

**Figure 3. TPS79530 Ground Current vs Junction Temperature**

**Figure 4. TPS79530 Output Spectral Noise Density vs Frequency**

**Figure 5. TPS79530 Output Spectral Noise Density vs Frequency**

**Figure 6. TPS79530 Output Spectral Noise Density vs Frequency**
Typical Characteristics (continued)

At $V_{EN} = V_{IN}$, $V_{IN} = V_{OUT(nom)} + 1$ V, $I_{OUT} = 1$ mA, $C_{OUT} = 10$ μF, $C_{NR} = 0.01$ μF, $C_{IN} = 2.2$ μF, and $T_J = 25^\circ C$, unless otherwise noted.

Figure 7. TPS79530 Root Mean Squared Output Noise vs $C_{NR}$

Figure 8. TPS79530 Dropout Voltage vs Junction Temperature

Figure 9. TPS79530 Ripple Rejection vs Frequency

Figure 10. TPS79530 Ripple Rejection vs Frequency

Figure 11. TPS79530 Ripple Rejection vs Frequency

Figure 12. TPS79530 Ripple Rejection vs Frequency
Typical Characteristics (continued)

At \( V_{\text{EN}} = V_{\text{IN}} \), \( V_{\text{IN}} = V_{\text{OUT(nom)}} + 1 \) V, \( I_{\text{OUT}} = 1 \) mA, \( C_{\text{OUT}} = 10 \) \( \mu \)F, \( C_{\text{NR}} = 0.01 \) \( \mu \)F, \( C_{\text{IN}} = 2.2 \) \( \mu \)F, and \( T_J = 25^\circ\text{C} \), unless otherwise noted.

---

**Figure 13. TPS79530 Start-Up Time**

**Figure 14. TPS79518 Line Transient Response**

**Figure 15. TPS79530 Line Transient Response**

**Figure 16. TPS79530 Load Transient Response**

**Figure 17. TPS79525 Power Up and Power Down**

**Figure 18. TPS79530 Dropout Voltage vs Output Current**
Typical Characteristics (continued)

At $V_{EN} = V_{IN}$, $V_{IN} = V_{OUT(nom)} + 1$ V, $I_{OUT} = 1$ mA, $C_{OUT} = 10 \mu F$, $C_{NR} = 0.01 \mu F$, $C_{IN} = 2.2 \mu F$, and $T_J = 25^\circ C$, unless otherwise noted.

Figure 19. TPS79501 Dropout Voltage vs Input Voltage

Figure 20. TPS79530 Typical Regions of Stability Equivalent Series Resistance (ESR) vs Output Current

Figure 21. TPS79530 Typical Regions of Stability Equivalent Series Resistance (ESR) vs Output Current

Figure 22. TPS79530 Typical Regions of Stability Equivalent Series Resistance (ESR) vs Output Current
7 Detailed Description

7.1 Overview
The TPS795 family of LDO regulators combines the high performance required of many RF and precision analog applications with low current consumption. High PSRR is provided by a high-gain, high-bandwidth error loop with good supply rejection at very low headroom (V_{IN} – V_{OUT}). A noise-reduction pin is provided to bypass noise generated by the band-gap reference and to improve PSRR, while a quick-start circuit quickly charges this capacitor at start-up. All versions have thermal and overcurrent protection, and are fully specified from –40°C to 125°C.

7.2 Functional Block Diagrams

![Figure 23. Functional Block Diagram—Adjustable Version](image1)

![Figure 24. Functional Block Diagram—Fixed Versions](image2)
7.3 Feature Description

7.3.1 Shutdown
The enable pin (EN) is active high and is compatible with standard and low-voltage TTL-CMOS levels. When shutdown capability is not required, EN can be connected to IN.

7.3.2 Start-Up
The TPS795 uses a start-up circuit to quickly charge the noise reduction capacitor, \(C_{NR}\), if present (see Functional Block Diagrams). This circuit allows for the combination of very low output noise and fast start-up times. The NR pin is high impedance so a low leakage \(C_{NR}\) capacitor must be used; most ceramic capacitors are appropriate for this configuration.

For the fastest start-up, apply \(V_{IN}\) first, and then drive the enable pin (EN) high. If EN is tied to IN, start-up is somewhat slower. To ensure that \(C_{NR}\) is fully charged during start-up, use a 0.1-\(\mu\)F or smaller capacitor.

7.3.3 Undervoltage Lockout (UVLO)
The TPS795 uses an undervoltage lockout circuit to keep the output shut off until internal circuitry is operating properly. The UVLO circuit has approximately 100 mV of hysteresis to help reject input voltage drops when the regulator first turns on.

7.3.4 Regulator Protection
The TPS795 PMOS-pass transistor has a built-in back diode that conducts reverse current when the input voltage drops below the output voltage (for example, during power down). Current is conducted from the output to the input and is not internally limited. If extended reverse voltage operation is anticipated, external limiting might be appropriate.

The TPS795 features internal current limiting and thermal protection. During normal operation, the TPS795 limits output current to approximately 2.8 A. When current limiting engages, the output voltage scales back linearly until the overcurrent condition ends. While current limiting is designed to prevent gross device failure, care should be taken not to exceed the power dissipation ratings of the package. If the temperature of the device exceeds approximately 165°C (\(T_{sd}\)), thermal-protection circuitry shuts it down. Once the device has cooled down to less than approximately 140°C, regulator operation resumes.
7.4 Device Functional Modes

Table 1 provides a quick comparison between the normal, dropout, and disabled modes of operation.

<table>
<thead>
<tr>
<th>OPERATING MODE</th>
<th>PARAMETER</th>
<th>EN</th>
<th>IOUT</th>
<th>TJ</th>
</tr>
</thead>
<tbody>
<tr>
<td>Normal</td>
<td>$V_{IN} &gt; V_{OUT\text{nom}} + V_{DO}$</td>
<td>$V_{EN} &gt; V_{EN(HI)}$</td>
<td>$I_{OUT} &lt; I_{CL}$</td>
<td>$T_J &lt; T_{sd}$</td>
</tr>
<tr>
<td>Dropout</td>
<td>$V_{IN} &lt; V_{OUT\text{nom}} + V_{DO}$</td>
<td>$V_{EN} &gt; V_{EN(HI)}$</td>
<td>$I_{OUT} &lt; I_{CL}$</td>
<td>$T_J &lt; T_{sd}$</td>
</tr>
<tr>
<td>Disabled</td>
<td>—</td>
<td>$V_{EN} &lt; V_{EN(LO)}$</td>
<td>—</td>
<td>$T_J &gt; T_{sd}$</td>
</tr>
</tbody>
</table>

7.4.1 Normal Operation

The device regulates to the nominal output voltage under the following conditions:

- The input voltage is greater than the nominal output voltage plus the dropout voltage ($V_{OUT\text{nom}} + V_{DO}$).
- The enable voltage has previously exceeded the enable rising threshold voltage and not yet decreased below the enable falling threshold.
- The output current is less than the current limit ($I_{OUT} < I_{CL}$).
- The device junction temperature is less than the thermal shutdown temperature ($T_J < T_{sd}$).

7.4.2 Dropout Operation

If the input voltage is lower than the nominal output voltage plus the specified dropout voltage, but all other conditions are met for normal operation, the device operates in dropout mode. In this mode, the output voltage tracks the input voltage. During this mode, the transient performance of the device becomes significantly degraded because the pass device is in the linear region and no longer controls the current through the LDO. Line or load transients in dropout can result in large output-voltage deviations.

7.4.3 Disabled

The device is disabled under the following conditions:

- The enable voltage is less than the enable falling threshold voltage or has not yet exceeded the enable rising threshold.
- The device junction temperature is greater than the thermal shutdown temperature ($T_J > T_{sd}$).
8 Application and Implementation

NOTE
Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI’s customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information
The TPS795 family of LDO regulators has been optimized for use in noise-sensitive equipment. The device features extremely low dropout voltages, high PSRR, ultralow output noise, low quiescent current (265 μA, typically), and an enable input to reduce supply currents to less than 1 μA when the regulator is turned off.

8.2 Typical Application
A typical application circuit is shown in Figure 25.

![Figure 25. Typical Application Circuit](image)

8.2.1 Design Requirements
Table 2 lists the design requirements.

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>DESIGN REQUIREMENT</th>
</tr>
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<tr>
<td>Input voltage</td>
<td>3.3 V</td>
</tr>
<tr>
<td>Output voltage</td>
<td>2.5 V</td>
</tr>
<tr>
<td>Maximum output current</td>
<td>500 mA</td>
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</table>

8.2.2 Detailed Design Procedure
Select the desired device based on the output voltage.

Provide an input supply with adequate headroom to account for dropout and output current to account for the GND terminal current, and power the load.

8.2.2.1 Input and Output Capacitor Requirements
Although not required, it is good analog design practice to place a 0.1-μF to 2.2-μF capacitor near the input of the regulator to counteract reactive input sources. A higher-value input capacitor may be necessary if large, fast-rise time load transients are anticipated and the device is located several inches from the power source.

Like most low dropout regulators, the TPS795 requires an output capacitor connected between OUT and GND to stabilize the internal control loop. The minimum recommended capacitor is 1 μF. Any 1-μF or larger ceramic capacitor is suitable.
8.2.2.2 Output Noise

The internal voltage reference is a key source of noise in an LDO regulator. The TPS795 has an NR pin which is connected to the voltage reference through a 250-kΩ internal resistor. The 250-kΩ internal resistor, in conjunction with an external bypass capacitor connected to the NR pin, creates a low-pass filter to reduce the voltage reference noise and, therefore, the noise at the regulator output. For the regulator to operate properly, the current flow out of the NR pin must be at a minimum, because any leakage current creates an IR drop across the internal resistor, thus creating an output error. Therefore, the bypass capacitor must have minimal leakage current. The bypass capacitor should be no more than 0.1 μF to ensure that it is fully charged during the quickstart time provided by the internal switch shown in Functional Block Diagrams.

For example, the TPS79530 exhibits 40 μVRMS of output voltage noise using a 0.1-μF ceramic bypass capacitor and a 10-μF ceramic output capacitor. The output starts up slower as the bypass capacitance increases due to the RC time constant at the bypass pin that is created by the internal 250-kΩ resistor and external capacitor.

8.2.2.3 Dropout Voltage

The TPS795 uses a PMOS pass transistor to achieve a low dropout voltage. When \((V_{IN} - V_{OUT})\) is less than the dropout voltage \(V_{DO}\), the PMOS pass device is in its linear region of operation and \(r_{DS(on)}\) of the PMOS pass element is the input-to-output resistance. Because the PMOS device behaves like a resistor in dropout, \(V_{DO}\) approximately scales with the output current.

As with any linear regulator, PSRR degrades as \((V_{IN} - V_{OUT})\) approaches dropout. This effect is illustrated in Figure 9 through Figure 12.

8.2.2.4 Programming the TPS79501 Adjustable LDO Regulator

The output voltage of the TPS79501 adjustable regulator is programmed using an external resistor divider as shown in Figure 26.

![Typical Application, Adjustable Output](image)

The output voltage is calculated using Equation 1.

\[
V_{OUT} = V_{REF} \times \left(1 + \frac{R_1}{R_2}\right)
\]

where

- \(V_{REF} = 1.2246\) V typical (the internal reference voltage) \hspace{1cm} (1)

Resistors \(R_1\) and \(R_2\) should be chosen for approximately 40-μA divider current. Lower value resistors can be used for improved noise performance, but the device wastes more power. Higher values should be avoided, as leakage current at FB increases the output voltage error.

The recommended design procedure is to choose \(R_2 = 30.1\) kΩ to set the divider current at 40 μA, \(C_1 = 15\) pF for stability, and then calculate \(R_1\) using Equation 2.

\[
R_1 = \left(\frac{V_{OUT}}{V_{REF}} - 1\right) \times R_2
\]

To improve the stability of the adjustable version, TI suggests placing a small compensation capacitor between OUT and FB.

The approximate value of this capacitor can be calculated using Equation 3.
\[ C_1 = \frac{3 \times 10^{-7} \times (R_1 + R_2)}{(R_1 \times R_2)} \]  

(3)

The suggested value of this capacitor for several resistor ratios is shown in the table within Figure 26. If this capacitor is not used (such as in a unity-gain configuration), then the minimum recommended output capacitor is 2.2 \( \mu \)F instead of 1 \( \mu \)F.

### 8.2.3 Application Curves

![Figure 27. TPS79530 Output Spectral Noise Density vs Frequency](image)

![Figure 28. TPS79530 Ripple Rejection vs Frequency](image)

### 8.3 Do’s and Don’ts

Place at least one 1-\( \mu \)F ceramic capacitor as close as possible to the OUT pin of the regulator.

Do not place the output capacitor more than 10 mm away from the regulator.

Connect a 0.1-\( \mu \)F or larger, low equivalent series resistance (ESR) capacitor across the IN pin and GND input of the regulator.

Do not exceed the absolute maximum ratings.
9 Power Supply Recommendations

These devices are designed to operate from an input voltage supply range from 2.7 V to 5.5 V. The input voltage range provides adequate headroom for the device to have a regulated output. This input supply is well-regulated and stable. If the input supply is noisy, additional input capacitors with low ESR can help improve the output noise performance.

10 Layout

10.1 Layout Guidelines

10.1.1 Board Layout Recommendation to Improve PSRR and Noise Performance

To improve AC measurements like PSRR, output noise, and transient response, TI recommends designing the board with separate ground planes for $V_{IN}$ and $V_{OUT}$, with each ground plane connected only at the ground pin of the device. In addition, the ground connection for the bypass capacitor should connect directly to the ground pin of the device.

10.1.2 Regulator Mounting

The tab of the 6-pin SOT-223 package is electrically connected to ground. For best thermal performance, solder the tab of the surface-mount version directly to a circuit-board copper area. Increasing the copper area improves heat dissipation.

Solder pad footprint recommendations for the devices are presented in application report SBFA015, *Solder Pad Recommendations for Surface-Mount Devices*, available from the TI website (www.ti.com).
10.2 Layout Examples

Figure 29. TPS79501 (Adjustable Voltage Version)—Layout Example
10.3 Thermal Considerations

Knowing the device power dissipation and proper sizing of the thermal plane that is connected to the tab or pad is critical to avoiding thermal shutdown and ensuring reliable operation.

Power dissipation of the device depends on input voltage and load conditions and can be calculated using Equation 4:

\[ P_D = (V_{IN} - V_{OUT}) \times I_{OUT} \]  

(4)

Power dissipation can be minimized and greater efficiency can be achieved by using the lowest possible input voltage necessary to achieve the required output voltage regulation.

On the WSON (DRB) package, the primary conduction path for heat is through the exposed pad to the printed-circuit-board (PCB). The pad can be connected to ground or be left floating; however, it should be attached to an appropriate amount of copper PCB area to ensure the device does not overheat. On the SOT-223 (DCQ) package, the primary conduction path for heat is through the tab to the PCB. The tab should be connected to ground. The maximum junction-to-ambient thermal resistance depends on the maximum ambient temperature, maximum device junction temperature, and power dissipation of the device and can be calculated using Equation 5:

\[ R_{JUA} = \frac{(+125°C - T_A)}{P_D} \]  

(5)
Thermal Considerations (continued)

Knowing the maximum $R_{θJA}$, the minimum amount of PCB copper area needed for appropriate heatsinking can be estimated using Figure 31.

![Figure 31. $θ_{JA}$ vs Board Size](image)

Note: $θ_{JA}$ value at board size of 9 in.$^2$ (that is, 3 in. × 3 in.) is a JEDEC standard.

**Figure 31. $θ_{JA}$ vs Board Size**

Figure 31 shows the variation of $θ_{JA}$ as a function of ground plane copper area in the board. It is intended only as a guideline to demonstrate the effect of heat spreading in the ground plane and should not be used to estimate the thermal performance in real application environments.

**NOTE**

When the device is mounted on an application PCB, it is strongly recommended to use $Ψ_{JT}$ and $Ψ_{JB}$, as explained in *Estimating Junction Temperature*.

10.4 Estimating Junction Temperature

Using the thermal metrics $Ψ_{JT}$ and $Ψ_{JB}$, as shown in *Thermal Information*, the junction temperature can be estimated with corresponding formulas (given in Equation 6). For backwards compatibility, an older $θ_{JC,top}$ parameter is also listed.

- $Ψ_{JT}$: $T_J = T_T + Ψ_{JT} \cdot P_D$
- $Ψ_{JB}$: $T_J = T_B + Ψ_{JB} \cdot P_D$

where

- $P_D$ is the power dissipation shown by Equation 5
- $T_T$ is the temperature at the center-top of the IC package
- $T_B$ is the PCB temperature measured 1 mm away from the IC package on the PCB surface (see Figure 33) (6)

**NOTE**

Both $T_T$ and $T_B$ can be measured on actual application boards using a thermo-gun (an infrared thermometer).

Estimating Junction Temperature (continued)

As shown in Figure 32, the new thermal metrics ($\Psi_{JT}$ and $\Psi_{JB}$) have little dependency on board size. That is, using $\Psi_{JT}$ or $\Psi_{JB}$ with Equation 6 is a good way to estimate $T_J$ by simply measuring $T_T$ or $T_B$, regardless of the application board size.

For a more detailed discussion of why TI does not recommend using $\theta_{JC(top)}$ to determine thermal characteristics, see the application report SBVA025, Using New Thermal Metrics, available at www.ti.com.

For further information, see the application report SPRA953, IC Package Thermal Metrics, also available on the TI website.
11 Device and Documentation Support

11.1 Device Support

11.1.1 Development Support

11.1.1.1 Evaluation Modules

An evaluation module (EVM) is available to assist in the initial circuit performance evaluation using the TPS795. The TPS79501DRBEVM evaluation module related (and user’s guide) can be requested at the TI website through the product folders or purchased directly from the TI eStore.

11.1.1.2 Spice Models

Computer simulation of circuit performance using SPICE is often useful when analyzing the performance of analog circuits and systems. A SPICE model for the TPS795 is available through the product folders under Tools & Software.

11.1.2 Device Nomenclature

Table 3. Device Nomenclature(1)

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<th>PRODUCT</th>
<th>V_{OUT}</th>
</tr>
</thead>
<tbody>
<tr>
<td>TPS795xx(x) yyy z</td>
<td>xx(x) is nominal output voltage (for example, 28 = 2.8 V, 285 = 2.85 V, 01 = Adjustable). yyy is package designator. z is package quantity.</td>
</tr>
</tbody>
</table>

(1) For the most current package and ordering information see the Package Option Addendum at the end of this document, or visit the device product folder at www.ti.com.

11.2 Documentation Support

11.2.1 Related Documentation

- Using New Thermal Metrics, SBVA025
- IC Package Thermal Metrics, SPRA953
- TPS79501DRBEVM User’s Guide, SBVU016
- Using New Thermal Metrics, SBVA025

11.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

**TI E2E™ Online Community TI's Engineer-to-Engineer (E2E) Community.** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

**Design Support TI’s Design Support** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.4 Trademarks

E2E is a trademark of Texas Instruments. Bluetooth is a registered trademark of Bluetooth SIG, Inc. All other trademarks are the property of their respective owners.

11.5 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.
11.6 Glossary
SLYZ022 — *TI Glossary.*
This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information
The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.
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<tr>
<th>Orderable Device</th>
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<th>Package Type</th>
<th>Package Drawing</th>
<th>Pins</th>
<th>Package Qty</th>
<th>Eco Plan</th>
<th>Lead/Ball Finish</th>
<th>MSL Peak Temp</th>
<th>Op Temp (°C)</th>
<th>Device Marking</th>
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(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSCOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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**TAPE AND REEL INFORMATION**

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![Reel Dimensions Diagram](image1)

**REEL DIMENSIONS**

**TAPE DIMENSIONS**

A0: Dimension designed to accommodate the component width
B0: Dimension designed to accommodate the component length
K0: Dimension designed to accommodate the component thickness
W: Overall width of the carrier tape
P1: Pitch between successive cavity centers

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**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**

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*All dimensions are nominal.*

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<tr>
<th>Device</th>
<th>Package Type</th>
<th>Package Drawing</th>
<th>Pins</th>
<th>SPQ</th>
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*All dimensions are nominal*
DCQ (R-PDSO-G6)  PLASTIC SMALL-OUTLINE

NOTES:

A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Controlling dimension in inches.
   Body length and width dimensions are determined at the outermost extremes of the plastic body exclusive of mold flash, tie bar burrs, gate burrs, and interlead flash, but including any mismatch between the top and the bottom of the plastic body.
   Lead width dimension does not include dambar protrusion.

\[ \Delta \] Lead width and thickness dimensions apply to solder plated leads.
C. Interlead flash allow 0.008 inch max.
H. Gate burr/protrusion max. 0.006 inch.
I. Datums A and B are to be determined at Datum H.
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC-SM-782 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.
F. Please refer to the product data sheet for specific via and thermal dissipation requirements.
NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Small Outline No–Lead (SON) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
THERMAL PAD MECHANICAL DATA

DRB (S-PVSON-N8)  PLASTIC SMALL OUTLINE NO-LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.

\[
\begin{array}{c}
\text{Exposed Thermal Pad Dimensions} \\
1,65\pm0,10 \\
2,40\pm0,10 \\
\end{array}
\]

NOTE: All linear dimensions are in millimeters
NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC-7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, QFN Packages, Texas Instruments Literature No. SLUS271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com.<http://www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for solder mask tolerances.
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