TPS797xx Ultra-Low I_Q, 50-mA Low-Dropout Linear Regulators With Power Good Output in SC70 Package

1 Features

- 50-mA Low-Dropout Regulator
- Ultra-Low 1.2-µA Quiescent Current at 10 mA
- 5-Pin SC70 (DCK) Package
- Integrated Power Good Output
- Stable With Any Capacitor Greater Than 0.47 µF
- Typical Dropout Voltage of 105 mV at 10 mA (TPS79733)
- Over-Current Limitation
- Operating Junction Temperature Range of –40°C to 85°C

2 Applications

- Battery-Powered Microcontrollers and Microprocessors

3 Description

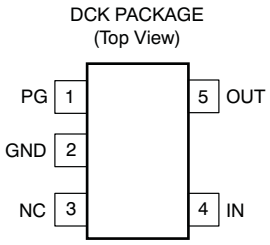
The TPS797xx family of low-dropout voltage regulators (LDOs) offers the benefits of low-dropout voltage and ultra-low-power operation. The device is stable with any capacitor greater than 0.47-µF. Therefore, implementations of this device require very little board space due to the miniaturized packaging and potentially small output capacitor. In addition, the family includes an integrated open drain active-high power good (PG) output. Intended for use in microcontroller-based, battery-powered applications, the TPS797xx family low dropout and ultra-low-power operation result in a significant increase in system battery operating life. The small packaging minimizes consumption of board space.

The device is enabled when the applied voltage exceeds the minimum input voltage. The usual PNP pass transistor has been replaced by a PMOS pass element. Because the PMOS pass element behaves as a low-value resistor, the dropout voltage is very low (typically, 105 mV at 10-mA of load current), and is directly proportional to the load current. The quiescent current is ultra-low (1.2-µA, typically) and is stable over the entire range of output load current (0 mA to 50 mA). When properly configured with a pullup resistor, the PG output can implement a power-on reset or low-battery indicator.

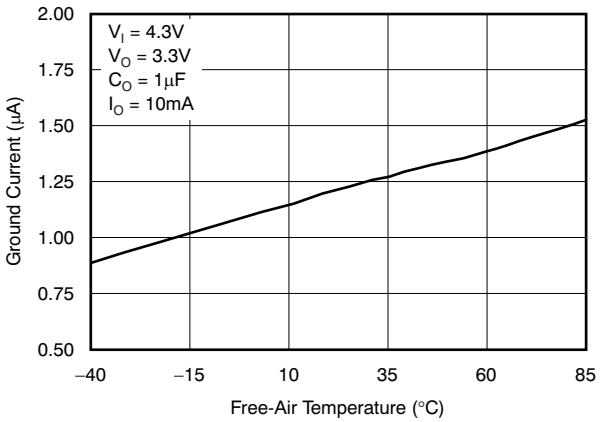
Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPS797xx	SC70 (5)	2.00 mm × 1.25 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.



Ground Current vs Free-Air Temperature



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision I (October 2013) to Revision J — **Page**

- Added *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section ... 1
- Deleted *Dissipation Ratings* table; see *Thermal Information* table ... 4
- Added *Thermal Information* table ... 5
- Changed Load Regulation parameter unit From: mV To: %/A ... 5
- Changed Output Spectral Noise Density vs Frequency graph Y-axis unit From: nV/$\sqrt{Hz}$ To: µV/$\sqrt{Hz}$ ... 7
- Changed IOUTx values From: I_{CL} To: I_{SC} ... 9

Changes from Revision H (April 2012) to Revision I — **Page**

- Changed Dropout Voltage vs Junction Temperature graph Y-axis unit From: V To: mV (typo) ... 8

Changes from Revision G (November 2009) to Revision H — **Page**

- Deleted sentence regarding thermal protection ... 12

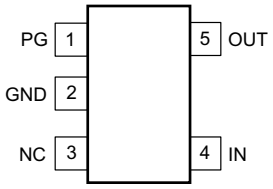
Changes from Revision F (May 2009) to Revision G — **Page**

- Changed document title ... 1
- Deleted references to SOT323 package throughout document ... 1
- Changed Test Conditions for *Electrical Characteristics* table ... 5
- Changed output voltage accuracy test conditions from 10 µA < I_{OUT} < 10 mA to 1 mA < I_{OUT} < 10 mA ... 5
- Deleted line regulation maximum specification ... 5
- Changed PG trip threshold voltage test conditions from V_{OUT} decreasing to V_{OUT} increasing; deleted minimum and maximum specifications ... 5
- Revised PG low output low voltage test conditions ... 5

- Updated PG leakage current test conditions 5

5 Pin Configuration and Functions

DCK Package
5-Pin SC70
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NO.	NAME		
1	PG	O	The PG pin for the fixed voltage option devices is an open drain, active-high output that indicates the status of V_O (output of the LDO). When V_O exceeds approximately 90% of the regulated voltage, PG goes to a high-impedance state. PG goes to a low-impedance state when V_O falls below approximately 90% (that is, overload condition) of the regulated voltage. The open drain output of the PG pin requires a pullup resistor.
2	GND	—	Ground
3	NC	—	No connection
4	IN	I	The IN pin is the power-supply input to the device.
5	OUT	O	The OUT pin provides the regulated output voltage of the device.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)

		MIN	MAX	UNIT
Voltage	Input voltage(2)	–0.3	6	V
	Maximum dc output voltage		4.9	V
Current	Peak output current	Internally limited		A
Temperature	Operating virtual junction temperature, T_J	–40	85	°C
	Storage temperature, T_{stg}	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to network ground pin.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_I	Input voltage	1.8		5.5	V
V_O	Output voltage	1.8		3.3	V
I_O	Output current	0		50	mA
C_I	Input capacitor	0	0.1		µF
C_O	Output capacitor	0.47	1		µF
T_J	Junction temperature	–40		85	°C

6.4 Thermal Information

THERMAL METRIC(1)		TPS797xx DCK (SC70) 5 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	230.9	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	98.3	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	70.7	°C/W
ψ_{JT}	Junction-to-top characterization parameter	3.9	°C/W
ψ_{JB}	Junction-to-board characterization parameter	70.1	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	—	°C/W

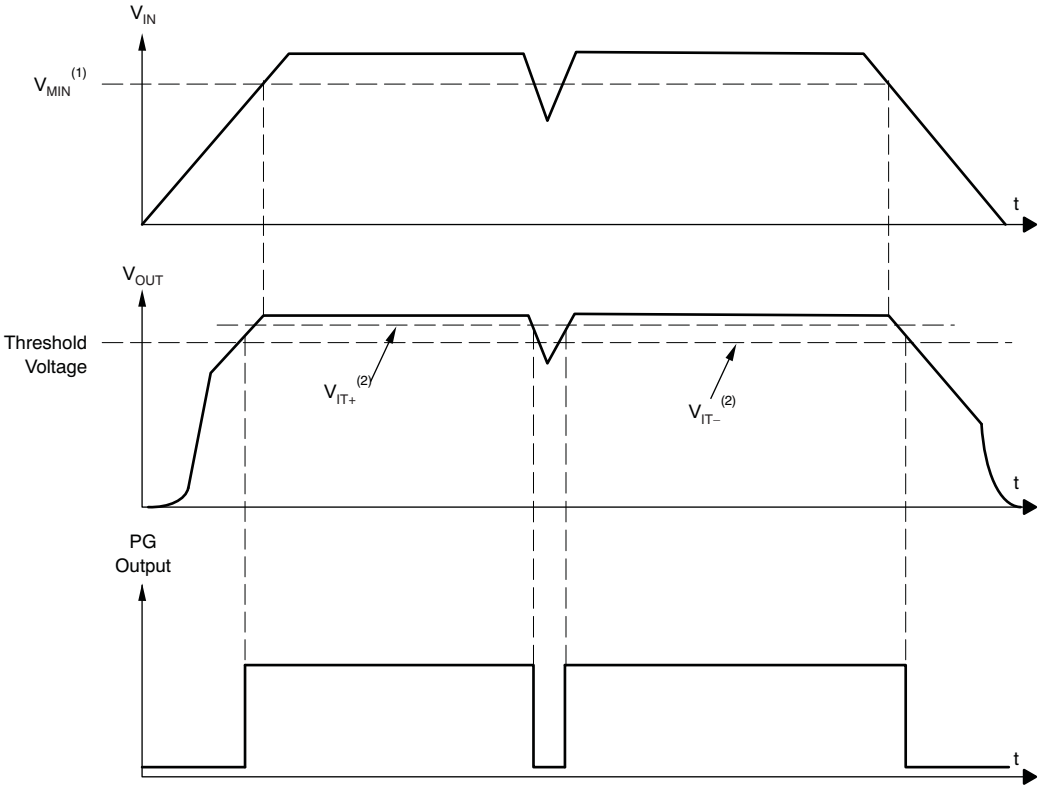
(1) For more information about traditional and new thermal metrics, see *Semiconductor and IC Package Thermal Metrics* (SPRA953).

6.5 Electrical Characteristics

over operating temperature range T_J = –40°C to 85°C, typical values are at T_A = 25°C, $V_I = V_{O\ (typ)}$ + 0.5 V or 2 V (whichever is greater); I_O = 0.5 mA, V_{SET}, $V_{EN} = V_I$, and C_O = 1 µF (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_I	Input voltage(1)	I_O = 3 mA	1.8		5.5	V
		I_O = 10 mA	2		5.5	
I_O	Continuous output current(2)		0		50	mA
V_O	Output voltage accuracy(3)	V_O + 1 V ≤ V_I ≤ 5.5 V 1 mA < I_O < 10 mA	–4%		4%	
$\Delta V_{O(\Delta VI)}$	Line regulation(3)	V_O + 1 V ≤ V_I ≤ 5.5 V		0.15%		V
$\Delta V_{O(\Delta IO)}$	Load regulation	1 µA < I_O < 10 mA		5%		A
$V_{(DO)}$	Dropout voltage(4), I_O = 10 mA $V_I = V_{O(NOM)}$ – 0.1 V	TPS79730		110	200	mV
		TPS79733		105	200	
I_{SC}	Output current limit	V_O = 0 V		190	300	mA
$I_{(GND)}$	Ground pin current(3)	I_O = 10 mA		1.2	2	µA
PSRR	Power-supply rejection ratio (ripple rejection)	f = 100 Hz, C_O = 10 µF, I_O = 10 mA		50		dB
V_n	Output noise voltage (TPS79718)	BW = 200 kHz to 100 kHz, C_O = 10 µF, I_O = 10 mA		600		μV_{RMS}
$V_{Imin(PG)}$	Minimum input voltage for valid PG	$V_{(PG)}$ ≥ 0.8 V, I_{PG} = 100 µA		1.2		V
V_{IT}	PG trip threshold voltage	V_{OUT} increasing		90%		V_{OUT}
$V_{OL(PG)}$	PG output low voltage	V_I = 1.4 V, I_{PG} = 30 µA, I_O = 1 mA		0.14	0.225	V
$I_{lkg(PG)}$	PG leakage current	$V_{(PG)}$ = 5 V, $V_I = V_O$ + 1 V, I_O = 1 mA	0.1			nA

(1) Minimum $V_I = V_O + V_{(DO)}$ or the minimum value specified here, whichever is greater.
(2) Continuous output current is limited by internal protection circuitry, but it is not recommended that the device operate above this maximum for extended periods of time.
(3) Minimum V_I is specified in (1).
(4) $V_{(DO)}$ is not measured for the TPS79718 because minimum V_I > 1.7 V.



NOTES: (1) $V_{MIN} = V_{OUT} + V_{DO}$.
(2) The PG trip voltage is typically 10% lower than the output voltage (90% V_O). V_{IT+} to V_{IT-} is the hysteresis voltage.

Figure 1. TPS797xx PG Timing Diagram

6.6 Typical Characteristics

over operating temperature range T_J = –40°C to 85°C, typical values are at T_A = 25°C, $V_I = V_O$ (typical) + 0.5 V or 2 V (whichever is greater); I_O = 0.5 mA, $V_{EN} = V_I$, and C_O = 1 µF (unless otherwise noted).

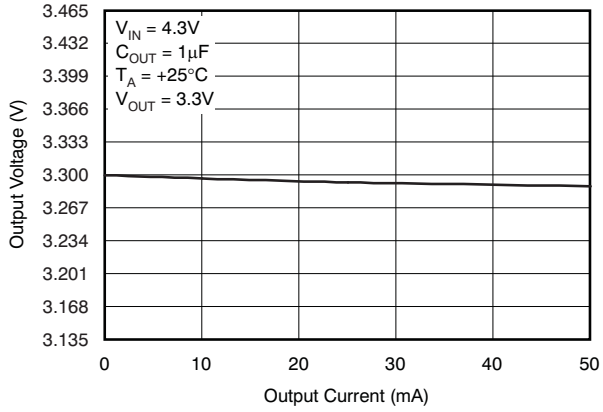


Figure 2. Output Voltage vs Output Current

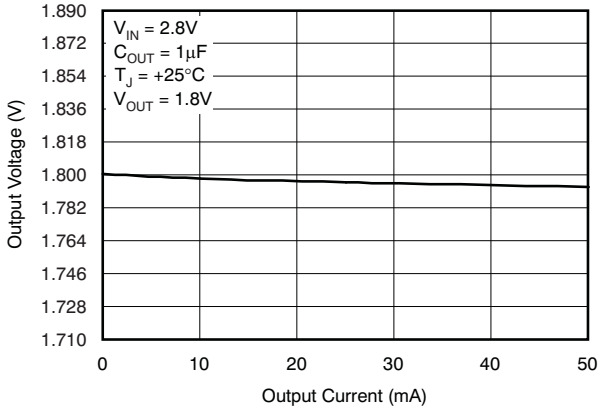


Figure 3. Output Voltage vs Output Current

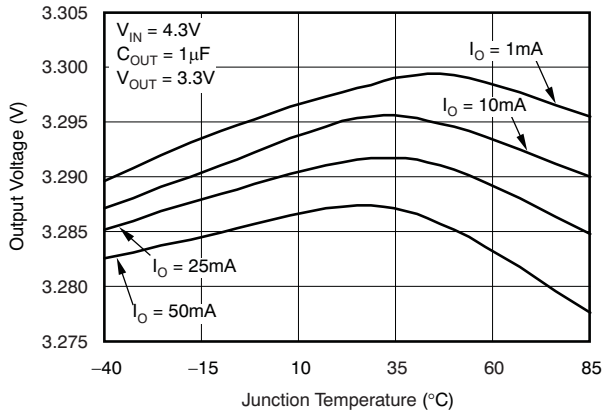


Figure 4. Output Voltage vs Junction Temperature

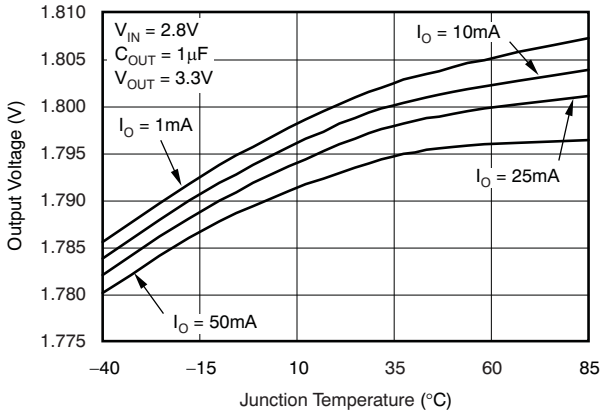


Figure 5. Output Voltage vs Junction Temperature

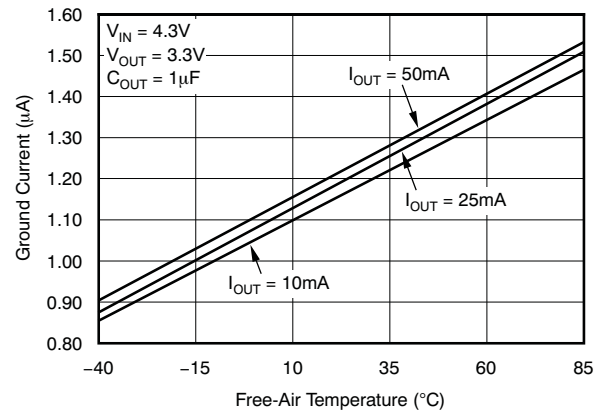


Figure 6. Ground Current vs Junction Temperature

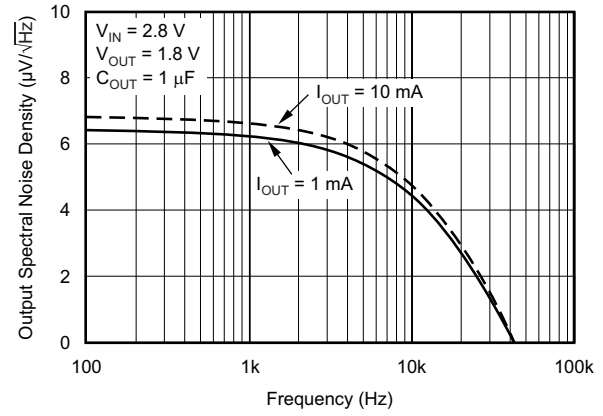


Figure 7. Output Spectral Noise Density vs Frequency

Typical Characteristics (continued)

over operating temperature range T_J = –40°C to 85°C, typical values are at T_A = 25°C, V_I = V_O (typical) + 0.5 V or 2 V (whichever is greater); I_O = 0.5 mA, V_{EN} = V_I, and C_O = 1 µF (unless otherwise noted).

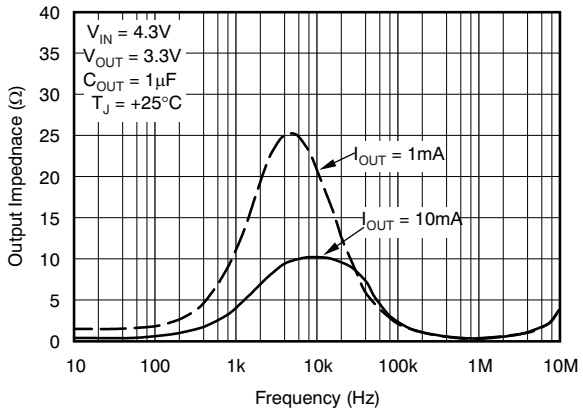


Figure 8. Output Impedance vs Frequency

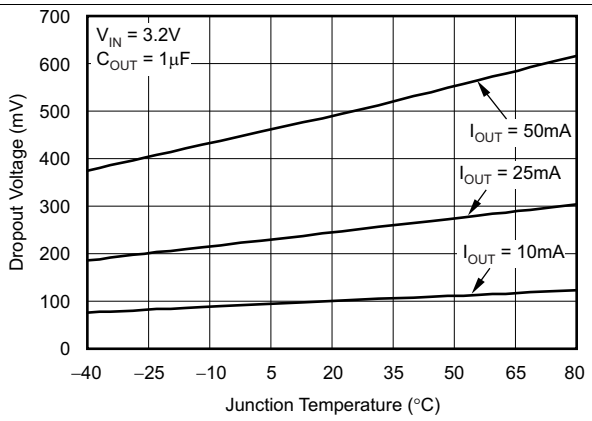


Figure 9. Dropout Voltage vs Junction Temperature

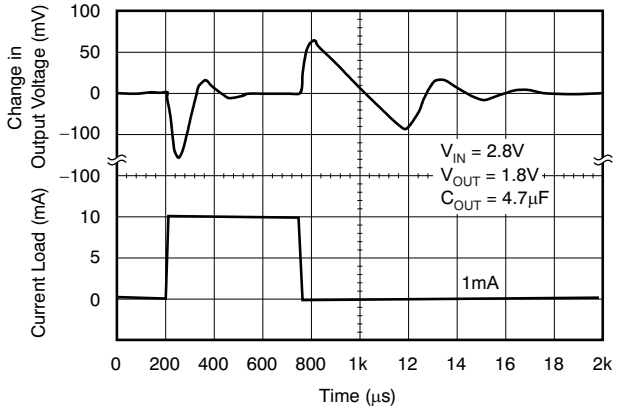


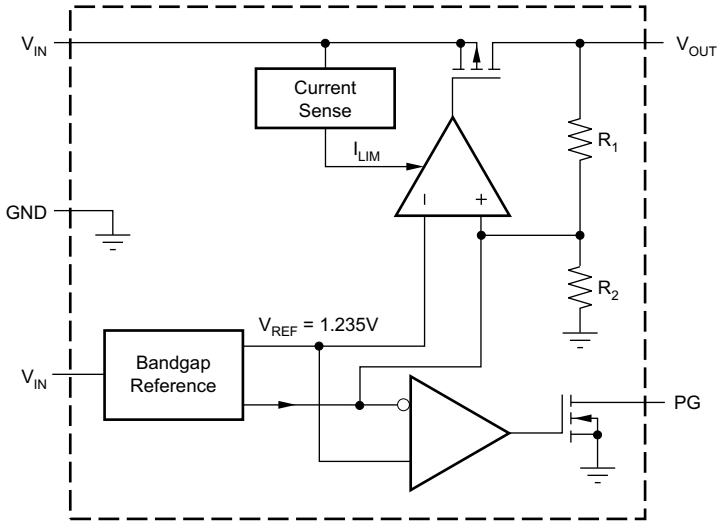
Figure 10. TPS79718 Load Transient Response

7 Detailed Description

7.1 Overview

The TPS797xx devices offer a low-dropout voltage, ultra-low-power operation, and are stable with any capacitor greater than 0.47 µF, and contains an integrated open-drain power good (PG) output.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Regulator Protection

The TPS797xx PMOS-pass transistor has a built-in back diode that conducts reverse current when the input voltage drops below the output voltage (for example, during power down). Current is conducted from the output to the input and is not internally limited. If extended reverse voltage operation is anticipated, external limiting might be appropriate.

The TPS797xx features internal current limiting. During normal operation, the TPS797xx limits output current to approximately 190 mA. When current limiting engages, the output voltage scales back linearly until the overcurrent condition ends. Take care not to exceed the power dissipation ratings of the package.

7.4 Device Functional Modes

Table 1 provides a quick comparison between the normal, dropout, and disabled modes of operation.

Table 1. Device Modes Comparison

OPERATING MODE	PARAMETER	
	V_I	I_{OUTx}
Normal(1)	$V_I > V_O + V_{(DO)}$	$I_{OUTx} < I_{SC}$
Dropout(1)	$V_I < V_O + V_{(DO)}$	$I_{OUTx} < I_{SC}$

(1) All table conditions must be met.

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The TPS797xx family of low-dropout (LDO) regulators are optimized for micropower applications. The family features extremely low dropout voltages and ultra-low quiescent current (typically 1.2-µA).

8.2 Typical Application

8.2.1 Powering Microcontrollers

This device is suited to provide a regulated input voltage and power good (PG) supervisory signal to low-power devices such as mixed-signal microcontrollers. The quiescent (or ground) current of the TPS797xx family is typically 1.2 µA, even at full load; therefore, the reduction in battery life by including the TPS797xx in the system is negligible.

Figure 11 shows an application where the TPS79718 powers TI's MSP430 mixed signal microcontroller.

Minimal board space is required to accommodate the DCK (SC70) packaged TPS79718, the 0.1-µF output capacitor, the 0.47-µF input capacitor, and the pullup resistor on the PG pin.

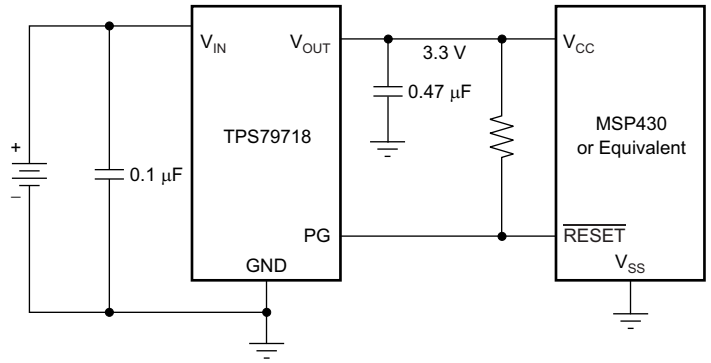


Figure 11. MSP430 Microcontroller Powered by the TPS79718 Regulator Diagram

8.2.1.1 Design Requirements

Table 2 lists the design parameters for this example.

Table 2. Design Parameters

PARAMETER	VALUE
Input voltage range	3.5 V to 5.5 V
Output voltage	3.3 V
Output current rating	50 mA
Minimum output capacitor	0.47 µF

8.2.1.2 Detailed Design Procedure

8.2.1.2.1 External Capacitor Requirements

Although not required, an input bypass capacitor with a value of 0.1-µF or larger (connected between IN and GND and placed close to the TPS797xx) is recommended, especially when a highly resistive power supply is powering the LDO in addition to other devices. Like all low-dropout regulators, the TPS797xx requires an output capacitor connected between OUT and GND to stabilize the internal control loop. The minimum recommended capacitance is 0.47-µF. Any 0.47-µF capacitor is suitable, and capacitor values larger than 0.47-µF are acceptable.

8.2.1.3 Application Curves

over operating temperature range T_J = –40°C to 85°C, typical values are at T_A = 25°C, $V_I = V_O$ (typical) + 0.5 V or 2 V (whichever is greater); I_O = 0.5 mA, $V_{EN} = V_I$, and C_O = 1 µF (unless otherwise noted)

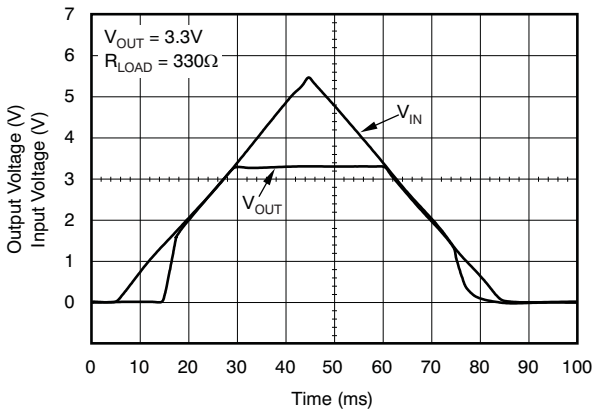


Figure 12. Power Up and Power Down

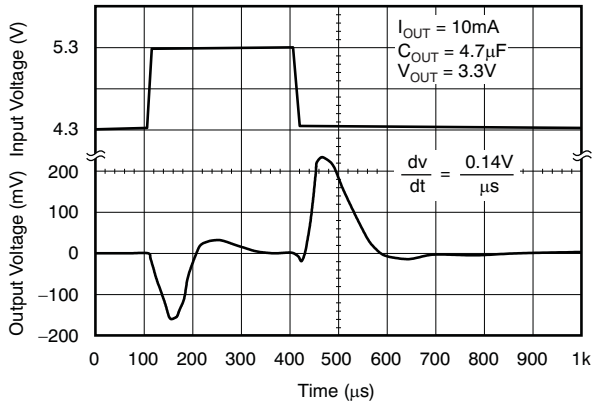


Figure 13. TPS79718 Line Transient Response

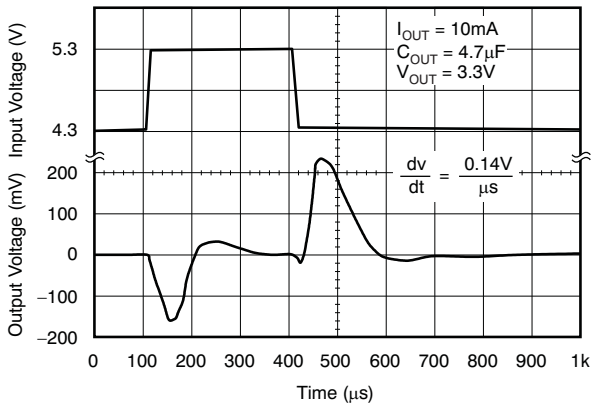


Figure 14. TPS79733 Line Transient Response

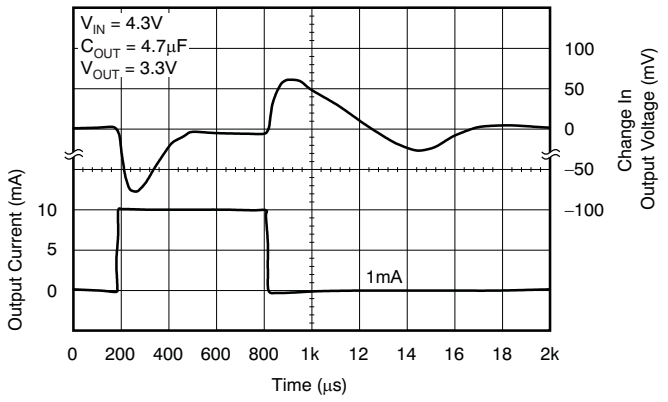


Figure 15. TPS79733 Load Transient Response

9 Power-Supply Recommendations

The TPS797xx is designed to operate from an input voltage range between 1.8 V and 5.5 V. The input voltage range must provide adequate headroom for the device to have a regulated output. This input supply must be well regulated. If the input supply is noisy, additional input capacitors with low ESR can help improve the output noise performance.

10 Layout

10.1 Layout Guidelines

General guidelines for linear regulator designs are to place all circuit components on the same side of the circuit board and as near as practical to the respective LDO pin connections. Place ground return connections to the input and output capacitor, and to the LDO ground pin as close to each other as possible, connected by a wide, component-side, copper surface. The use of vias and long traces to create LDO circuit connections is strongly discouraged and negatively affects system performance.

10.2 Layout Example

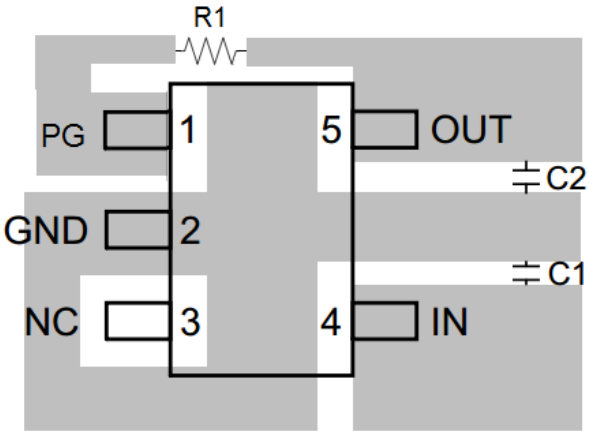


Figure 16. Layout Example

10.3 Power Dissipation and Junction Temperature

Specified regulator operation is ensured for a junction temperature of up to 85°C; restrict the maximum junction temperature to 85°C under normal operating conditions. This restriction limits the power dissipation the regulator can handle in any given application. To ensure the junction temperature is within acceptable limits, calculate the maximum allowable dissipation ($P_{D(MAX)}$) and the actual dissipation (P_D), which must be less than or equal to $P_{D(MAX)}$.

The maximum-power-dissipation limit is determined using Equation 1.

$$P_{D(max)} = \frac{T_J max - T_A}{R_{\theta JA}} \quad (1)$$

where

- $T_{J(max)}$ is the maximum allowable junction temperature
- $R_{\theta JA}$ is the thermal resistance junction-to-ambient for the package (see *Thermal Information*)
- T_A is the ambient temperature

The regulator dissipation is calculated using Equation 2.

$$P_D = (V_I - V_O) \times I_O \quad (2)$$

Power dissipation resulting from quiescent current is negligible.

11 Device and Documentation Support

11.1 Related Links

Table 3 lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 3. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
TPS79718	Click here	Click here	Click here	Click here	Click here
TPS797285	Click here	Click here	Click here	Click here	Click here
TPS79730	Click here	Click here	Click here	Click here	Click here
TPS79733	Click here	Click here	Click here	Click here	Click here

11.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.4 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

11.5 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS79718DCKR	ACTIVE	SC70	DCK	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU | CU NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	ATD	Samples
TPS79718DCKRG4	ACTIVE	SC70	DCK	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	ATD	Samples
TPS79718DCKT	ACTIVE	SC70	DCK	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU | CU NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	ATD	Samples
TPS79718DCKTG4	ACTIVE	SC70	DCK	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	ATD	Samples
TPS797285DCKR	ACTIVE	SC70	DCK	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	OEB	Samples
TPS797285DCKT	ACTIVE	SC70	DCK	5	250	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	OEB	Samples
TPS79730DCKR	ACTIVE	SC70	DCK	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU | CU NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	ATE	Samples
TPS79730DCKRG4	ACTIVE	SC70	DCK	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	ATE	Samples
TPS79730DCKT	ACTIVE	SC70	DCK	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU | CU NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	ATE	Samples
TPS79733DCKR	ACTIVE	SC70	DCK	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU | CU NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	ATF	Samples
TPS79733DCKRG4	ACTIVE	SC70	DCK	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	ATF	Samples
TPS79733DCKT	ACTIVE	SC70	DCK	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU | CU NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	ATF	Samples
TPS79733DCKTG4	ACTIVE	SC70	DCK	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	ATF	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) RoHS: TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

OTHER QUALIFIED VERSIONS OF TPS797 :

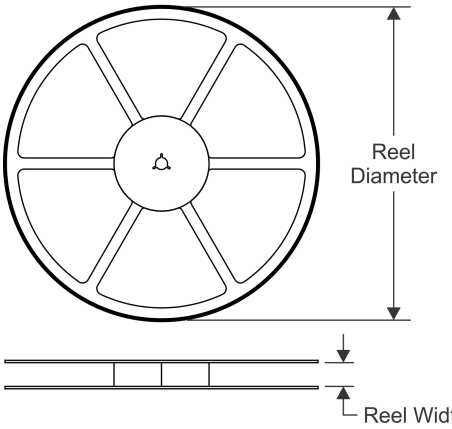
- Automotive: TPS797-Q1

NOTE: Qualified Version Definitions:

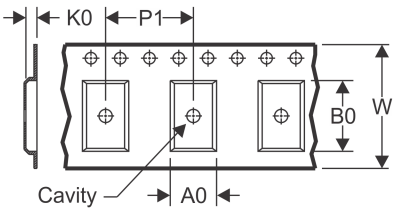
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

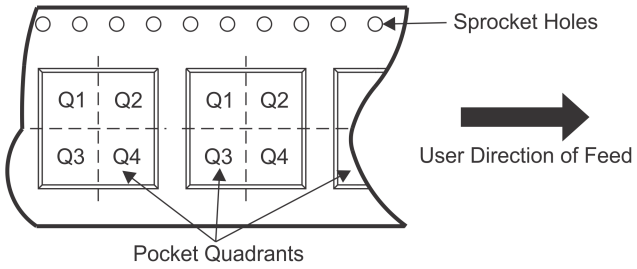


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

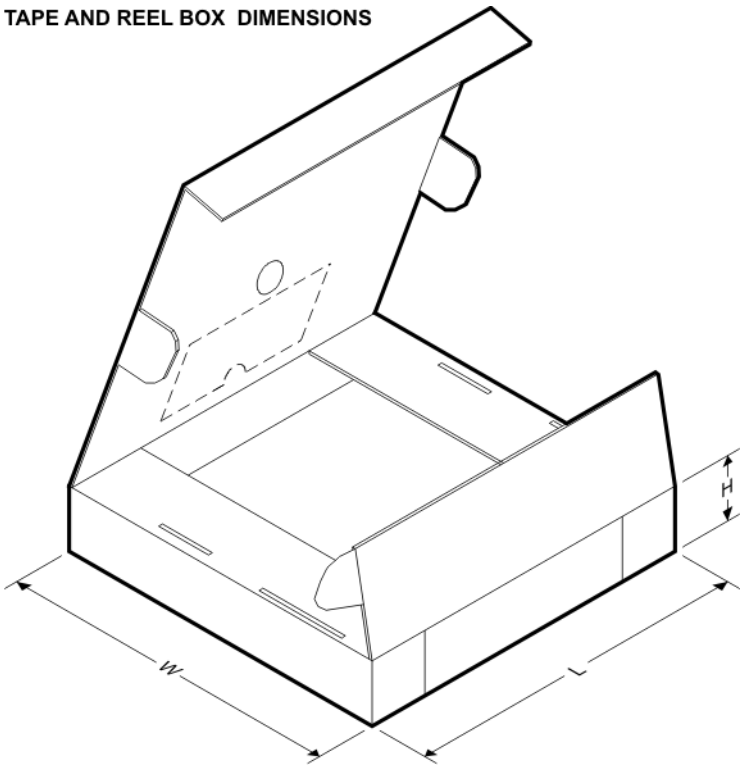
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS79718DCKR	SC70	DCK	5	3000	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
TPS79718DCKR	SC70	DCK	5	3000	180.0	8.4	2.41	2.41	1.2	4.0	8.0	Q3
TPS79718DCKT	SC70	DCK	5	250	180.0	8.4	2.41	2.41	1.2	4.0	8.0	Q3
TPS79718DCKT	SC70	DCK	5	250	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
TPS797285DCKR	SC70	DCK	5	3000	180.0	8.4	2.41	2.41	1.2	4.0	8.0	Q3
TPS797285DCKT	SC70	DCK	5	250	180.0	8.4	2.47	2.3	1.25	4.0	8.0	Q3
TPS79730DCKR	SC70	DCK	5	3000	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
TPS79730DCKR	SC70	DCK	5	3000	180.0	8.4	2.41	2.41	1.2	4.0	8.0	Q3
TPS79730DCKT	SC70	DCK	5	250	180.0	8.4	2.41	2.41	1.2	4.0	8.0	Q3
TPS79730DCKT	SC70	DCK	5	250	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
TPS79733DCKR	SC70	DCK	5	3000	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
TPS79733DCKR	SC70	DCK	5	3000	180.0	8.4	2.41	2.41	1.2	4.0	8.0	Q3
TPS79733DCKT	SC70	DCK	5	250	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
TPS79733DCKT	SC70	DCK	5	250	180.0	8.4	2.41	2.41	1.2	4.0	8.0	Q3

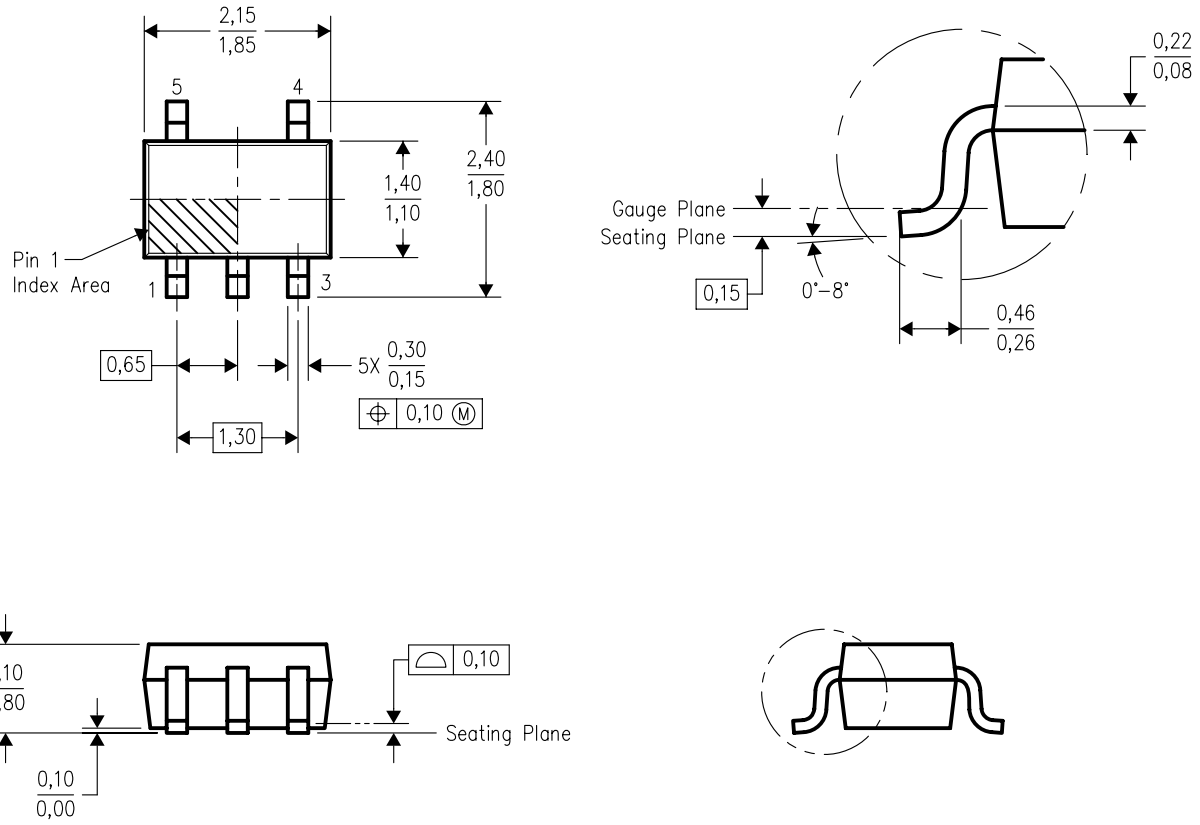
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS79718DCKR	SC70	DCK	5	3000	180.0	180.0	18.0
TPS79718DCKR	SC70	DCK	5	3000	183.0	183.0	20.0
TPS79718DCKT	SC70	DCK	5	250	183.0	183.0	20.0
TPS79718DCKT	SC70	DCK	5	250	180.0	180.0	18.0
TPS797285DCKR	SC70	DCK	5	3000	183.0	183.0	20.0
TPS797285DCKT	SC70	DCK	5	250	183.0	183.0	20.0
TPS79730DCKR	SC70	DCK	5	3000	180.0	180.0	18.0
TPS79730DCKR	SC70	DCK	5	3000	183.0	183.0	20.0
TPS79730DCKT	SC70	DCK	5	250	183.0	183.0	20.0
TPS79730DCKT	SC70	DCK	5	250	180.0	180.0	18.0
TPS79733DCKR	SC70	DCK	5	3000	180.0	180.0	18.0
TPS79733DCKR	SC70	DCK	5	3000	183.0	183.0	20.0
TPS79733DCKT	SC70	DCK	5	250	180.0	180.0	18.0
TPS79733DCKT	SC70	DCK	5	250	183.0	183.0	20.0

DCK (R–PDSO–G5) PLASTIC SMALL–OUTLINE PACKAGE



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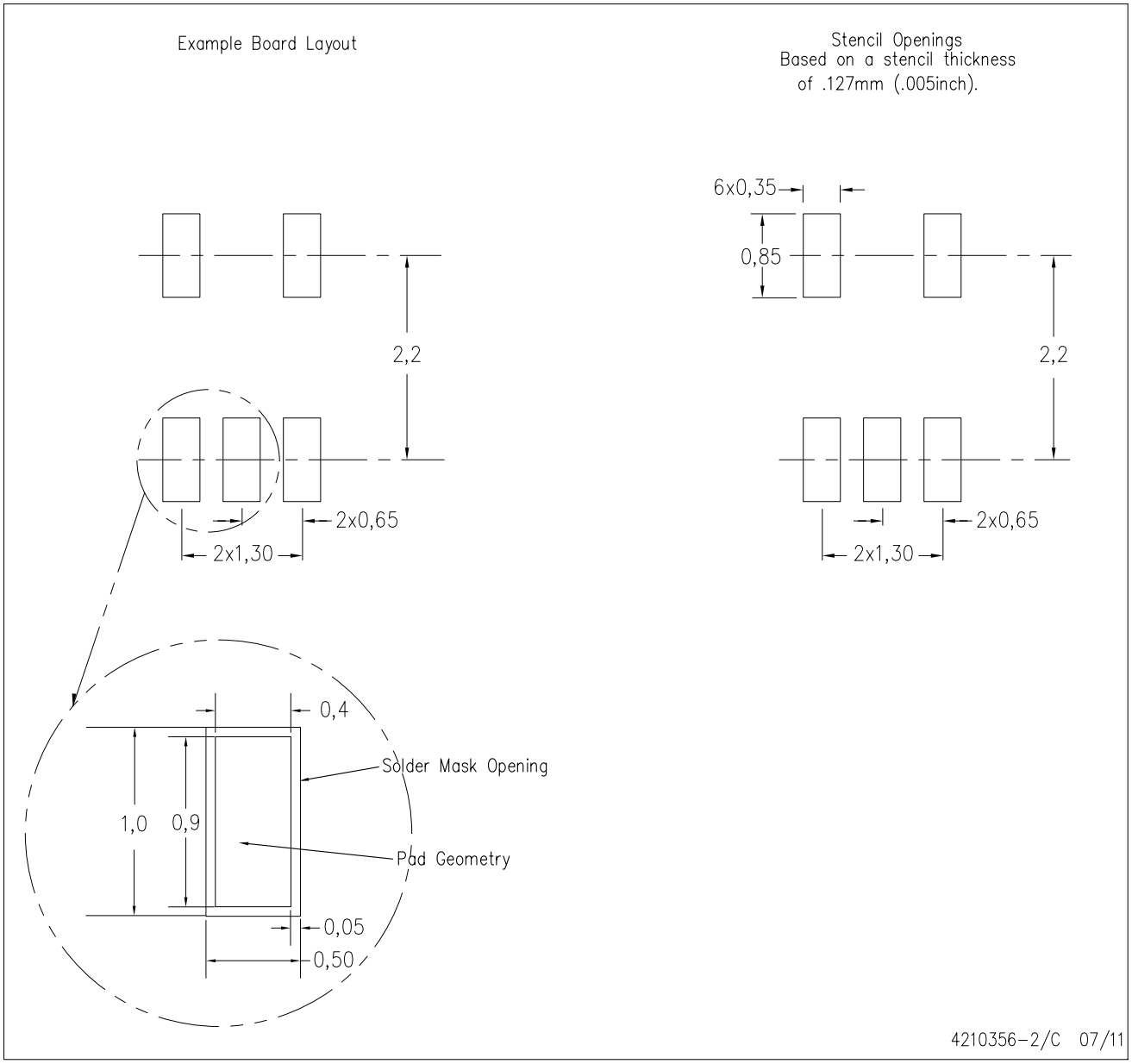
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
D. Falls within JEDEC MO–203 variation AA.

DCK (R–PDSO–G5) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.

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