## FEATURES
- **Input Voltage Range:** −3V to −36V
- **Noise:**
  - $14\mu V_{\text{RMS}}$ (20Hz to 20kHz)
  - $15.1\mu V_{\text{RMS}}$ (10Hz to 100kHz)
- **Power-Supply Ripple Rejection:**
  - 72dB (120Hz)
  - ≥ 55dB (10Hz to 700kHz)
- **Adjustable Output:** −1.18V to −35V
- **Maximum Output Current:** 200mA
- **Dropout Voltage:** 216mV at 100mA
- **Stable with Ceramic Capacitors** ≥ 2.2μF
- **CMOS Logic-Level-Compatible Enable Pin**
- **Built-In, Fixed, Current-Limit and Thermal Shutdown Protection**
- **Available in High Thermal Performance MSOP-8 PowerPAD™ Package**

## APPLICATIONS
- **Supply Rails for Op Amps, DACs, ADCs, and Other High-Precision Analog Circuitry**
- **Audio**
- **Post DC/DC Converter Regulation and Ripple Filtering**
- **Test and Measurement**
- **RX, TX, and PA Circuitry**
- **Industrial Instrumentation**
- **Base Stations and Telecom Infrastructure**
- **−12V and −24V Industrial Buses**

## SUPPORTS DEFENSE, AEROSPACE, AND MEDICAL APPLICATIONS
- **Controlled Baseline**
- **One Assembly/Test Site**
- **One Fabrication Site**
- **Available in Military (−55°C/125°C) Temperature Range**
- **Extended Product Life Cycle**
- **Extended Product-Change Notification**
- **Product Traceability**

### DESCRIPTION
The TPS7A3001 is a negative, high-voltage (−36V), ultralow-noise ($15.1\mu V_{\text{RMS}}, 72$dB PSRR) linear regulator capable of sourcing a maximum load of 200mA.

These linear regulators include a CMOS logic-level-compatible enable pin and capacitor-programmable soft-start function that allows for customized power-management schemes. Other features available include built-in current limit and thermal shutdown protection to safeguard the device and system during fault conditions.

The TPS7A3001 is designed using bipolar technology, and is ideal for high-accuracy, high-precision instrumentation applications where clean voltage rails are critical to maximize system performance. This design makes it an excellent choice to power operational amplifiers, analog-to-digital converters (ADCs), digital-to-analog converters (DACs), and other high-performance analog circuitry.

---

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PowerPAD is a trademark of Texas Instruments.

All other trademarks are the property of their respective owners.
In addition, the TPS7A3001 of linear regulators is suitable for post dc/dc converter regulation. By filtering out the output voltage ripple inherent to dc/dc switching conversion, maximum system performance is provided in sensitive instrumentation, test and measurement, audio, and RF applications.

For applications where positive and negative high-performance rails are required, consider TI's TPS7A49xx family of positive high-voltage, ultralow-noise linear regulators.

**Figure 1. Typical Application**

Post DC/DC Converter Regulation for High-Performance Analog Circuitry
This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

### ORDERING INFORMATION(1)

<table>
<thead>
<tr>
<th>T&lt;sub&gt;J&lt;/sub&gt;</th>
<th>PACKAGE</th>
<th>ORDERABLE PART NUMBER</th>
<th>TOP-SIDE MARKING</th>
<th>VID NUMBER</th>
</tr>
</thead>
<tbody>
<tr>
<td>–55°C to 125°C</td>
<td>DGN</td>
<td>TPS7A3001MDGNTEP</td>
<td>PXCM</td>
<td>V62/11619-01XE</td>
</tr>
</tbody>
</table>

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.

### ABSOLUTE MAXIMUM RATINGS(1)

Over operating free-air temperature range (unless otherwise noted).

<table>
<thead>
<tr>
<th>Voltage</th>
<th>VALUE</th>
<th>MIN</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>IN pin to GND pin</td>
<td>–36</td>
<td>+0.3</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>OUT pin to GND pin</td>
<td>–33</td>
<td>+0.3</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>OUT pin to IN pin</td>
<td>–0.3</td>
<td>+36</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>FB pin to GND pin</td>
<td>–2</td>
<td>+0.3</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>FB pin to IN pin</td>
<td>–0.3</td>
<td>+36</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>EN pin to IN pin</td>
<td>–0.3</td>
<td>+36</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>EN pin to GND pin</td>
<td>–36</td>
<td>+36</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>NR/SS pin to IN pin</td>
<td>–0.3</td>
<td>+36</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>NR/SS pin to GND pin</td>
<td>–2</td>
<td>+0.3</td>
<td>V</td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Current</th>
<th>VALUE</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>Peak output</td>
<td>Internally limited</td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Temperature</th>
<th>VALUE</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>Operating virtual junction, T&lt;sub&gt;J&lt;/sub&gt;</td>
<td>–55</td>
<td>+135</td>
</tr>
<tr>
<td>Storage, T&lt;sub&gt;stg&lt;/sub&gt;</td>
<td>–65</td>
<td>+150</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Electrostatic discharge rating</th>
<th>VALUE</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>Human body model (HBM)</td>
<td>1500</td>
<td>V</td>
</tr>
<tr>
<td>Charged device model (CDM)</td>
<td>500</td>
<td>V</td>
</tr>
</tbody>
</table>

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated is not implied. Exposure to absolute-maximum rated conditions for extended periods may affect device reliability.

### THERMAL INFORMATION

<table>
<thead>
<tr>
<th>THERMAL METRIC(1)</th>
<th>TPS7A3001</th>
<th>UNITS</th>
</tr>
</thead>
<tbody>
<tr>
<td>θ&lt;sub&gt;JA&lt;/sub&gt;</td>
<td>DGN</td>
<td>69.3</td>
</tr>
<tr>
<td>θ&lt;sub&gt;JC(top)&lt;/sub&gt;</td>
<td>40.3</td>
<td></td>
</tr>
<tr>
<td>θ&lt;sub&gt;JB&lt;/sub&gt;</td>
<td>39.0</td>
<td></td>
</tr>
<tr>
<td>Ψ&lt;sub&gt;JT&lt;/sub&gt;</td>
<td>2.4</td>
<td></td>
</tr>
<tr>
<td>Ψ&lt;sub&gt;JB&lt;/sub&gt;</td>
<td>38.7</td>
<td></td>
</tr>
<tr>
<td>θ&lt;sub&gt;JC(bottom)&lt;/sub&gt;</td>
<td>17.8</td>
<td></td>
</tr>
</tbody>
</table>

(1) For more information about traditional and new thermal metrics, see the IC Package Thermal Metrics application report, SPRA953.
### ELECTRICAL CHARACTERISTICS

At $T_J = -55^\circ \text{C}$ to $+125^\circ \text{C}$, $|V_{IN}| = |V_{OUT(NOM)}| + 1.0 \text{V}$ or $|V_{IN}| = 3.0 \text{V}$ (whichever is greater), $V_{EN} = V_{IN}$, $I_{OUT} = 1 \text{mA}$, $C_{IN} = 2.2 \mu \text{F}$, $C_{OUT} = 2.2 \mu \text{F}$, $C_{NR/SS} = 0 \text{nF}$, and the FB pin tied to OUT, unless otherwise noted.

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{IN}$</td>
<td>Input voltage range</td>
<td>$-36.0$</td>
<td>$-3.0$</td>
<td>$V$</td>
<td></td>
</tr>
<tr>
<td>$V_{REF}$</td>
<td>Internal reference</td>
<td>$-1.22$</td>
<td>$-1.184$</td>
<td>$-1.142$</td>
<td>$V$</td>
</tr>
<tr>
<td>$V_{OUT}$</td>
<td>Output voltage range $^{(2)}$</td>
<td>$-35.0$</td>
<td>$V_{REF}$</td>
<td>$V$</td>
<td></td>
</tr>
<tr>
<td>Nominal accuracy</td>
<td>$T_J = +25^\circ \text{C}$, $</td>
<td>V_{IN}</td>
<td>=</td>
<td>V_{OUT(NOM)}</td>
<td>+ 0.5 \text{V}$</td>
</tr>
<tr>
<td>Overall accuracy</td>
<td>$</td>
<td>V_{OUT(NOM)}</td>
<td>= 1.0 \text{V}$ $\leq</td>
<td>V_{IN}</td>
<td>\leq 35 \text{V}$ $1 \text{mA} \leq I_{OUT} \leq 200 \text{mA}$</td>
</tr>
<tr>
<td>$</td>
<td>V_{OUT&gt;(V_{IN})}</td>
<td>$ Line regulation</td>
<td>$T_J = +25^\circ \text{C}$, $</td>
<td>V_{OUT(NOM)}</td>
<td>+ 1.0 \text{V} \leq</td>
</tr>
<tr>
<td>$</td>
<td>V_{OUT&gt;(V_{IN})}</td>
<td>$ Load regulation</td>
<td>$T_J = +25^\circ \text{C}$, $1 \text{mA} \leq I_{OUT} \leq 200 \text{mA}$</td>
<td>$0.04$</td>
<td>$%V_{OUT}$</td>
</tr>
<tr>
<td>$I_{DO}$ Dropout voltage</td>
<td>$V_{IN} = 95%$ $V_{OUT(NOM)}$, $I_{OUT} = 100 \text{mA}$</td>
<td>$216$</td>
<td>$\text{mV}$</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Current limit</td>
<td>$V_{OUT} = 90%$ $V_{OUT(NOM)}$</td>
<td>$220$</td>
<td>$330$</td>
<td>$500$</td>
<td>$\text{mA}$</td>
</tr>
<tr>
<td>$I_{GND}$ Ground current</td>
<td>$I_{OUT} = 0 \text{mA}$</td>
<td>$55$</td>
<td>$100$</td>
<td>$\mu \text{A}$</td>
<td></td>
</tr>
<tr>
<td>$I_{GND}$</td>
<td>$I_{OUT} = 100 \text{mA}$</td>
<td>$950$</td>
<td>$\mu \text{A}$</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$I_{SHDN}$ Shutdown supply current</td>
<td>$V_{EN} = +0.4 \text{V}$</td>
<td>$1.0$</td>
<td>$3.0$</td>
<td>$\mu \text{A}$</td>
<td></td>
</tr>
<tr>
<td>$I_{SHDN}$</td>
<td>$V_{EN} = -0.4 \text{V}$</td>
<td>$1.0$</td>
<td>$3.0$</td>
<td>$\mu \text{A}$</td>
<td></td>
</tr>
<tr>
<td>$I_{FB}$ Feedback current $^{(3)}$</td>
<td></td>
<td>$14$</td>
<td>$100$</td>
<td>$\text{nA}$</td>
<td></td>
</tr>
<tr>
<td>$I_{EN}$ Enable current</td>
<td>$V_{EN} =</td>
<td>V_{IN}</td>
<td>=</td>
<td>V_{OUT(NOM)}</td>
<td>+ 1.0 \text{V}$</td>
</tr>
<tr>
<td>$I_{EN}$</td>
<td>$V_{IN} = V_{EN} = -35 \text{V}$</td>
<td>$0.51$</td>
<td>$1.0$</td>
<td>$\mu \text{A}$</td>
<td></td>
</tr>
<tr>
<td>$I_{EN}$</td>
<td>$V_{IN} = -35 \text{V}, V_{EN} = +15 \text{V}$</td>
<td>$0.50$</td>
<td>$1.2$</td>
<td>$\mu \text{A}$</td>
<td></td>
</tr>
<tr>
<td>$V_{EN HI}$ Positive enable high-level voltage</td>
<td>$T_J = -55^\circ \text{C}$ to $+125^\circ \text{C}$</td>
<td>$+2.0$</td>
<td>$+15$</td>
<td>$\text{V}$</td>
<td></td>
</tr>
<tr>
<td>$V_{EN LO}$ Positive enable low-level voltage</td>
<td>$0$</td>
<td>$+0.4$</td>
<td>$\text{V}$</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$V_{EN HI}$ Negative enable high-level voltage</td>
<td>$V_{IN}$</td>
<td>$-2.0$</td>
<td>$\text{V}$</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$V_{EN LO}$ Negative enable low-level voltage</td>
<td>$-0.4$</td>
<td>$0$</td>
<td>$\text{V}$</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$V_{NOISE}$ Output noise voltage</td>
<td>$V_{IN} = -3 \text{V}, V_{OUT(NOM)} = V_{REF}, C_{OUT} = 10 \mu \text{F}$, $C_{NR/SS} = 10 \mu \text{F}, \text{BW} = 10 \text{Hz to } 100 \text{kHz}$</td>
<td>$15.1$</td>
<td>$\mu \text{VRMS}$</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$V_{NOISE}$</td>
<td>$V_{IN} = -6.2 \text{V}, V_{OUT(NOM)} = -5 \text{V}, C_{OUT} = 10 \mu \text{F}$, $C_{NR/SS} = C_{BYP} = 10 \mu \text{F}, \text{BW} = 10 \text{Hz to } 100 \text{kHz}$</td>
<td>$17.5$</td>
<td>$\mu \text{VRMS}$</td>
<td></td>
<td></td>
</tr>
<tr>
<td>PSRR Power-supply rejection ratio</td>
<td>$V_{IN} = -6.2 \text{V}, V_{OUT(NOM)} = -5 \text{V}, C_{OUT} = 10 \mu \text{F}$, $C_{NR/SS} = C_{BYP} = 10 \mu \text{F}, f = 120 \text{Hz}$</td>
<td>$72$</td>
<td>$\text{dB}$</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$T_{SD}$ Thermal shutdown temperature</td>
<td>Shutdown, temperature increasing</td>
<td>$+170$</td>
<td>$\degree \text{C}$</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$T_{SD}$</td>
<td>Reset, temperature decreasing</td>
<td>$+150$</td>
<td>$\degree \text{C}$</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$T_J$ Operating junction temperature range</td>
<td>$-55$</td>
<td>$+125$</td>
<td>$\degree \text{C}$</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

$^{(1)}$ At operating conditions, $V_{IN} \leq 0 \text{V}$, $V_{OUT(NOM)} \leq V_{REF} \leq 0 \text{V}$. At regulation, $V_{IN} \leq V_{OUT(NOM)} - |V_{DO}|$, $I_{OUT} > 0$ flows from OUT to IN.

$^{(2)}$ To ensure stability at no load conditions, a current from the feedback resistive network equal to or greater than $5 \mu \text{A}$ is required.

$^{(3)}$ $I_{FB} > 0$ flows into the device.

$^{(4)}$ $C_{BYP}$ refers to a bypass capacitor connected to the FB and OUT pins.
FUNCTIONAL BLOCK DIAGRAM

Where:
\[ V_{OUT} = \frac{R_1 + R_2}{R_1} \left( \frac{V_{OUT}}{V_{REF}} - 1 \right) \]

Maximize PSRR Performance and Minimize RMS Noise
PIN CONFIGURATION

DGN PACKAGE
MSOP-8
(TOP VIEW)

OUT 1 2 3 4 5 6 7 8 IN
FB 2 3 4 5 6 7 8 DNC
NC 3 4 5 6 7 8 NR/SS
GND 4 5 6 7 8 9 EN

PIN DESCRIPTIONS

<table>
<thead>
<tr>
<th>NAME</th>
<th>NO.</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>OUT</td>
<td>1</td>
<td>Regulator output. A capacitor $\geq 2.2\mu F$ must be tied from this pin to ground to assure stability.</td>
</tr>
<tr>
<td>FB</td>
<td>2</td>
<td>This pin is the input to the control-loop error amplifier. It is used to set the output voltage of the device.</td>
</tr>
<tr>
<td>NC</td>
<td>3</td>
<td>Not internally connected. This pin must either be left open or tied to GND.</td>
</tr>
<tr>
<td>GND</td>
<td>4</td>
<td>Ground</td>
</tr>
<tr>
<td>EN</td>
<td>5</td>
<td>This pin turns the regulator on or off. If $V_{EN} \geq V_{EN,HI}$ or $V_{EN} \leq V_{EN,HI}$, the regulator is enabled. If $V_{EN,LO} \geq V_{EN} \geq V_{EN,LO}$, the regulator is disabled. The EN pin can be connected to IN, if not used. $</td>
</tr>
<tr>
<td>NR/SS</td>
<td>6</td>
<td>Noise reduction pin. Connecting an external capacitor to this pin bypasses noise generated by the internal bandgap. This capacitor allows RMS noise to be reduced to very low levels and also controls the soft-start function.</td>
</tr>
<tr>
<td>DNC</td>
<td>7</td>
<td><strong>DO NOT CONNECT.</strong> Do not route this pin to any electrical net, not even GND or IN.</td>
</tr>
<tr>
<td>IN</td>
<td>8</td>
<td>Input supply</td>
</tr>
<tr>
<td>PowerPAD</td>
<td></td>
<td>Must either be left open or tied to GND. Solder to printed circuit board (PCB) plane to enhance thermal performance.</td>
</tr>
</tbody>
</table>
TYPICAL CHARACTERISTICS

At $T_J = -55^\circ C$ to $+125^\circ C$, $|V_{IN}| = |V_{OUT(NOM)}| + 1.0V$ or $|V_{IN}| = 3.0V$ (whichever is greater), $V_{EN} = V_{IN}$, $I_{OUT} = 1mA$, $C_{IN} = 2.2\mu F$, $C_{OUT} = 2.2\mu F$, $C_{NR/SS} = 0nF$, and the FB pin tied to OUT, unless otherwise noted.

- FEEDBACK VOLTAGE vs INPUT VOLTAGE
- FEEDBACK CURRENT vs TEMPERATURE
- GROUND CURRENT vs VIN
- GROUND CURRENT vs OUT
- GROUND CURRENT vs EN
- ENABLE CURRENT vs EN

Figure 2.
Figure 3.
Figure 4.
Figure 5.
Figure 6.
Figure 7.

Copyright © 2011, Texas Instruments Incorporated
Submit Documentation Feedback
TYPICAL CHARACTERISTICS (continued)

At $T_J = -55^\circ\text{C}$ to $+125^\circ\text{C}$, $|V_{\text{IN}}| = |V_{\text{OUT(NOM)}}| + 1.0\text{V}$ or $|V_{\text{IN}}| = 3.0\text{V}$ (whichever is greater), $V_{\text{EN}} = V_{\text{IN}}$, $I_{\text{OUT}} = 1\text{mA}$, $C_{\text{IN}} = 2.2\mu\text{F}$, $C_{\text{OUT}} = 2.2\mu\text{F}$, $C_{\text{NR/SS}} = 0\text{F}$, and the FB pin tied to OUT, unless otherwise noted.

QUIESCENT CURRENT vs INPUT VOLTAGE

SHUTDOWN CURRENT vs INPUT VOLTAGE

DROPOUT VOLTAGE vs OUTPUT CURRENT

DROPOUT VOLTAGE vs TEMPERATURE

CURRENT LIMIT vs INPUT VOLTAGE

CURRENT LIMIT vs TEMPERATURE

Submit Documentation Feedback

Copyright © 2011, Texas Instruments Incorporated
TYPICAL CHARACTERISTICS (continued)

At $T_J = -55^\circ$C to $+125^\circ$C, $|V_{IN}| = |V_{OUT(NOM)}| + 1.0$V or $|V_{IN}| = 3.0$V (whichever is greater), $V_{EN} = V_{IN}$, $I_{OUT} = 1$mA, $C_{IN} = 2.2\mu$F, $C_{OUT} = 2.2\mu$F, $C_{NR/SS} = 0$F, and the FB pin tied to OUT, unless otherwise noted.

**ENABLE THRESHOLD VOLTAGE vs TEMPERATURE**

![Figure 14.]

**LINE REGULATION**

![Figure 16.]

**LOAD REGULATION**

![Figure 18.]

**POWER-SUPPLY REJECTION RATIO vs $C_{OUT}$**

![Figure 15.]

**POWER-SUPPLY REJECTION RATIO vs $C_{NR/SS}$**

![Figure 17.]

**POWER-SUPPLY REJECTION RATIO vs $C_{BYP}$**

![Figure 19.]

Copyright © 2011, Texas Instruments Incorporated
TYPICAL CHARACTERISTICS (continued)

At $T_J = -55^\circ\text{C}$ to $+125^\circ\text{C}$, $|V_{IN}| = |V_{OUT(NOM)}| + 1.0\text{V}$ or $|V_{IN}| = 3.0\text{V}$ (whichever is greater), $V_{REN} = V_{IN}$, $I_{OUT} = 1\text{mA}$, $C_{IN} = 2.2\mu\text{F}$, $C_{OUT} = 2.2\mu\text{F}$, $C_{NR/SS} = 0\text{nF}$, and the FB pin tied to OUT, unless otherwise noted.

### OUTPUT SPECTRAL NOISE DENSITY vs OUTPUT CURRENT

![Figure 20. Output Spectral Noise Density vs Output Current](image)

<table>
<thead>
<tr>
<th>$I_{OUT}$</th>
<th>RMS Noise</th>
</tr>
</thead>
<tbody>
<tr>
<td>$1\text{mA}$</td>
<td>15.13</td>
</tr>
<tr>
<td>$200\text{mA}$</td>
<td>17.13</td>
</tr>
</tbody>
</table>

### OUTPUT SPECTRAL NOISE DENSITY vs $C_{NR/SS}$

![Figure 21. Output Spectral Noise Density vs $C_{NR/SS}$](image)

<table>
<thead>
<tr>
<th>$C_{NR/SS}$</th>
<th>RMS Noise</th>
</tr>
</thead>
<tbody>
<tr>
<td>$0\text{nF}$</td>
<td>80.00</td>
</tr>
<tr>
<td>$10\text{nF}$</td>
<td>17.29</td>
</tr>
</tbody>
</table>

### OUTPUT SPECTRAL NOISE DENSITY vs $V_{OUT(NOM)}$

![Figure 22. Output Spectral Noise Density vs $V_{OUT(NOM)}$](image)

<table>
<thead>
<tr>
<th>$V_{OUT(NOM)}$</th>
<th>RMS Noise</th>
</tr>
</thead>
<tbody>
<tr>
<td>$-5\text{V}$</td>
<td>17.50</td>
</tr>
<tr>
<td>$-1.2\text{V}$</td>
<td>15.13</td>
</tr>
</tbody>
</table>
TYPICAL CHARACTERISTICS (continued)

At $T_J = -55°C$ to $+125°C$, $|V_{IN}| = |V_{OUT(NOM)}| + 1.0V$ or $|V_{IN}| = 3.0V$ (whichever is greater), $V_{EN} = V_{IN}$, $I_{OUT} = 1mA$, $C_{IN} = 2.2\mu F$, $C_{OUT} = 2.2\mu F$, $C_{NR/SS} = 0nF$, and the FB pin tied to OUT, unless otherwise noted.

CAPACITOR-PROGRAMMABLE SOFT START

- $V_{OUT} = -1.2V$
- $V_{IN} = -3V$
- $I_{OUT} = 1mA$
- $C_{IN} = C_{OUT} = 2.2\mu F$
- $C_{NR/SS} = 0pF$

Time (10us/div)

Figure 23.

CAPACITOR-PROGRAMMABLE SOFT START

- $V_{OUT} = -1.2V$
- $V_{IN} = -3V$
- $I_{OUT} = 1mA$
- $C_{IN} = C_{OUT} = 2.2\mu F$
- $C_{NR/SS} = 0pF$

Time (20us/div)

Figure 24.

CAPACITOR-PROGRAMMABLE SOFT START

- $V_{OUT} = -1.2V$
- $V_{IN} = -3V$
- $I_{OUT} = 1mA$
- $C_{IN} = C_{OUT} = 2.2\mu F$
- $C_{NR/SS} = 10nF$

Time (1ms/div)

Figure 25.

CAPACITOR-PROGRAMMABLE SOFT START

- $V_{OUT} = -1.2V$
- $V_{IN} = -3V$
- $I_{OUT} = 1mA$
- $C_{IN} = C_{OUT} = 2.2\mu F$
- $C_{NR/SS} = 100pF$

Time (1ms/div)

Figure 26.

LINE TRANSIENT RESPONSE

- $V_{IN} = -20V$ to $-4.3V$
- $I_{OUT} = 200mA$
- $C_{OUT} = 2.2\mu F$

Time (10us/div)

Figure 27.

LINE TRANSIENT RESPONSE

- $V_{IN} = -4.3V$ to $-20V$
- $I_{OUT} = 200mA$
- $C_{OUT} = 2.2\mu F$

Time (10us/div)

Figure 28.
TYPICAL CHARACTERISTICS (continued)

At $T_J = -55^\circ C$ to $+125^\circ C$, $|V_{IN}| = |V_{OUT(NOM)}| + 1.0V$ or $|V_{IN}| = 3.0V$ (whichever is greater), $V_{EN} = V_{IN}$, $I_{OUT} = 1mA$, $C_{IN} = 2.2\mu F$, $C_{OUT} = 2.2\mu F$, $C_{NR/SS} = 0nF$, and the FB pin tied to OUT, unless otherwise noted.

**LOAD TRANSIENT RESPONSE**

![Graph showing load transient response](image_url)

*Figure 29.*
THEORY OF OPERATION

GENERAL DESCRIPTION

The TPS7A3001 belongs to a family of new generation linear regulators that use an innovative bipolar process to achieve ultralow-noise and very high PSRR levels at a wide input voltage range. These features, combined with a high thermal performance MSOP-8 with PowerPAD package make this device ideal for high-performance analog applications.

ADJUSTABLE OPERATION

The TPS7A3001 has an output voltage range of −1.174 to −35V. The nominal output voltage of the device is set by two external resistors, as shown in Figure 30.

\[
R_1 = R_2 \left( \frac{V_{\text{OUT}}}{V_{\text{REF}}} - 1 \right), \text{ where } \frac{V_{\text{OUT}}}{R_1 + R_2} \geq 5 \mu\text{A}
\]

(1)

If greater voltage accuracy is required, take into account the output voltage offset contributions because of the feedback pin current and use 0.1% tolerance resistors.

ENABLE PIN OPERATION

The TPS7A3001 provides a dual polarity enable pin (EN) that turns on the regulator when \(|V_{\text{EN}}| > 2.0\text{V}\), whether the voltage is positive or negative, as shown in Figure 31.

This functionality allows for different system power management topologies:

- Connecting the EN pin directly to a negative voltage, such as \(V_{\text{IN}}\), or
- Connecting the EN pin directly to a positive voltage, such as the output of digital logic circuitry.

Figure 30. Adjustable Operation for Maximum AC Performance

Figure 31. Enable Pin Positive/Negative Threshold
CAPACITOR RECOMMENDATIONS
Low ESR capacitors should be used for the input, output, noise reduction, and bypass capacitors. Ceramic capacitors with X7R and X5R dielectrics are preferred. These dielectrics offer more stable characteristics. Ceramic X7R capacitors offer improved over-temperature performance, while ceramic X5R capacitors are the most cost-effective and are available in higher values.

Note that high ESR capacitors may degrade PSRR.

INPUT AND OUTPUT CAPACITOR REQUIREMENTS
This negative, high-voltage linear regulator achieves stability with a minimum input and output capacitance of 2.2μF; however, it is highly recommended to use a 10μF capacitor to maximize ac performance.

NOISE REDUCTION AND BYPASS CAPACITOR REQUIREMENTS
Although noise reduction and bypass capacitors (C_{NR/SS} and C_{BYP}, respectively) are not needed to achieve stability, it is highly recommended to use 0.01μF capacitors to minimize noise and maximize ac performance.

MAXIMUM AC PERFORMANCE
In order to maximize noise and PSRR performance, it is recommended to include 10μF or higher input and output capacitors, and 0.01μF noise reduction and bypass capacitors, as shown in Figure 30. The solution shown delivers minimum noise levels of 15.1μV_{RMS} and power-supply rejection levels above 55dB from 10Hz to 700kHz; see Figure 19 and Figure 20.

OUTPUT NOISE
The TPS7A3001 provides low output noise when a noise reduction capacitor (C_{NR/SS}) is used.

The noise reduction capacitor serves as a filter for the internal reference. By using a 0.01μF noise reduction capacitor, the output noise is reduced by almost 80% (from 80μV_{RMS} to 17μV_{RMS}); see Figure 21.

TPS7A3001 low output voltage noise makes it an ideal solution for powering noise-sensitive circuitry.

POWER-SUPPLY REJECTION
The 0.01μF noise reduction capacitor greatly improves TPS7A3001 power-supply rejection, achieving up to 20dB of additional power-supply rejection for frequencies between 110Hz and 400KHz.

Additionally, ac performance can be maximized by adding a 0.01μF bypass capacitor (C_{BYP}) from the FB pin to the OUT pin. This capacitor greatly improves power-supply rejection at lower frequencies, for the band from 10Hz to 200kHz; see Figure 19.

The very high power-supply rejection of the TPS7A3001 makes it a good choice for powering high-performance analog circuitry, such as operational amplifiers, ADGs, DACS, and audio amplifiers.

TRANSIENT RESPONSE
As with any regulator, increasing the size of the output capacitor reduces over/undershoot magnitude but increases duration of the transient response.
APPLICATION INFORMATION

POWER FOR PRECISION ANALOG

One of the primary TPS7A3001 applications is to provide ultralow noise voltage rails to high-performance analog circuitry in order to maximize system accuracy and precision.

In conjunction with its positive counterpart, the TPS7A49xx family of positive high-voltage linear regulators, this negative high voltage linear regulator provides ultralow noise positive and negative voltage rails to high-performance analog circuitry, such as operational amplifiers, ADCs, DACs, and audio amplifiers.

Because of the ultralow noise levels at high voltages, analog circuitry with high-voltage input supplies can be used. This characteristic allows for high-performance analog solutions to optimize the voltage range, maximizing system accuracy.

POST DC/DC CONVERTER FILTERING

Most of the time, the voltage rails available in a system do not match the voltage specifications demanded by one or more of its circuits; these rails must be stepped up or down, depending on specific voltage requirements.

DC/DC converters are the preferred solution to step up or down a voltage rail when current consumption is not negligible. They offer high efficiency with minimum heat generation, but they have one primary disadvantage: they introduce a high-frequency component, and the associated harmonics, on top of the dc output signal.

This high-frequency component, if not filtered properly, degrades analog circuitry performance, reducing overall system accuracy and precision.

The TPS7A3001 offers a wide-bandwidth, very-high power-supply rejection ratio. This specification makes it ideal for post dc/dc converter filtering, as shown in Figure 32. It is highly recommended to use the maximum performance schematic shown in Figure 30. Also, verify that the fundamental frequency (and its first harmonic, if possible) is within the bandwidth of the regulator PSRR, shown in Figure 19.

![Figure 32. Post DC/DC Converter Regulation to High-Performance Analog Circuitry](image)

AUDIO APPLICATIONS

Audio applications are extremely sensitive to any distortion and noise in the audio band from 20Hz to 20kHz. This stringent requirement demands clean voltage rails to power critical high-performance audio systems.

The very-high power-supply rejection ratio (> 55dB) and low noise at the audio band of the TPS7A3001 maximize performance for audio applications; see Figure 19.
PACKAGE MOUNTING

Solder pad footprint recommendations for the TPS7A3001 are available at the end of this product datasheet and at www.ti.com.

BOARD LAYOUT RECOMMENDATIONS TO IMPROVE PSRR AND NOISE PERFORMANCE

To improve ac performance such as PSRR, output noise, and transient response, it is recommended that the board be designed with separate ground planes for IN and OUT, with each ground plane connected only at the GND pin of the device. In addition, the ground connection for the output capacitor should connect directly to the GND pin of the device.

Equivalent series inductance (ESL) and equivalent series resistance (ESR) must be minimized in order to maximize performance and ensure stability. Every capacitor (C_{IN}, C_{OUT}, C_{NR/SS}, C_{BYP}) must be placed as close as possible to the device and on the same side of the printed circuit board (PCB) as the regulator itself.

Do not place any of the capacitors on the opposite side of the PCB from where the regulator is installed. The use of vias and long traces is strongly discouraged because they may impact system performance negatively and even cause instability.

If possible, and to ensure the maximum performance denoted in this product datasheet, use the same layout pattern used for TPS7A30 evaluation board, available at www.ti.com.

THERMAL PROTECTION

Thermal protection disables the output when the junction temperature rises to approximately +170°C, allowing the device to cool. When the junction temperature cools to approximately +150°C, the output circuitry is enabled. Depending on power dissipation, thermal resistance, and ambient temperature, the thermal protection circuit may cycle on and off. This cycling limits the dissipation of the regulator, protecting it from damage as a result of overheating.

Any tendency to activate the thermal protection circuit indicates excessive power dissipation or an inadequate heatsink. For reliable operation, junction temperature should be limited to a maximum of +125°C. To estimate the margin of safety in a complete design (including heatsink), increase the ambient temperature until the thermal protection is triggered; use worst-case loads and signal conditions. For good reliability, thermal protection should trigger at least +35°C above the maximum expected ambient condition of your particular application. This configuration produces a worst-case junction temperature of +125°C at the highest expected ambient temperature and worst-case load.

The internal protection circuitry of the TPS7A3001 has been designed to protect against overload conditions. It was not intended to replace proper heatsinking. Continuously running the TPS7A3001 into thermal shutdown degrades device reliability.

POWER DISSIPATION

The ability to remove heat from the die is different for each package type, presenting different considerations in the PCB layout. The PCB area around the device that is free of other components moves the heat from the device to the ambient air. Using heavier copper increases the effectiveness in removing heat from the device. The addition of plated through-holes to heat dissipating layers also improves the heatsink effectiveness.

Power dissipation depends on input voltage and load conditions. Power dissipation (P_D) is equal to the product of the output current times the voltage drop across the output pass element, as shown in Equation 2:

\[ P_D = (V_{IN} - V_{OUT}) I_{OUT} \]  

SUGGESTED LAYOUT AND SCHEMATIC

Layout is a critical part of good power-supply design. There are several signal paths that conduct fast-changing currents or voltages that can interact with stray inductance or parasitic capacitance to generate noise or degrade the power-supply performance. To help eliminate these problems, the IN pin should be bypassed to ground with a low ESR ceramic bypass capacitor with a X5R or X7R dielectric.
The GND pin should be tied directly to the PowerPAD under the IC. The PowerPAD should be connected to any internal PCB ground planes using multiple vias directly under the IC.

It may be possible to obtain acceptable performance with alternate PCB layouts; however, the layout shown in Figure 33 and the schematic shown in Figure 34 have been shown to produce good results and are meant as a guideline.

**Figure 33. PCB Layout Example**

**Figure 34. Schematic for PCB Layout Example**
PACKAGING INFORMATION

<table>
<thead>
<tr>
<th>Orderable Device</th>
<th>Status (1)</th>
<th>Package Type</th>
<th>Package Drawing</th>
<th>Pins</th>
<th>Package Qty</th>
<th>Eco Plan (2)</th>
<th>Lead/Ball Finish (3)</th>
<th>MSL Peak Temp</th>
<th>Op Temp (°C)</th>
<th>Device Marking (4/5)</th>
<th>Samples</th>
</tr>
</thead>
<tbody>
<tr>
<td>TPS7A3001MDGNTEP</td>
<td>ACTIVE</td>
<td>HVSSOP</td>
<td>DGN</td>
<td>8</td>
<td>250</td>
<td>Green (RoHS &amp; no Sb/Br)</td>
<td>CU NIPDAU</td>
<td>Level-2-260C-1 YEAR</td>
<td>-55 to 125</td>
<td>PXCM</td>
<td>Samples</td>
</tr>
<tr>
<td>V62/11619-01XE</td>
<td>ACTIVE</td>
<td>HVSSOP</td>
<td>DGN</td>
<td>8</td>
<td>250</td>
<td>Green (RoHS &amp; no Sb/Br)</td>
<td>CU NIPDAU</td>
<td>Level-2-260C-1 YEAR</td>
<td>-55 to 125</td>
<td>PXCM</td>
<td>Samples</td>
</tr>
</tbody>
</table>

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) RoHS: TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.
### TAPE AND REEL INFORMATION

<table>
<thead>
<tr>
<th>Device</th>
<th>Package Type</th>
<th>Package Drawing</th>
<th>Pins</th>
<th>SPQ</th>
<th>Reel Diameter (mm)</th>
<th>Reel Width W1 (mm)</th>
<th>A0 (mm)</th>
<th>B0 (mm)</th>
<th>K0 (mm)</th>
<th>P1 (mm)</th>
<th>W (mm)</th>
<th>Pin1 Quadrant</th>
</tr>
</thead>
<tbody>
<tr>
<td>TPS7A3001MDGNTEP</td>
<td>HVSSOP</td>
<td>DGN</td>
<td>8</td>
<td>250</td>
<td>180.0</td>
<td>12.4</td>
<td>5.3</td>
<td>3.4</td>
<td>1.4</td>
<td>8.0</td>
<td>12.0</td>
<td>Q1</td>
</tr>
</tbody>
</table>

*All dimensions are nominal.*

---

*Dimensions designed to accommodate the component width,*

*Dimension designed to accommodate the component length,*

*Dimension designed to accommodate the component thickness,*

*Overall width of the carrier tape,*

*Pitch between successive cavity centers.*
## TAPE AND REEL BOX DIMENSIONS

*All dimensions are nominal

<table>
<thead>
<tr>
<th>Device</th>
<th>Package Type</th>
<th>Package Drawing</th>
<th>Pins</th>
<th>SPQ</th>
<th>Length (mm)</th>
<th>Width (mm)</th>
<th>Height (mm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>TPS7A3001MDGNTEP</td>
<td>HVSSOP</td>
<td>DGN</td>
<td>8</td>
<td>250</td>
<td>210.0</td>
<td>185.0</td>
<td>35.0</td>
</tr>
</tbody>
</table>
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http://www.ti.com>.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Falls within JEDEC MO-187 variation AA-T

PowerPAD is a trademark of Texas Instruments.

Texas Instruments
www.ti.com
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.

PowerPAD is a trademark of Texas Instruments.
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.
NOTES: (continued)

10. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate
design recommendations.
11. Board assembly site may have different recommendations for stencil design.
IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to TI's Terms of Sale (www.ti.com/legal/termsofsale.html) or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2019, Texas Instruments Incorporated