1A Peak Sink/Source PCDDR3 Termination Regulator with Integrated Isolation Switch and Low Power Mode Operation

Check for Samples: TS3DDR32611

FEATURES

- **VDD Range – 3.0V to 3.6V**
- **R_{ON} 1.75Ω typical**
- **Channel Count – 26**
- **V_{DDQ} – Input Voltage 1.2V to 3.5V**
- **V_{TT} – V_{DDQ}/2 typical with 1A sink/source capability**
- **V_{REF} – V_{DDQ}/2±1% × V_{DDQ}**
- **Switch Time – ($T_{ON/OFF}$) 100ns Max**
- **I_{DD} Supply Current**
  - **High Speed Mode ($I_{DD,HS}$) 220 µA Max**
  - **Low Speed Mode ($I_{DD,LS}$) 220 µA Max**
  - **Power Down Mode ($I_{DD,PD}$) 5 µA Max**
- **Special Features**
  - **1.8-V Compatible Control Inputs (VTT_EN, ODT_EN)**
  - **High current Sinking/Sourcing Capability: 1A Max**
- **48-Ball ZQC Package (4mm x 4mm, 0.5mm pitch)**

APPLICATIONS

- **Double Data Rate type 3 (PCDDR3) termination and regulation in mobile devices**

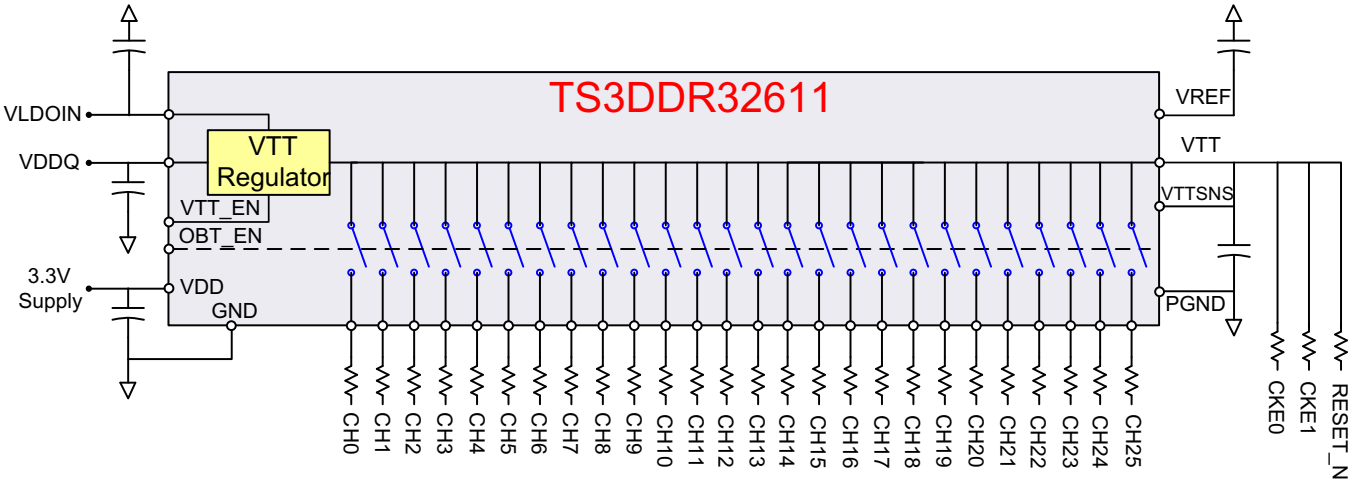
DESCRIPTION

The TS3DDR32611 is a sink/source double data rate type III (PCDDR3) termination regulator with a 1% accuracy buffered reference output. It has built-in termination SPST switches that can be disconnected when the memory system undergoes lower speed operation without the need of voltage termination. Turning off these switches enables significant power saving on the memory system. The switches on-state resistance has a typical value of only 1.75Ω which helps retain signal integrity on the signal lines.

The TS3DDR32611 is powered from a 3.3V supply. The V_{DDQ} pin takes 1.2V to 1.8V input while the output voltage at V_{TT} pin is tracking 1/2 × V_{DDQ}. The regulator's V_{TT} output is capable of sinking/sourcing up to 1A current, while the V_{REF} pin output is $1/2V_{DDQ}$±1% × V_{DDQ} with 5mA current sinking/sourcing capability. The TS3DDR32611 has 4 modes of operation: high speed, low speed, V_{REF} mode and power down mode, depending on the control signals VTT_EN and ODT_EN. These different modes of operation provide flexibility to establish a memory system's performance and power consumption.

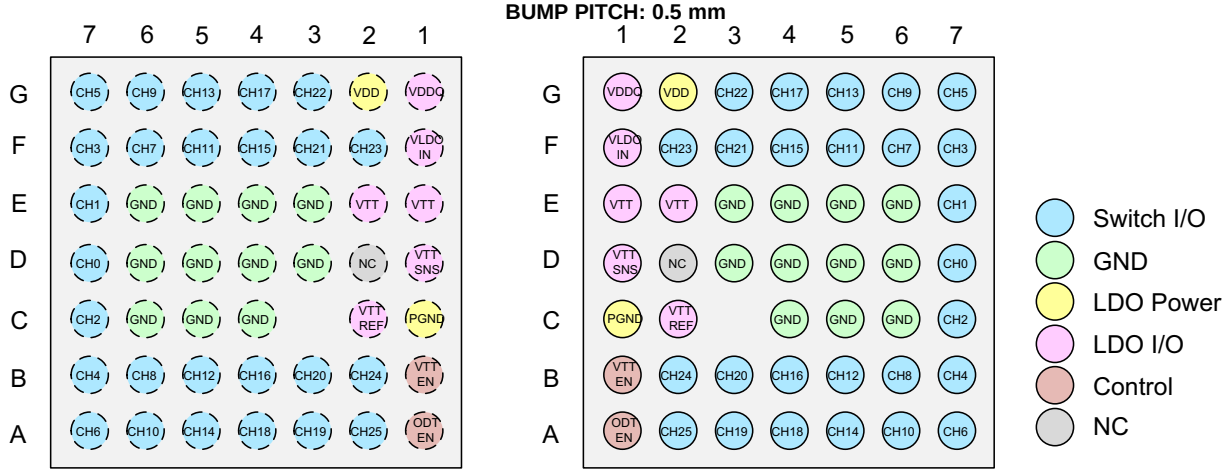
The TS3DDR32611 is situated within a small 48 balls BGA package with only 4mm x 4mm in size, which makes it a perfect candidate to be used in mobile applications.

SWITCH DIAGRAM



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

DIE SIZE: 4.0 mm × 4.0 mm
BUMP PITCH: 0.5 mm



TS3DDR32611 Pin Mapping(1)

	7	6	5	4	3	2	1
G	CH5	CH9	CH13	CH17	CH22	VDD	VDDQ
F	CH3	CH7	CH11	CH15	CH21	CH23	VLODIN
E	CH1	GND	GND	GND	GND	VTT	VTT
D	CH0	GND	GND	GND	GND	NC	VTTSNS
C	CH2	GND	GND	GND		VREF	PGND
B	CH4	CH8	CH12	CH16	CH20	CH24	VTT_EN
A	CH6	CH10	CH14	CH18	CH19	CH25	ODT_EN

(1) The NC must be floating, and cannot be connected to anything.

PIN FUNCTIONS

PIN		TYPE	DESCRIPTION
NO.	NAME		
C4, C5, C6, D3, D4, D5, D6, E3, E4, E5, E6	GND	—	Signal Ground
E1, E2	VTT	O	Power output for VTT LDO, need to connect 10-µF or greater MLCC for stability
C1	PGND	—	Power GND for VTT LDO
D1	VTTSNS	I	VTT LDO voltage sense input
F1	VLDOIN	I	Power supply input for VTT/ VTTREF
C2	VREF	O	VREF buffered reference output. Need to connect 0.22-µF or greater MLCC for stability.
B1	VTT_EN	I	Enable signal for VTT and VREF output
A1	ODT_EN	I	Enable signal for Switch
G1	VDDQ	I	VDDQ input, reference input for VREF
G2	VDD	I	Device power supply input 3.3 V typical
D7, E7, C7, F7, B7, G7, A7, F6, B6, G6, A6, F5, B5, G5, A5, F4, B4, G4, A4, A3, B3, F3, G3, F2, B2, A2	CH0-CH25	I/O	Switch input or output
D2	NC	—	Not connected, must be floating and cannot be connected to any signal

FUNCTION TABLE

STATE	VTT_EN(1)	ODT_EN(1)	VTT	VREF	SWITCH
Power Down mode(2)	L	L	OFF(Discharge)	OFF(Discharge)	Disabled
Low Speed mode	H	L	ON	ON	Disabled
High Speed mode	H	H	ON	ON	Enabled

(1) The VTT_EN and ODT_EN pins has 6MΩ weak pull-down resistor to GND to make its default value to be LOW.
(2) For VTT_EN= L and ODE_EN= H, the TS3DDR32611 will also stays in the power down mode. However, there will be an increased leakage current of up to max 25µA depending on the voltage level of ODT_EN and is thus not a recommended setting to use.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)(1) (2)

		MIN	MAX	UNIT
V_{DD}	Supply voltage range(3)	–0.3	5.5	V
V_{CTRL}	Control input (VTT_EN, ODT_EN) voltage range(3)	–0.3	5.5	V
V_{DDQ}	V_{DDQ} input voltage range(3)	–0.3	3.6	V
V_{LDOIN}	V_{LDOIN} input voltage range(3)	–0.3	3.6	V
V_{TT}, V_{REF}	V_{TT}, V_{REF} output voltage range(3)	–0.3	3.6	V
V_{TTSNS}	V_{TTSNS} input voltage range(3)	–0.3	3.6	V
PGND	PGND input voltage range(3)	–0.3	0.3	V
HBM	Electrostatic discharge QSS 009-105 (JESD22-A114A)		2	kV
CDM	Electrostatic discharge QSS 009-147 (JESD22-C101B.01)		500	V
T_J	Junction temperature	–40	125	°C
T_A	Operating free-air temperature	–55	150	°C

(1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not implied.
(2) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum.
(3) All voltages are with respect to GND, unless otherwise specified.

PACKAGE THERMAL IMPEDANCE(1)

			TYP	UNIT
θ_{JA}	Package thermal impedance	ZQC package	101(2)	°C/W

(1) The package thermal impedance is calculated in accordance with JESD 51-7.
(2) 69.2°C/W With 4 Central GND vias when layout.

RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_{DD}	Supply voltage range(1)	3.0	3.6	V
V_{CTRL}	Control input (VTT_EN, ODT_EN) voltage range(1)	0	3.6	V
V_{DDQ}	V_{DDQ} input voltage range(1)	1.2	1.5	V
V_{LDOIN}	VLDOIN input voltage range(1)	VTT+0.4	1.5	V
V_{TT}, V_{REF}	V_{TT}, V_{REF} output voltage range(1)	0	0.75	V
V_{TTSNS}	V_{TTSNS} input voltage range(1)	0	0.75	V
PGND	PGND input voltage range(1)	–0.1	0.1	V
T_A	Operating free-air temperature	–40	85	°C

(1) All voltages are with respect to GND, unless otherwise specified.

ELECTRICAL CHARACTERISTICS

T_A = –40°C to 85°C, Typical values are at V_{DD} = 3.3V, T_A = 25°C, (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
SUPPLY CURRENT							
$I_{VDD(HS)}$	V_{DD} supply current in high speed mode(1)	V_{DD} = 3.3V	No load, VTT_EN=ODT_EN= 1.8V, V_{DDQ}=1.5 V		150	220	µA
$I_{VDD(LS)}$	V_{DD} supply current in low speed mode(1)	V_{DD} = 3.3V	No load, VTT_EN=1.8V, ODT_EN= 0V, V_{DDQ}=1.5V		150	220	µA
$I_{VDD(PD)}$	V_{DD} supply current in power down mode(1)	V_{DD} = 3.3V	No load, VTT_EN=0V,ODT_EN= 0V, V_{DDQ}=1.5V		1	5	µA
I_{VLDOIN}	V_{LDOIN} supply current in high or low speed mode	V_{DD} = 3.3V	No load, VTT_EN=H, ODT_EN= H or L, V_{DDQ}=1.5V		1	5	µA
$I_{VLDOIN(PD)}$	V_{LDOIN} supply current in power down mode	V_{DD} = 3.3V	No load, VTT_EN=L, ODT_EN=H or L, V_{DDQ}=1.5V		1	5	µA
V_{TT} OUTPUT							
V_{TT}	Output voltage				V_{DDQ}/2		V
V_{TTTOL}	Output voltage tolerance to 1/2V_{DDQ}	V_{DDQ} = 1.25V, 1.35V, 1.5V	$\|I_{VTT}\|$< 60 mA	-20	±15	20	mV
			$\|I_{VTT}\|$< 550 mA	-35	±25	35	
			$\|I_{VTT}\|$< 1 A	-60	±35	60	
$I_{VTT(SRC)}$	Source current limit	V_{DDQ} = 1.5 V	V_{TT}=V_{TTSNS}=0.6 V	1000			mA
$I_{VTT(SINK)}$	Sink current limit	V_{DDQ} = 1.5 V	V_{TT}=V_{TTSNS}=0.9 V	1000			mA
$I_{VTT(max)}$	Max Source or Sink current capability	V_{DDQ} = 1.5 V	V_{TT}=V_{TTSNS}=0 V			1.5	A
$I_{VTT(DIS)}$	V_{TT} Discharge current	V_{DDQ} = 0 V	VTT_EN=L, ODT_EN=H or L, V_{TT} = 0.5 V, T_A=25°C			10	mA
$I_{VTTSNS(BIAS)}$	V_{TTSNS} Input Bias current	V_{TTSNS}=V_{REF}	No load, VTT_EN=H, ODT_EN= H	–0.1		0.1	µA
V_{REF} OUTPUT							
V_{REF}	Output voltage				V_{DDQ}/2		V
V_{REFTOL}	Output voltage tolerance to 1/2V_{DDQ}	V_{DDQ} = 1.25V, 1.35V, 1.5V	$\|IV_{REF}\|$< 5 mA	-1.0%*V_{DDQ}		1.0%*V_{DDQ}	mV
$I_{VREF(SRC)}$	Source current limit	V_{DDQ} = 1.5V	V_{REF}=0 V	10			mA
$I_{VREF(SINK)}$	Sink current limit	V_{DDQ} = 0V	V_{REF}=1.5 V	10			mA
$V_{VREF(DIS)}$	VREF Discharge current	V_{DDQ} = 0V	VTT_EN=L,ODT_EN=H or L, V_{REF}=0.5 V, T_A = 25°C			2	mA
V_{DDQ} INPUT							
I_{VDDQ}	V_{DDQ} input current	V_{DDQ} = 1.5V			30	40	µA
ISOLATION SWITCH							
R_{ON}	ON-state resistance	V_{DD} = 3.3V	$V_{I/O}$ = 0.75 V, $\|I_{VTT}\|$= 18 mA		1.75	4	Ω
$R_{ON, FLAT}$	ON-state resistance flatness	V_{DD} = 3.3V	$V_{I/O}$ = 0 V to 0.75 V, $\|I_{VTT}\|$= 18 mA		0.2	0.4	Ω
ΔR_{ON}	ON-state resistance match between channels	V_{DD} = 3.3V	$V_{I/O}$ = 0.75 V, $\|I_{VTT}\|$= 18 mA		0.2		Ω
DIGITAL CONTROL INPUTS (VTT_EN, ODT_EN)							
V_{IH}	Input logic high	V_{DD} = 3.0 V to 3.6 V		1.3			V
V_{IL}	Input logic low	V_{DD} = 3.0 V to 3.6 V				0.6	V
V_{LHYST}	Hysteresis voltage				0.5		V
I_{LK}	Input leak current			–1		1	µA
OVER-TEMPERATURE PROTECTION							
T_{OTP}	Over temperature protection	Shutdown temperature			150		°C
		Hysteresis			30		

(1) For ODT_EN and VTT_EN, If the V_{IH} is less than 1.8V but more than Max V_{IH}, or V_{IL} is more than 0V but less than Max V_{IL}, it will cause the I_{VDD} has the max 25µA increase based on the voltage at ODT_EN and VTT_EN.

DYNAMIC CHARACTERISTICS

T_A = –40°C to 85°C, Typical values are at V_{CC} = 3.3V, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$t_{ON\ /OFF}$	Switching time between low speed and high speed mode	R_L = 50Ω, C_L = 5pF	V_{DD} = 3.0 V to 3.6 V			100	ns
$t_{RAMP(VTT)}$	V_{TT} ramp time	C_{VTT}= 20 µF	V_{DD} = 3.0V to 3.6V, I_{VTT}=0			50	µs
$t_{RAMP(VREF)}$	V_{REF} ramp time	C_{VREF}= 220 nF	V_{DD} = 3.0V to 3.6V, I_{VREF} =0			30	µs

TYPICAL CHARACTERISTICS

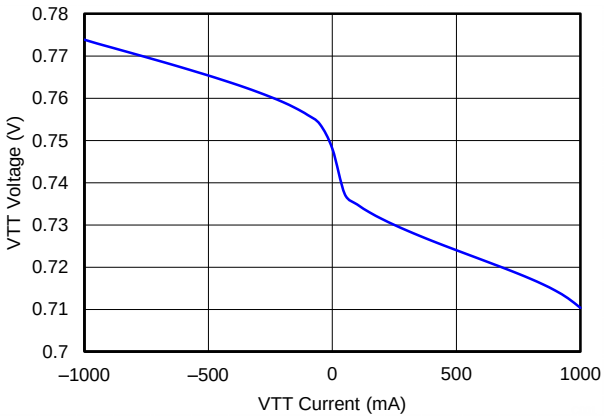


Figure 1. VTT Load Regulation (0.75V)

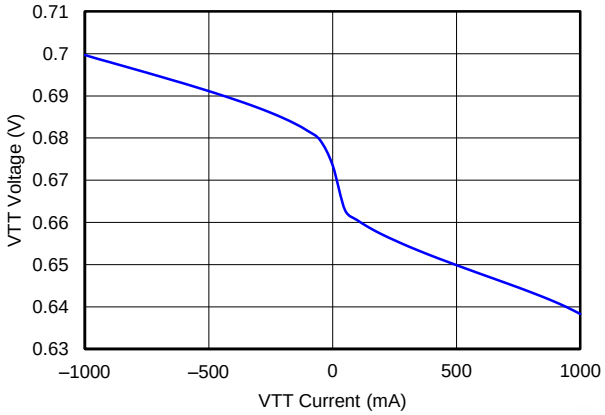


Figure 2. VTT Load Regulation (0.675V)

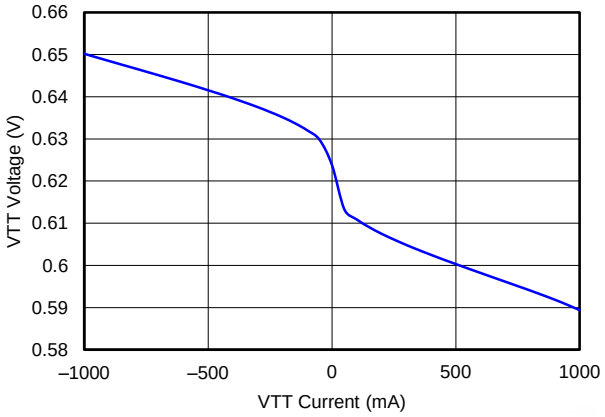


Figure 3. VTT Load Regulation (0.625V)

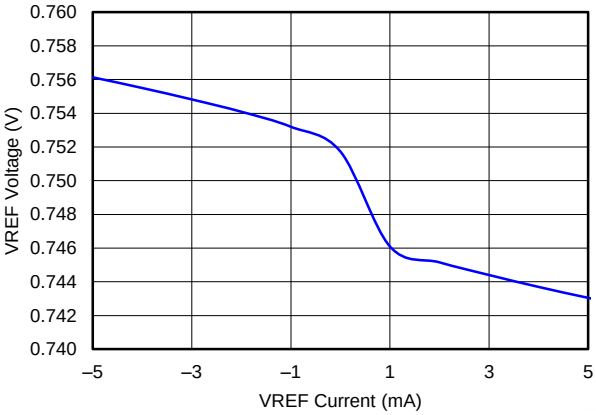


Figure 4. VREF Load Regulation (0.75V)

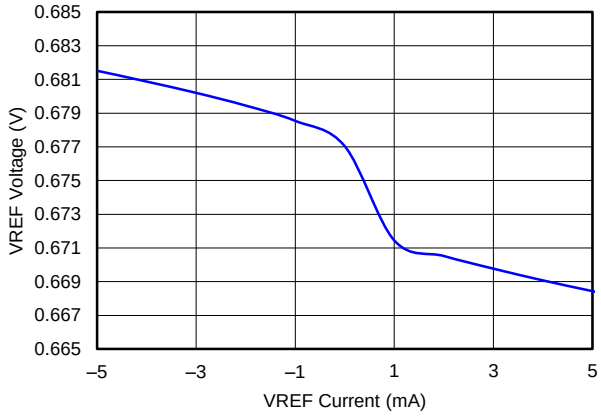


Figure 5. VREF Load Regulation (0.675V)

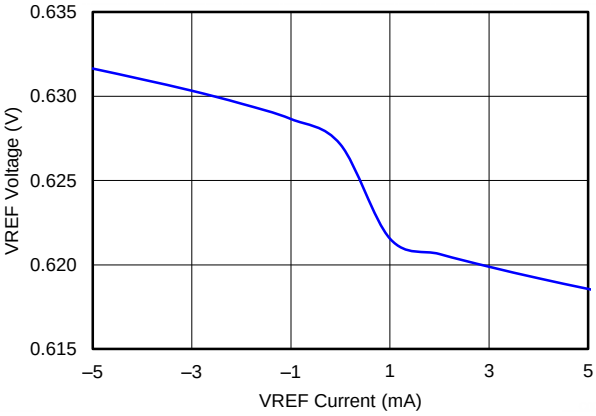


Figure 6. VREF Load Regulation (0.625V)

TYPICAL CHARACTERISTICS (continued)

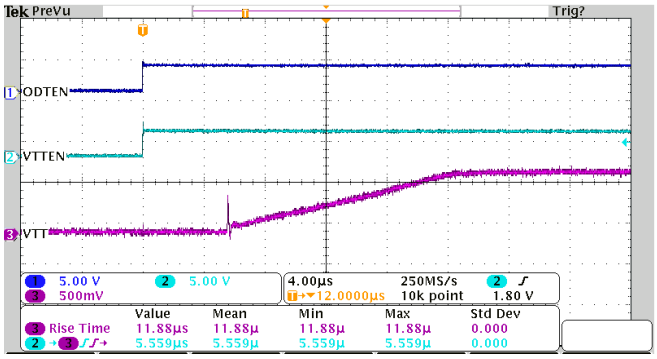


Figure 7. Start-up Waveform for VTT (Power-down to High Speed)

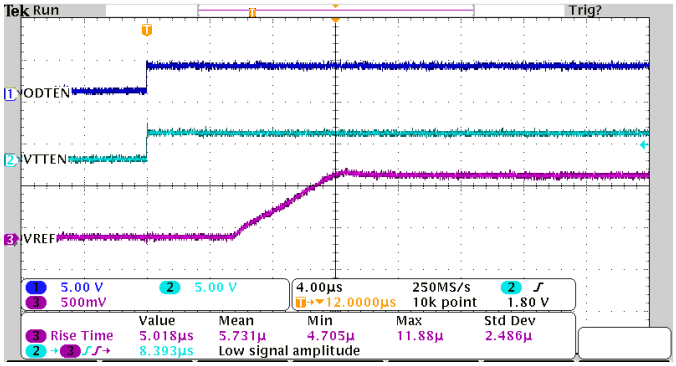


Figure 8. Start-up Waveform for VREF (Power-down to High Speed)

REVISION HISTORY

Changes from Original (August 2013) to Revision A	Page
• Added TYPICAL CHARACTERISTICS section.	6

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TS3DDR32611ZQCR	NRND	BGA MICROSTAR JUNIOR	ZQC	48	2500	Green (RoHS & no Sb/Br)	SNAGCU	Level-2-260C-1 YEAR	-40 to 85	XSL2611	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

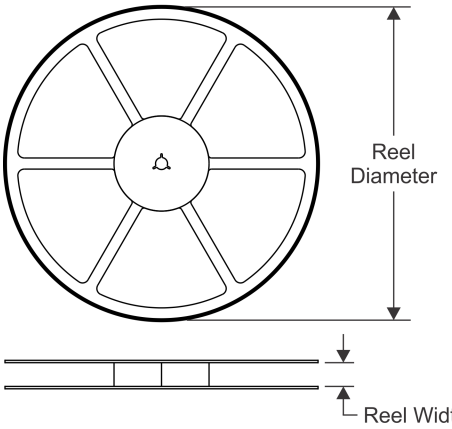
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

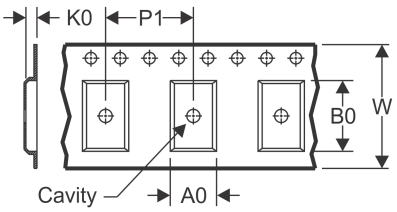
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

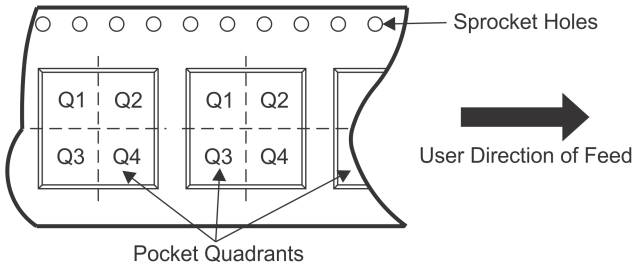


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

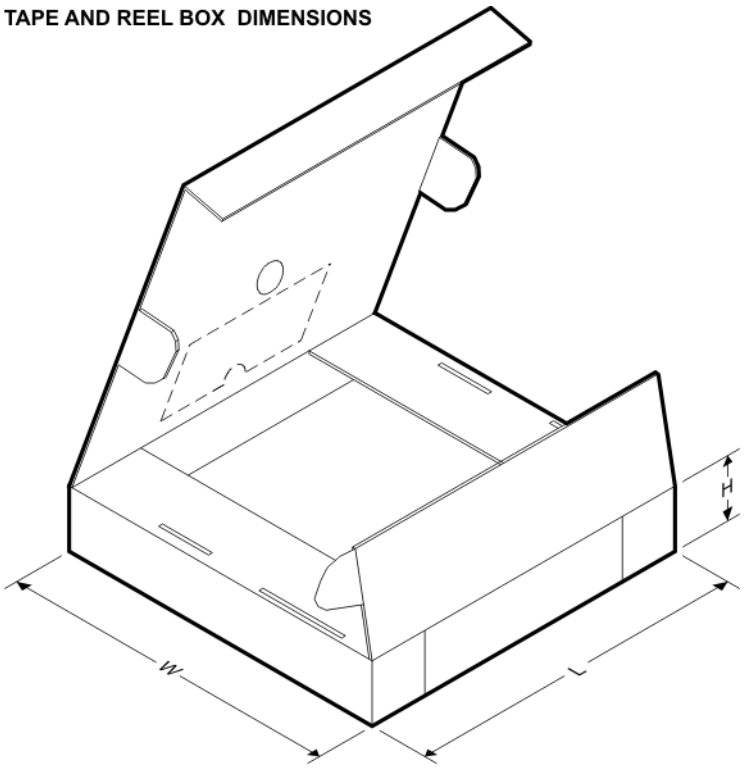
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TS3DDR32611ZQCR	BGA MICROSTAR JUNIOR	ZQC	48	2500	330.0	12.4	4.3	4.3	1.5	8.0	12.0	Q1

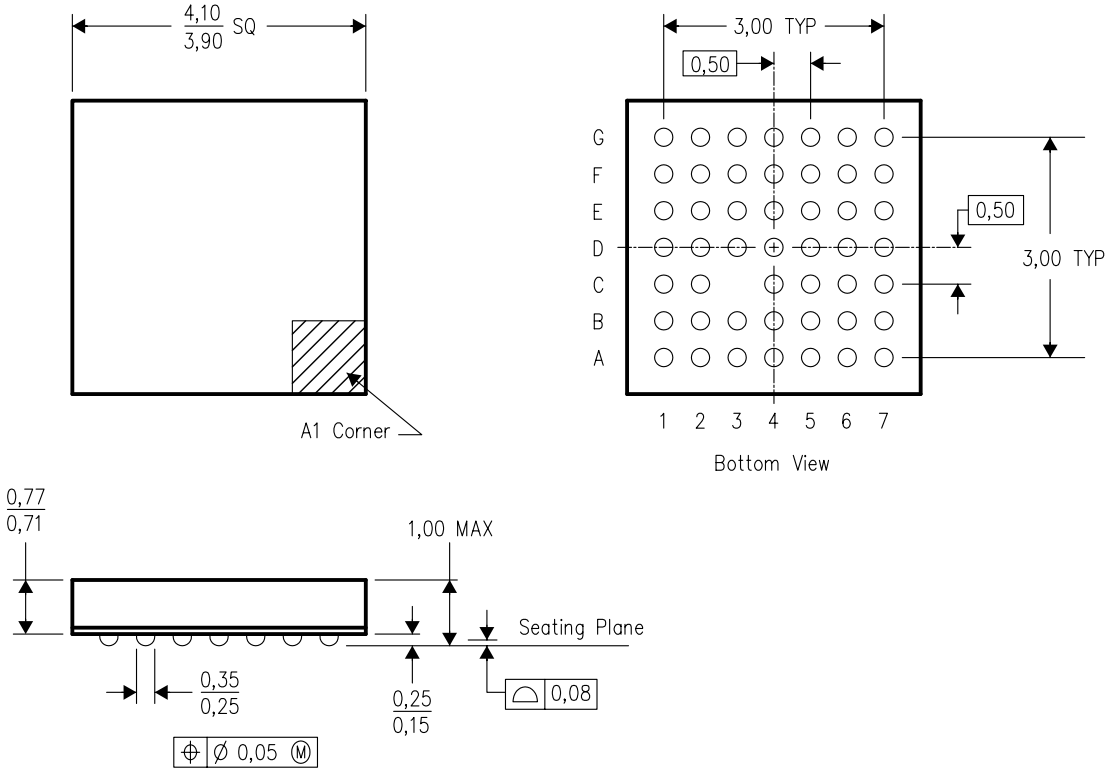
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TS3DDR32611ZQCR	BGA MICROSTAR JUNIOR	ZQC	48	2500	336.6	336.6	31.8

ZQC (S–PBGA–N48) PLASTIC BALL GRID ARRAY



4204659/A 09/02

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. MicroStar Junior™ BGA configuration
D. Falls within JEDEC MO–225
E. This package is lead–free.

MicroStar Junior is a trademark of Texas Instruments.

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