

## 16-BIT TO 8-BIT SPDT GIGABIT LAN SWITCH WITH LED SWITCH AND ENHANCED ESD PROTECTION

### FEATURES

- Wide Bandwidth (BW = 950 MHz Typ)
- Low Crosstalk ( $X_{TALK} = -37$  dB Typ)
- Low Bit-to-Bit Skew ( $t_{sk(o)} = 100$  ps Max)
- Low and Flat ON-State Resistance ( $r_{on} = 4 \Omega$  Typ,  $r_{on(Flat)} = 0.5 \Omega$  Typ)
- Low Input/Output Capacitance ( $C_{ON} = 8$  pF Typ)
- Rail-to-Rail Switching on Data I/O Ports (0 to 3.6 V)
- $V_{CC}$  Operating Range From 3 V to 3.6 V
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II

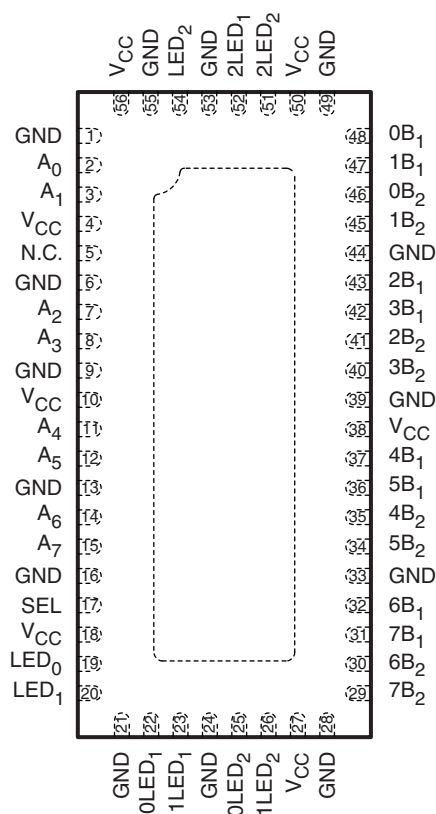
### ESD Performance

- 8-kV IEC61000-4-2, Contact Discharge on Switch IOs
- 3-kV Human Body Model Per JESD22-A114E
- 14-kV Human Body Model (Switch Pins to GND)

### APPLICATIONS

- 10/100/1000 Base-T Signal Switching
- Differential (LVDS, LVPECL) Signal Switching
- Audio/Video Switching
- Hub and Router Signal Switching

RHU PACKAGE  
(TOP VIEW)



N.C. – Not internally connected



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

## DESCRIPTION/ORDERING INFORMATION

The TS3L500AE is a 16-bit to 8-bit multiplexer/demultiplexer LAN switch with a single select (SEL) input. SEL controls the data path of the multiplexer/demultiplexer. The device provides additional I/Os for switching status indicating LED signals and includes high ESD protection.

The device provides a low and flat ON-state resistance ( $r_{on}$ ) and an excellent ON-state resistance match. Low input/output capacitance, high bandwidth, low skew, and low crosstalk among channels make this device suitable for various LAN applications, such as 10/100/1000 Base-T.

This device can be used to replace mechanical relays in LAN applications. It also can be used to route signals from a 10/100 Base-T ethernet transceiver to the RJ-45 LAN connectors in laptops or in docking stations.

## ORDERING INFORMATION

$T_A$	PACKAGE <sup>(1), (2)</sup>		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	TQFN – RHU	Tape and reel	TS3L500AERHUR	TK500AE

- (1) Package drawings, thermal data, and symbolization are available at [www.ti.com/packaging](http://www.ti.com/packaging).  
 (2) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at [www.ti.com](http://www.ti.com).

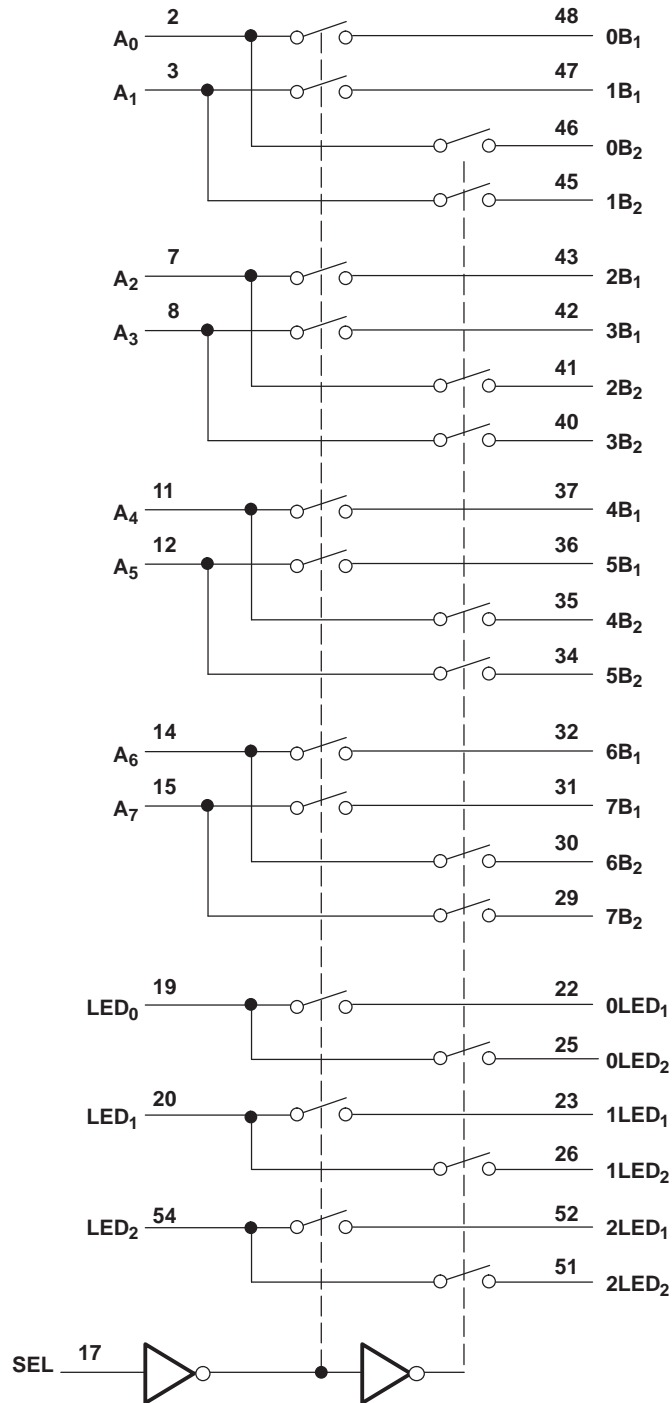
## FUNCTION TABLE

INPUT SEL	INPUT/OUTPUT $A_n$	FUNCTION
L	$nB_1$	$A_n = nB_1$ , $LED_x = XLED_1$
H	$nB_2$	$A_n = nB_2$ , $LED_x = XLED_2$

## PIN DESCRIPTION

NAME	DESCRIPTION
$A_n$	Data I/Os
$nB_m$	Data I/Os
SEL	Select input
$LED_x$	LED I/O port
$XLED_m$	LED I/O port

**LOGIC DIAGRAM (POSITIVE LOGIC)**



**ABSOLUTE MAXIMUM RATINGS<sup>(1)</sup>**

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
$V_{CC}$	Supply voltage range	-0.5	4.6	V
$V_{IN}$	Control input voltage range <sup>(2)(3)</sup>	-0.5	7	V
$V_{I/O}$	Switch I/O voltage range <sup>(2)(3)(4)</sup>	-0.5	7	V
$I_{IK}$	Control input clamp current	$V_{IN} < 0$	-50	mA
$I_{I/OK}$	I/O port clamp current	$V_{I/O} < 0$	-50	mA
$I_{I/O}$	ON-state switch current <sup>(5)</sup>		±128	mA
	Continuous current through $V_{DD}$ or GND		±100	mA
$\theta_{JA}$	Package thermal impedance <sup>(6)</sup>		31.8	°C/W
$T_{stg}$	Storage temperature range	-65	150	°C

- (1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltages are with respect to ground, unless otherwise specified.
- (3) The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
- (4)  $V_I$  and  $V_O$  are used to denote specific conditions for  $V_{I/O}$ .
- (5)  $I_I$  and  $I_O$  are used to denote specific conditions for  $I_{I/O}$ .
- (6) The package thermal impedance is calculated in accordance with JESD 51-7.

**RECOMMENDED OPERATING CONDITIONS<sup>(1)</sup>**

		MIN	MAX	UNIT
$V_{CC}$	Supply voltage	3	3.6	V
$V_{IH}$	High-level control input voltage (SEL)	2	5.5	V
$V_{IL}$	Low-level control input voltage (SEL)	0	0.8	V
$V_I$	Input voltage (SEL)	0	5.5	V
$V_{I/O}$	Input/output voltage	0	$V_{CC}$	V
$T_A$	Operating free-air temperature	-40	85	°C

- (1) All unused control inputs of the device must be held at  $V_{DD}$  or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

## ELECTRICAL CHARACTERISTICS

for 1000 Base-T Ethernet switching over recommended operating free-air temperature range,  $V_{DD} = 3.3 \text{ V} \pm 0.3 \text{ V}$   
(unless otherwise noted)

PARAMETER		TEST CONDITIONS <sup>(1)</sup>		MIN	TYP <sup>(2)</sup>	MAX	UNIT		
$V_{IK}$	SEL	$V_{CC} = 3.6 \text{ V}$ ,	$I_{IN} = -18 \text{ mA}$	-0.7	-1.2		V		
$I_{IH}$	SEL	$V_{CC} = 3.6 \text{ V}$ ,	$V_{IN} = V_{DD}$			$\pm 1$	$\mu\text{A}$		
$I_{IL}$	SEL	$V_{CC} = 3.6 \text{ V}$ ,	$V_{IN} = \text{GND}$			$\pm 1$	$\mu\text{A}$		
$I_{OFF}$	SEL	$V_{CC} = 0 \text{ V}$ ,	$V_{IN} = 0 \text{ to } 3.6 \text{ V}$			$\pm 1$	$\mu\text{A}$		
$I_{CC}$		$V_{CC} = 3.6 \text{ V}$ ,	$I_{I/O} = 0$ ,	Switch ON or OFF		250	600	$\mu\text{A}$	
$C_{IN}$	SEL	$f = 1 \text{ MHz}$ ,	$V_{IN} = 0$		2	2.5	pF		
$C_{OFF}$	B port	$V_I = 0$ ,	$f = 1 \text{ MHz}$ ,	Outputs open,	Switch OFF		3	4	pF
$C_{ON}$		$V_I = 0$ ,	$f = 1 \text{ MHz}$ ,	Outputs open,	Switch ON		9	9.8	pF
$r_{on}$		$V_{CC} = 3 \text{ V}$ ,	$1.5 \text{ V} \leq V_I \leq V_{CC}$ ,	$I_O = -40 \text{ mA}$		4	8	$\Omega$	
$r_{on(\text{flat})}$ <sup>(3)</sup>		$V_{CC} = 3 \text{ V}$ ,	$V_I = 1.5 \text{ V}$ and $V_{CC}$ ,	$I_O = -40 \text{ mA}$		0.7		$\Omega$	
$\Delta r_{on}$ <sup>(4)</sup>		$V_{CC} = 3 \text{ V}$ ,	$1.5 \text{ V} \leq V_I \leq V_{CC}$ ,	$I_O = -40 \text{ mA}$		0.2	1.2	$\Omega$	

- (1)  $V_I$ ,  $V_O$ ,  $I_I$ , and  $I_O$  refer to I/O pins.  $V_{IN}$  refers to the control inputs.  
 (2) All typical values are at  $V_{DD} = 3.3 \text{ V}$  (unless otherwise noted),  $T_A = 25^\circ\text{C}$ .  
 (3)  $r_{on(\text{flat})}$  is the difference of  $r_{on}$  in a given channel at specified voltages.  
 (4)  $\Delta r_{on}$  is the difference of  $r_{on}$  from center ( $A_4$ ,  $A_5$ ) ports to any other port.

## ELECTRICAL CHARACTERISTICS

for 10/100 Base-T Ethernet switching over recommended operating free-air temperature range,  $V_{DD} = 3.3 \text{ V} \pm 0.3 \text{ V}$   
(unless otherwise noted)

PARAMETER		TEST CONDITIONS <sup>(1)</sup>		MIN	TYP <sup>(2)</sup>	MAX	UNIT		
$V_{IK}$	SEL	$V_{CC} = 3.6 \text{ V}$ ,	$I_{IN} = -18 \text{ mA}$	-0.7	-1.2		V		
$I_{IH}$	SEL	$V_{CC} = 3.6 \text{ V}$ ,	$V_{IN} = V_{DD}$			$\pm 1$	$\mu\text{A}$		
$I_{IL}$	SEL	$V_{CC} = 3.6 \text{ V}$ ,	$V_{IN} = \text{GND}$			$\pm 1$	$\mu\text{A}$		
$I_{OFF}$	SEL	$V_{CC} = 0 \text{ V}$ ,	$V_{IN} = 0 \text{ to } 3.6 \text{ V}$			$\pm 1$	$\mu\text{A}$		
$I_{CC}$		$V_{CC} = 3.6 \text{ V}$ ,	$I_{I/O} = 0$ ,	Switch ON or OFF		250	600	$\mu\text{A}$	
$C_{IN}$	SEL	$f = 1 \text{ MHz}$ ,	$V_{IN} = 0$		2	2.5	pF		
$C_{OFF}$	B port	$V_I = 0$ ,	$f = 1 \text{ MHz}$ ,	Outputs open,	Switch OFF		3	4	pF
$C_{ON}$		$V_I = 0$ ,	$f = 1 \text{ MHz}$ ,	Outputs open,	Switch ON		9	9.8	pF
$r_{on}$		$V_{CC} = 3 \text{ V}$ ,	$1.25 \text{ V} \leq V_I \leq V_{CC}$ ,	$I_O = -10 \text{ mA to } -30 \text{ mA}$		4	6	$\Omega$	
$r_{on(\text{flat})}$ <sup>(3)</sup>		$V_{CC} = 3 \text{ V}$ ,	$V_I = 1.25 \text{ V}$ and $V_{CC}$ ,	$I_O = -10 \text{ mA to } -30 \text{ mA}$		0.5		$\Omega$	
$\Delta r_{on}$ <sup>(4)</sup>		$V_{CC} = 3 \text{ V}$ ,	$1.25 \text{ V} \leq V_I \leq V_{CC}$ ,	$I_O = -10 \text{ mA to } -30 \text{ mA}$		0.4	1	$\Omega$	

- (1)  $V_I$ ,  $V_O$ ,  $I_I$ , and  $I_O$  refer to I/O pins.  $V_{IN}$  refers to the control inputs.  
 (2) All typical values are at  $V_{DD} = 3.3 \text{ V}$  (unless otherwise noted),  $T_A = 25^\circ\text{C}$ .  
 (3)  $r_{on(\text{flat})}$  is the difference of  $r_{on}$  in a given channel at specified voltages.  
 (4)  $\Delta r_{on}$  is the difference of  $r_{on}$  from center ( $A_4$ ,  $A_5$ ) ports to any other port.

## SWITCHING CHARACTERISTICS

over recommended operating free-air temperature range,  $V_{DD} = 3.3 \text{ V} \pm 0.3 \text{ V}$ ,  $R_L = 200 \ \Omega$ ,  $C_L = 10 \text{ pF}$   
(unless otherwise noted) (see Figures 4 and 5)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	TYP <sup>(1)</sup>	MAX	UNIT
$t_{pd}$ <sup>(2)</sup>	A or B	B or A		0.25		ns
$t_{PZH}$ , $t_{PZL}$	SEL	A or B	0.5		15	ns
$t_{PHZ}$ , $t_{PLZ}$	SEL	A or B	0.9		9	ns
$t_{sk(o)}$ <sup>(3)</sup>	A or B	B or A		50	100	ps
$t_{sk(p)}$ <sup>(4)</sup>				50	100	ps

- (1) All typical values are at  $V_{DD} = 3.3 \text{ V}$  (unless otherwise noted),  $T_A = 25^\circ\text{C}$ .
- (2) The propagation delay is the calculated RC time constant of the typical ON-state resistance of the switch and the specified load capacitance when driven by an ideal voltage source (zero output impedance).
- (3) Output skew between center port ( $A_4$  to  $A_5$ ) to any other port
- (4) Skew between opposite transitions of the same output in a given device  $|t_{PHL} - t_{PLH}|$

## DYNAMIC CHARACTERISTICS

over recommended operating free-air temperature range,  $V_{DD} = 3.3 \text{ V} \pm 0.3 \text{ V}$  (unless otherwise noted)

PARAMETER	TEST CONDITIONS			TYP <sup>(1)</sup>	UNIT
$X_{TALK}$	$R_L = 100 \ \Omega$ ,	$f = 250 \text{ MHz}$ ,	See Figure 8	-37	dB
$O_{IRR}$	$R_L = 100 \ \Omega$ ,	$f = 250 \text{ MHz}$ ,	See Figure 9	-37	dB
BW	$R_L = 100 \ \Omega$ ,	See Figure 7		950	MHz

- (1) All typical values are at  $V_{CC} = 3.3 \text{ V}$  (unless otherwise noted),  $T_A = 25^\circ\text{C}$ .

OPERATING CHARACTERISTICS

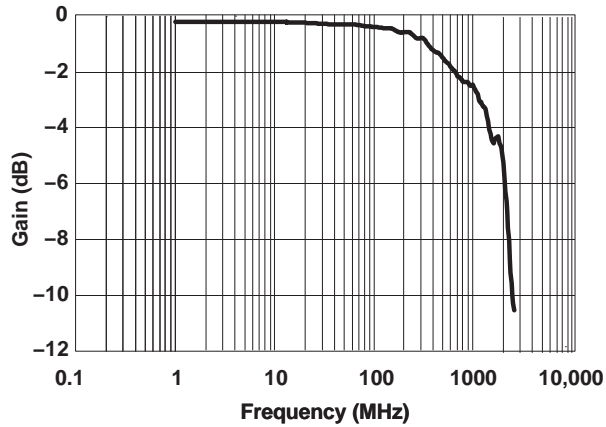


Figure 1. Gain vs Frequency

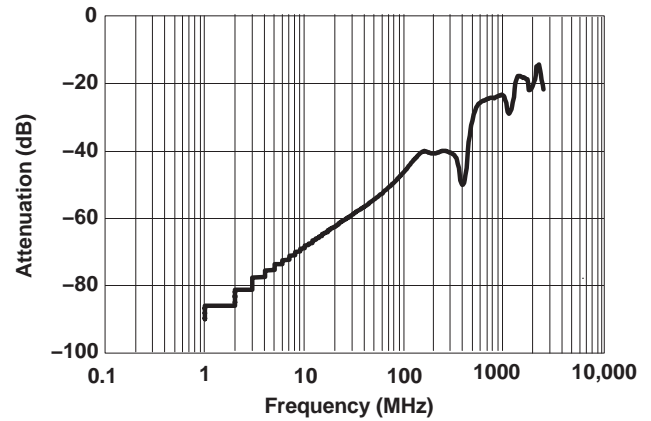


Figure 2. OFF Isolation vs Frequency

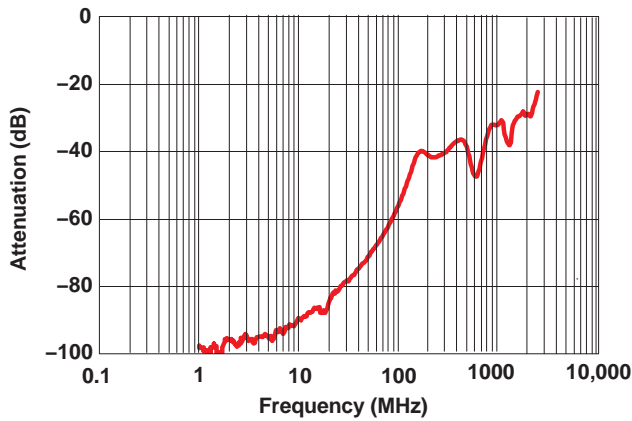


Figure 3. Crosstalk vs Frequency

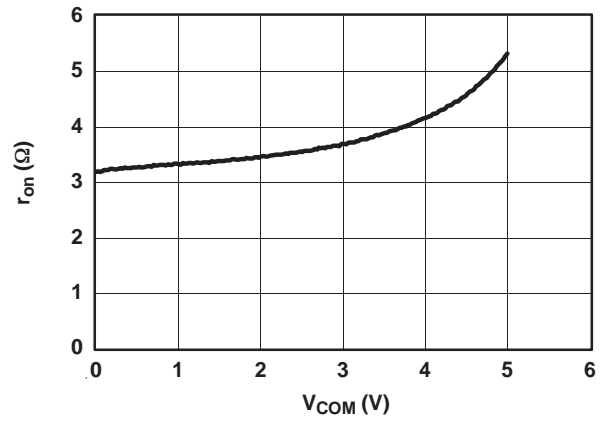
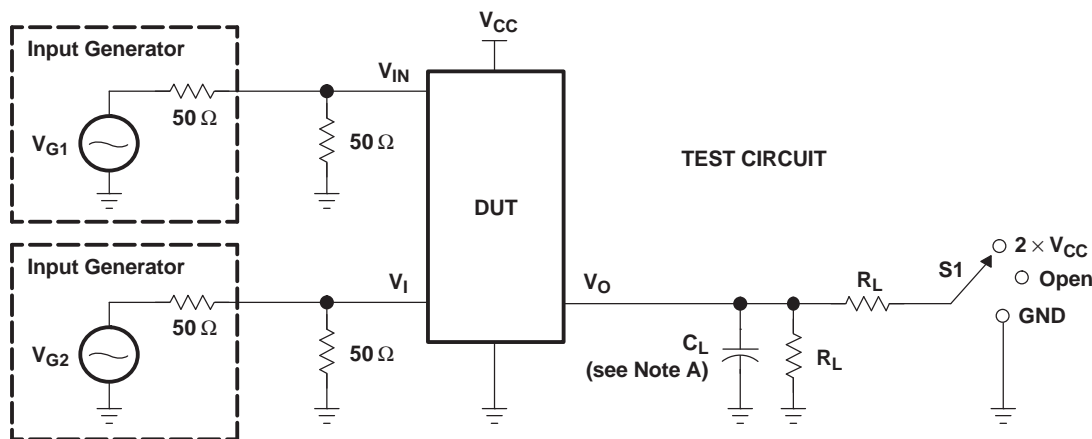
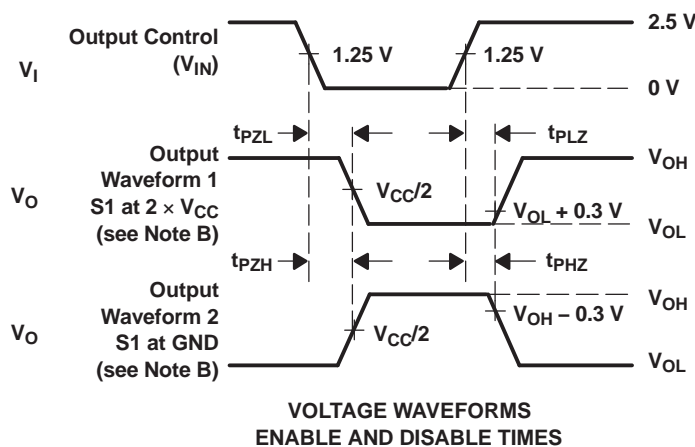


Figure 4. r<sub>on</sub> (Ω) vs V<sub>com</sub> (V)

### PARAMETER MEASUREMENT INFORMATION (Enable and Disable Times)



TEST	V <sub>CC</sub>	S1	R <sub>L</sub>	V <sub>in</sub>	C <sub>L</sub>	V <sub>Δ</sub>
t <sub>PLZ</sub> /t <sub>PZL</sub>	3.3 V ± 0.3 V	2 × V <sub>CC</sub>	200 Ω	GND	10 pF	0.3 V
t <sub>PHZ</sub> /t <sub>PZH</sub>	3.3 V ± 0.3 V	GND	200 Ω	V <sub>CC</sub>	10 pF	0.3 V

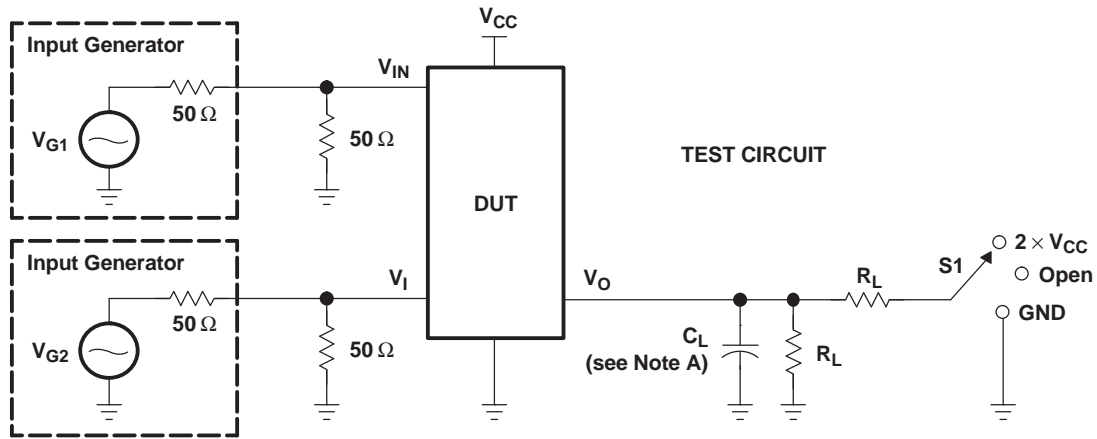


- NOTES:
- A. C<sub>L</sub> includes probe and jig capacitance.
  - B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
  - C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z<sub>O</sub> = 50 Ω, t<sub>r</sub> ≤ 2.5 ns, t<sub>f</sub> ≤ 2.5 ns.
  - D. The outputs are measured one at a time, with one transition per measurement.
  - E. t<sub>PLZ</sub> and t<sub>PHZ</sub> are the same as t<sub>dis</sub>.
  - F. t<sub>PZL</sub> and t<sub>PZH</sub> are the same as t<sub>en</sub>.

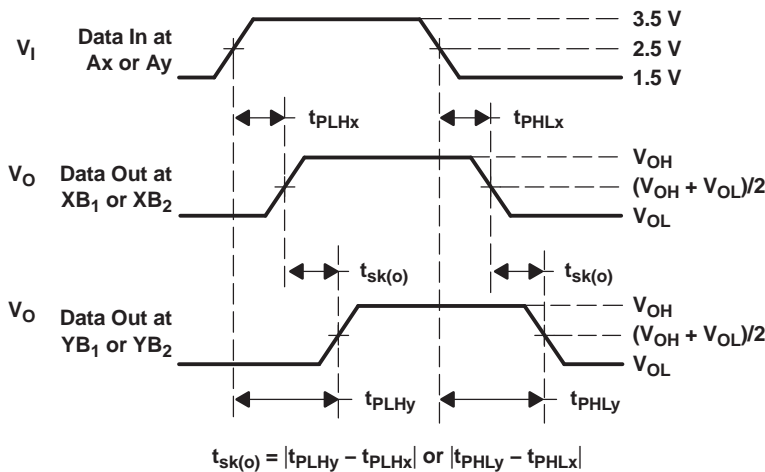
Figure 5. Test Circuit and Voltage Waveforms



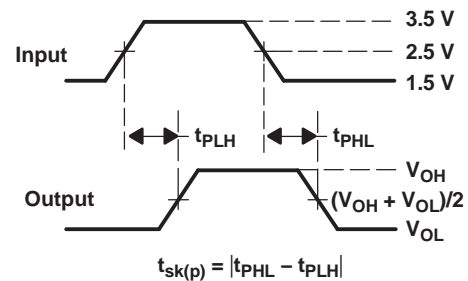
PARAMETER MEASUREMENT INFORMATION  
(Skew)



TEST	V <sub>CC</sub>	S1	R <sub>L</sub>	V <sub>in</sub>	C <sub>L</sub>
t <sub>sk(o)</sub>	3.3 V ± 0.3 V	Open	200 Ω	V <sub>CC</sub> or GND	10 pF
t <sub>sk(p)</sub>	3.3 V ± 0.3 V	Open	200 Ω	V <sub>CC</sub> or GND	10 pF



VOLTAGE WAVEFORMS  
OUTPUT SKEW [t<sub>sk(o)</sub>]

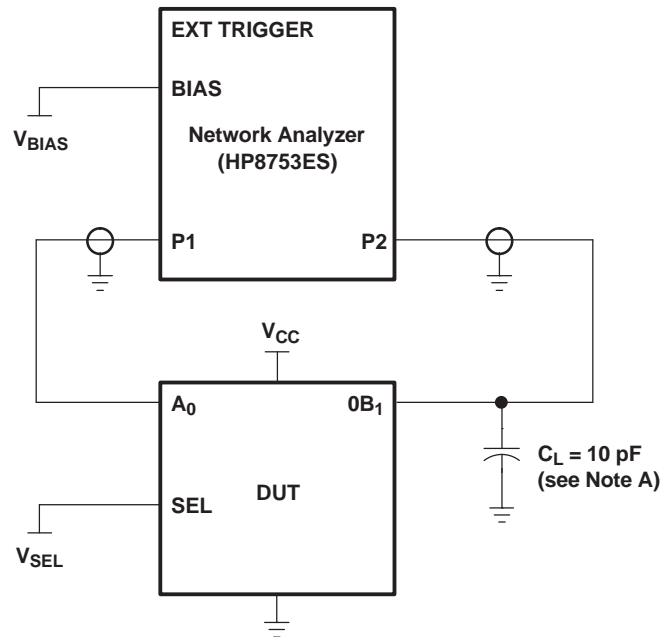


VOLTAGE WAVEFORMS  
PULSE SKEW [t<sub>sk(p)</sub>]

- NOTES: A. C<sub>L</sub> includes probe and jig capacitance.  
 B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.  
 C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z<sub>O</sub> = 50 Ω, t<sub>r</sub> ≤ 2.5 ns, t<sub>f</sub> ≤ 2.5 ns.  
 D. The outputs are measured one at a time, with one transition per measurement.

Figure 6. Test Circuit and Voltage Waveforms

## PARAMETER MEASUREMENT INFORMATION



A.  $C_L$  includes probe and jig capacitance.

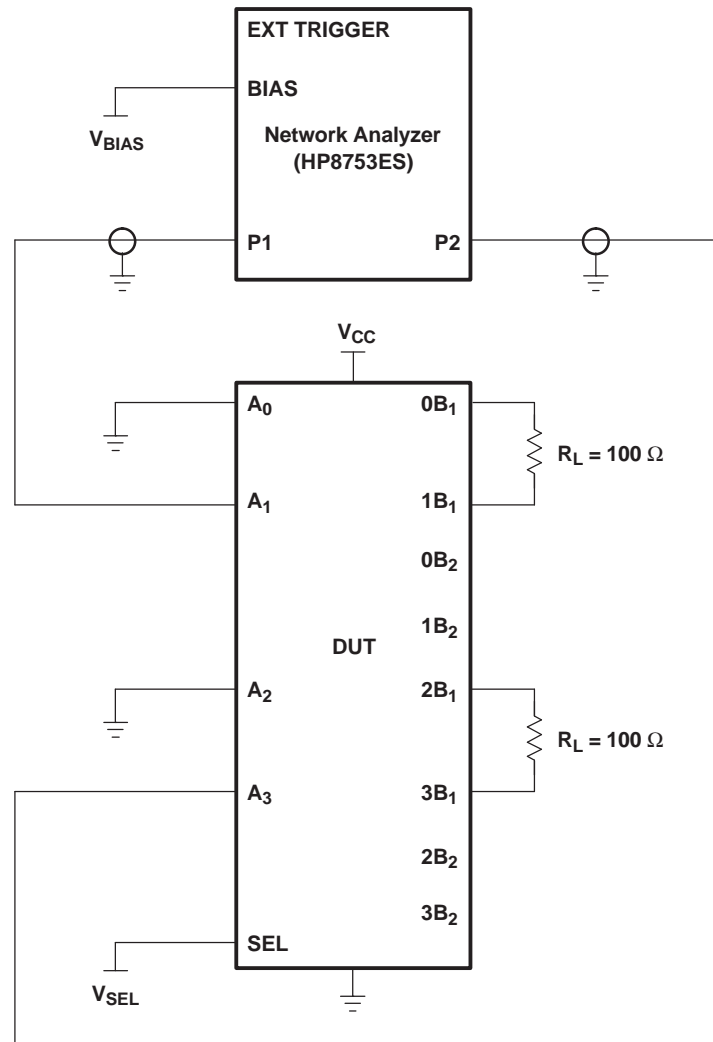
**Figure 7. Test Circuit for Frequency Response (BW)**

Frequency response is measured at the output of the ON channel. For example, when  $V_{SEL} = 0$  and  $A_0$  is the input, the output is measured at  $0B_1$ . All unused analog I/O ports are left open.

### HP8753ES Setup

Average = 4  
 RBW = 3 kHz  
 $V_{BIAS} = 0.35$  V  
 ST = 2 s  
 P1 = 0 dBm

PARAMETER MEASUREMENT INFORMATION (continued)



- A.  $C_L$  includes probe and jig capacitance.
- B. A 50- $\Omega$  termination resistor is needed to match the loading of the network analyzer.

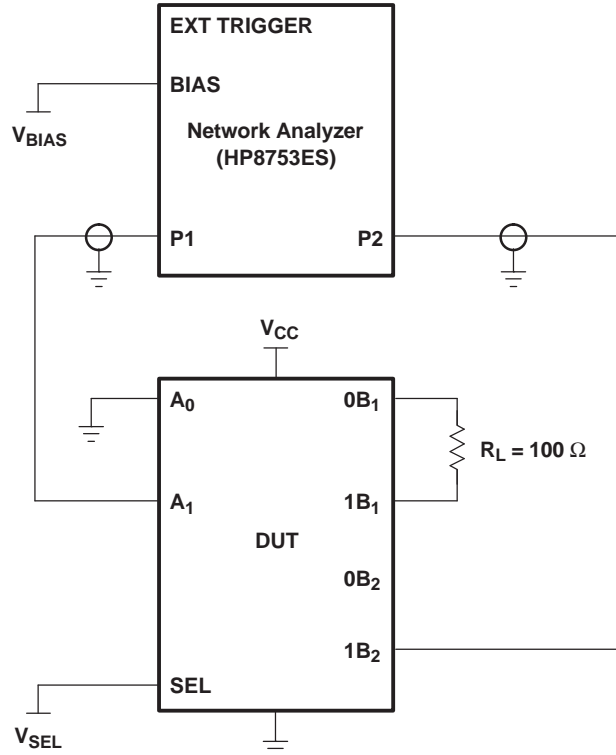
**Figure 8. Test Circuit for Crosstalk ( $X_{TALK}$ )**

Crosstalk is measured at the output of the nonadjacent ON channel. For example, when  $V_{SEL} = 0$  and  $A_1$  is the input, the output is measured at  $A_3$ . All unused analog input (A) ports are connected to GND, and output (B) ports are left open.

**HP8753ES Setup**

Average = 4  
 RBW = 3 kHz  
 $V_{BIAS} = 0.35$  V  
 ST = 2 s  
 P1 = 0 dBm

## PARAMETER MEASUREMENT INFORMATION (continued)



- A.  $C_L$  includes probe and jig capacitance.
- B. A 50- $\Omega$  termination resistor is needed to match the loading of the network analyzer.

**Figure 9. Test Circuit for OFF Isolation ( $O_{IRR}$ )**

OFF isolation is measured at the output of the OFF channel. For example, when  $V_{SEL} = GND$  and  $A_1$  is the input, the output is measured at  $1B_2$ . All unused analog input (A) ports are connected to ground, and output (B) ports are left open.

### HP8753ES Setup

Average = 4  
 RBW = 3 kHz  
 $V_{BIAS} = 0.35$  V  
 ST = 2 s  
 P1 = 0 dBm

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TS3L500AERHUR	ACTIVE	WQFN	RHU	56	2000	Green (RoHS & no Sb/Br)	CU NIPDAU   CU NIPDAUAG	Level-2-260C-1 YEAR	-40 to 85	TK500AE	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

**Important Information and Disclaimer:**The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

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## TAPE AND REEL INFORMATION



### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TS3L500AERHUR	WQFN	RHU	56	2000	330.0	24.4	5.3	11.3	1.0	12.0	24.0	Q1

**TAPE AND REEL BOX DIMENSIONS**

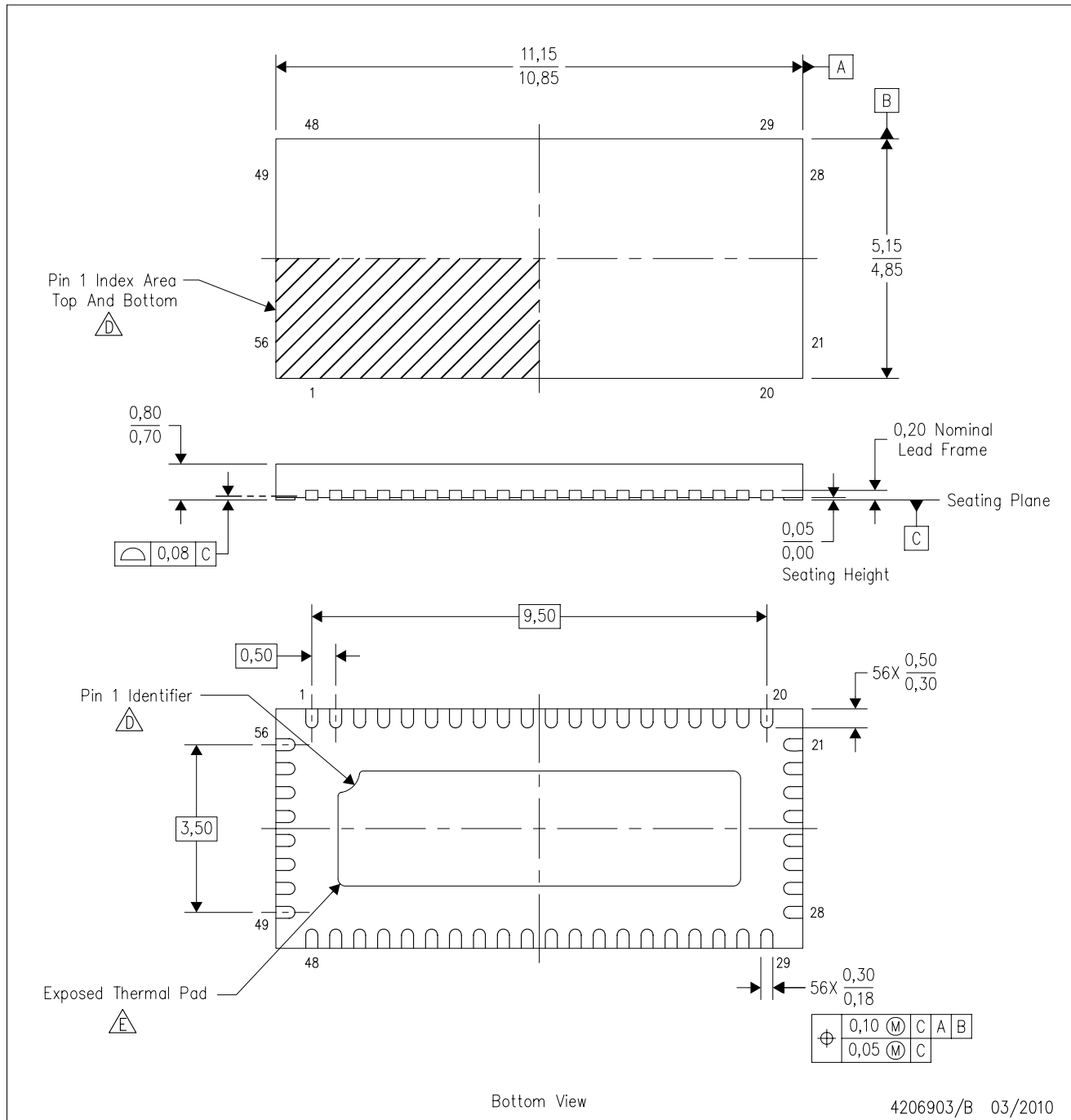




\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TS3L500AERHUR	WQFN	RHU	56	2000	346.0	346.0	35.0

RHU (R-PWQFN-N56)

PLASTIC QUAD FLATPACK NO-LEAD



- Notes:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
  - B. This drawing is subject to change without notice.
  - C. QFN (Quad Flatpack No-Lead) package configuration.
  -  Pin 1 identifiers are located on both top and bottom of the package and within the zone indicated. The Pin 1 identifiers are either a molded, marked, or metal feature.
  -  The package thermal pad must be soldered to the board for thermal and mechanical performance.
  - F. JEDEC MO-220 package registration is pending.



# THERMAL PAD MECHANICAL DATA

RHU (R-PWQFN-N56)

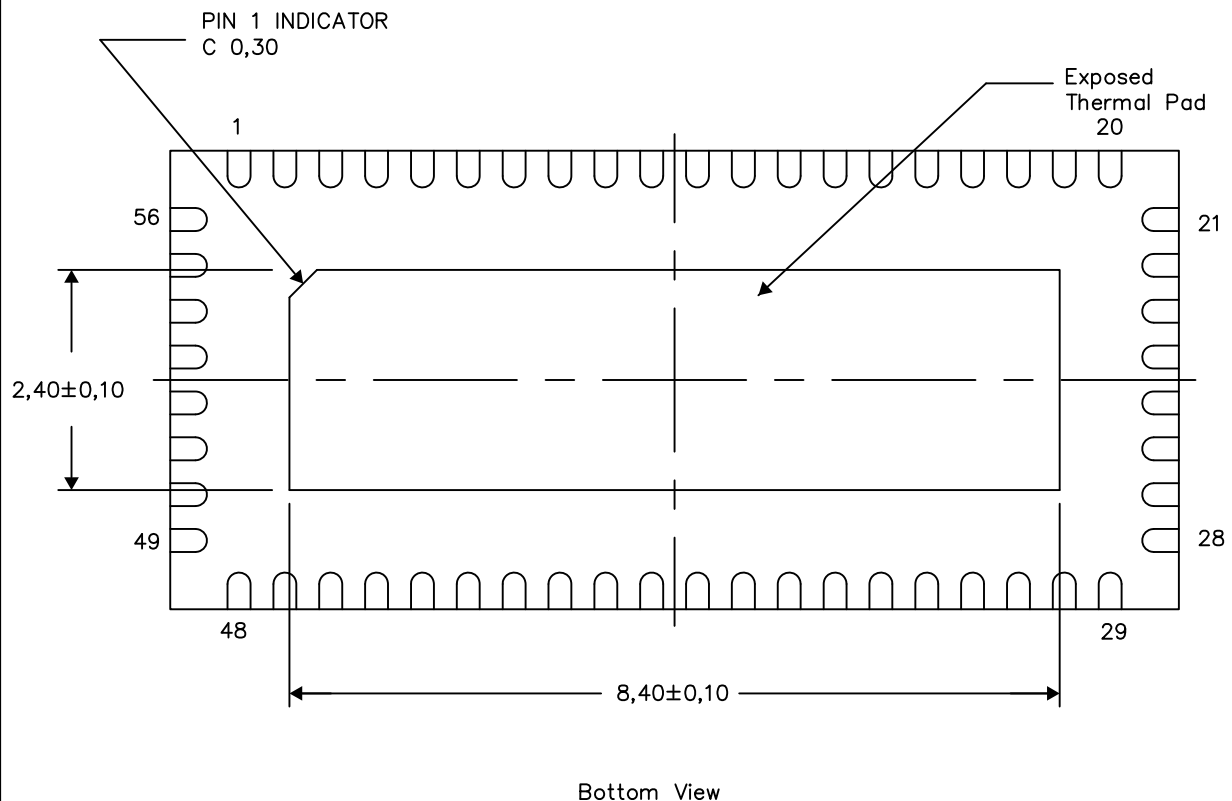
PLASTIC QUAD FLATPACK NO-LEAD

## THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at [www.ti.com](http://www.ti.com).

The exposed thermal pad dimensions for this package are shown in the following illustration.



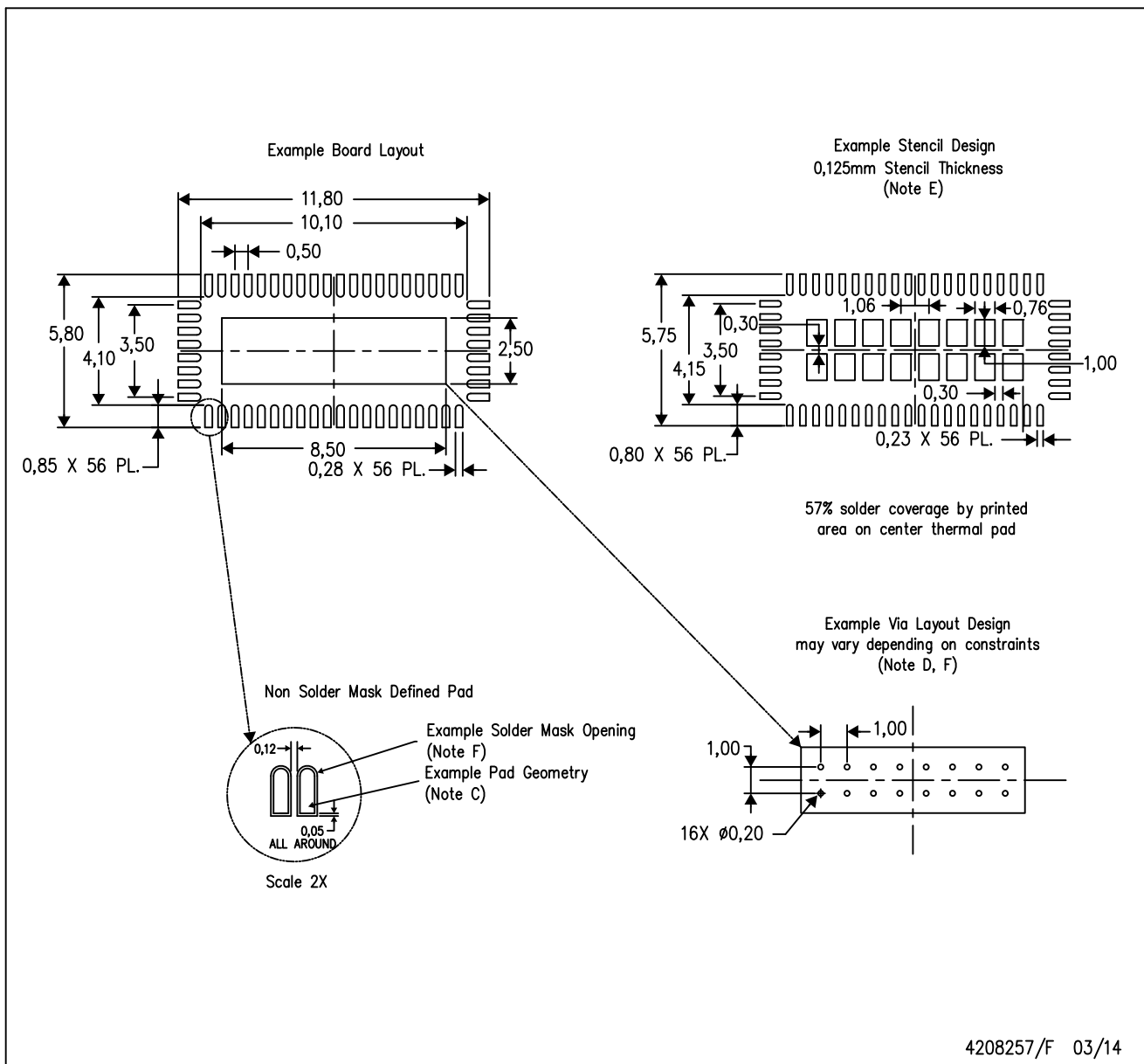
Exposed Thermal Pad Dimensions

4206904/G 03/14

NOTE: All linear dimensions are in millimeters

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- NOTES:
- All linear dimensions are in millimeters.
  - This drawing is subject to change without notice.
  - Publication IPC-7351 is recommended for alternate designs.
  - This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat-Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at [www.ti.com](http://www.ti.com) <<http://www.ti.com>>.
  - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.

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