1 Features

- $V_{CC}$ Operation at 2.5 V to 3.3 V
- $V_{I/O}$ Accepts Signals Up to 5.5 V
- 1.8-V Compatible Control Pin Inputs
- Low-Power Mode When $OE$ Is Disabled (1 μA)
- $R_{ON} = 6 \Omega$ Maximum
- $\Delta R_{ON} = 0.2 \Omega$ Typical
- $C_{io(on)} = 6 \text{ pF}$ Typical
- Low Power Consumption (30 μA Maximum)
- High Bandwidth (900 MHz Typical)
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Performance Tested Per JESD 22
  - 7000-V Human-Body Model (A114-B, Class II)
  - 1000-V Charged-Device Model (C101)
- ESD Performance I/O to GND
  - 12-kV Human-Body Model

2 Applications

- Routes Signals for USB 1.0, 1.1, and 2.0
- Mobile Phones
- Cameras
- Notebooks
- USB I/O expansion

3 Description

The TS3USB221A device is a high-bandwidth switch specially designed for the switching of high-speed USB 2.0 signals in handset and consumer applications, such as cell phones, digital cameras, and notebooks with hubs or controllers with limited USB I/Os. The wide bandwidth (900 MHz) of this switch allows signals to pass with minimum edge and phase distortion. The device multiplexes differential outputs from a USB host device to one of two corresponding outputs. The switch is bidirectional and offers little or no attenuation of the high-speed signals at the outputs. The device also has a low power mode that will reduce the power consumption to 1 μA for portable applications with a battery or limited power budget. The device is designed for low bit-to-bit skew and high channel-to-channel noise isolation, and is compatible with various standards, such as high-speed USB 2.0 (480 Mbps).

The TS3USB221A device integrates ESD protection cells on all pins, is available in a tiny μQFN package (2 mm × 1.5 mm) and is characterized over the free air temperature range from −40°C to 85°C.

4 Simplified Schematic

EN is the internal enable signal applied to the switch.
Table of Contents

1 Features ................................................................. 1
2 Applications ........................................................... 1
3 Description ................................................................ 1
4 Simplified Schematic .............................................. 1
5 Revision History ....................................................... 1
6 Pin Configuration and Functions .............................. 3
7 Specifications ......................................................... 4
   7.1 Absolute Maximum Ratings ................................. 4
   7.2 ESD Ratings ....................................................... 4
   7.3 Recommended Operating Conditions .................... 4
   7.4 Thermal Information ............................................ 4
   7.5 Electrical Characteristics .................................... 5
   7.6 Dynamic Electrical Characteristics, V_{CC} = 3.3 V ±10% 5
   7.7 Dynamic Electrical Characteristics, V_{CC} = 2.5 V ±10% 6
   7.8 Switching Characteristics, V_{CC} = 3.3 V ±10% ......... 6
   7.9 Switching Characteristics, V_{CC} = 2.5 V ±10% ......... 6
   7.10 Typical Characteristics .................................... 7
8 Parameter Measurement Information .................... 8
9 Detailed Description ................................................ 12
   9.1 Overview ......................................................... 12
   9.2 Functional Block Diagram .................................... 12
   9.3 Feature Description ............................................ 13
   9.4 Device Functional Modes .................................... 13
10 Application and Implementation ........................... 14
   10.1 Application Information ..................................... 14
   10.2 Typical Application .......................................... 14
11 Power Supply Recommendations .......................... 16
12 Layout ................................................................. 16
   12.1 Layout Guidelines ............................................ 16
   12.2 Layout Example .............................................. 17
13 Device and Documentation Support ....................... 18
   13.1 Trademarks ..................................................... 18
   13.2 Electrostatic Discharge Caution .......................... 18
   13.3 Glossary ........................................................ 18
14 Mechanical, Packaging, and Orderable Information .... 18

5 Revision History

Changes from Original (November 2008) to Revision A

- Added ESD Ratings table, Feature Description section, Device Functional Modes, Application and Implementation section, Power Supply Recommendations section, Layout section, Device and Documentation Support section, and Mechanical, Packaging, and Orderable Information section. ................................................................. 1
- Deleted the Ordering Information table from the data sheet. See the Mechanical, Packaging, and Orderable Information section for the ordering information................................................................. 1
- Update the document to the new TI data sheet standard ..................................................................................................................... 1
# 6 Pin Configuration and Functions

## Pin Functions

<table>
<thead>
<tr>
<th>PIN</th>
<th>NO.</th>
<th>I/O</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>1D+</td>
<td>1</td>
<td>I/O</td>
<td>USB port 1</td>
</tr>
<tr>
<td>1D-</td>
<td>2</td>
<td>I/O</td>
<td></td>
</tr>
<tr>
<td>2D+</td>
<td>3</td>
<td>I/O</td>
<td>USB port 2</td>
</tr>
<tr>
<td>2D-</td>
<td>4</td>
<td>I/O</td>
<td></td>
</tr>
<tr>
<td>GND</td>
<td>5</td>
<td>-</td>
<td>Ground</td>
</tr>
<tr>
<td>OE</td>
<td>6</td>
<td>I</td>
<td>Bus-switch enable</td>
</tr>
<tr>
<td>D+</td>
<td>8</td>
<td>I/O</td>
<td>Common USB port</td>
</tr>
<tr>
<td>D-</td>
<td>7</td>
<td>I/O</td>
<td></td>
</tr>
<tr>
<td>S</td>
<td>9</td>
<td>I</td>
<td>Select input</td>
</tr>
<tr>
<td>VCC</td>
<td>10</td>
<td>-</td>
<td>Supply voltage</td>
</tr>
</tbody>
</table>

---

**10-Pin µQFN RSE Package (Top View)**

- **VCC**
- **1D+**
- **1D−**
- **2D+**
- **2D−**
- **S**
- **OE**
- **D+**
- **D−**
- **GND**

**10-Pin µQFN RSE Package (Bottom View)**

- **VCC**
- **S**
- **D+**
- **D−**
- **OE**
- **GND**
- **1D+**
- **1D−**
- **2D+**
- **2D−**
# 7 Specifications

## 7.1 Absolute Maximum Ratings

<table>
<thead>
<tr>
<th>Parameter</th>
<th>MIN</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>Supply voltage, ( V_{CC} )</td>
<td>(-0.5)</td>
<td>4.6</td>
<td>V</td>
</tr>
<tr>
<td>Control input voltage, ( V_{S}, V_{OE} )</td>
<td>(-0.5)</td>
<td>7</td>
<td>V</td>
</tr>
<tr>
<td>Switch I/O voltage, ( V_{IO} )</td>
<td>(-0.5)</td>
<td>7</td>
<td>V</td>
</tr>
<tr>
<td>Control input clamp current, ( I_{IK} )</td>
<td>( V_{IN} &lt; 0 )</td>
<td>(-50)</td>
<td>mA</td>
</tr>
<tr>
<td>I/O port clamp current, ( I_{IOK} )</td>
<td>( V_{IO} &lt; 0 )</td>
<td>(-50)</td>
<td>mA</td>
</tr>
<tr>
<td>ON-state switch current, ( I_{IO} )</td>
<td>(</td>
<td>I_{IO}</td>
<td>\leq120)</td>
</tr>
<tr>
<td>Continuous current through ( V_{CC} ) or GND</td>
<td>(</td>
<td>I_{CC}</td>
<td>\leq100)</td>
</tr>
<tr>
<td>Storage temperature range</td>
<td>(-65)</td>
<td>150</td>
<td>°C</td>
</tr>
</tbody>
</table>

(1) Stresses beyond those listed under **absolute maximum ratings** may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under **recommended operating conditions** is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) All voltages are with respect to ground, unless otherwise specified.

(3) The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

(4) \( V_{I} \) and \( V_{O} \) are used to denote specific conditions for \( V_{I/O} \).

(5) \( I_{I} \) and \( I_{O} \) are used to denote specific conditions for \( I_{I/O} \).

## 7.2 ESD Ratings

<table>
<thead>
<tr>
<th>Parameter</th>
<th>VALUE</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>( V_{ESD} ) Electrostatic discharge</td>
<td>Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)</td>
<td>( \pm7000 )</td>
</tr>
<tr>
<td></td>
<td>All pins except I/O to GND</td>
<td>( \pm7000 )</td>
</tr>
<tr>
<td></td>
<td>I/O to GND</td>
<td>( \pm12000 )</td>
</tr>
<tr>
<td></td>
<td>Charged-device model (CDM), per JEDEC specification JESD22-C101(2)</td>
<td>All pins</td>
</tr>
</tbody>
</table>

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 500-V HBM is possible with the necessary precautions.

(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 250-V CDM is possible with the necessary precautions.

## 7.3 Recommended Operating Conditions

<table>
<thead>
<tr>
<th>Parameter</th>
<th>MIN</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>( V_{CC} ) Supply voltage</td>
<td>2.3</td>
<td>3.6</td>
<td>V</td>
</tr>
<tr>
<td>( V_{S}, V_{OE} ) High-level control input voltage</td>
<td>( V_{CC} = 2.3 ) to ( 2.7 ) V</td>
<td>( 0.46 \times V_{CC} )</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td>( V_{CC} = 2.7 ) to ( 3.6 ) V</td>
<td>( 0.46 \times V_{CC} )</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td>Low-level control input voltage</td>
<td>( V_{CC} = 2.3 ) to ( 2.7 ) V</td>
<td>0</td>
</tr>
<tr>
<td></td>
<td></td>
<td>( V_{CC} = 2.7 ) to ( 3.6 ) V</td>
<td>0</td>
</tr>
<tr>
<td>( V_{IO} ) Data input/output voltage</td>
<td>0</td>
<td>5.5</td>
<td>V</td>
</tr>
<tr>
<td>( T_{A} ) Operating free-air temperature</td>
<td>(-40)</td>
<td>85</td>
<td>°C</td>
</tr>
</tbody>
</table>

## 7.4 Thermal Information

<table>
<thead>
<tr>
<th>THERMAL METRIC(1)</th>
<th>RSE</th>
</tr>
</thead>
<tbody>
<tr>
<td>( R_{JA} ) Junction-to-ambient thermal resistance</td>
<td>179.7</td>
</tr>
<tr>
<td>( R_{JC(top)} ) Junction-to-case (top) thermal resistance</td>
<td>107.9</td>
</tr>
<tr>
<td>( R_{JUB} ) Junction-to-board thermal resistance</td>
<td>100.7</td>
</tr>
<tr>
<td>( \psi_{JT} ) Junction-to-top characterization parameter</td>
<td>7.1</td>
</tr>
<tr>
<td>( \psi_{JB} ) Junction-to-board characterization parameter</td>
<td>100.0</td>
</tr>
</tbody>
</table>

(1) For more information about traditional and new thermal metrics, see the **IC Package Thermal Metrics** application report, SPRA953.
7.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>MIN</th>
<th>TYP(2)</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>V_{IK}</strong> Input-Source Clamp Voltage</td>
<td>$V_{CC} = 3.6$ V, $2.7$ V, $I_i = –18$ mA</td>
<td>–1.8</td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td><strong>I_{IN}</strong> Input leakage current, control inputs</td>
<td>$V_{CC} = 3.6$ V, $2.7$ V, $0$ V, $V_{IN} = 0$ V to $3.6$ V</td>
<td>±1</td>
<td></td>
<td></td>
<td>μA</td>
</tr>
<tr>
<td><strong>I_{OZ}</strong> (3) Off-state leakage current</td>
<td>$V_{CC} = 3.6$ V, $2.7$ V, $V_{O} = 0$ V to $5.25$ V, $V_{I} = 0$ V, $V_{IN} = V_{CC}$ or GND, Switch OFF</td>
<td>±1</td>
<td></td>
<td></td>
<td>μA</td>
</tr>
<tr>
<td><strong>I_{(OFF)}</strong> Power-off leakage current</td>
<td>$V_{CC} = 0$ V</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>$V_{IO} = 0$ V to $5.25$ V</td>
<td>±2</td>
<td></td>
<td></td>
<td>μA</td>
</tr>
<tr>
<td></td>
<td>$V_{IO} = 0$ V to $3.6$ V</td>
<td>±2</td>
<td></td>
<td></td>
<td>μA</td>
</tr>
<tr>
<td></td>
<td>$V_{IO} = 0$ V to $2.7$ V</td>
<td>±1</td>
<td></td>
<td></td>
<td>μA</td>
</tr>
<tr>
<td><strong>I_{CC}</strong> Supply Current</td>
<td>$V_{CC} = 3.6$ V, $2.7$ V, $V_{IN} = V_{CC}$ or GND, $I_{IO}$ = 0 V, Switch ON or OFF</td>
<td>30</td>
<td></td>
<td></td>
<td>μA</td>
</tr>
<tr>
<td><strong>I_{CC}</strong> Supply Current (low power mode)</td>
<td>$V_{CC} = 3.6$ V, $2.7$ V, $V_{IN} = V_{CC}$ or GND, Switch disabled, OE in high state</td>
<td>1</td>
<td></td>
<td></td>
<td>μA</td>
</tr>
<tr>
<td><strong>ΔI_{CC}</strong> (4) Supply-current change, control inputs</td>
<td>One input at 1.8 V, Other inputs at $V_{CC}$ or GND</td>
<td>20</td>
<td></td>
<td></td>
<td>μA</td>
</tr>
<tr>
<td></td>
<td>$V_{GC} = 3.6$ V</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>$V_{CC} = 2.7$ V</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>C_{in}</strong> Input capacitance, control inputs</td>
<td>$V_{CC} = 3.3$ V, $2.5$ V, $V_{IN} = V_{CC}$ or $0$ V</td>
<td>1.5</td>
<td>2.5</td>
<td></td>
<td>pF</td>
</tr>
<tr>
<td><strong>C_{w(OF)}</strong> OFF capacitance</td>
<td>$V_{CC} = 3.3$ V, $2.5$ V, $V_{IO} = V_{CC}$ or $0$ V, Switch OFF</td>
<td>3.5</td>
<td>5</td>
<td></td>
<td>pF</td>
</tr>
<tr>
<td><strong>C_{w(on)}</strong> ON capacitance</td>
<td>$V_{CC} = 3.3$ V, $2.5$ V, $V_{IO} = V_{CC}$ or $0$ V, Switch ON</td>
<td>6</td>
<td>7.5</td>
<td></td>
<td>pF</td>
</tr>
<tr>
<td><strong>R_{ON}</strong> (5) ON-state resistance</td>
<td>$V_{CC} = 3$ V, $2.3$ V</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>$V_{I} = 0$ V, $I_{O} = 30$ mA</td>
<td>3</td>
<td>6</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>$V_{I} = 2.4$ V, $I_{O} = –15$ mA</td>
<td>3.4</td>
<td>6</td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>ΔR_{ON}</strong> ON-state resistance match between channels</td>
<td>$V_{CC} = 3$ V, $2.3$ V</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>$V_{I} = 0$ V, $I_{O} = 30$ mA</td>
<td>0.2</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>$V_{I} = 1.7$ V, $I_{O} = –15$ mA</td>
<td>0.2</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>R_{ON(flat)}</strong> ON-state resistance flatness</td>
<td>$V_{CC} = 3$ V, $2.3$ V</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>$V_{I} = 0$ V, $I_{O} = 30$ mA</td>
<td>1</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>$V_{I} = 1.7$ V, $I_{O} = –15$ mA</td>
<td>1</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

(1) $V_{IN}$ and $I_{IN}$ refer to control inputs. $V_i$, $V_O$, $I_i$, and $I_O$ refer to data pins.
(2) All typical values are at $V_{CC} = 3.3$ V (unless otherwise noted), $T_A = 25^\circ$C.
(3) For I/O ports, the parameter $I_{OZ}$ includes the input leakage current.
(4) This is the increase in supply current for each input that is at the specified TTL voltage level, rather than $V_{CC}$ or GND.
(5) Measured by the voltage drop between the A and B terminals at the indicated current through the switch. ON-state resistance is determined by the lower of the voltages of the two (A or B) terminals.

7.6 Dynamic Electrical Characteristics, $V_{CC} = 3.3$ V ±10%

over operating range, $T_A = –40^\circ$C to $85^\circ$C, $V_{CC} = 3.3$ V ±10%, GND = 0 V

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>$X_{TALK}$ Crosstalk</td>
<td>$R_L = 50$ Ω, $f = 250$ MHz</td>
<td>–40</td>
<td></td>
<td></td>
<td>dB</td>
</tr>
<tr>
<td>$O_{IRR}$ OFF isolation</td>
<td>$R_L = 50$ Ω, $f = 250$ MHz</td>
<td>–41</td>
<td></td>
<td></td>
<td>dB</td>
</tr>
<tr>
<td>$BW$ Bandwidth (–3 dB)</td>
<td>$R_L = 50$ Ω</td>
<td>0.9</td>
<td></td>
<td></td>
<td>GHz</td>
</tr>
</tbody>
</table>
7.7 Dynamic Electrical Characteristics, \( V_{CC} = 2.5 \text{ V } \pm 10\% \)

over operating range, \( T_A = -40^\circ\text{C} \text{ to } 85^\circ\text{C}, \ V_{CC} = 2.5 \text{ V } \pm 10\%, \ GND = 0 \text{ V} \)

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>( X_{TALK} )</td>
<td>Crosstalk ( R_L = 50, f = 250 \text{ MHz} )</td>
<td>–39</td>
<td>dB</td>
<td></td>
<td></td>
</tr>
<tr>
<td>( O_{IRR} )</td>
<td>OFF isolation ( R_L = 50, f = 250 \text{ MHz} )</td>
<td>–40</td>
<td>dB</td>
<td></td>
<td></td>
</tr>
<tr>
<td>BW</td>
<td>Bandwidth (3 dB) ( R_L = 50 )</td>
<td>0.9</td>
<td>GHz</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

7.8 Switching Characteristics, \( V_{CC} = 3.3 \text{ V } \pm 10\% \)

over operating range, \( T_A = -40^\circ\text{C} \text{ to } 85^\circ\text{C}, \ V_{CC} = 3.3 \text{ V } \pm 10\%, \ GND = 0 \text{ V} \)

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>MIN</th>
<th>TYP(1)</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>( t_{pd} )</td>
<td>Propagation delay(2) (3)</td>
<td>0.25</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>( t_{ON} )</td>
<td>Line enable time ( S \text{ to } D, nD )</td>
<td>30</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>( t_{OFF} )</td>
<td>Line disable time ( \overline{OE} \text{ to } D, nD )</td>
<td>12</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>( t_{SK(O)} )</td>
<td>Output skew between center port to any other port(2)</td>
<td>0.1</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>( t_{SK(P)} )</td>
<td>Skew between opposite transitions of the same output ( (t_{PHL} - t_{PLH}) ) (2)</td>
<td>0.1</td>
<td>ns</td>
<td></td>
</tr>
</tbody>
</table>

(1) For Max or Min conditions, use the appropriate value specified under Electrical Characteristics for the applicable device type.
(2) Specified by design
(3) The bus switch contributes no propagational delay other than the RC delay of the on resistance of the switch and the load capacitance. The time constant for the switch alone is of the order of 0.25 ns for 10-pF load. Since this time constant is much smaller than the rise/fall times of typical driving signals, it adds very little propagational delay to the system. Propagational delay of the bus switch, when used in a system, is determined by the driving circuit on the driving side of the switch and its interactions with the load on the driven side.

7.9 Switching Characteristics, \( V_{CC} = 2.5 \text{ V } \pm 10\% \)

over operating range, \( T_A = -40^\circ\text{C} \text{ to } 85^\circ\text{C}, \ V_{CC} = 2.5 \text{ V } \pm 10\%, \ GND = 0 \text{ V} \)

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>MIN</th>
<th>TYP(1)</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>( t_{pd} )</td>
<td>Propagation delay(2) (3)</td>
<td>0.25</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>( t_{ON} )</td>
<td>Line enable time ( S \text{ to } D, nD )</td>
<td>50</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>( t_{OFF} )</td>
<td>Line disable time ( \overline{OE} \text{ to } D, nD )</td>
<td>23</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>( t_{SK(O)} )</td>
<td>Output skew between center port to any other port(2)</td>
<td>0.1</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>( t_{SK(P)} )</td>
<td>Skew between opposite transitions of the same output ( (t_{PHL} - t_{PLH}) ) (2)</td>
<td>0.1</td>
<td>ns</td>
<td></td>
</tr>
</tbody>
</table>

(1) For Max or Min conditions, use the appropriate value specified under Electrical Characteristics for the applicable device type.
(2) Specified by design
(3) The bus switch contributes no propagational delay other than the RC delay of the on resistance of the switch and the load capacitance. The time constant for the switch alone is of the order of 0.25 ns for 10-pF load. Since this time constant is much smaller than the rise/fall times of typical driving signals, it adds very little propagational delay to the system. Propagational delay of the bus switch, when used in a system, is determined by the driving circuit on the driving side of the switch and its interactions with the load on the driven side.
7.10 Typical Characteristics

![Figure 1. Gain vs Frequency](image1)

![Figure 2. OFF Isolation vs Frequency](image2)

![Figure 3. Crosstalk vs Frequency](image3)

![Figure 4. $r_{on}$ vs $V_{IN}$ ($I_{OUT} = -15$ mA)](image4)

![Figure 5. $r_{ON}$ vs $V_{IN}$ ($I_{OUT} = 30$ mA)](image5)
8 Parameter Measurement Information

(1) All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z₀ = 50 Ω, tᵣ < 5 ns, tᵢ < 5 ns.

(2) C_L includes probe and jig capacitance.

Figure 6. Turn-On (t_ON) and Turn-Off Time (t_OFF)

Figure 7. OFF Isolation (O_ISO)
Parameter Measurement Information (continued)

Figure 8. Crosstalk ($X_{\text{TALK}}$)

Figure 9. Bandwidth (BW)

Figure 10. Propagation Delay
Parameter Measurement Information (continued)

\[ t_{\text{SUP}} = |t_{\text{PLH}} - t_{\text{PHL}}| \]

**PULSE SKEW** \( t_{\text{SUP}} \)

\[ t_{\text{SK(O)}} = |t_{\text{PLH1}} - t_{\text{PLH2}}| \]

**OUTPUT SKEW** \( t_{\text{SK(O)}} \)

**Figure 11. Skew Test**

**Figure 12. ON-State Resistance (\( r_{\text{on}} \))**
Parameter Measurement Information (continued)

Figure 13. OFF-State Leakage Current

Figure 14. Capacitance
9 Detailed Description

9.1 Overview

The TS3USB221A device is a 2-channel SPDT switch specially designed for the switching of high-speed USB 2.0 signals in handset and consumer applications, such as cell phones, digital cameras, and notebooks with hubs or controllers with limited USB I/Os. The wide bandwidth (900 MHz) of this switch allows signals to pass with minimum edge and phase distortion. The device multiplexes differential outputs from a USB host device to one of two corresponding outputs. The switch is bidirectional and offers little or no attenuation of the high-speed signals at the outputs. The device also has a low power mode that will reduce the power consumption to 1 μA for portable applications with a battery or limited power budget.

The device is designed for low bit-to-bit skew and high channel-to-channel noise isolation, and is compatible with various standards, such as high-speed USB 2.0 (480 Mbps).

The TS3USB221A device integrates ESD protection cells on all pins, is available in a tiny μQFN package (2 mm × 1.5 mm) and is characterized over the free air temperature range from –40°C to 85°C.

9.2 Functional Block Diagram

A. EN is the internal enable signal applied to the switch.

Figure 15. Simplified Schematic of Each FET Switch (SW)
9.1 Feature Description

9.1.1 Low Power Mode
The TS3USB221A has a low power mode that reduces the power consumption to 1 μA while the devices is not in use. To put the device in low power mode and disable the switch, the bus-switch enable pin OE must be supplied with a logic "High" signal.

9.2 Device Functional Modes

Table 1. Truth Table

<table>
<thead>
<tr>
<th>S</th>
<th>OE</th>
<th>FUNCTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>X</td>
<td>H</td>
<td>Disconnect</td>
</tr>
<tr>
<td>L</td>
<td>L</td>
<td>D = 1D</td>
</tr>
<tr>
<td>H</td>
<td>L</td>
<td>D = 2D</td>
</tr>
</tbody>
</table>
10 Application and Implementation

NOTE
Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI’s customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

10.1 Application Information
There are many USB applications in which the USB hubs or controllers have a limited number of USB I/Os. The TS3USB221A solution can effectively expand the limited USB I/Os by switching between multiple USB buses in order to interface them to a single USB hub or controller.

10.2 Typical Application

![Application Schematic](image)

Figure 16. Application Schematic
Typical Application (continued)

10.2.1 Design Requirements

Design requirements of the USB 1.0, 1.1, and 2.0 standards should be followed.

It is recommended that the digital control pins S and OE be pulled up to V\textsubscript{CC} or down to GND to avoid undesired switch positions that could result from the floating pin.

10.2.2 Detailed Design Procedure

The TS3USB221A can be properly operated without any external components. However, it is recommended that unused pins should be connected to ground through a 50-Ω resistor to prevent signal reflections back into the device.

10.2.3 Application Curves

![Figure 17. Eye Pattern: 480-Mbps USB Signal With No Switch (Through Path)](image)

![Figure 18. Eye Pattern: 480-Mbps USB Signal With Switch NC Path](image)

![Figure 19. Eye Pattern: 480-Mbps USB Signal With Switch NO Path](image)
11 Power Supply Recommendations

Power to the device is supplied through the VCC pin and should follow the USB 1.0, 1.1, and 2.0 standards. A bypass capacitor is recommended to be placed as close to the supply pin VCC to help smooth out lower frequency noise to provide better load regulation across the frequency spectrum.

12 Layout

12.1 Layout Guidelines

Place supply bypass capacitors as close to VCC pin as possible and avoid placing the bypass caps near the D+/D- traces.

The high speed D+/D- traces should always be matched lengths and must be no more than 4 inches; otherwise, the eye diagram performance may be degraded. A high-speed USB connection is made through a shielded, twisted pair cable with a differential characteristic impedance. In layout, the impedance of D+ and D- traces should match the cable characteristic differential impedance for optimal performance.

Route the high-speed USB signals using a minimum of vias and corners which will reduce signal reflections and impedance changes. When a via must be used, increase the clearance size around it to minimize its capacitance. Each via introduces discontinuities in the signal’s transmission line and increases the chance of picking up interference from the other layers of the board. Be careful when designing test points on twisted pair lines; through-hole pins are not recommended.

When it becomes necessary to turn 90°, use two 45° turns or an arc instead of making a single 90° turn. This reduces reflections on the signal traces by minimizing impedance discontinuities.

Do not route USB traces under or near crystals, oscillators, clock signal generators, switching regulators, mounting holes, magnetic devices or IC’s that use or duplicate clock signals.

Avoid stubs on the high-speed USB signals because they cause signal reflections. If a stub is unavoidable, then the stub should be less than 200 mm.

Route all high-speed USB signal traces over continuous planes (VCC or GND), with no interruptions.

Avoid crossing over anti-etch, commonly found with plane splits.

Due to high frequencies associated with the USB, a printed circuit board with at least four layers is recommended; two signal layers separated by a ground and power layer as shown in Figure 20.

![Figure 20. Four-Layer Board Stack-Up](image)

The majority of signal traces should run on a single layer, preferably Signal 1. Immediately next to this layer should be the GND plane, which is solid with no cuts. Avoid running signal traces across a split in the ground or power plane. When running across split planes is unavoidable, sufficient decoupling must be used. Minimizing the number of signal vias reduces EMI by reducing inductance at high frequencies.
12.2 Layout Example

**LEGEND**
- VIA to Power Plane
- VIA to GND Plane
- Polygonal Copper Pour

---

**Figure 21. Package Layout Diagram**

USB Port 1
- 1: D+
- 2: D-

USB Port 2
- 3: 2D+
- 4: 2D-

VCC
- 10

GND
- 5

Bypass Capacitor

To Microcontroller

To USB Host

To USB Port 1

To USB Port 2
13 Device and Documentation Support

13.1 Trademarks
All trademarks are the property of their respective owners.

13.2 Electrostatic Discharge Caution
These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

13.3 Glossary
SLYZ022 — *Ti Glossary.*
This glossary lists and explains terms, acronyms, and definitions.

14 Mechanical, Packaging, and Orderable Information
The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.
# PACKAGING INFORMATION

<table>
<thead>
<tr>
<th>Orderable Device</th>
<th>Status</th>
<th>Package Type</th>
<th>Package Drawing</th>
<th>Pins</th>
<th>Package Qty</th>
<th>Eco Plan</th>
<th>Lead/Ball Finish</th>
<th>MSL Peak Temp</th>
<th>Op Temp (°C)</th>
<th>Device Marking</th>
<th>Samples</th>
</tr>
</thead>
<tbody>
<tr>
<td>TS3USB221ARSER</td>
<td>ACTIVE</td>
<td>UQFN</td>
<td>RSE</td>
<td>10</td>
<td>3000</td>
<td>Green (RoHS &amp; no Sb/Br)</td>
<td>CU NIPDAU</td>
<td>Level-1-260C-UNLIM</td>
<td>-40 to 85</td>
<td>(LH7, LHR, LHV)</td>
<td></td>
</tr>
<tr>
<td>TS3USB221ARSERG4</td>
<td>ACTIVE</td>
<td>UQFN</td>
<td>RSE</td>
<td>10</td>
<td>3000</td>
<td>Green (RoHS &amp; no Sb/Br)</td>
<td>CU NIPDAU</td>
<td>Level-1-260C-UNLIM</td>
<td>-40 to 85</td>
<td>(LH7, LHR, LHV)</td>
<td>Samples</td>
</tr>
</tbody>
</table>

(1) The marketing status values are defined as follows:
- **ACTIVE**: Product device recommended for new designs.
- **LIFEBUY**: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
- **NRND**: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
- **PREVIEW**: Device has been announced but is not in production. Samples may or may not be available.
- **OBSOLETE**: TI has discontinued the production of the device.

(2) **RoHS**: TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
- **RoHS Exempt**: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
- **Green**: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) **MSL, Peak Temp.** - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

**Important Information and Disclaimer:** The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.
OTHER QUALIFIED VERSIONS OF TS3USB221A:

- Automotive: TS3USB221A-Q1

NOTE: Qualified Version Definitions:

- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects
TAPE AND REEL INFORMATION

<table>
<thead>
<tr>
<th>Device</th>
<th>Package Type</th>
<th>Package Drawing</th>
<th>Pins</th>
<th>SPQ</th>
<th>Reel Diameter (mm)</th>
<th>Reel Width W1 (mm)</th>
<th>A0  (mm)</th>
<th>B0  (mm)</th>
<th>K0  (mm)</th>
<th>P1  (mm)</th>
<th>W   (mm)</th>
<th>Pin1 Quadrant</th>
</tr>
</thead>
<tbody>
<tr>
<td>TS3USB221ARSER</td>
<td>UQFN</td>
<td>RSE</td>
<td>10</td>
<td>3000</td>
<td>180.0</td>
<td>9.5</td>
<td>1.7</td>
<td>2.3</td>
<td>0.75</td>
<td>4.0</td>
<td>8.0</td>
<td>Q1</td>
</tr>
<tr>
<td>TS3USB221ARSER</td>
<td>UQFN</td>
<td>RSE</td>
<td>10</td>
<td>3000</td>
<td>180.0</td>
<td>9.5</td>
<td>1.7</td>
<td>2.2</td>
<td>0.75</td>
<td>4.0</td>
<td>8.0</td>
<td>Q1</td>
</tr>
<tr>
<td>TS3USB221ARSER</td>
<td>UQFN</td>
<td>RSE</td>
<td>10</td>
<td>3000</td>
<td>180.0</td>
<td>8.4</td>
<td>1.68</td>
<td>2.13</td>
<td>0.76</td>
<td>4.0</td>
<td>8.0</td>
<td>Q1</td>
</tr>
</tbody>
</table>

*All dimensions are nominal.*
### TAPE AND REEL BOX DIMENSIONS

*All dimensions are nominal*

<table>
<thead>
<tr>
<th>Device</th>
<th>Package Type</th>
<th>Package Drawing</th>
<th>Pins</th>
<th>SPQ</th>
<th>Length (mm)</th>
<th>Width (mm)</th>
<th>Height (mm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>TS3USB221ARSER</td>
<td>UQFN</td>
<td>RSE</td>
<td>10</td>
<td>3000</td>
<td>184.0</td>
<td>184.0</td>
<td>19.0</td>
</tr>
<tr>
<td>TS3USB221ARSER</td>
<td>UQFN</td>
<td>RSE</td>
<td>10</td>
<td>3000</td>
<td>189.0</td>
<td>185.0</td>
<td>36.0</td>
</tr>
<tr>
<td>TS3USB221ARSER</td>
<td>UQFN</td>
<td>RSE</td>
<td>10</td>
<td>3000</td>
<td>202.0</td>
<td>201.0</td>
<td>28.0</td>
</tr>
</tbody>
</table>
NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. QFN (Quad Flatpack No-Lead) package configuration.
D. This package complies to JEDEC MO-298 variation UEFD.
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC-7351 is recommended for alternate designs.
D. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.
E. Maximum stencil thickness 0.127 mm (5 mils). All linear dimensions are in millimeters.
F. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
G. Side aperture dimensions over-print land for acceptable area ratio > 0.66. Customers may reduce side aperture dimensions if stencil manufacturing process allows for sufficient release at smaller opening.
Texas Instruments Incorporated (TI) reserves the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete.

TI's published terms of sale for semiconductor products (http://www.ti.com/sc/docs/stdterms.htm) apply to the sale of packaged integrated circuit products that TI has qualified and released to market. Additional terms may apply to the use or sale of other types of TI products and services.

Reproduction of significant portions of TI information in TI data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such reproduced documentation. Information of third parties may be subject to additional restrictions. Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and/or implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyers and others who are developing systems that incorporate TI products (collectively, “Designers”) understand and agree that Designers remain responsible for using their independent analysis, evaluation and judgment in designing their applications and that Designers have full and exclusive responsibility to assure the safety of Designers’ applications and compliance of their applications (and of all TI products used in or for Designers’ applications) with all applicable regulations, laws and other applicable requirements. Designers represent that, with respect to their applications, Designers have all the necessary expertise to design and implement safeguards that (1) anticipate dangerous consequences of failures, (2) monitor failures and their consequences, and (3) lessen the likelihood of failures that might cause harm and take appropriate actions. Designers agree that prior to using or distributing any applications that include TI products, Designers will thoroughly test such applications and the functionality of such TI products as used in such applications.

TI’s provision of technical, application or other design advice, quality characterization, reliability data or other services or information, including, but not limited to, reference designs and materials relating to evaluation modules, (collectively, “TI Resources”) are intended to assist designers who are developing applications that incorporate TI products; by downloading, accessing or using TI Resources in any way, Designer (individually or, if Designer is acting on behalf of a company, Designer’s company) agrees to use any particular TI Resource solely for this purpose and subject to the terms of this Notice.

TI’s provision of TI Resources does not expand or otherwise alter TI’s applicable published warranties or warranty disclaimers for TI products, and no additional obligations or liabilities arise from TI providing such TI Resources. TI reserves the right to make corrections, enhancements, improvements and other changes to its TI Resources. TI has not conducted any testing other than that specifically described in the published documentation for a particular TI Resource.

Designers are authorized to use, copy and modify any individual TI Resource only in connection with the development of applications that include the TI product(s) identified in such TI Resource. NO OTHER LICENSE, EXPRESS OR IMPLIED, BY ESTOPPEL OR OTHERWISE TO ANY TECHNOLOGY, PATENT, COPYRIGHT, TRADE SECRET, TRADE NAME, TRADE PRACTICE, TRADE CUSTOM, DEVICE PACKAGE, NAME OR OTHER INTELLECTUAL PROPERTY RIGHT OF TI OR ANY THIRD PARTY IS GRANTED HEREIN, including but not limited to any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information regarding or referencing third-party products or services does not constitute a license to use such products or services, or a warranty or endorsement thereof. Use of TI Resources may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

TI RESOURCES ARE PROVIDED “AS IS” AND WITH ALL FAULTS. TI DISCLAIMS ALL OTHER WARRANTIES OR REPRESENTATIONS, EXPRESS OR IMPLIED, REGARDING RESOURCES OR USE THEREOF, INCLUDING BUT NOT LIMITED TO ACCURACY OR COMPLETENESS, TITLE, ANY EPIDEMIC FAILURE WARRANTY AND ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, AND NON-INFRINGEMENT OF ANY THIRD PARTY INTELLECTUAL PROPERTY RIGHTS. TI SHALL NOT BE LIABLE FOR AND SHALL NOT DEFEND OR INDEMNIFY DESIGNER AGAINST ANY CLAIM, INCLUDING BUT NOT LIMITED TO ANY INFRINGEMENT CLAIM THAT RELATES TO OR IS BASED ON ANY COMBINATION OF PRODUCTS EVEN IF DESCRIBED IN TI RESOURCES OR OTHERWISE. IN NO EVENT SHALL TI BE LIABLE FOR ANY ACTUAL, DIRECT, SPECIAL, COLLATERAL, INDIRECT, PUNITIVE, INCIDENTAL, CONSEQUENTIAL OR EXEMPLARY DAMAGES IN CONNECTION WITH OR ARISING OUT OF TI RESOURCES OR USE THEREOF, AND REGARDLESS OF WHETHER TI HAS BEEN ADVISED OF THE POSSIBILITY OF SUCH DAMAGES.

Unless TI has explicitly designated an individual product as meeting the requirements of a particular industry standard (e.g., ISO/TS 16949 and ISO 26262), TI is not responsible for any failure to meet such industry standard requirements.

Where TI specifically promotes products as facilitating functional safety or as compliant with industry functional safety standards, such products are intended to help enable customers to design and create their own applications that meet applicable functional safety standards and requirements. Using products in an application does not by itself establish any safety features in the application. Designers must ensure compliance with safety-related requirements and standards applicable to their applications. Designers may not use any TI products in life-critical medical equipment unless authorized officers of the parties have executed a special contract specifically governing such use. Life-critical medical equipment is medical equipment where failure of such equipment would cause serious bodily injury or death (e.g., life support, pacemakers, defibrillators, heart pumps, neurostimulators, and implantables). Such equipment includes, without limitation, all medical devices identified by the U.S. Food and Drug Administration as Class III devices and equivalent classifications outside the U.S.

TI may expressly designate certain products as completing a particular qualification (e.g., Q100, Military Grade, or Enhanced Product). Designers agree that it has the necessary expertise to select the product with the appropriate qualification designation for their applications and that proper product selection is at Designers’ own risk. Designers are solely responsible for compliance with all legal and regulatory requirements in connection with such selection.

Designer will fully indemnify TI and its representatives against any damages, costs, losses, and/or liabilities arising out of Designer’s non-compliance with the terms and provisions of this Notice.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2017, Texas Instruments Incorporated