TS5A9411 10-Ω 1:2 SPDT Analog Switch
Single-Channel 2:1 Multiplexer and Demultiplexer

1 Features
• Specified Break-Before-Make Switching
• Low ON-State Resistance
  (10-Ω Maximum at V_{CC} = 5 V)
• Low Power Consumption
• TTL- and CMOS-Compatible Control Input
• Low Input and Output Capacitance
• Excellent ON-State Resistance Matching
• Low Total Harmonic Distortion
• 2.25-V to 5.5-V Single-Supply Operation
• Latch-Up Performance Exceeds 100 mA
  Per JESD 78, Class II
• ESD Performance Tested Per JESD 22
  – 2000-V Human-Body Model
    (A114-B, Class II)
  – 1000-V Charged-Device Model (C101)
• Control Inputs Are 5.5-V Tolerant

2 Applications
• Cell Phones
• Communication Systems
• Portable Test Equipment
• Battery Operated Systems
• Sample-and-Hold Circuits

3 Description
The TS5A9411 device is a bidirectional, single-pole double-throw (SPDT) analog switch that is designed to operate from 2.25 V to 5.5 V. The device offers low ON-state resistance, low leakage, and low power with a break-before-make feature. These features make this device suitable for portable and battery-powered applications.

Device Information

<table>
<thead>
<tr>
<th>PART NUMBER</th>
<th>PACKAGE</th>
<th>BODY SIZE (NOM)</th>
</tr>
</thead>
<tbody>
<tr>
<td>TS5A9411</td>
<td>SOT (6)</td>
<td>2.00 mm x 1.25 mm</td>
</tr>
</tbody>
</table>

(1) For all available packages, see the orderable addendum at the end of the data sheet.

An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.
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4 Revision History
NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (July 2008) to Revision B  Page

- Added Device Information table, Pin Configuration and Functions section, Specifications section, ESD Ratings table, Recommended Operating Conditions table, Detailed Description section, Application and Implementation section, Power Supply Recommendations section, Layout section, Device and Documentation Support section, and Mechanical, Packaging, and Orderable Information section ........................................ 1
- Deleted Ordering Information table; see Package Option Addendum at the end of the data sheet .............................. 1
- Deleted Summary of Characteristics table .................................................................................................................. 1
- Moved ON-state switch current and ON-state peak switch current From: Absolute Maximum Ratings table To: Recommended Operating Conditions table ........................................................................ 4
- Added Thermal Information table ................................................................................................................................. 4
- Changed Package thermal impedance, $R_{IN}$, value in Thermal Information table From: 259°C/W To: 346.7°C/W .............. 4
- Deleted Charge Injection vs $V_{COM}$ graph from Typical Characteristics ........................................................................... 7
- Changed graph title From: OFF Isolation vs Crosstalk ($V_{CC} = 3$ V) To: Crosstalk and Insertion Loss vs Frequency ($V_{CC} = 3$ V) in Typical Characteristics ................................................................................................................................. 7
- Changed $V_{+}$ to $V_{CC}$ and IN to $V_{IN}$ on all images in Parameter Measurement Information .................................................. 8
5 Pin Configuration and Functions

### Pin Functions

<table>
<thead>
<tr>
<th>PIN NAME</th>
<th>PIN NO.</th>
<th>I/O</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>COM</td>
<td>5</td>
<td>I/O</td>
<td>Common signal path</td>
</tr>
<tr>
<td>GND</td>
<td>3</td>
<td>—</td>
<td>Digital ground</td>
</tr>
<tr>
<td>IN</td>
<td>1</td>
<td>I/O</td>
<td>Digital control input. High = COM connected to NO; Low = COM connected to NC.</td>
</tr>
<tr>
<td>NC</td>
<td>4</td>
<td>I/O</td>
<td>Normally closed signal path</td>
</tr>
<tr>
<td>NO</td>
<td>6</td>
<td>I/O</td>
<td>Normally open signal path</td>
</tr>
<tr>
<td>VCC</td>
<td>2</td>
<td>—</td>
<td>Power supply</td>
</tr>
</tbody>
</table>

6 Specifications

6.1 Absolute Maximum Ratings

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>MIN</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>Supply voltage</td>
<td>-0.3</td>
<td>6</td>
<td>V</td>
</tr>
<tr>
<td>Analog voltage</td>
<td>-0.3</td>
<td>$V_{CC} + 0.3$</td>
<td>V</td>
</tr>
<tr>
<td>Digital input voltage</td>
<td>-0.5</td>
<td>$V_{CC} + 0.3$</td>
<td>V</td>
</tr>
<tr>
<td>Analog port diode current ($V_{NC}$, $V_{NO}$, $V_{COM} &lt; 0$)</td>
<td>-50</td>
<td>mA</td>
<td></td>
</tr>
<tr>
<td>Digital input clamp current ($V_{I} &lt; 0$)</td>
<td>-50</td>
<td>mA</td>
<td></td>
</tr>
<tr>
<td>Continuous current through VCC</td>
<td>100</td>
<td>mA</td>
<td></td>
</tr>
<tr>
<td>Continuous current through GND</td>
<td></td>
<td>mA</td>
<td></td>
</tr>
<tr>
<td>Storage temperature, $T_{stg}$</td>
<td>-65</td>
<td>150</td>
<td>°C</td>
</tr>
</tbody>
</table>

(1) Stresses beyond those listed under **Absolute Maximum Ratings** may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under **Recommended Operating Conditions**. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) All voltages are with respect to ground, unless otherwise specified.

(3) This value is limited to 5.5 V (maximum).

6.2 ESD Ratings

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>VALUE</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{(ESD)}$ (Electrostatic discharge)</td>
<td>Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001</td>
<td>±2000</td>
</tr>
<tr>
<td></td>
<td>Charged-device model (CDM), per JEDEC specification JESD22-C101</td>
<td>±1000</td>
</tr>
</tbody>
</table>

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.
### 6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>MIN</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>(V_{CC}) Supply voltage</td>
<td>2.25</td>
<td>5.5</td>
<td>V</td>
</tr>
<tr>
<td>(V_{NO}) Analog voltage</td>
<td>0</td>
<td>(V_{CC})</td>
<td>V</td>
</tr>
<tr>
<td>(V_{NC}) Digital input voltage</td>
<td>0</td>
<td>(V_{CC})</td>
<td>V</td>
</tr>
<tr>
<td>(V_{COM}) Digital input voltage</td>
<td>0</td>
<td>(V_{CC})</td>
<td>V</td>
</tr>
<tr>
<td>(V_I) ON-state switch current ((V_{NO}, V_{NC}, V_{COM} = 0) to (V_{CC}))</td>
<td>−50</td>
<td>50</td>
<td>mA</td>
</tr>
<tr>
<td>(V_I) ON-state peak switch current ((V_{NO}, V_{NC}, V_{COM} = 0) to (V_{CC}))</td>
<td>−200</td>
<td>200</td>
<td>mA</td>
</tr>
</tbody>
</table>

(1) Pulse at 1-ms duration < 10% duty cycle

### 6.4 Thermal Information

<table>
<thead>
<tr>
<th>THERMAL METRIC(1)</th>
<th>TSSA9411 DCK (SOT)</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>(R_{UA}) Junction-to-ambient thermal resistance</td>
<td>346.7</td>
<td>°C/W</td>
</tr>
<tr>
<td>(R_{UJC(top)}) Junction-to-case (top) thermal resistance</td>
<td>163.7</td>
<td>°C/W</td>
</tr>
<tr>
<td>(R_{UB}) Junction-to-board thermal resistance</td>
<td>154.5</td>
<td>°C/W</td>
</tr>
<tr>
<td>(\psi_{JT}) Junction-to-top characterization parameter</td>
<td>17.4</td>
<td>°C/W</td>
</tr>
<tr>
<td>(\psi_{UB}) Junction-to-board characterization parameter</td>
<td>153.8</td>
<td>°C/W</td>
</tr>
</tbody>
</table>

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

### 6.5 Electrical Characteristics: 5-V Supply

\(V_{CC} = 5\) V, \(T_A = 25^\circ\)C (unless otherwise noted)

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>(I_{ON}) ON-state resistance</td>
<td>(V_{NO} = 3) V, (V_{NC} = 4.5) V, (I_{COM} = -10) mA, Switch ON, see Figure 5</td>
<td>(T_A = 25^\circ)C</td>
<td>5.3</td>
<td>9</td>
<td>Ω</td>
</tr>
<tr>
<td>(\Delta I_{ON}) ON-state resistance match between channels</td>
<td>(V_{NO} = 3) V, (V_{CC} = 4.5) V, (I_{COM} = -10) mA, Switch ON, see Figure 5</td>
<td>(T_A = 25^\circ)C</td>
<td>0.03</td>
<td>0.3</td>
<td>Ω</td>
</tr>
<tr>
<td>(I_{ON(FLAT)}) ON-state resistance flatness</td>
<td>(0 \leq (V_{NO} \leq V_{CC}) \leq 4.5) V, (I_{COM} = -10) mA, Switch ON, see Figure 5</td>
<td>(T_A = 25^\circ)C</td>
<td>2</td>
<td></td>
<td></td>
</tr>
<tr>
<td>(I_{NO(OFF)}, I_{NO(OFF)}) NC, NO OFF leakage current</td>
<td>(V_{NO} = 1) V and (I_{COM} = 0) to (4.5) V, or (V_{NO} = 4.5) V and (I_{COM} = 1) V, (V_{CC} = 5.5) V, Switch OFF, see Figure 6</td>
<td>(T_A = 25^\circ)C</td>
<td>−500</td>
<td>500</td>
<td>pA</td>
</tr>
<tr>
<td>(I_{NO(ON)}, I_{NO(ON)}) NC, NO ON leakage current</td>
<td>(V_{NO} = 1) V and (I_{COM} = 1) V or (V_{NO} = 4.5) V and (I_{COM} = 1) V, (V_{CC} = 5.5) V, Switch ON, see Figure 7</td>
<td>(T_A = 25^\circ)C</td>
<td>−500</td>
<td>500</td>
<td>pA</td>
</tr>
<tr>
<td>(I_{COM(ON)}) COM ON leakage current</td>
<td>(V_{NO} = 1) V or (V_{CC} = 5.5) V, Switch ON, see Figure 7</td>
<td>(T_A = 25^\circ)C</td>
<td>−3</td>
<td>3</td>
<td>nA</td>
</tr>
</tbody>
</table>

**DIGITAL INPUT (IN)(1)**

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>(V_{IH}) Input logic high</td>
<td>(−40^\circ)C (\leq T_A \leq 85^\circ)C</td>
<td>(4.5) V (\leq V_{CC} \leq 5.5) V</td>
<td>2.4</td>
<td>5.5</td>
<td>V</td>
</tr>
<tr>
<td>(V_{IL}) Input logic low</td>
<td>(4.5) V (\leq V_{CC} \leq 5.5) V, (−40^\circ)C (\leq T_A \leq 85^\circ)C</td>
<td>(V_{CC} = 4.5) V</td>
<td>2</td>
<td>5.5</td>
<td>V</td>
</tr>
<tr>
<td>(I_{H\rightarrow L}, I_{L\rightarrow H}) Input leakage current</td>
<td>(V_{I} = 5.5) V or 0, (V_{CC} = 5.5) V</td>
<td>(T_A = 25^\circ)C</td>
<td>−0.05</td>
<td>0.05</td>
<td>μA</td>
</tr>
<tr>
<td>(T_A = 85^\circ)C</td>
<td>−0.05</td>
<td>0.05</td>
<td>μA</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**DYNAMIC**

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>MIN</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>(t_{ON}) Turnon time</td>
<td>(V_{COM} = 3) V, (R_L = 300) Ω, (C_L = 35) pF, see Figure 9</td>
<td>(V_{CC} = 5) V, (T_A = 25^\circ)C</td>
<td>(4.5) V (\leq V_{CC} \leq 5.5) V, (−40^\circ)C (\leq T_A \leq 85^\circ)C</td>
<td>9</td>
</tr>
</tbody>
</table>

(1) All unused digital inputs of the device must be held at \(V_{CC}\) or GND to ensure proper device operation. See Implications of Slow or Floating CMOS Inputs (SCBA004).


6.6 Electrical Characteristics: 3-V Supply

\( V_{CC} = 3 \text{ V}, T_A = 25\degree C \) (unless otherwise noted)

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th></th>
<th>TEST CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>( I_{ON} )</td>
<td>ON-state resistance</td>
<td>( V_{NO} ) or ( V_{NC} = 1.5 \text{ V}, V_{CC} = 2.7 \text{ V}, )</td>
<td>( T_A = 25\degree C )</td>
<td>11.5</td>
<td>15</td>
<td>( \Omega )</td>
</tr>
<tr>
<td></td>
<td></td>
<td>( I_{COM} = –10 \text{ mA}, ) Switch ON, see Figure 5</td>
<td>( –40\degree C \leq T_A \leq 85\degree C )</td>
<td>20</td>
<td></td>
<td></td>
</tr>
<tr>
<td>( \Delta I_{ON} )</td>
<td>ON-state resistance match between channels</td>
<td>( V_{NO} ) or ( V_{NC} = 1.5 \text{ V}, V_{CC} = 2.7 \text{ V}, )</td>
<td>( T_A = 25\degree C )</td>
<td>0.05</td>
<td>0.3</td>
<td>( \Omega )</td>
</tr>
<tr>
<td></td>
<td></td>
<td>( I_{COM} = –10 \text{ mA}, ) Switch ON, see Figure 5</td>
<td>( –40\degree C \leq T_A \leq 85\degree C )</td>
<td>0.3</td>
<td></td>
<td></td>
</tr>
<tr>
<td>( I_{ON} ) (FLAT)</td>
<td>ON-state resistance flatness</td>
<td>( 0 \leq (V_{NO} ) or ( V_{NC} ) ( \leq V_{CC}, I_{COM} = –10 \text{ mA}, ) Switch ON, see Figure 5</td>
<td>( T_A = 25\degree C )</td>
<td>2</td>
<td></td>
<td>( \Omega )</td>
</tr>
<tr>
<td>( \Delta I_{NO(OFF)}, \Delta I_{NO(OFF)} )</td>
<td>NC, NO OFF leakage current</td>
<td>( V_{NC} ) or ( V_{NO} = 1 \text{ V} ) and ( V_{COM} = 1 \text{ V} ) to 3 \text{ V}, or ( V_{NC} ) or ( V_{NO} = 3 \text{ V} ) and ( V_{COM} = 1 \text{ V} ); ( V_{CC} = 3.3 \text{ V}, ) Switch OFF, see Figure 6</td>
<td>( T_A = 25\degree C )</td>
<td>–400</td>
<td>400</td>
<td>( \mu A )</td>
</tr>
<tr>
<td></td>
<td></td>
<td>( I_{COM} = –10 \text{ mA}, ) Switch OFF, see Figure 6</td>
<td>( –40\degree C \leq T_A \leq 85\degree C )</td>
<td>–2</td>
<td>2</td>
<td></td>
</tr>
<tr>
<td>( \Delta I_{NO(OFF)}, \Delta I_{NO(OFF)} )</td>
<td>NC, NO ON leakage current</td>
<td>( V_{NC} ) or ( V_{NO} = 1 \text{ V} ) and ( V_{COM} = 1 \text{ V} ) or ( V_{NC} ) or ( V_{NO} = 3 \text{ V} ) and ( V_{COM} = 3 \text{ V} ); ( V_{CC} = 3.3 \text{ V}, ) Switch OFF, see Figure 7</td>
<td>( T_A = 25\degree C )</td>
<td>–400</td>
<td>400</td>
<td>( \mu A )</td>
</tr>
<tr>
<td></td>
<td></td>
<td>( I_{COM} = –10 \text{ mA}, ) Switch OFF, see Figure 7</td>
<td>( –40\degree C \leq T_A \leq 85\degree C )</td>
<td>–2</td>
<td>2</td>
<td></td>
</tr>
<tr>
<td>( I_{COM} ) (ON)</td>
<td>COM ON leakage current</td>
<td>( V_{NC} ) or ( V_{NO} = ) Open, ( V_{COM} = 1 \text{ V} ) or 3 \text{ V}, ( V_{CC} = 3.3 \text{ V}, ) Switch ON, see Figure 7</td>
<td>( T_A = 25\degree C )</td>
<td>–400</td>
<td>400</td>
<td>( \mu A )</td>
</tr>
<tr>
<td></td>
<td></td>
<td>( I_{COM} = –10 \text{ mA}, ) Switch ON, see Figure 7</td>
<td>( –40\degree C \leq T_A \leq 85\degree C )</td>
<td>–2</td>
<td>2</td>
<td></td>
</tr>
</tbody>
</table>

(1) All unused digital inputs of the device must be held at \( V_{CC} \) or GND to ensure proper device operation. See Implications of Slow or Floating CMOS Inputs (SCBA004).
**Electrical Characteristics: 3-V Supply (continued)**

\( V_{CC} = 3 \text{ V, } T_A = 25^\circ \text{C (unless otherwise noted)} \)

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>( C_{NO} ) (ON) ( C_{NO}(OFF) )</td>
<td>( \text{NC, NO OFF capacitance} ) ( V_{NO} ) or ( V_{NO} = V_{CC} ) or GND, ( f = 1 \text{ MHz} ), Switch OFF, see Figure 8</td>
<td>3.5</td>
<td></td>
<td></td>
<td>pF</td>
</tr>
<tr>
<td>( C_{NO} ) (ON) ( C_{NO}(OFF) )</td>
<td>( \text{NC, NO ON capacitance} ) ( V_{NO} ) or ( V_{NO} = V_{CC} ) or GND, ( f = 1 \text{ MHz} ), Switch OFF, see Figure 8</td>
<td>8.5</td>
<td></td>
<td></td>
<td>pF</td>
</tr>
<tr>
<td>( C_{COM}(ON) ) ( C_{COM}(OFF) )</td>
<td>( \text{COM ON capacitance} ) ( V_{COM} = V_{CC} ) or GND, ( f = 1 \text{ MHz} ), Switch OFF, see Figure 8</td>
<td>8.5</td>
<td></td>
<td></td>
<td>pF</td>
</tr>
<tr>
<td>( C_t )</td>
<td>( \text{Digital input capacitance} ) ( V_t = V_{CC} ) or GND, ( f = 1 \text{ MHz} ), see Figure 8</td>
<td>2.5</td>
<td></td>
<td></td>
<td>pF</td>
</tr>
<tr>
<td>( BW )</td>
<td>( \text{Bandwidth} ) ( R_L = 50 ) ( \Omega ), Switch ON, see Figure 11</td>
<td>100</td>
<td></td>
<td></td>
<td>MHz</td>
</tr>
<tr>
<td>( Q_{NO} )</td>
<td>( \text{OFF isolation} ) ( R_L = 50 ) ( \Omega ), ( f = 1 \text{ MHz} ), Switch OFF, see Figure 12</td>
<td>–84</td>
<td></td>
<td></td>
<td>dB</td>
</tr>
<tr>
<td>( X_{TALK} )</td>
<td>( \text{Crosstalk} ) ( R_L = 50 ) ( \Omega ), ( f = 1 \text{ MHz} ), Switch ON, see Figure 13</td>
<td>–85</td>
<td></td>
<td></td>
<td>dB</td>
</tr>
<tr>
<td>( \text{THD} )</td>
<td>( \text{Total harmonic distortion} ) ( R_L = 600 ) ( \Omega ), ( C_L = 50 ) pF, ( f = 20 \text{ Hz to 20 khz} ), see Figure 15</td>
<td>0.09%</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**SUPPLY**

| \( I_{CC} \)                            | \( \text{Positive supply current} \) \( V_t = V_{CC} \) or GND, \( V_{CC} = 3.6 \) V, Switch ON or OFF |    |     |     |      |
|                                        | \( T_A = 25^\circ \text{C} \) \(-40^\circ \text{C} \leq T_A \leq 85^\circ \text{C} \) | 0.01 |     | 0.5 | \( \mu \text{A} \) |

**6.7 Electrical Characteristics: 2.5-V Supply**

\( V_{CC} = 2.5 \text{ V, } T_A = 25^\circ \text{C (unless otherwise noted)} \)

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>( f_{ON} )</td>
<td>( \text{ON-state resistance} ) ( V_{NO} ) or ( V_{NO} = 1 \text{ V} ), ( V_{CC} = 2.25 \text{ V} ), ( I_{COM} = 10 ) mA, Switch ON, see Figure 5</td>
<td>15</td>
<td>25</td>
<td></td>
<td>( \Omega )</td>
</tr>
<tr>
<td>( \Delta f_{ON} )</td>
<td>( \text{ON-state resistance match between channels} ) ( V_{NO} ) or ( V_{NO} = 1 \text{ V} ), ( V_{CC} = 2.25 \text{ V} ), ( I_{COM} = 10 ) mA, Switch ON, see Figure 5</td>
<td>0.06</td>
<td>0.3</td>
<td></td>
<td>( \Omega )</td>
</tr>
<tr>
<td>( f_{ON}(FLAT) )</td>
<td>( \text{ON-state resistance flatness} ) ( V_{NO} ) or ( V_{NO} = 1 \text{ V} ), ( V_{CC} = 2.25 \text{ V} ), ( I_{COM} = 10 ) mA, Switch ON, see Figure 5</td>
<td>4</td>
<td></td>
<td></td>
<td>( \Omega )</td>
</tr>
<tr>
<td>( I_{NO}(OFF) ) ( I_{NO}(OFF) )</td>
<td>( \text{NC, NO OFF leakage current} ) ( V_{NO} ) or ( V_{NO} = 1.5 \text{ V} ) and ( V_{COM} = 0.5 \text{ V} ) to 1.5 ( V ), or ( V_{CC} = 2.75 \text{ V} ), Switch OFF, see Figure 6</td>
<td>–300</td>
<td>300</td>
<td></td>
<td>pA</td>
</tr>
<tr>
<td>( I_{NO}(ON) ) ( I_{NO}(ON) )</td>
<td>( \text{NC, NO ON leakage current} ) ( V_{NO} ) or ( V_{NO} = 1.5 \text{ V} ) and ( V_{COM} = 0.5 \text{ V} ) to 1.5 ( V ), or ( V_{CC} = 2.75 \text{ V} ), Switch ON, see Figure 7</td>
<td>–300</td>
<td>300</td>
<td></td>
<td>nA</td>
</tr>
<tr>
<td>( I_{COM}(ON) )</td>
<td>( \text{COM ON leakage current} ) ( V_{NO} ) or ( V_{NO} = 1 \text{ V} ), ( V_{COM} = 0.5 \text{ V} ) or 1.5 ( V ), ( V_{CC} = 2.75 \text{ V} ), Switch ON, see Figure 7</td>
<td>–300</td>
<td>300</td>
<td></td>
<td>nA</td>
</tr>
</tbody>
</table>

**DIGITAL INPUT (IN)\(^{(1)}\)**

| \( V_{HI} \)                              | \( \text{Input logic high} \) \(-40^\circ \text{C} \leq T_A \leq 85^\circ \text{C} \) | 2   |     | 5.5 | V    |
| \( V_{IL} \)                              | \( \text{Input logic low} \) \(-40^\circ \text{C} \leq T_A \leq 85^\circ \text{C} \) | 0   |     | 0.4 | V    |
| \( I_{HI}, I_{IL} \)                      | \( \text{Input leakage current} \) \( V_t = 5.5 \text{ V} \) or 0 \( \text{ V} \), \( V_{CC} = 2.75 \text{ V} \) \(-40^\circ \text{C} \leq T_A \leq 85^\circ \text{C} \) | –0.05 | 0.05 |     | \( \mu \text{A} \) |

**DYNAMIC**

| \( t_{ON} \)                              | \( \text{Tumten time} \) \( V_{COM} = 2 \text{ V} \), \( R_L = 30 \) \( \Omega \), \( C_L = 35 \) pF, see Figure 9 | 18  |     | 20  | ns   |
| \( t_{OFF} \)                             | \( \text{Turnoff time} \) \( V_{COM} = 2 \text{ V} \), \( R_L = 30 \) \( \Omega \), \( C_L = 35 \) pF, see Figure 9 | 8   |     | 9.5 | ns   |
| \( t_{BBM} \)                             | \( \text{Break-before-make time} \) \( V_{NO} = 2 \text{ V} \), \( R_L = 30 \) \( \Omega \), \( C_L = 35 \) pF, see Figure 10 | 1   |     |     | ns   |
| \( Q_c \)                                 | \( \text{Charge injection} \) \( V_{GEN} = 0 \), \( R_{GEN} = 0 \), \( C_L = 1 \) nF, see Figure 14 | 4.5 |     |     | pC   |
| \( C_{NO} \) \( C_{NO}(OFF) \)           | \( \text{NC, NO OFF capacitance} \) \( V_{NO} \) or \( V_{NO} = V_{CC} \) or GND, \( f = 1 \text{ MHz} \), Switch OFF, see Figure 8 | 3.5 |     |     | pF   |
| \( C_{NO} \) \( C_{NO}(OFF) \)           | \( \text{NC, NO ON capacitance} \) \( V_{NO} \) or \( V_{NO} = V_{CC} \) or GND, \( f = 1 \text{ MHz} \), Switch OFF, see Figure 8 | 8.5 |     |     | pF   |

\( ^{(1)} \) All unused digital inputs of the device must be held at \( V_{CC} \) or GND to ensure proper device operation. See Implications of Slow or Floating CMOS Inputs (SCBA004).
Electrical Characteristics: 2.5-V Supply (continued)

\( V_{CC} = 2.5 \, \text{V}, \; T_A = 25^\circ\text{C} \) (unless otherwise noted)

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>( C_{\text{COM(ON)}} )</td>
<td>( V_{\text{COM}} = V_{\text{CC}} ) or GND, ( f = 1 , \text{MHz} ), Switch OFF, see Figure 8</td>
<td>8.5</td>
<td>pF</td>
<td></td>
<td></td>
</tr>
<tr>
<td>( C_i )</td>
<td>Digital input capacitance ( V_i = V_{\text{CC}} ) or GND, ( f = 1 , \text{MHz} ), see Figure 8</td>
<td>2.5</td>
<td>pF</td>
<td></td>
<td></td>
</tr>
<tr>
<td>BW</td>
<td>Bandwidth ( R_L = 50 , \Omega ), Switch ON, see Figure 11</td>
<td>100</td>
<td>MHz</td>
<td></td>
<td></td>
</tr>
<tr>
<td>( O_{\text{ISO}} )</td>
<td>OFF isolation ( R_L = 50 , \Omega ), ( f = 1 , \text{MHz} ), Switch OFF, see Figure 12</td>
<td>–84</td>
<td>dB</td>
<td></td>
<td></td>
</tr>
<tr>
<td>( X_{\text{TALK}} )</td>
<td>Crosstalk ( R_L = 50 , \Omega ), ( f = 1 , \text{MHz} ), Switch ON, see Figure 13</td>
<td>–84</td>
<td>dB</td>
<td></td>
<td></td>
</tr>
<tr>
<td>THD</td>
<td>Total harmonic distortion ( R_L = 600 , \Omega ), ( C_L = 50 , \text{pF} ), ( f = 20 , \text{Hz} ) to ( 20 , \text{kHz} ), see Figure 15</td>
<td>0.15%</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**SUPPLY**

<table>
<thead>
<tr>
<th>( I_{\text{CC}} )</th>
<th>Positive supply current ( V_i = V_{\text{CC}} ) or GND, ( V_{\text{CC}} = 2.75 , \text{V} ), Switch ON or OFF ( T_A = 25^\circ\text{C} )</th>
<th>( –40^\circ\text{C} \leq T_A \leq 85^\circ\text{C} )</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>( 0.01 , \mu\text{A} )</td>
<td>( 0.5 , \mu\text{A} )</td>
</tr>
</tbody>
</table>

### 6.8 Typical Characteristics

#### Figure 1. \( r_{\text{ON}} \) vs \( V_{\text{COM}} \)

#### Figure 2. Bandwidth (\( V_{\text{CC}} = 3 \, \text{V} \))

#### Figure 3. Crosstalk and Insertion Loss vs Frequency (\( V_{\text{CC}} = 3 \, \text{V} \))

#### Figure 4. Total Harmonic Distortion vs Frequency
7 Parameter Measurement Information

Channel ON

ON-State Leakage Current

\[ V_{IN} = V_{IH} \text{ or } V_{IL} \]

\[ r_{ON} = \frac{V_{COM} - V_{NO} \text{ or } V_{NC}}{I_{COM}} \]

\[ V_{IN} = V_{IH} \text{ or } V_{IL} \]

Figure 5. ON-State Resistance

OFF-State Leakage Current

\[ I_{NC(OFF)}, I_{NC(PWROFF)}, I_{NO(OFF)}, I_{NO(PWROFF)}, I_{COM(OFF)}, I_{COM(PWROFF)} \]

Figure 6. OFF-State Leakage Current

ON-State Leakage Current

\[ I_{COM(ON)}, I_{NC(ON)}, I_{NO(ON)} \]

Figure 7. ON-State Leakage Current
Parameter Measurement Information (continued)

Figure 8. Capacitance

Figure 9. Turnon and Turnoff Time

(1) All input pulses are supplied by generators having the following characteristics:
   • PRR ≤ 10 MHz
   • $Z_O = 50 \, \Omega$
   • $t_r < 5 \, \text{ns}$
   • $t_f < 5 \, \text{ns}$

(2) $C_L$ includes probe and jig capacitance.
Parameter Measurement Information (continued)

(1) All input pulses are supplied by generators having the following characteristics:
- PRR ≤ 10 MHz
- Z₀ = 50 Ω
- tᵣ < 5 ns
- tᵣ < 5 ns

(2) Cᴸ includes probe and jig capacitance.

**Figure 10. Break-Before-Make Time**

**Figure 11. Bandwidth**

**Figure 12. OFF Isolation**
Network Analyzer

Channel ON: NC to COM
Channel OFF: NO to COM
VIN = VCC or GND

Network Analyzer Setup
Source Power = 0 dBm
(632-mV P-P at 50-Ω load)
DC Bias = 350 mV

Source
Signal
RL = 600 Ω
CL = 50 pF

Source Power = VCC P-P
f SOURCE = 20 Hz to 20 kHz

Audio Analyzer

VIN = VIH or VIL

Logic Input

Logic Input (VIN)

Logic Input (VIN)

VCOM

VIN

VCC

VCOM

ON

OFF

VIL

VIH

VCC

VCOM

VGEN

NC or NO

NC or NO

NC or NO

NC or NO

Logic
Input

(1) All input pulses are supplied by generators having the following characteristics:
• PRR ≤ 10 MHz
• ZO = 50 Ω
• tr < 5 ns
• tf < 5 ns

(2) CL includes probe and jig capacitance.

VGEN = 0 to VCC
RGEN = 0
CL = 1 nF
QC = CL × ΔVCOM
VIN = VIH or VIL

Figure 13. Crosstalk

Figure 14. Charge Injection

Figure 15. Total Harmonic Distortion

Product Folder Links: TSSA9411
8 Detailed Description

8.1 Overview
The TS5A9411 device is a 1:2 or single-pole-double-throw (SPDT) solid-state analog switch. The TS5A9411, like all analog switches, is bidirectional. When powered on, each COM pin is connected to the NC pin or NO pin depending on the status of the IN pin. If IN is low, COM is connected to NC. If IN is high, COM is connected to NO. The TS5A9411 is a break-before-make switch. This means that during switching, a connection is broken before a new connection is established. The NC and NO pins are never connected to each other.

8.2 Functional Block Diagram

![Functional Block Diagram](image)

8.3 Feature Description
The low ON-state resistance, ON-state resistance matching, and charge injection in the TS5A9411 make this switch an excellent choice for analog signals that require minimal distortion. The 2.25-V to 5.5-V operation allows compatibility with more voltage nodes, and the bidirectional I/Os can pass analog signals from 0 V to $V_{CC}$ with low distortion.

8.4 Device Functional Modes
Table 1 lists the functional modes of the TS5A9411. If IN pin is low, COM is connected to NC. If IN is high, COM is connected to NO.

<table>
<thead>
<tr>
<th>IN</th>
<th>NC TO COM, COM TO NC</th>
<th>NO TO COM, COM TO NO</th>
</tr>
</thead>
<tbody>
<tr>
<td>L</td>
<td>ON</td>
<td>OFF</td>
</tr>
<tr>
<td>H</td>
<td>OFF</td>
<td>ON</td>
</tr>
</tbody>
</table>
9 Application and Implementation

NOTE
Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information
The switches are bidirectional, so the NO, NC, and COM pins can be used as either inputs or outputs. The device is used in systems where multiple analog or digital signals must be selected to pass across a single line.

9.2 Typical Application

![Typical Application Diagram](image)

**Figure 16. Typical Application Diagram**

9.2.1 Design Requirements
Pull the digitally controlled input select pin (IN) to VCC or GND to avoid unwanted switch states that could result if the logic control pin is left floating.

9.2.2 Detailed Design Procedure
Select the appropriate supply voltage to cover the entire voltage swing of the signal passing through the switch because the input or output signal swing of the device is dependant of the supply voltage (VCC).
Typical Application (continued)

9.2.3 Application Curve

![Graph showing $r_{ON} vs V_{COM}$](image)

$V_{+} = 5 \text{V}$

$V_{+} = 2.5 \text{V}$

$V = 3.3 \text{V}$

10 Power Supply Recommendations

Proper power-supply sequencing is recommended for all CMOS devices. Do not exceed the absolute maximum ratings, because stresses beyond the listed ratings can cause permanent damage to the device. Always sequence $VCC$ on first, followed by NO, NC, or COM pins.

Although it is not required, power-supply bypassing improves noise margin and prevents switching noise propagation from the $VCC$ supply to other components. A 0.1-μF capacitor, connected from $VCC$ to $GND$, is adequate for most applications.

11 Layout

11.1 Layout Guidelines

TI recommends placing a bypass capacitor as close to the supply pins ($VCC$ and $–VCC$) as possible to help smooth out lower frequency noise to provide better load regulation across the frequency spectrum. Minimize trace lengths and vias on the signal paths to preserve signal integrity.

11.2 Layout Example

![Layout recommendation diagram](image)
12 Device and Documentation Support

12.1 Device Support

12.1.1 Device Nomenclature

**BW** Bandwidth of the switch. This is the frequency in which the gain of an ON channel is –3 dB below the DC gain.

**C<sub>COM(ON)</sub>** Capacitance at the COM port when the corresponding channel (COM to NC or COM to NO) is ON.

**C<sub>NC(OFF)</sub>** Capacitance at the NC port when the corresponding channel (NC to COM) is OFF.

**C<sub>NC(ON)</sub>** Capacitance at the NC port when the corresponding channel (NC to COM) is ON.

**C<sub>NO(OFF)</sub>** Capacitance at the NO port when the corresponding channel (NO to COM) is OFF.

**C<sub>NO(ON)</sub>** Capacitance at the NO port when the corresponding channel (NO to COM) is ON.

**C<sub>I</sub>** Capacitance of control input (IN).

**I<sub>CC</sub>** Static power-supply current with the control (IN) pin at V<sub>CC</sub> or GND.

**I<sub>COM(ON)</sub>** Leakage current measured at the COM port, with the corresponding channel (COM to NO or COM to NC) in the ON state and the output (NC or NO) open.

**I<sub>COM(PWROFF)</sub>** Leakage current measured at the COM port during the power-down condition (V<sub>CC</sub> = 0).

**I<sub>HI</sub>, I<sub>IL</sub>** Leakage current measured at the control input (IN).

**I<sub>NC(OFF)</sub>** Leakage current measured at the NC port, with the corresponding channel (NC to COM) in the OFF state under worst-case input and output conditions.

**I<sub>NC(ON)</sub>** Leakage current measured at the NC port, with the corresponding channel (NC to COM) in the ON state and the output (COM) open.

**I<sub>NO(OFF)</sub>** Leakage current measured at the NO port, with the corresponding channel (NO to COM) in the OFF state under worst-case input and output conditions.

**I<sub>NO(ON)</sub>** Leakage current measured at the NO port, with the corresponding channel (NO to COM) in the ON state and the output (COM) open.

**O<sub>ISO</sub>** OFF isolation of the switch is a measurement of OFF-state switch impedance. This is measured in dB in a specific frequency, with the corresponding channel (NC to COM or NO to COM) in the OFF state.

**Q<sub>C</sub>** Charge injection is a measurement of unwanted signal coupling from the control (IN) input to the analog (NC, NO, or COM) output. This is measured in coulomb (C) and measured by the total charge induced due to switching of the control input. Charge injection, \( Q_C = C_L \times \Delta V_{COM} \), \( C_L \) is the load capacitance and \( \Delta V_{COM} \) is the change in analog output voltage.

**Δr<sub>ON</sub>** Difference of \( r_{ON} \) between channels in a specific device.

**r<sub>ON</sub>** Resistance between COM and NC or COM and NO ports when the channel is ON.

**r<sub>ON(FLAT)</sub>** Difference of \( r_{ON} \) in a channel over the specified range of conditions.

**t<sub>BBM</sub>** Break-before-make time. This parameter is measured under the specified range of conditions and by the propagation delay between the output of two adjacent analog channels (NC and NO) when the control signal changes state.

**t<sub>OFF</sub>** Turnoff time for the switch. This parameter is measured under the specified range of conditions and by the propagation delay between the digital control (IN) signal and analog output (COM, NC, or NO) signal when the switch is turning OFF.

**t<sub>ON</sub>** Turnon time for the switch. This parameter is measured under the specified range of conditions and by the propagation delay between the digital control (IN) signal and analog output (COM, NC, or NO) signal when the switch is turning ON.

**THD** Total harmonic distortion describes the signal distortion caused by the analog switch. This is
Device Support (continued)

defined as the ratio of root mean square (RMS) value of the second, third, and higher harmonic to the absolute magnitude of the fundamental harmonic.

\[ V_{\text{COM}} \] Voltage at COM.
\[ V_I \] Voltage at the control input (IN).
\[ V_{\text{IH}} \] Minimum input voltage for logic high for the control input (IN).
\[ V_{\text{IL}} \] Maximum input voltage for logic low for the control input (IN).
\[ V_{\text{NC}} \] Voltage at NC.
\[ V_{\text{NO}} \] Voltage at NO.
\[ X_{\text{TALK}} \] Crosstalk is a measurement of unwanted signal coupling from an ON channel to an OFF channel (NC to NO or NO to NC). This is measured in a specific frequency and in dB.

12.2 Documentation Support

12.2.1 Related Documentation

For related documentation see the following:

*Implications of Slow or Floating CMOS Inputs* (SCBA004)

12.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.4 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

**TI E2E™ Online Community**  *TI's Engineer-to-Engineer (E2E) Community.* Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

**Design Support**  *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.5 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

12.6 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.7 Glossary

**SLYZ022 — TI Glossary.**

This glossary lists and explains terms, acronyms, and definitions.
13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.
## PACKAGING INFORMATION

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<tr>
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<th>Status (1)</th>
<th>Package Type</th>
<th>Package Drawing</th>
<th>Pins</th>
<th>Package Qty</th>
<th>Eco Plan (2)</th>
<th>Lead/Ball Finish</th>
<th>MSL Peak Temp (3)</th>
<th>Op Temp (°C)</th>
<th>Device Marking (4/5)</th>
<th>Samples</th>
</tr>
</thead>
<tbody>
<tr>
<td>TSSA9411DCKR</td>
<td>ACTIVE</td>
<td>SC70</td>
<td>DCK</td>
<td>6</td>
<td>3000</td>
<td>Green (RoHS &amp; no Sb/Br)</td>
<td>CU NIPDAU</td>
<td>Level-1-260C-UNLIM</td>
<td>-40 to 85</td>
<td>(32F, 32R) (32H, 32P)</td>
<td>Samples</td>
</tr>
<tr>
<td>TSSA9411DCKT</td>
<td>ACTIVE</td>
<td>SC70</td>
<td>DCK</td>
<td>6</td>
<td>250</td>
<td>Green (RoHS &amp; no Sb/Br)</td>
<td>CU NIPDAU</td>
<td>Level-1-260C-UNLIM</td>
<td>-40 to 85</td>
<td>(32F, 32R) 32H</td>
<td>Samples</td>
</tr>
<tr>
<td>TSSA9411DCKTG4</td>
<td>ACTIVE</td>
<td>SC70</td>
<td>DCK</td>
<td>6</td>
<td>250</td>
<td>Green (RoHS &amp; no Sb/Br)</td>
<td>CU NIPDAU</td>
<td>Level-1-260C-UNLIM</td>
<td>-40 to 85</td>
<td>(32F, 32R) 32H</td>
<td>Samples</td>
</tr>
</tbody>
</table>

(1) The marketing status values are defined as follows:
- **ACTIVE:** Product device recommended for new designs.
- **LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
- **NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
- **PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
- **OBsolete:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
- **RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
- **Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.
## TAPE AND REEL INFORMATION

### REEL DIMENSIONS

- **Diameter (mm)**: 180.0
- **Width (mm)**: 8.4
- **Pocket Quadrants**: Q1, Q2, Q3, Q4
- **User Direction of Feed**: Right

### TAPE DIMENSIONS

- **A0**: Dimension designed to accommodate the component width
- **B0**: Dimension designed to accommodate the component length
- **K0**: Dimension designed to accommodate the component thickness
- **W**: Overall width of the carrier tape
- **P1**: Pitch between successive cavity centers

### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

- **Sprocket Holes**: Located at each quadrant

### Package Materials - Page 1

<table>
<thead>
<tr>
<th>Device</th>
<th>Package Type</th>
<th>Package Drawing</th>
<th>Pins</th>
<th>SPQ</th>
<th>Reel Diameter (mm)</th>
<th>Reel Width W1 (mm)</th>
<th>A0 (mm)</th>
<th>B0 (mm)</th>
<th>K0 (mm)</th>
<th>P1 (mm)</th>
<th>W (mm)</th>
<th>Pin1 Quadrant</th>
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<tr>
<td>TS5A9411DCKR</td>
<td>SC70</td>
<td>DCK</td>
<td>6</td>
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<td>1.2</td>
<td>4.0</td>
<td>8.0</td>
<td>Q3</td>
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<tr>
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<td>DCK</td>
<td>6</td>
<td>250</td>
<td>180.0</td>
<td>8.4</td>
<td>2.41</td>
<td>2.41</td>
<td>1.2</td>
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<td>Q3</td>
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</table>

*All dimensions are nominal.*
### TAPE AND REEL BOX DIMENSIONS

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<th>Device</th>
<th>Package Type</th>
<th>Package Drawing</th>
<th>Pins</th>
<th>SPQ</th>
<th>Length (mm)</th>
<th>Width (mm)</th>
<th>Height (mm)</th>
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<td>202.0</td>
<td>201.0</td>
<td>28.0</td>
</tr>
</tbody>
</table>

*All dimensions are nominal*
DCK (R-PDSO-G6)  PLASTIC SMALL-OUTLINE PACKAGE

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
D. Falls within JEDEC MO-203 variation AB.

4093553-4/G  01/2007
**LAND PATTERN DATA**

**DCK (R-PDSO-G6) PLASTIC SMALL OUTLINE**

**Example Board Layout**

**Stencil Openings**
Based on a stencil thickness of 0.127mm (0.005 inch).

**Notes:**
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. Publication IPC-7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.
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