12-Bit, Nanopower, 4-Wire Micro TOUCH SCREEN CONTROLLER with I²C™ Interface

Check for Samples: TSC2017

FEATURES

- **4-Wire Touch Screen Interface**
- **Single 1.6V to 3.6V Supply/Reference**
- **Ratiometric Conversion**
- **Effective Throughput Rate:**
  - **Up to 20kHz (8-Bit) or 10kHz (12-Bit)**
- **Preprocessing to Reduce Bus Activity**
- **I²C Interface Supports:**
  - **Standard, Fast, and High-Speed Modes**
- **Simple, Command-Based User Interface:**
  - **TSC2003/TSC2007 Compatible**
  - **8- or 12-Bit Resolution**
- **On-Chip Temperature Measurement**
- **Touch Pressure Measurement**
- **Digital Buffered $\overline{\text{PENIRQ}}$**
- **On-Chip, Programmable $\overline{\text{PENIRQ}}$ Pull-Up**
- **Comprehensive Reset Schemes:**
  - **Power-On, Software, and Hardware Resets**
- **Auto Power-Down Control**
- **Low Power (12-Bit):**
  - **39.31µA at 1.8V, Fast Mode, 8.2kHz Eq Rate**
  - **53.32µA at 2.7V, Fast Mode, 8.2kHz Eq Rate**
- **Enhanced ESD Protection for IEC Testing:**
  - **±8kV HBM**
  - **±1kV CDM**
  - **±25kV Air Gap Discharge**
  - **±15kV Contact Discharge**
- **2.1 x 1.6 WCSP-12 Package**

U.S. Patent NO. 6246394; other patents pending.

APPLICATIONS

- **Cellular Phones**
- **PDA, GPS, and Media Players**
- **Portable Instruments**
- **Point-of-Sale Terminals**
- **Multiscreen Touch Control Systems**

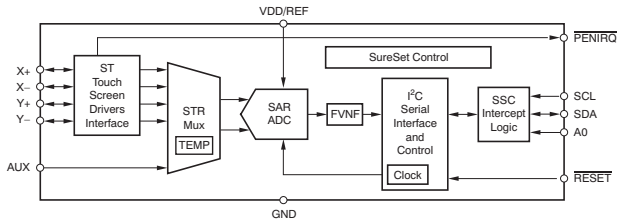
DESCRIPTION

The TSC2017 is a very low-power touch screen controller designed to work with power-sensitive, handheld applications that are based on an advanced low-voltage processor. It works with a supply voltage as low as 1.6V, which can be supplied by a single-cell battery. It contains a complete, ultra-low power, 12-bit, analog-to-digital (A/D) resistive touch screen converter, including drivers and the control logic to measure touch pressure.

In addition to these standard features, the TSC2017 offers preprocessing of the touch screen measurements to reduce bus loading, thus reducing the consumption of host processor resources that can then be redirected to more critical functions.

The TSC2017 supports I²C serial bus and data transmission protocol in all three defined modes: standard, fast, and high-speed. It offers programmable resolution of 8 or 12 bits to accommodate different screen sizes and performance needs.

The TSC2017 is available in a 12-lead, (1.555 ±0,055mm) x (2.055 ±0,055mm), 3 x 4 array, wafer chip-scale package (WCSP). The TSC2017 is characterized for the –40°C to +85°C industrial temperature range.



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This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ORDERING INFORMATION(1)

PRODUCT	TYPICAL INTEGRAL LINEARITY (LSB)	TYPICAL GAIN ERROR (LSB)	NO MISSING CODES RESOLUTION (BITS)	PACKAGE TYPE	PACKAGE DESIGNATOR	SPECIFIED TEMPERATURE RANGE	PACKAGE MARKING	ORDERING NUMBER	TRANSPORT MEDIA, QUANTITY
TSC2017I	±1.5	0.1	11	12-Pin, 3 x 4 Array, WCSP	YZG	–40°C to +85°C	TSC2017I	TSC2017IYZGT	Small Tape and Reel, 250
								TSC2017IYZGR	Tape and Reel, 3000

(1) For the most current package and ordering information, see the Package Option Addendum located at the end of this data sheet, or see the TI website at www.ti.com.

ABSOLUTE MAXIMUM RATINGS(1)

Over operating free-air temperature range, unless otherwise noted.

			TSC2017	UNIT
Voltage range	Analog input X+, Y+, AUX to GND		–0.4 to V_{DD} + 0.1	V
	Analog input X–, Y– to GND		–0.4 to V_{DD} + 0.1	V
	VDD/REF pin to GND		–0.3 to +5	V
Digital input voltage to GND			–0.3 to V_{DD} + 0.3	V
Digital output voltage to GND			–0.3 to V_{DD} + 0.3	V
Power dissipation			(T_J Max - T_A)/θ_{JA}	
Thermal impedance, θ_{JA}	WCSP package	Low-K	113	°C/W
		High-K	62	
Operating free-air temperature range, T_A			–40 to +85	°C
Storage temperature range, T_{STG}			–65 to +150	°C
Junction temperature, T_J Max			+150	°C
IEC contact discharge(2)	X+, X–, Y+, Y–		±15	kV
IEC air discharge(2)	X+, X–, Y+, Y–		±25	kV

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated is not implied. Exposure to absolute-maximum rated conditions for extended periods may affect device reliability.
(2) Test method based on IEC standard 61000-4-2. Contact Texas Instruments for test details.

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ELECTRICAL CHARACTERISTICS

At T_A = –40°C to +85°C, V_{DD} = +1.6V to +3.6V, unless otherwise noted.

PARAMETER		TEST CONDITIONS		TSC2017 MIN	TSC2017 TYP	TSC2017 MAX	UNIT
AUXILIARY ANALOG INPUT							
Input voltage range				0		V_{DD}	V
Input capacitance					12		pF
Input leakage current				–1		+1	µA
A/D CONVERTER							
Resolution		Programmable: 8 or 12 bits				12	Bits
No missing codes		12-bit resolution		11			Bits
Integral linearity					±1.5		LSB (1)
Offset error		V_{DD} = 1.8V			–1.2		LSB
		V_{DD} = 3.0V			–3.1		LSB
Gain error		V_{DD} = 1.8V			0.7		LSB
		V_{DD} = 3.0V			0.1		LSB
TOUCH SENSORS							
$\overline{\text{PENIRQ}}$ pull-up resistor, R_{IRQ}		T_A = +25°C, V_{DD} = 1.8V, command '1011' set '0000'			51		kΩ
		T_A = +25°C, V_{DD} = 1.8V, command '1011' set '0001'			90		kΩ
Switch on-resistance	Y+, X+				6		Ω
	Y–, X–				5		Ω
Switch drivers drive current (2)		100ms duration				50	mA
INTERNAL TEMPERATURE SENSOR							
Temperature range				–40		+85	°C
Resolution		Differential method (3)	V_{DD} = 3V		1.94		°C/LSB
			V_{DD} = 1.6V		1.04		°C/LSB
		TEMP1 (4)	V_{DD} = 3V		0.35		°C/LSB
			V_{DD} = 1.6V		0.19		°C/LSB
Accuracy		Differential method (3)	V_{DD} = 3V		±2		°C/LSB
			V_{DD} = 1.6V		±2		°C/LSB
		TEMP1 (4)	V_{DD} = 3V		±3		°C/LSB
			V_{DD} = 1.6V		±3		°C/LSB
INTERNAL OSCILLATOR							
Internal clock frequency, f_{CCLK}		8-Bit	V_{DD} = 1.6V		3.61		MHz
			V_{DD} = 1.8V		3.66		MHz
			V_{DD} = 2.7V		3.78		MHz
			V_{DD} = 3.6V		3.82		MHz
		12-Bit	V_{DD} = 1.6V		1.8		MHz
			V_{DD} = 1.8V		1.83		MHz
			V_{DD} = 2.7V		1.88		MHz
			V_{DD} = 3.6V		1.91		MHz
Frequency drift		V_{DD} = 1.6V			0.0056		%/°C
		V_{DD} = 3.0V			0.012		%/°C

(1) LSB means Least Significant Bit. With VDD/REF pin = +1.6V, one LSB is 391µV.
(2) Specified by design, but not tested. Exceeding 50mA source current may result in device degradation.
(3) Difference between TEMP1 and TEMP2 measurement; no calibration necessary.
(4) Temperature drift is –2.1mV/°C.

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ELECTRICAL CHARACTERISTICS (continued)

At T_A = –40°C to +85°C, V_{DD} = +1.6V to +3.6V, unless otherwise noted.

PARAMETER		TEST CONDITIONS			TSC2017 MIN	TSC2017 TYP	TSC2017 MAX	UNIT
DIGITAL INPUT/OUTPUT								
Logic family						CMOS		
Logic level	V_{IH}	1.6V ≤ V_{DD} ≤ 3.6V			0.7 × V_{DD}		V_{DD} + 0.3	V
	V_{IL}	1.6V ≤ V_{DD} ≤ 3.6V			–0.3		0.3 × V_{DD}	V
	I_{IL}	SCL and SDA pins			–1		1	µA
	C_{IN}	SCL and SDA pins					10	pF
	V_{OH}	I_{OH} = 2 TTL loads			V_{DD} – 0.2		V_{DD}	V
	V_{OL}	I_{OL} = 2 TTL loads			0		0.2	V
	I_{LEAK}	Floating output			–1		1	µA
	C_{OUT}	Floating output					10	pF
Data format						Straight binary		
POWER-SUPPLY REQUIREMENTS								
Power-supply voltage, V_{DD}		Specified performance			1.6		3.6	V
Quiescent supply current (V_{DD} with sensor off)		12-bit Fast mode (clock = 400kHz) PD[1:0] = 0,0	V_{DD} = 1.6V	32.56k eq rate		145	206	µA
				8.2k eq rate		34.77		µA
			V_{DD} = 1.8V	34.42k eq rate		165	240	µA
				8.2k eq rate		39.31		µA
			V_{DD} = 2.7V	34.79k eq rate		226.2	335	µA
				8.2k eq rate		53.32		µA
Power down supply current		Not addressed, SCL = SDA = 1				0	0.8	µA
POWER ON/OFF SLOPE REQUIREMENTS								
V_{DD} off ramp		T_A = –40°C to +85°C			50		1,000,000	V/s
V_{DD} off time		T_A = –40°C to +85°C, V_{DD} ≤ 0.4V			20			µs
V_{DD} on ramp		T_A = –40°C to +85°C			90		1,000,000	V/s

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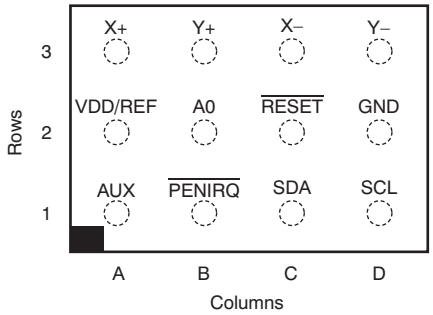
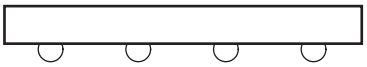
PIN CONFIGURATIONS

YZG PACKAGE
WCSP-12
(TOP VIEW, SOLDER BUMPS ON BOTTOM SIDE)



(FRONT VIEW)



PIN ASSIGNMENTS

NO.	NAME	I/O	A/D	DESCRIPTION
A1	AUX	I	A	Auxiliary channel input
A2	VDD/REF			Supply voltage and external reference input
A3	X+	I	A	X+ channel input
B1	$\overline{\text{PENIRQ}}$	O	D	Data available interrupt output. A delayed (process delay) pen touch detect. Pin polarity with active low.
B2	A0	I	D	Address input bit 0
B3	Y+	I	A	Y+ channel input
C1	SDA	I/O	D	Serial data I/O
C2	$\overline{\text{RESET}}$	I	D	External hardware-reset input
C3	X–	I	A	X– channel input
D1	SCL	I/O	D	Serial clock. This pin is normally an input, but acts as an output when the device stretches the clock to delay a bus transfer.
D2	GND			Ground
D3	Y–	I	A	Y– channel input

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TIMING INFORMATION

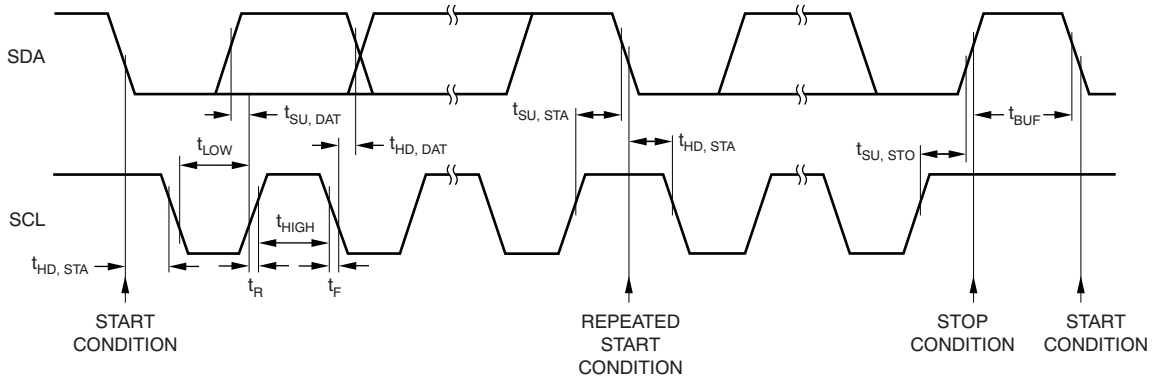

Figure 1. Detailed I/O Timing

TIMING REQUIREMENTS

All specifications typical at –40°C to +85°C, V_{DD} = 1.6V, unless otherwise noted.

2-WIRE STANDARD MODE PARAMETERS		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Reset low time	$t_{WL(RESET)}$	3.6V ≥ VDD ≥ 1.6V	200			ns

TIMING REQUIREMENTS: I²C Standard Mode (SCL = 100kHz)

All specifications typical at –40°C to +85°C, V_{DD} = 1.6V, unless otherwise noted.

TWO-WIRE STANDARD MODE PARAMETERS			TEST CONDITIONS	MIN	TYP	MAX	UNIT
SCL clock frequency		f_{SCL}		0		100	kHz
Bus free time between a STOP and START condition		t_{BUF}		4.7			µs
Hold time (repeated) START condition		$t_{HD, STA}$		4.0			µs
Low period of SCL clock		t_{LOW}		4.7			µs
High period of the SCL clock		t_{HIGH}		4.0			µs
Setup time for a repeated START condition		$t_{SU, STA}$		4.7			µs
Data hold time		$t_{HD, DAT}$		0		3.45	µs
Data setup time		$t_{SU, DAT}$		250			ns
Rise time for both SDA and SCL signals (receiving)		t_R	C_b = total bus capacitance			1000	ns
Fall time for both SDA and SCL signals (receiving)		t_F	C_b = total bus capacitance			300	ns
Fall time for both SDA and SCL signals (transmitting)		t_F	C_b = total bus capacitance			250	ns
Setup time for STOP condition		$t_{SU, STO}$		4.0			µs
Capacitive load for each bus line		C_b	C_b = total capacitance of one bus line in pF			400	pF
Cycle time	8 bits		40 SCL + 127 CCLK, V_{DD} = 1.8V		434.7		µs
	12 bits		49 SCL + 148 CCLK, V_{DD} = 1.8V		570.9		µs
Effective throughput	8 bits		V_{DD} = 1.8V		2.3		kSPS
	12 bits		V_{DD} = 1.8V		1.75		kSPS
Equivalent rate = effective throughput × 7	8 bits		V_{DD} = 1.8V		16.1		kHz
	12 bits		V_{DD} = 1.8V		12.26		kHz

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TIMING REQUIREMENTS: I²C Fast Mode (SCL = 400kHz)

All specifications typical at –40°C to +85°C, V_{DD} = 1.6V, unless otherwise noted.

TWO-WIRE FAST MODE PARAMETERS			TEST CONDITIONS	MIN	TYP	MAX	UNIT
SCL clock frequency		f_{SCL}		0		400	kHz
Bus free time between a STOP and START condition		t_{BUF}		1.3			µs
Hold time (repeated) START condition		$t_{HD, STA}$		0.6			µs
Low period of SCL clock		t_{LOW}		1.3			µs
High period of the SCL clock		t_{HIGH}		0.6			µs
Setup time for a repeated START condition		$t_{SU, STA}$		0.6			µs
Data hold time		$t_{HD, DAT}$		0		0.9	µs
Data setup time		$t_{SU, DAT}$		100			ns
Rise time for both SDA and SCL signals (receiving)		t_R	C_b = total bus capacitance	20+0.1×C_b		300	ns
Fall time for both SDA and SCL signals (receiving)		t_F	C_b = total bus capacitance	20+0.1×C_b		300	ns
Fall time for both SDA and SCL signals (transmitting)		t_F	C_b = total bus capacitance	20+0.1×C_b		250	ns
Setup time for STOP condition		$t_{SU, STO}$		0.6			µs
Capacitive load for each bus line		C_b	C_b = total capacitance of one bus line in pF			400	pF
Cycle time	8 bits		40 SCL + 127 CCLK, V_{DD} = 1.8V		134.7		µs
	12 bits		49 SCL + 148 CCLK, V_{DD} = 1.8V		203.4		µs
Effective throughput	8 bits		V_{DD} = 1.8V		7.42		kSPS
	12 bits		V_{DD} = 1.8V		4.92		kSPS
Equivalent rate = effective throughput × 7	8 bits		V_{DD} = 1.8V		51.97		kHz
	12 bits		V_{DD} = 1.8V		34.42		kHz

TIMING REQUIREMENTS: I²C High-Speed Mode (SCL = 1.7MHz)

All specifications typical at –40°C to +85°C, V_{DD} = 1.6V, unless otherwise noted.

TWO-WIRE HIGH-SPEED MODE PARAMETERS			TEST CONDITIONS	MIN	TYP	MAX	UNIT
SCL clock frequency		f_{SCL}		0		1.7	MHz
Hold time (repeated) START condition		$t_{HD, STA}$		160			ns
Low period of SCL clock		t_{LOW}		320			ns
High period of the SCL clock		t_{HIGH}		120			ns
Setup time for a repeated START condition		$t_{SU, STA}$		160			ns
Data hold time		$t_{HD, DAT}$		0		150	ns
Data setup time		$t_{SU, DAT}$		10			ns
Rise time for SCL signal (receiving)		t_R	C_b = total bus capacitance	20		80	ns
Rise time for SDA signal (receiving)		t_R	C_b = total bus capacitance	20		160	ns
Fall time for SCL signal (receiving)		t_F	C_b = total bus capacitance	20		80	ns
Fall time for SDA signal (receiving)		t_F	C_b = total bus capacitance	20		160	ns
Fall time for both SDA and SCL signals (transmitting)		t_F	C_b = total bus capacitance	20		160	ns
Setup time for STOP condition		$t_{SU, STO}$		160			ns
Capacitive load for each bus line		C_b	C_b = total capacitance of one bus line in pF			400	pF
Cycle time	8 bits		40 SCL + 127 CCLK, V_{DD} = 1.8V		58.2		µs
	12 bits		49 SCL + 148 CCLK, V_{DD} = 1.8V		109.7		µs
Effective throughput	8 bits		V_{DD} = 1.8V		17.17		kSPS
	12 bits		V_{DD} = 1.8V		9.12		kSPS
Equivalent rate = effective throughput × 7	8 bits		V_{DD} = 1.8V		120.22		kHz
	12 bits		V_{DD} = 1.8V		63.81		kHz

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TIMING REQUIREMENTS: I²C High-Speed Mode (SCL = 3.4MHz)

All specifications typical at –40°C to +85°C, V_{DD} = 1.6V, unless otherwise noted.

TWO-WIRE HIGH-SPEED MODE PARAMETERS			TEST CONDITIONS	MIN	TYP	MAX	UNIT
SCL clock frequency		f_{SCL}		0		3.4	MHz
Hold time (repeated) START condition		$t_{HD, STA}$		160			ns
Low period of SCL clock		t_{LOW}		160			ns
High period of the SCL clock		t_{HIGH}		60			ns
Setup time for a repeated START condition		$t_{SU, STA}$		160			ns
Data hold time		$t_{HD, DAT}$		0		70	ns
Data setup time		$t_{SU, DAT}$		10			ns
Rise time for SCL signal (receiving)		t_R	C_b = total bus capacitance	10		40	ns
Rise time for SDA signal (receiving)		t_R	C_b = total bus capacitance	10		80	ns
Fall time for SCL signal (receiving)		t_F	C_b = total bus capacitance	10		40	ns
Fall time for SDA signal (receiving)		t_F	C_b = total bus capacitance	10		80	ns
Fall time for both SDA and SCL signals (transmitting)		t_F	C_b = total bus capacitance	10		80	ns
Setup time for STOP condition		$t_{SU, STO}$		160			ns
Capacitive load for each bus line		C_b	C_b = total capacitance of one bus line in pF			100	pF
Cycle time	8 bits		40 SCL + 127 CCLK, V_{DD} = 1.8V		46.5		µs
	12 bits		49 SCL + 148 CCLK, V_{DD} = 1.8V		95.3		µs
Effective throughput	8 bits		V_{DD} = 1.8V		21.52		kSPS
	12 bits		V_{DD} = 1.8V		10.49		kSPS
Equivalent rate = effective throughput × 7	8 bits		V_{DD} = 1.8V		150.65		kHz
	12 bits		V_{DD} = 1.8V		73.46		kHz

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TYPICAL CHARACTERISTICS

At T_A = –40°C to +85°C, V_{DD} = +1.6V to +3.6V, PD1 = PD0 = 0, Fast mode, 12-bit mode, non-continuous AUX measurement, and MAV filter enabled (see MAV Filter section), unless otherwise noted.

POWER-DOWN SUPPLY CURRENT vs TEMPERATURE

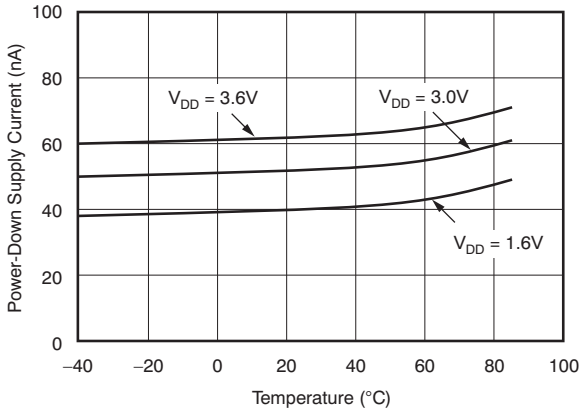

Figure 2.

SUPPLY CURRENT vs TEMPERATURE

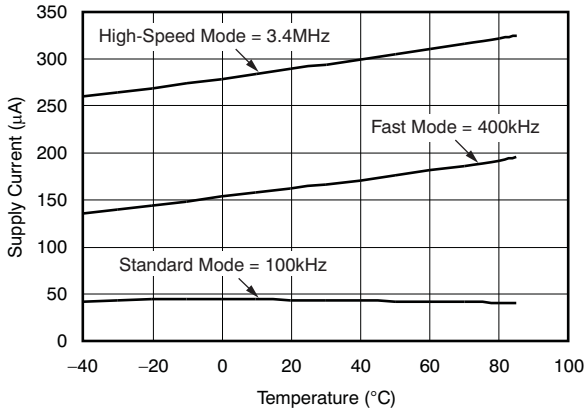

Figure 3.

SUPPLY CURRENT vs SUPPLY VOLTAGE (AUX Conversion)

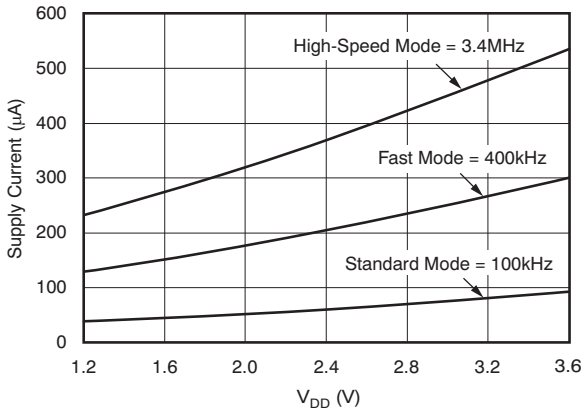

Figure 4.

SUPPLY CURRENT vs SUPPLY VOLTAGE

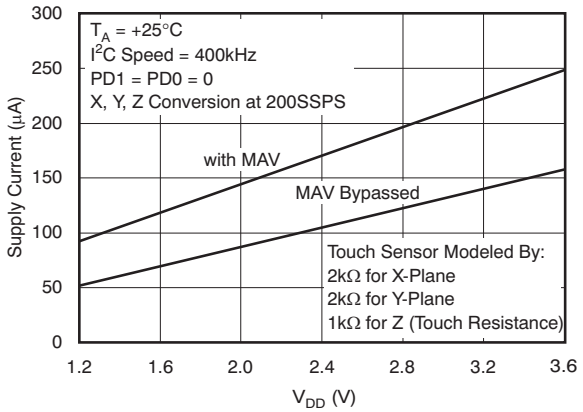

Figure 5.

SUPPLY CURRENT (Part Not Addressed) vs TEMPERATURE

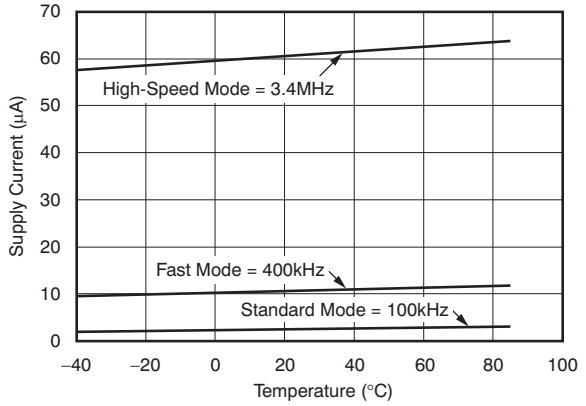

Figure 6.

SUPPLY CURRENT (Part Not Addressed) vs SUPPLY VOLTAGE

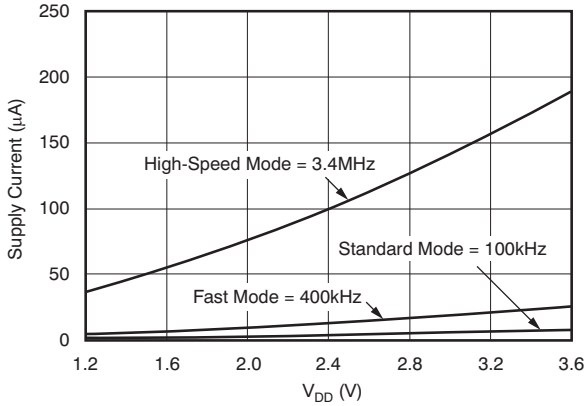

Figure 7.

TYPICAL CHARACTERISTICS (continued)

At T_A = –40°C to +85°C, V_{DD} = +1.6V to +3.6V, PD1 = PD0 = 0, Fast mode, 12-bit mode, non-continuous AUX measurement, and MAV filter enabled (see MAV Filter section), unless otherwise noted.

CHANGE IN GAIN vs TEMPERATURE

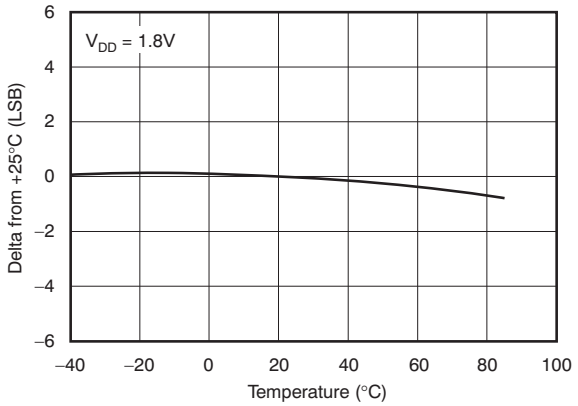

Figure 8.

CHANGE IN OFFSET vs TEMPERATURE

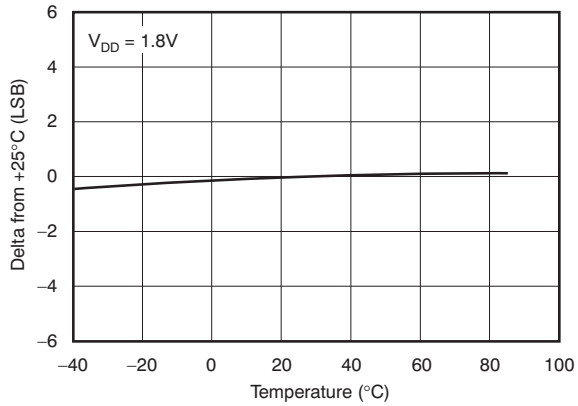

Figure 9.

SWITCH ON-RESISTANCE vs SUPPLY VOLTAGE

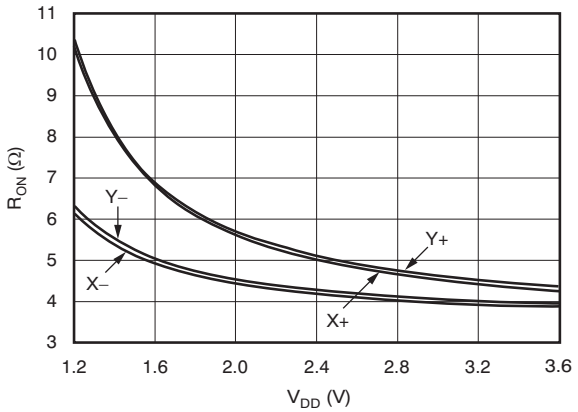

Figure 10.

SWITCH ON-RESISTANCE vs TEMPERATURE

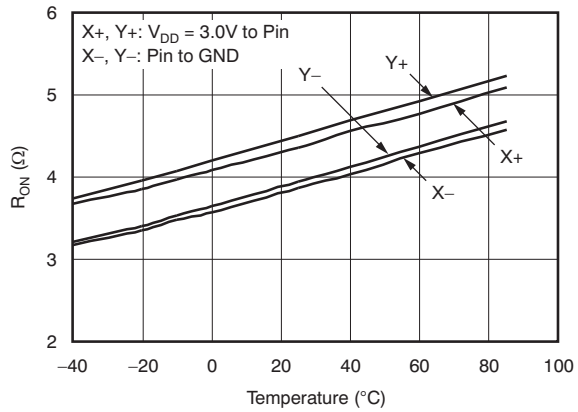

Figure 11.

SWITCH ON-RESISTANCE vs TEMPERATURE

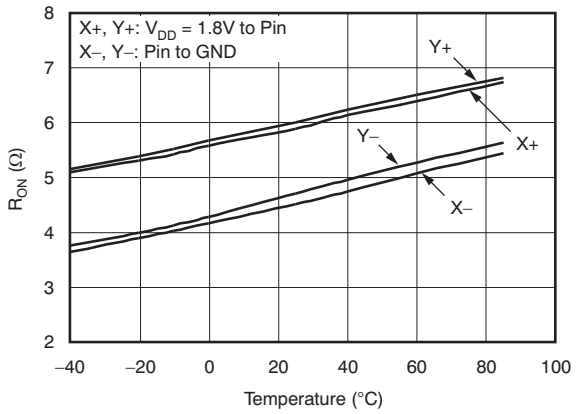

Figure 12.

TEMP DIODE VOLTAGE vs TEMPERATURE

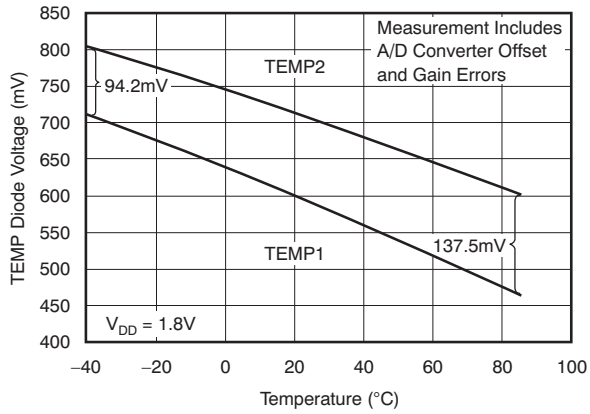

Figure 13.

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TYPICAL CHARACTERISTICS (continued)

At T_A = –40°C to +85°C, V_{DD} = +1.6V to +3.6V, PD1 = PD0 = 0, Fast mode, 12-bit mode, non-continuous AUX measurement, and MAV filter enabled (see MAV Filter section), unless otherwise noted.

TEMP1 DIODE VOLTAGE vs SUPPLY VOLTAGE

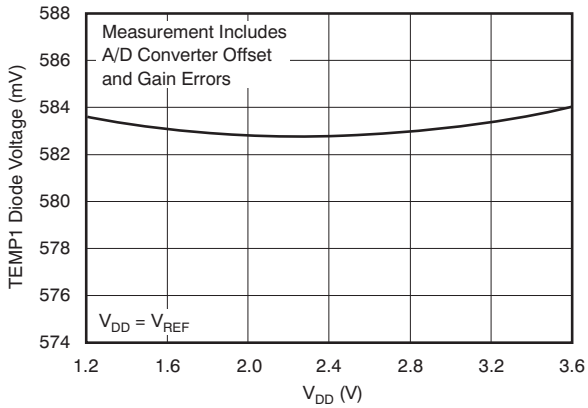

Figure 14.

TEMP2 DIODE VOLTAGE vs SUPPLY VOLTAGE

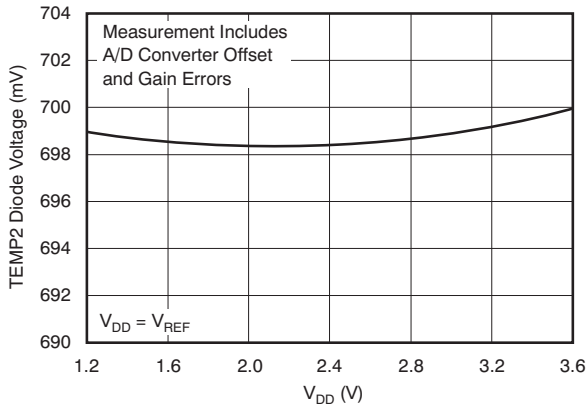

Figure 15.

INTERNAL OSCILLATOR CLOCK FREQUENCY vs TEMPERATURE

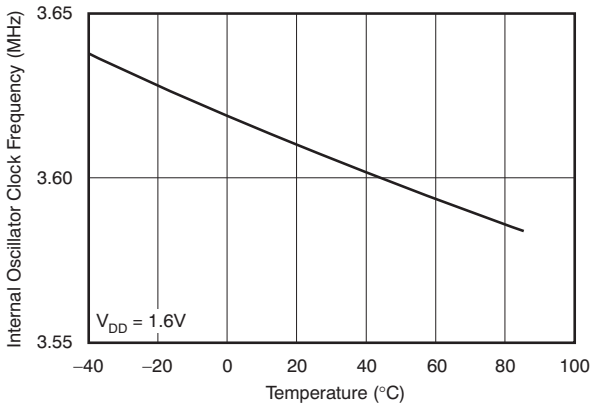

Figure 16.

INTERNAL OSCILLATOR CLOCK FREQUENCY vs TEMPERATURE

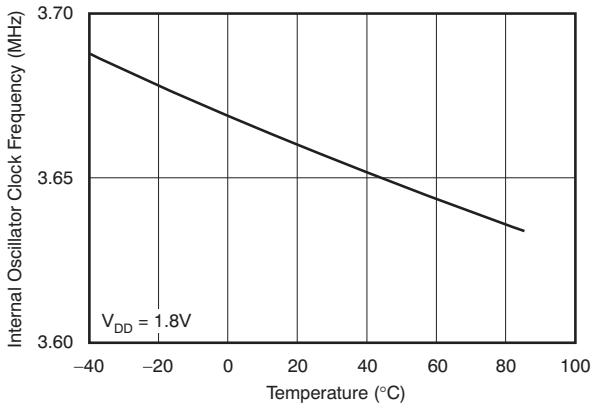

Figure 17.

INTERNAL OSCILLATOR CLOCK FREQUENCY vs TEMPERATURE

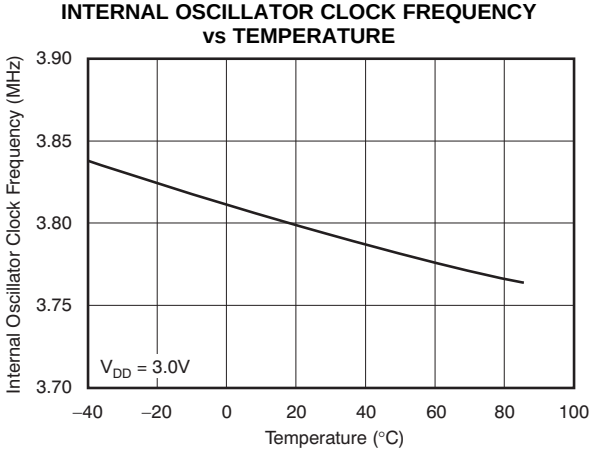

Figure 18.

OVERVIEW

The TSC2017 is an analog interface circuit for a human interface touch screen device. All peripheral functions are controlled through the command byte and onboard state machines. The TSC2017 features include:

- Very low-power touch screen controller
- Very small onboard footprint
- Relieves host from tedious routine tasks by preprocessing, thus saving resources for more critical tasks
- Ability to work on very low supply voltage
- Minimal connection interface allows easiest isolation and reduces the number of dedicated I/O pins required
- Miniature, yet complete; requires no external supporting component
- Enhanced electrostatic discharge (ESD) protection

The TSC2017 consists of the following blocks (refer to the block diagram on the front page):

- Touch Screen Sensor Interface
- Auxiliary Input (AUX)
- Temperature Sensor
- Acquisition Activity Preprocessing
- Internal Conversion Clock
- I^2C Interface

Communication with the TSC2017 is done via an I^2C serial interface. The TSC2017 is an I^2C slave device; therefore, data are shifted into or out of the TSC2017 under control of the host microprocessor, which also provides the serial data clock.

Control of the TSC2017 and its functions is accomplished by writing to the command register of an internal state machine. A simple command protocol compatible with I^2C is used to address this register.

A typical application of the TSC2017 is shown in Figure 19.

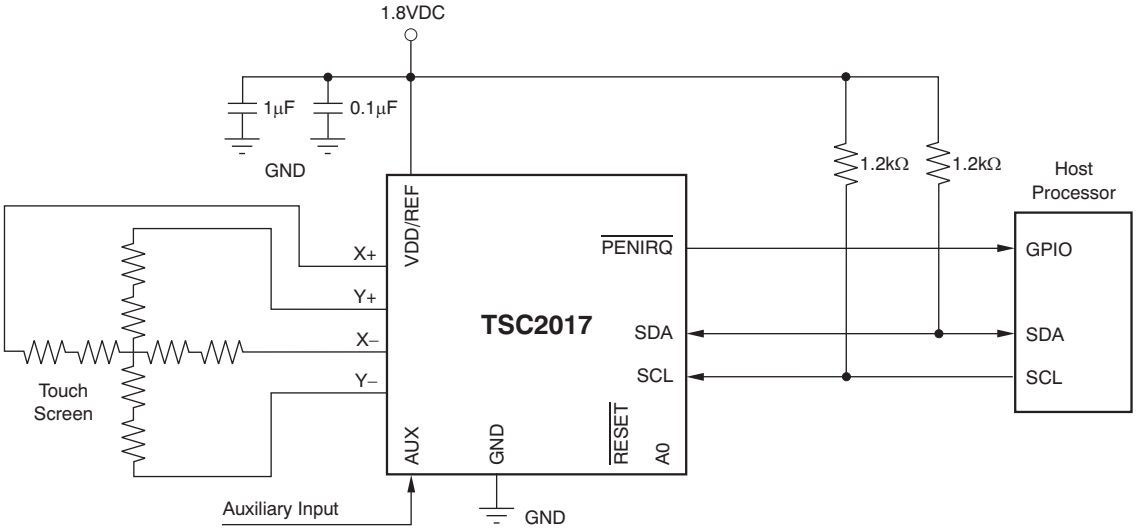

Figure 19. Typical Circuit Configuration

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TOUCH SCREEN OPERATION

A resistive touch screen operates by applying a voltage across a resistor network and measuring the change in resistance at a given point on the matrix where the screen is touched by an input (stylus, pen, or finger). The change in the resistance ratio marks the location on the touch screen.

The TSC2017 supports resistive 4-wire configurations, as shown in Figure 20. The circuit determines location in two coordinate pair dimensions, although a third dimension can be added for measuring pressure.

4-WIRE TOUCH SCREEN COORDINATE PAIR MEASUREMENT

A 4-wire touch screen is typically constructed as shown in Figure 20. It consists of two transparent resistive layers separated by insulating spacers.

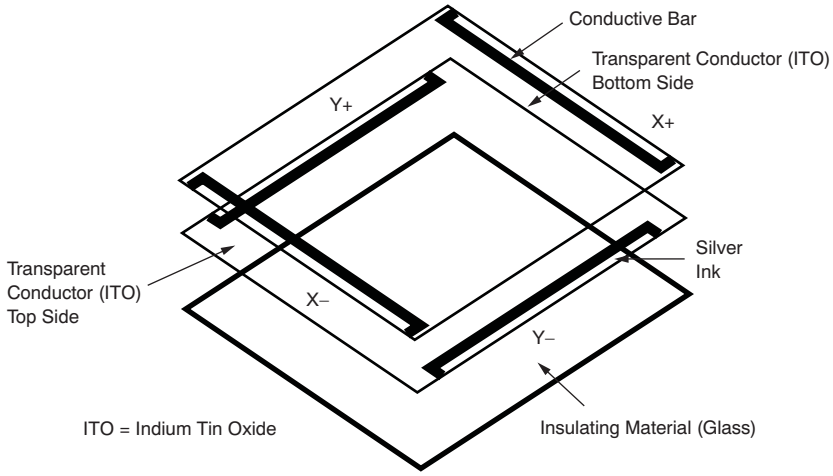

Figure 20. 4-Wire Touch Screen Construction

The 4-wire touch screen panel works by applying a voltage across the vertical or horizontal resistive network. The A/D converter converts the voltage measured at the point where the panel is touched. A measurement of the Y position of the pointing device is made by connecting the X+ input to a data converter chip, turning on the Y+ and Y– drivers, and digitizing the voltage seen at the X+ input. The voltage measured is determined by the voltage divider developed at the point of touch. For this measurement, the horizontal panel resistance in the X+ lead does not affect the conversion because of the high input impedance of the A/D converter.

Voltage is then applied to the other axis, and the A/D converter converts the voltage representing the X position on the screen. This process provides the X and Y coordinates to the associated processor.

Measuring touch pressure (Z) can also be done with the TSC2017. To determine pen or finger touch, the pressure of the *touch* must be determined. Generally, it is not necessary to have very high performance for this test; therefore, 8-bit resolution mode may be sufficient (however, data sheet calculations are shown using the 12-bit resolution mode). There are several different ways of performing this measurement. The TSC2017 supports two methods. The first method requires knowing the X-plate resistance, the measurement of the X-position, and two additional cross panel measurements (Z_2 and Z_1) of the touch screen (see Figure 21). Equation 1 calculates the touch resistance:

$$R_{TOUCH} = R_{X-plate} \cdot \frac{X_{Position}}{4096}\left(\frac{Z_2}{Z_1} - 1\right) \quad (1)$$

The second method requires knowing both the X-plate and Y-plate resistance, measurement of X-position and Y-position, and Z_1. Equation 2 also calculates the touch resistance:

$$R_{TOUCH} = \frac{R_{X-plate} \cdot X_{Position}}{4096}\left(\frac{4096}{Z_1} - 1\right) - R_{Y-plate} \cdot \left(1 - \frac{Y_{Position}}{4096}\right) \quad (2)$$

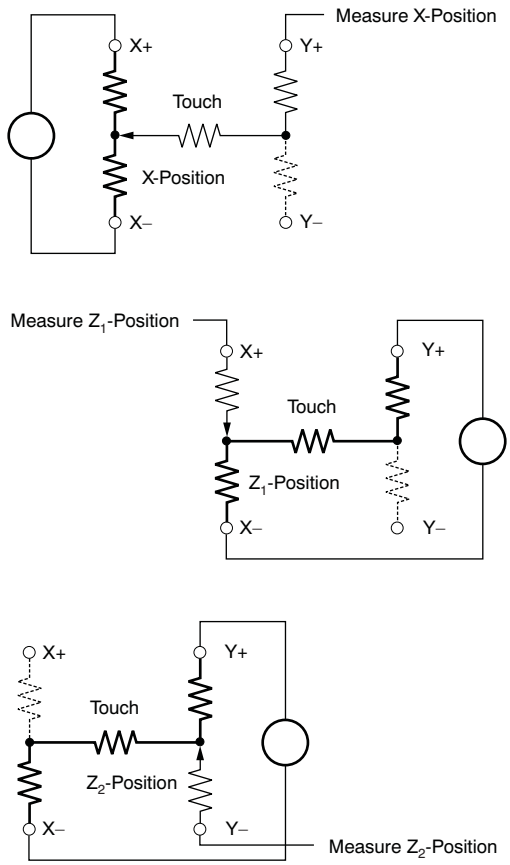

Figure 21. Pressure Measurement

When the touch panel is pressed or touched and the drivers to the panel are turned on, the voltage across the touch panel often overshoots and then slowly settles down (decays) to a stable dc value. This effect is a result of mechanical bouncing caused by vibration of the top layer sheet of the touch panel when the panel is pressed. This settling time must be accounted for, or else the converted value is incorrect. Therefore, a delay must be introduced between the time the driver for a particular measurement is turned on, and the time a measurement is made.

In some applications, external capacitors may be required across the touch screen for filtering noise picked up by the touch screen (for example, noise generated by the LCD panel or back-light circuitry). The value of these capacitors provides a low-pass filter to reduce the noise, but creates an additional settling time requirement when the panel is touched. The settling time typically shows up as gain error.

To solve this problem, the TSC2017 can be commanded to turn on the drivers only, without performing a conversion. Time can then be allowed to perform a conversion before the command is issued.

The TSC2017 touch screen interface can measure position (X,Y) and pressure (Z).

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INTERNAL TEMPERATURE SENSOR

In some applications, such as battery recharging, an ambient temperature measurement is required. The temperature measurement technique used in the TSC2017 relies on the characteristics of a semiconductor junction operating at a fixed current level. The forward diode voltage (V_{BE}) has a well-defined characteristic versus temperature. The ambient temperature can be predicted in applications by knowing the +25°C value of the V_{BE} voltage and then monitoring the delta of that voltage as the temperature changes.

The TSC2017 offers two modes of temperature measurement. The first mode requires calibration at a known temperature, but only requires a single reading to predict the ambient temperature. The TEMP1 diode, shown in Figure 22, is used during this measurement cycle. This voltage is typically 580mV at +25°C with a 10µA current. The absolute value of this diode voltage can vary by a few millivolts; the temperature coefficient (T_C) of this voltage is very consistent at –2.1mV/°C. During the final test of the end product, the diode voltage would be stored at a known room temperature, in system memory, for calibration purposes by the user. The result is an equivalent temperature measurement resolution of 0.35°C/LSB (1LSB = 732µV with V_{REF} = 3.0V).

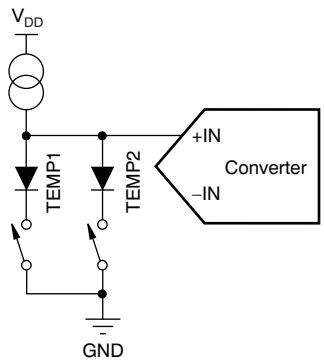

Figure 22. Functional Block Diagram of Temperature Measurement Mode

The second mode does not require a test temperature calibration, but uses a two-measurement (differential) method to eliminate the need for absolute temperature calibration and for achieving 2°C/LSB accuracy. This mode requires a second conversion of the voltage across the TEMP2 diode with a resistance 91 times larger than the TEMP1 diode. The voltage difference between the first (TEMP1) and second (TEMP2) conversion is represented by:

$$\Delta V = \frac{kT}{q} \cdot \ln(N) \tag{3}$$

Where:

N = the resistance ratio = 91.

k = Boltzmann's constant = 1.3807×10^{-23} J/K (joules/kelvins).

q = the electron charge = 1.6022×10^{-19} C (coulombs).

T = temperature in kelvins (K).

This method can provide a much improved absolute temperature measurement, but a lower resolution of 1.6°C/LSB. The resulting equation to solve for T is:

$$T = \frac{q \cdot \Delta V}{k \cdot \ln(N)} \tag{4}$$

Where:

$\Delta V = V_{BE}$ (TEMP2) – V_{BE}(TEMP1) (in mV)

$\therefore$ T = 2.573 · ΔV (in K)

or T = 2.573 · ΔV – 273 (in °C)

Temperature 1 and temperature 2 measurements have the same timing as the other data acquisition cycles shown in Figure 33 and Figure 34.

ANALOG-TO-DIGITAL CONVERTER

Figure 23 shows the analog inputs of the TSC2017. The analog inputs (X, Y, and Z touch panel coordinates, chip temperature and auxiliary inputs) are provided via a multiplexer to the Successive Approximation Register (SAR) A/D converter. The A/D architecture is based on capacitive redistribution architecture, which inherently includes a sample-and-hold function.

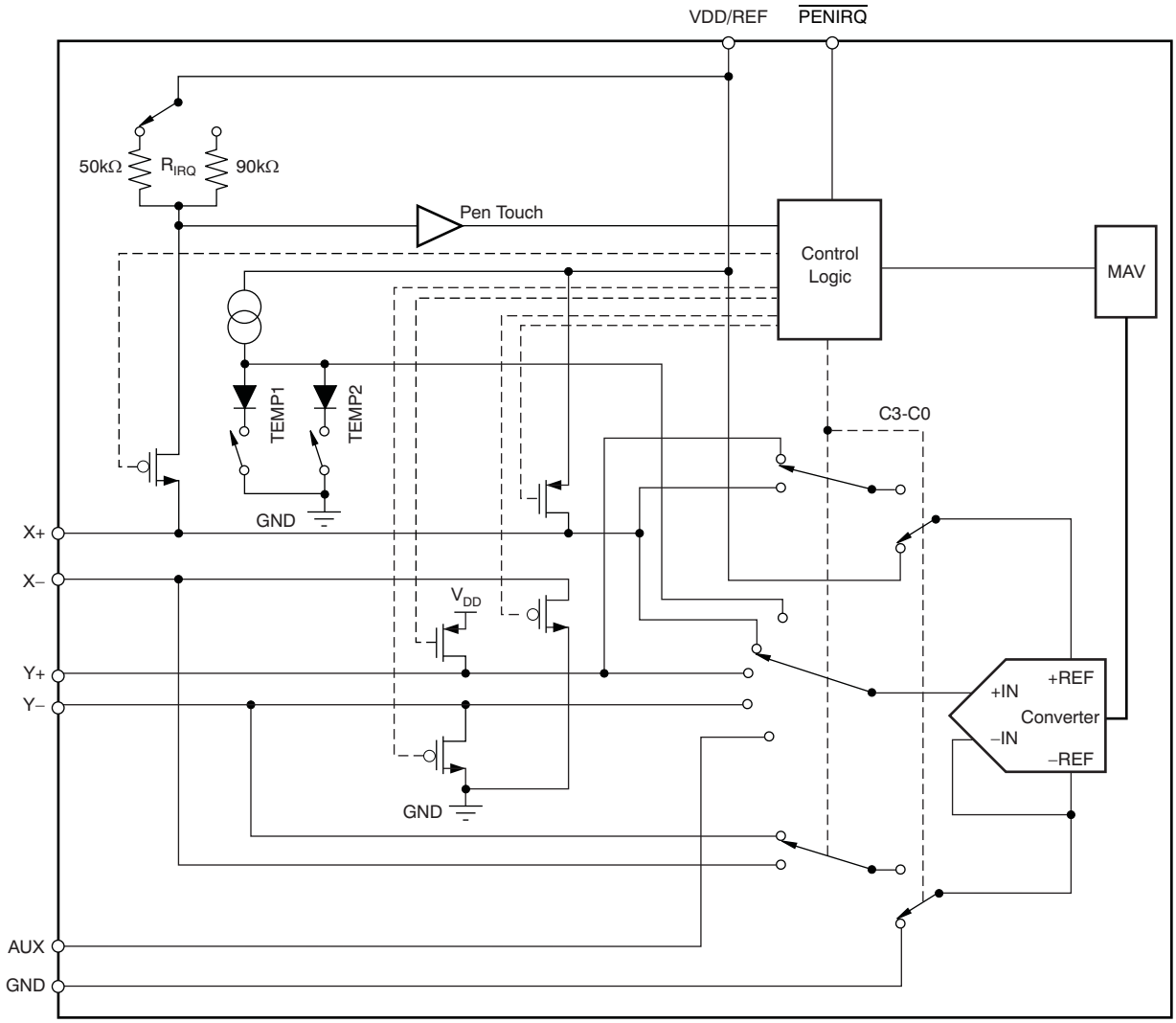

Figure 23. Analog Input Section (Simplified Diagram)

A unique configuration of low on-resistance switches allows an unselected A/D converter input channel to provide power and an accompanying pin to provide ground for driving the touch panel. By maintaining a differential input to the converter and a differential reference input architecture, it is possible to negate errors caused by the driver switch on-resistance.

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Reference

The TSC2017 uses an external voltage reference that is applied to the VDD/REF pin. The upper reference voltage range is the same as the supply voltage range, which allows for simple, 1.6V to 3.6V, single-supply operation of the chip.

Reference Mode

There is a critical item regarding the reference when making measurements while the switch drivers are on. For this discussion, it is useful to consider the basic operation of the TSC2017 (see Figure 19). The application used in the following example shows the device being used to digitize a resistive touch screen. If the touch screen controller uses a single-ended reference mode, as shown in Figure 24, a measurement of the current Y position of the pointing device is made by connecting the X+ input to the A/D converter, turning on the Y+ and Y– drivers, and digitizing the voltage on X+. For this measurement, the resistance in the X+ lead does not affect the conversion; it does affect the settling time, but the resistance is usually small enough that this timing is not a concern. However, because the resistance between Y+ and Y– is fairly low, the on-resistance of the Y drivers does make a small difference. Under the situation outlined so far, it would not be possible to achieve a 0V input or a full-scale input regardless of where the pointing device is on the touch screen because some voltage is lost across the internal switches. In addition, the internal switch resistance is unlikely to track the resistance of the touch screen, providing an additional source of error. Therefore, the TSC2017 does not support single-ended reference mode.

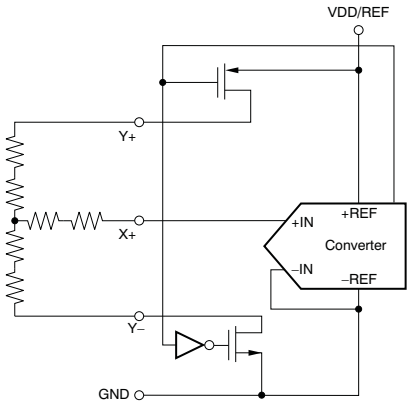


Figure 24. Simplified Diagram of Single-Ended Reference

This situation is resolved, as shown in Figure 25, by using the differential mode; the +REF and –REF inputs are connected directly to Y+ and Y–, respectively. This mode makes the A/D converter ratiometric. The result of the conversion is always a percentage of the external reference, regardless of how it changes in relation to the on-resistance of the internal switches.

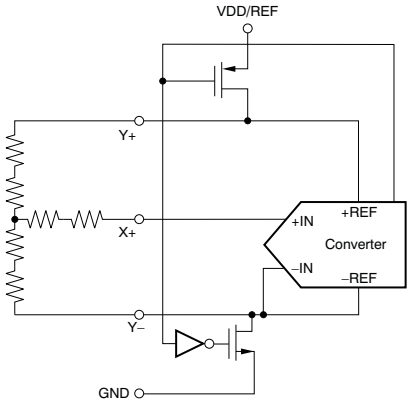


Figure 25. Simplified Diagram of Differential Reference (Both Y Switches Enabled, X+ is Analog Input)

Touch Screen Settling

In some applications, external capacitors may be required across the touch screen to filter noise picked up by the touch screen (that is, noise generated by the LCD panel or backlight circuitry). These capacitors provide a low-pass filter to reduce the noise, but they also cause a settling time requirement when the panel is touched. The settling time typically shows up as a gain error. The problem is that the input and/or reference has not settled to its final steady-state value before the A/D converter samples the input(s) and provides the digital output. Additionally, the reference voltage may continue to change during the measurement cycle.

To resolve these settling-time problems, the TSC2017 can be commanded to turn on the drivers only without performing a conversion (see Table 3). Time can then be allowed, before the command is issued, to perform a conversion. Generally, the time it takes to communicate the conversion command over the I^2C bus is adequate for the touch screen to settle.

Variable Resolution

The TSC2017 provides either 8-bit or 12-bit resolution for the A/D converter. Lower resolution is often practical for measuring slow changing signals such as touch pressure. Performing the conversions at lower resolution reduces the amount of time it takes for the A/D converter to complete its conversion process, which also lowers power consumption.

8-Bit Conversion

The TSC2017 provides an 8-bit conversion mode (M = 1) that can be used when faster throughput is needed, and the digital result is not as critical (for example, measuring pressure). By switching to the 8-bit mode, a conversion result can be read by transferring only one data byte. The internal clock runs twice as fast at 4MHz.

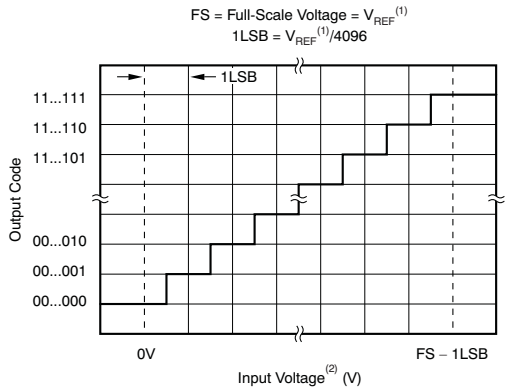
The faster clock shortens each conversion by four bits and reduces data transfer time, which results in fewer clock cycles and provides lower power consumption.

Conversion Clock and Conversion Time

The TSC2017 contains an internal clock, which drives the state machines inside the device that perform the many functions of the part. This clock is divided down to provide a clock that runs the A/D converter. The frequency of this clock is 4MHz clock for 8-bit mode, and 2MHz for the 12-bit mode.

Data Format

The TSC2017 output data are in straight binary format as shown in Figure 26. This figure shows the ideal output code for the given input voltage and does not include the effects of offset, gain, or noise.



(1) Reference voltage at converter: +REF – (–REF). See Figure 23.

(2) Input voltage at converter, after multiplexer: +IN – (–IN). See Figure 23.

Figure 26. Ideal Input Voltages and Output Codes

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Touch Detect

The $\overline{\text{PENIRQ}}$ can be used as an interrupt to the host. R_{IRQ} is an internal pull-up resistor with a programmable value of either 50kΩ (default) or 90kΩ. Write command '1011' (setup command) followed by data '0001' sets the pull-up to 90kΩ. **NOTE:** The first three bits must be '0's and the select bit is the last bit. To change the pull-up back to 50kΩ, issue write command '1011' followed by data '0000'.

An example for the Y-position measurement is detailed in Figure 27. The $\overline{\text{PENIRQ}}$ output is pulled high by an internal pull-up. While in power-down mode with PD0 = 0, the Y– driver is on and connected to GND, and the $\overline{\text{PENIRQ}}$ output is connected to the X+ input. When the panel is touched, the X+ input is pulled to ground through the touch screen, and the $\overline{\text{PENIRQ}}$ output goes low because of the current path through the panel to GND, initiating an interrupt to the processor. During the measurement cycle for X-, Y-, and Z-position, the X+ input is disconnected from the $\overline{\text{PENIRQ}}$ pull-down transistor to eliminate any pull-up resistor leakage current from flowing through the touch screen, thus causing no errors.

In addition to the measurement cycles for X-, Y-, and Z-position, commands that activate the X-drivers, Y-drivers, and Y+ and X-drivers without performing a measurement also disconnect the X+ input from the $\overline{\text{PENIRQ}}$ pull-down transistor, and disable the pen-interrupt output function, regardless of the value of the PD0 bit. Under these conditions, the $\overline{\text{PENIRQ}}$ output is forced low. Furthermore, if the last command byte written to the TSC2017 contains PD0 = 1, the pen-interrupt output function is disabled and cannot detect when the panel is touched. In order to re-enable the pen-interrupt output function under these circumstances, a command byte must be written to the TSC2017 with PD0 = 0.

When the bus master sends the address byte with the R/$\overline{\text{W}}$ bit = 0, and the TSC2017 sends an acknowledge, the pen-interrupt function is disabled. If the command that follows the address byte contains PD0 = 0, then the pen-interrupt function is enabled at the end of a conversion. This action is approximately 100µs (12-bit mode) or 50µs (8-bit mode) after the TSC2017 receives a STOP/START condition, following the receipt of a command byte (see Figure 31 and Figure 30 for further details about when the conversion cycle begins).

In both cases previously listed, it is recommended that whenever the host writes to the TSC2017, the master processor masks the interrupt associated to $\overline{\text{PENIRQ}}$. This masking prevents false triggering of interrupts when the $\overline{\text{PENIRQ}}$ line is disabled in the cases previously listed.

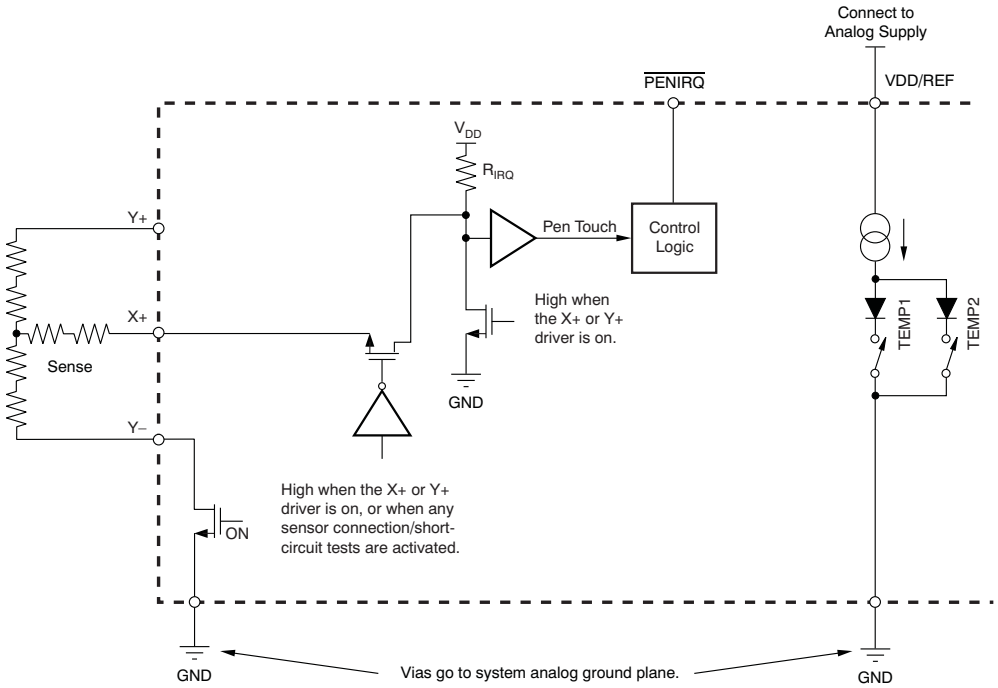

Figure 27. Example of a Pen-Touch Induced Interrupt via the $\overline{\text{PENIRQ}}$ Pin

Preprocessing

The TSC2017 has a combined MAV filter (median value filter and averaging filter).

MAV Filter

If the acquired signal source is noisy because of the digital switching circuit, it may necessary to evaluate the data without noise. In this case, the median value filter operation helps remove the *noise*. The array of seven converted results is sorted first. The middle three values are then averaged to produce the output value of the MAV filter.

The MAV filter is applied to all measurements for all analog inputs including the touch screen inputs, temperature measurements TEMP1 and TEMP2, and auxiliary input AUX. To shorten the conversion time, the MAV filter may be bypassed through the setup command; see Table 3 and Table 4.

Figure 28. MAV Filter Operation (Patent Pending)

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I²C INTERFACE

The TSC2017 supports the I²C serial bus and data transmission protocol in all three defined modes: standard, fast, and high-speed. A device that sends data onto the bus is defined as a transmitter, and a device receiving data as a receiver. The device that controls the message is called a *master*. The devices that are controlled by the master are *slaves*. The bus must be controlled by a master device that generates the serial clock (SCL), controls the bus access, and generates the START and STOP conditions. The TSC2017 operates as a slave on the I²C bus. Connections to the bus are made via the open-drain I/O lines, SDA and SCL.

The following bus protocol has been defined (see Figure 29):

- Data transfer may be initiated only when the bus is not busy.
- During data transfer, the data line must remain stable whenever the clock line is HIGH. Changes in the data line while the clock line is HIGH will be interpreted as control signals.

Accordingly, the following bus conditions have been defined:

Bus Not Busy Both data and clock lines remain HIGH.

Start Data Transfer A change in the state of the data line, from HIGH to LOW, while the clock is HIGH, defines a START condition.

Stop Data Transfer A change in the state of the data line, from LOW to HIGH, while the clock line is HIGH, defines the STOP condition.

Data Valid The state of the data line represents valid data, when, after a START condition, the data line is stable for the duration of the HIGH period of the clock signal. There is one clock pulse per bit of data.

Each data transfer is initiated with a START condition and terminated with a STOP condition. The number of data bytes transferred between START and STOP conditions is not limited and is determined by the master device. The information is transferred byte-wise and each receiver acknowledges with a ninth bit.

Within the I²C bus specifications, a standard mode (100kHz clock rate), a fast mode (400kHz clock rate), and a high-speed mode (1.7MHz or 3.4MHz clock rate) are each defined. The TSC2017 works in all three modes.

Acknowledge Each receiving device, when addressed, is obliged to generate an acknowledge after the reception of each byte. The master device must generate an extra clock pulse that is associated with this acknowledge bit.

A device that acknowledges must pull down the SDA line during the acknowledge clock pulse in such a way that the SDA line is stable LOW during the HIGH period of the acknowledge clock pulse. Of course, setup and hold times must be taken into account. A master must signal an end of data to the slave by not generating an acknowledge bit on the last byte that has been clocked out of the slave. In this case, the slave must leave the data line HIGH to enable the master to generate the STOP condition.

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Figure 29 details how data transfer is accomplished on the I^{2}C bus. Depending upon the state of the R/$\overline{W}$ bit, two types of data transfer are possible:

1. **Data transfer from a master transmitter to a slave receiver.** The first byte transmitted by the master is the slave address. Next follows a number of data bytes. The slave returns an acknowledge bit after the slave address and each received byte.
2. **Data transfer from a slave transmitter to a master receiver.** The first byte, the slave address, is transmitted by the master. The slave then returns an acknowledge bit. Next, a number of data bytes are transmitted by the slave to the master. The master returns an acknowledge bit after all received bytes other than the last byte. At the end of the last received byte, a not-acknowledge is returned.

The master device generates all of the serial clock pulses and the START and STOP conditions. A transfer ends with a STOP condition or a repeated START condition. Because a repeated START condition is also the beginning of the next serial transfer, the bus is not released.

The TSC2017 may operate in the following two modes:

1. **Slave Receiver Mode**: Serial data and clock are received through SDA and SCL. After each byte is received, an acknowledge bit is transmitted. START and STOP conditions are recognized as the beginning and end of a serial transfer. Address recognition is performed by hardware after reception of the slave address and direction bit.
2. **Slave Transmitter Mode**: The first byte (the slave address) is received and handled as in the slave receiver mode. However, in this mode, the direction bit indicates that the transfer direction is reversed. Serial data are transmitted on SDA by the TSC2017 while the serial clock is input on SCL. START and STOP conditions are recognized as the beginning and end of a serial transfer.

I^{2}C Fast or Standard Mode (F/S Mode)

In I^{2}C Fast or Standard (F/S) mode, serial data transfer must meet the timing shown in the Timing Information section.

In the serial transfer format of F/S mode, the master signals the beginning of a transmission to a slave with a START condition (S), which is a high-to-low transition on the SDA input while SCL is high. When the master has finished communicating with the slave, the master issues a STOP condition (P), which is a low-to-high transition on SDA while SCL is high, as shown in Figure 29. The bus is free for another transmission after a STOP condition has occurred. Figure 29 shows the complete F/S mode transfer on the I^{2}C, 2-wire serial interface. The address byte, control byte, and data byte are transmitted between the START and STOP conditions. The SDA state is only allowed to change while SCL is low, except for the START and STOP conditions. Data are transmitted in 8-bit words. Nine clock cycles are required to transfer the data into or out of the device (8-bit word plus acknowledge bit).

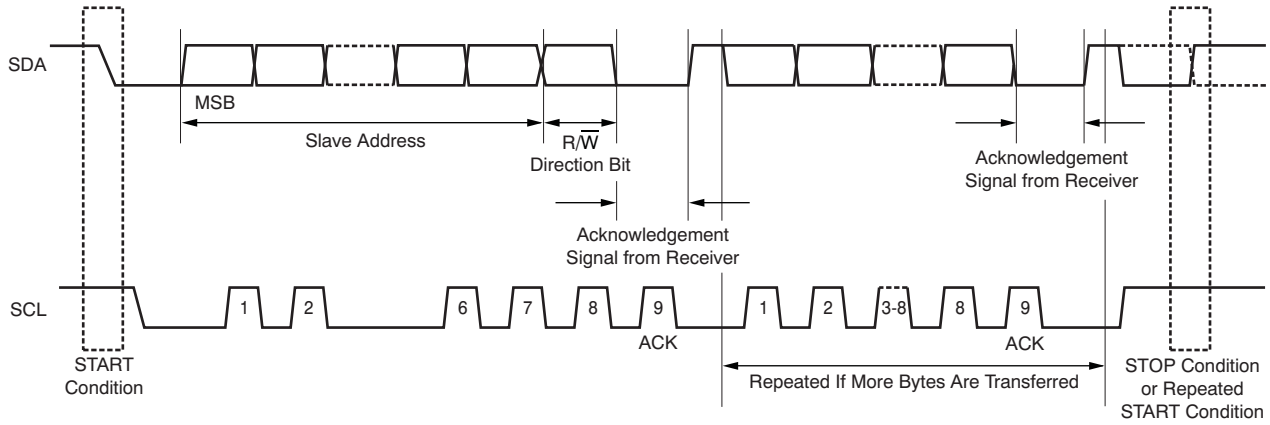

Figure 29. Complete Fast- or Standard-Mode Transfer

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I²C High-Speed Mode (Hs Mode)

The TSC2017 can operate with high-speed I²C masters. To do so, the pull-up resistor on SCL must be changed to an active pull-up, as recommended in the I²C specification.

Serial data transfer format in High-Speed (Hs) mode meets the Fast or Standard (F/S) mode I²C bus specification. Hs mode can only commence after the following conditions (all of which are in F/S mode) exist:

1. START condition (S)
2. 8-bit master code (00001xxx)
3. Not-acknowledge bit (N)

Figure 30 shows this sequence in more detail. Hs-mode master codes are reserved 8-bit codes used only for triggering Hs mode, and are not to be used for slave addressing or any other purpose. The master code indicates to other devices that an Hs-mode transfer is about to begin and the connected devices must meet the Hs mode specification. Because no device is allowed to acknowledge the master code, the master code is followed by a not-acknowledge bit (N).

After the not-acknowledge bit (N) and SCL have been pulled-up to a HIGH level, the master switches to Hs-mode and enables the current-source pull-up circuit for SCL (at time t_H shown in Figure 30). Because other devices can delay the serial transfer before t_H by stretching the LOW period of SCL, the master enables the current-source pull-up circuit when all devices have released SCL, and SCL has reached a HIGH level, thus speeding up the last part of the rise time of the SCL.

The master then sends a repeated START condition (Sr) followed by a 7-bit slave address with a R/$\overline{W}$ bit address, and receives an acknowledge bit (A) from the selected slave. After a repeated START (Sr) condition and after each acknowledge bit (A) or not-acknowledge bit (N), the master disables its current-source pull-up circuit. This disabling enables other devices, such as the TSC2017, to delay the serial transfer (until the converted data are stored in the TSC internal shift register) by stretching the LOW period of SCL. The master re-enables its current-source pull-up circuit again when all devices have released SCL, and SCL reaches a HIGH level, which speeds up the last part of the SCL signal rise time.

Data transfer continues in Hs mode after the next repeated START (Sr), and only switches back to F/S mode after a STOP condition (P). To reduce the overhead of the master code, it is possible for the master to link a number of Hs mode transfers, separated by repeated START conditions (Sr).

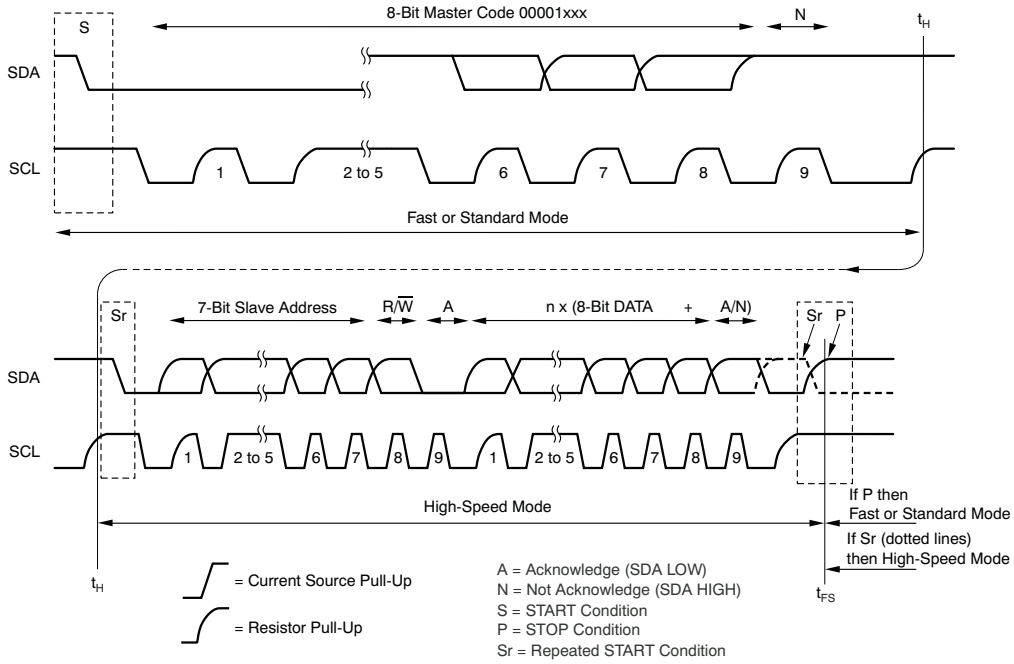

Figure 30. Complete High-Speed Mode Transfer

DIGITAL INTERFACE

ADDRESS BYTE

The TSC2017 has a 7-bit slave address word. The first six bits (MSBs) of the slave address are factory-preset to comply with the I^2C standard for A/D converters and are always set at '100100'. The logic state of the address input pin (A0) determines the LSB of the device address to activate communication. Therefore, a maximum of two devices with the same preset code can be connected on the same bus at one time.

The A0 address input is read whenever an address byte is received, and should be connected to the supply pin (VDD/REF) or the ground pin (GND). The slave address is latched into the TSC2017 on the falling edge of SCL after the read/write bit has been received by the slave.

The last bit of the address byte (R/$\overline{W}$) defines the operation to be performed. When set to a '1', a read operation is selected; when set to a '0', a write operation is selected. Following the START condition, the TSC2017 monitors the SDA bus, checking the device type identifier being transmitted. The slave device outputs an acknowledge signal on the SDA line upon receiving the '100100' code, the appropriate device select bit, and the R/$\overline{W}$ bit.

Table 1. I^2C Slave Address Byte

MSB D7	D6	D5	D4	D3	D2	D1	LSB D0
1	0	0	1	0	0	A0	R/$\overline{W}$

Bit D0: R/$\overline{W}$

1: I^2C master read from TSC (I^2C read addressing).

0: I^2C master write to TSC (I^2C write addressing).

COMMAND BYTE

Table 2. Command Byte Definition (Excluding the Setup Command)(1)

BIT	NAME	DESCRIPTION
D7-D4	C3-C0	All Converter Function Select bits as detailed in Table 3, except for the setup command ('1011').
D3-D2	PD1-PD0	00: Power down between cycles. $\overline{PENIRQ}$ enabled. 01: A/D converter on. $\overline{PENIRQ}$ disabled. 10: A/D converter off. $\overline{PENIRQ}$ enabled. 11: A/D converter on. $\overline{PENIRQ}$ disabled.
D1	M	0: 12-bit (Lower speed referred to as the 2MHz clock). 1: 8-bit (Higher speed referred to as the 4MHz clock).
D0	X	Don't care.

(1) The command byte definition for the setup command is shown in Table 4.

Bits D7-D4: C3-C0—Converter function select bits. These bits select the input to be converted and the converter function to be executed, activate the drivers, and configure the $\overline{PENIRQ}$ pull-up resistor (R_{IRQ}). Table 3 lists the possible converter functions.

Bits D3-D2: PD1-PD0—Power-down bits. These two bits select the power-down mode that the TSC2017 will be in after the current command completes, as shown in Table 2.

It is recommended to set PD0 = 0 in each command byte to get the lowest power consumption possible. If multiple X-, Y-, and Z-position measurements will be done one right after another (such as when averaging), PD0 =1 will leave the touch screen drivers on at the end of each conversion cycle.

Bit D1: M—Mode bit. If M = 0, the TSC2017 is in 12-bit mode. If M = 1, 8-bit mode is selected.

Bit D0: X—Don't care.

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When the TSC2017 powers up, the power-down bits must be written to ensure that the device is placed into the mode that achieves the lowest power. Therefore, immediately after power-up, send a command byte that sets PD1 = PD0 = 0, so that the device is in the lowest power mode, powering down between conversions.

Table 3. Converter Function Select

C3	C2	C1	C0	FUNCTION	INPUT TO A/D CONVERTER	X-DRIVERS	Y-DRIVERS	ACK	REFERENCE MODE
0	0	0	0	Measure TEMP0	TEMP0	OFF	OFF	Y	Single-Ended
0	0	0	1	Reserved	N/A	OFF	OFF	N	Single-Ended
0	0	1	0	Measure AUX	AUX	OFF	OFF	Y	Single-Ended
0	0	1	1	Reserved	N/A	OFF	OFF	N	Single-Ended
0	1	0	0	Measure TEMP1	TEMP1	OFF	OFF	Y	Single-Ended
0	1	0	1	Reserved	N/A	OFF	OFF	N	Single-Ended
0	1	1	0	Reserved	N/A	OFF	OFF	N	Single-Ended
0	1	1	1	Reserved	N/A	OFF	OFF	N	Single-Ended
1	0	0	0	Activate X– drivers	N/A	ON	OFF	Y	Differential
1	0	0	1	Activate Y– drivers	N/A	OFF	ON	Y	Differential
1	0	1	0	Activate Y+, X– drivers	N/A	X– ON	Y+ ON	Y	Differential
1	0	1	1	Setup command(1)	N/A	OFF	OFF	Y	N/A
1	1	0	0	Measure X position	Y+	ON	OFF	Y	Differential
1	1	0	1	Measure Y position	X+	OFF	ON	Y	Differential
1	1	1	0	Measure Z1 position	X+	X– ON	Y+ ON	Y	Differential
1	1	1	1	Measure Z2 position	Y–	X– ON	Y+ ON	Y	Differential

(1) The setup command has an additional four bits of data. These data are static; that is, they are not changed by other commands, except for the power-on reset. The default value for these bits after power-on reset is 0000. Table 4 shows the definition of these data bits.

Table 4. Command Byte Definition for the Setup Command

BIT	NAME	DESCRIPTION
D7-D4	C3-C0 = '1011'	Setup command; must write '1011'.
D3	Reserved	Reserved; must write '0'.
D2	Software reset	0: Normal operation, not reset. 1: Reset all registers to default values (this bit is self-clearing).
D1	Filter control	0: Use the onboard MAV filter (default). 1: Bypass the onboard MAV filter.
D0	$\overline{\text{PENIRQ}}$ pull-up resistor (R_{IRQ}) select	0: R_{IRQ} = 50kΩ (default). 1: R_{IRQ} = 90kΩ.

START A CONVERTER FUNCTION/WRITE CYCLE

A conversion/write cycle begins when the master issues the address byte containing the slave address of the TSC2017, with the eighth bit equal to a 0 (R/$\overline{W}$ = 0), as shown in Table 1. Once the eighth bit has been received, and the address matches the A0 address input pin setting, the TSC2017 issues an acknowledge.

When the master receives the acknowledge bit from the TSC2017, the master writes the command byte to the slave (see Table 2). After the command byte is received by the slave, the slave issues another acknowledge bit. The master then ends the write cycle by issuing a repeated START or a STOP condition, as shown in Figure 31.

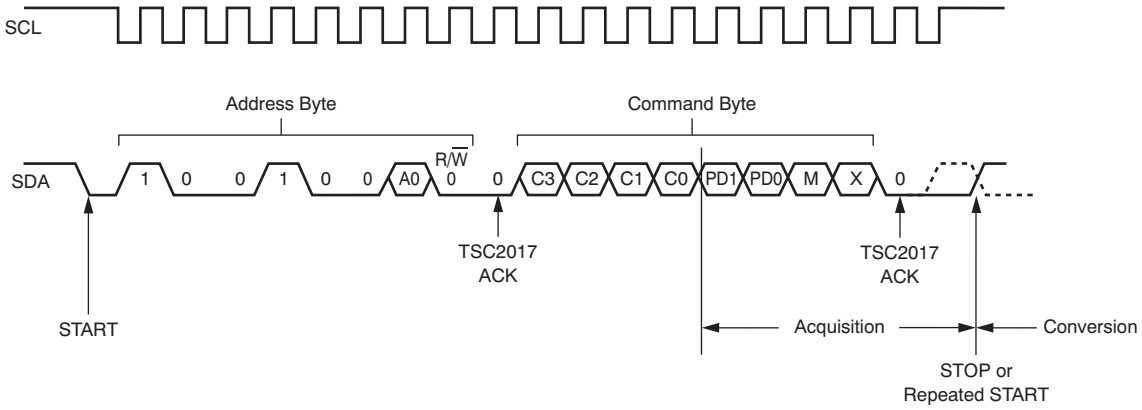

Figure 31. Complete I²C Serial Write Transmission

If the master sends additional command bytes after the initial byte, but before sending a STOP or repeated START condition, the TSC2017 does not acknowledge those bytes.

The input multiplexer channel for the A/D converter is selected when bits C3 through C0 are clocked in. If the selected channel is an X-,Y-, or Z-position measurement, the appropriate drivers turn on once the acquisition period begins.

When R/$\overline{W}$ = 0, the input sample acquisition period starts on the falling edge of SCL when the C0 bit of the command byte has been latched, and ends when a STOP or repeated START condition has been issued. A/D conversion starts immediately after the acquisition period. The multiplexer inputs to the A/D converter are disabled once the conversion period starts. However, if an X-, Y-, or Z-position is being measured, the respective touch screen drivers remain on during the conversion period. A complete write cycle is shown in Figure 31.

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READ A CONVERSION/READ CYCLE

For best performance, the I^{2}C bus should remain in an idle state while an A/D conversion is taking place. This idling prevents digital clock noise from affecting the bit decisions being made by the TSC2017. The master should wait for at least 10µs before attempting to read data from the TSC2017 to realize this best performance. However, the master does not need to wait for a completed conversion before beginning a read from the slave, if full 12-bit performance is not necessary.

Data access begins with the master issuing a START condition followed by the address byte (see Table 1) with R/$\overline{W}$ = 1.

When the eighth bit has been received and the address matches, the slave issues an acknowledge. The first byte of serial data then follows (D11-D4, MSB first).

After the first byte has been sent by the slave, it releases the SDA line for the master to issue an acknowledge. The slave responds with the second byte of serial data upon receiving the acknowledge from the master (D3-D0, followed by four 0 bits). The second byte is followed by a NOT acknowledge bit (ACK = 1) from the master to indicate that the last data byte has been received. If the master somehow acknowledges the second data byte, invalid data are returned (FFh). This condition applies to both 12-and 8-bit modes. See Figure 32 for a complete I^{2}C read transmission.

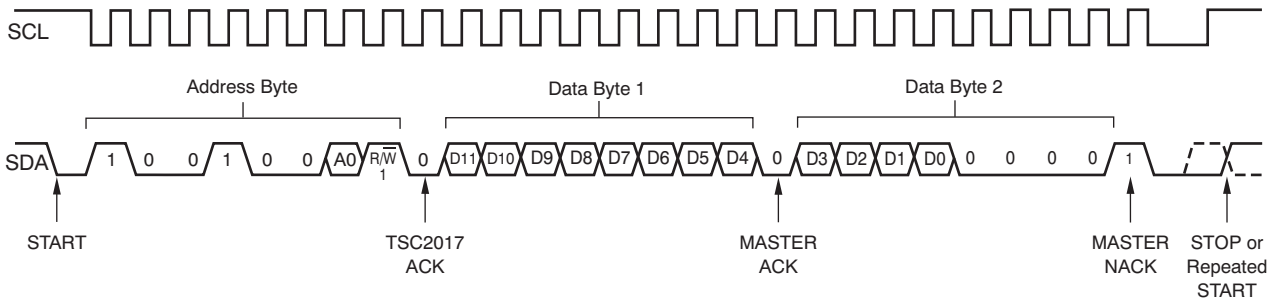

Figure 32. Complete I^{2}C Serial Read Transmission

THROUGHPUT RATE AND I²C BUS TRAFFIC

Although the internal A/D converter has a sample rate of up to 200kSPS, the throughput presented at the bus is much lower. The rate is reduced because preprocessing manages the redundant work of filtering out noise. The throughput is further limited by the I²C bus bandwidth. The effective throughput is approximately 20kSPS at 8-bit resolution, or 10kSPS at 12-bit resolution. This preprocessing saves a large portion of the I²C bandwidth for the system to use on other devices.

Each sample and conversion takes 19 CCLK cycles (12-bit), or 16 CCLK cycles (8-bit). For a typical internal 4MHz OSC clock, the frequency actually ranges from 3.66MHz to 3.82MHz. For V_{DD} = 1.6V, the frequency reduces to 3.61MHz, which gives a 3.61MHz/16 = 225kSPS raw A/D converter sample rate.

12-Bit Operation

For 12-bit operation, sending the conversion result across the I²C bus takes 49 bus clocks (SCL clock). Each write cycle takes 20 I²C cycles (START, STOP, address byte, two ACKs, and command byte). Each read cycle takes 29 I²C cycles (START, STOP, address byte, three ACKs, and data bytes 1 and 2). Seven sample-and-conversions take 19 x 7 internal clocks to complete. The MAV filter loop requires 19 internal clocks. For V_{DD} = 1.6V, the complete processed data cycle time calculations are shown in Table 5. Because the first acquisition cycle overlaps with the I/O cycle, four CCLKs should be deducted from the total CCLK cycles. For 12-bit mode, (19 × 7 + 19) – 4 = 148 CCLKs plus I/O are required.

8-Bit Operation

For 8-bit operation, sending the conversion result across the I²C bus takes 40 bus clocks (SCL clock). Each write cycle takes 20 I²C cycles (START, STOP, address byte, two ACKs, and command byte). Each read cycle takes 20 I²C cycles (START, STOP, address byte, 2 ACKs, and data byte 1). Seven sample-and-conversions takes 16 x 7 internal clocks to complete. The MAV filter loop requires 19 internal clocks. For V_{DD} = 1.6V, the complete processed data cycle time calculations are shown in Table 5. Because the first acquisition cycle overlaps with the I/O cycle, four CCLKs should be deducted from the total CCLK cycles. For 8-bit mode, (16 × 7 + 19) – 4 = 127 CCLKs plus I/O are required.

Table 5. Measurement Cycle Time Calculations

STANDARD MODE: 100kHz (Period = 10µs)	
8-Bit	40 × 10µs + 127 × 277ns = 435.2µs (2.3kSPS through the I²C bus)
12-Bit	49 × 10µs + 148 × 555ns = 572.2µs (1.75kSPS through the I²C bus)
FAST MODE: 400kHz (Period = 2.5µs)	
8-Bit	40 × 2.5µs + 127 × 277ns = 135.2µs (7.4kSPS through the I²C bus)
12-Bit	49 × 2.5µs + 148 × 555ns = 204.7µs (4.88kSPS through the I²C bus)
HIGH-SPEED MODE: 1.7MHz (Period = 588ns)	
8-Bit	40 × 588ns + 127 × 277ns = 58.7µs (17.03kSPS through the I²C bus)
12-Bit	49 × 588ns + 148 × 555ns = 111µs (9.01kSPS through the I²C bus)
HIGH-SPEED MODE: 3.4MHz (Period = 294ns)	
8-Bit	40 × 294ns + 127 × 277ns = 46.9µs (21.3kSPS through the I²C bus)
12-Bit	49 × 294ns + 148 × 555ns = 96.6µs (10.35kSPS through the I²C bus)

As an example, use V_{DD} = 1.6V and 12-bit mode with the Fast-mode I²C clock (f_{SCL} = 400kHz). The equivalent TSC throughput is at least seven times faster than the effective throughput across the bus (4.88k x 7 = 34.19kSPS). The supply current to the TSC for this rate and configuration is 145µA. To achieve an equivalent sample throughput of 8.2kSPS using the device without preprocessing, the TSC2017 consumes only (8.2/34.19) × 145µA = 34.7µA.

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Table 6. Effective and Equivalent Throughput Rates

SUPPLY VOLTAGE	I^2C BUS SPEED (f_{SCL})	RESOLUTION	TSC CONVERSION CYCLE TIME (µs)	EFFECTIVE THROUGHPUT (kSPS)	EQUIVALENT THROUGHPUT (kSPS)	NO. OF SCL	NO. OF CCLK	f_{CCLK} (kHz)	CCLK PERIODS (ns)
2.7V	100kHz Standard	8-bit	433.6	2.31	16.14	40	127	3780	264.6
		12-bit	568.7	1.76	12.31	49	148	1880	531.9
	400kHz Fast	8-bit	133.6	7.49	52.40	40	127	3780	264.6
		12-bit	201.2	4.97	34.79	49	148	1880	531.9
	1.7MHz High-Speed	8-bit	57.1	17.50	122.53	40	127	3780	264.6
		12-bit	107.5	9.30	65.09	49	148	1880	531.9
	3.4MHz High-Speed	8-bit	45.4	22.04	154.31	40	127	3780	264.6
		12-bit	93.1	10.74	75.16	49	148	1880	531.9
1.8V	100kHz Standard	8-bit	434.7	2.30	16.10	40	127	3660	273.2
		12-bit	570.9	1.75	12.26	49	148	1830	546.4
	400kHz Fast	8-bit	134.7	7.42	51.97	40	127	3660	273.2
		12-bit	203.4	4.92	34.42	49	148	1830	546.4
	1.7MHz High-Speed	8-bit	58.2	17.17	120.22	40	127	3660	273.2
		12-bit	109.7	9.12	63.81	49	148	1830	546.4
	3.4MHz High-Speed	8-bit	46.5	21.52	150.65	40	127	3660	273.2
		12-bit	95.3	10.49	73.46	49	148	1830	546.4
1.6V	100kHz Standard	8-bit	435.2	2.30	16.09	40	127	3610	277.0
		12-bit	572.2	1.75	12.23	49	148	1800	555.5
	400kHz Fast	8-bit	135.2	7.40	51.78	40	127	3610	277.0
		12-bit	204.7	4.88	34.19	49	148	1800	555.5
	1.7MHz High-Speed	8-bit	58.7	17.03	119.23	40	127	3610	277.0
		12-bit	111.0	9.01	63.04	49	148	1800	555.5
	3.4MHz High-Speed	8-bit	46.9	21.30	149.11	40	127	3610	277.0
		12-bit	96.6	10.35	72.44	49	148	1800	555.5

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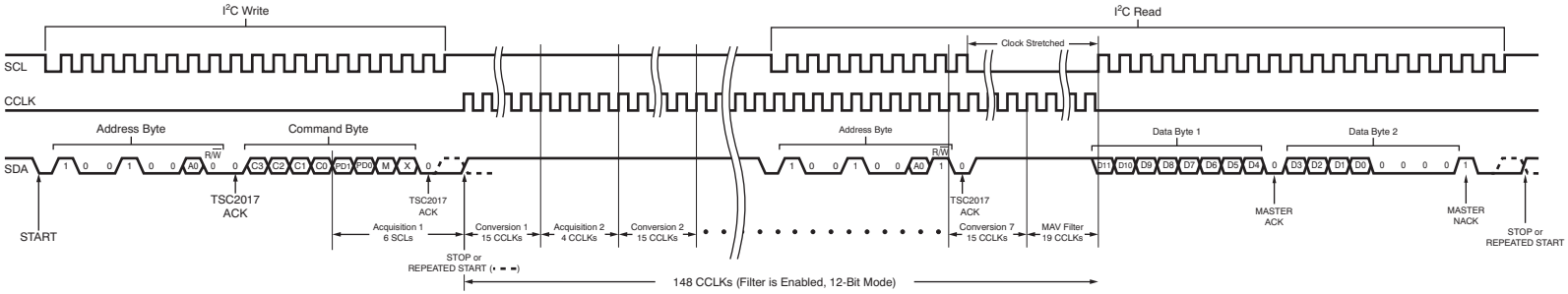

Figure 33. Data Acquisition Cycle (Filter Enabled)

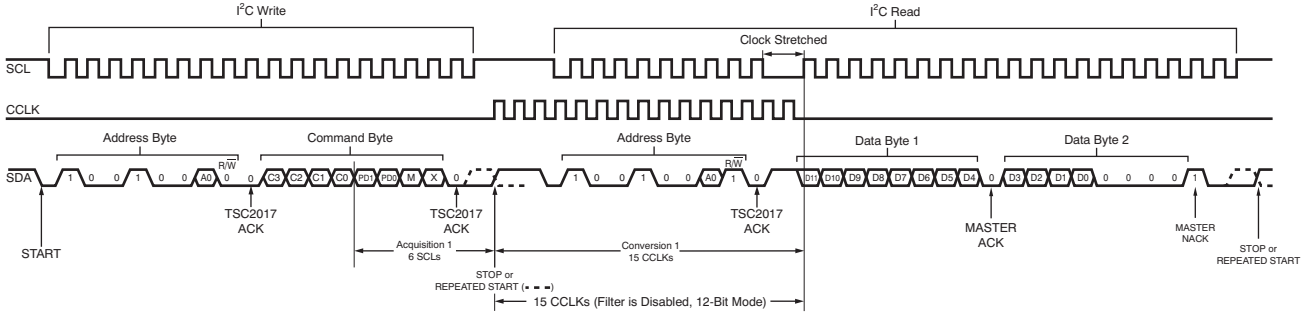

Figure 34. Data Acquisition Cycle (Filter Disabled)

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RESET FUNCTION

The reset function is controlled by the SureSet™ control logic (SSC). There are three methods to reset the device: hardware reset, software reset, and power-on reset (POR).

Hardware Reset

Hardware system reset can be performed using the $\overline{\text{RESET}}$ pin. After hardware reset, the device returns to the default configuration and all the settings in the control byte are reset to the default values (see Table 2 and Table 4). To ensure proper reset, the reset pulse width must have a duration of greater than 200ns. Note that a pulse width of less than 200ns will have unexpected results. See Figure 35 for the external reset timing diagram.

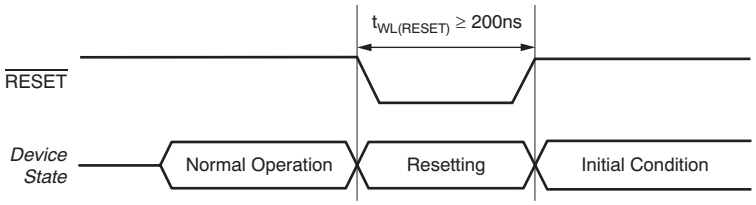

Figure 35. External Reset Timing

Software Reset

The TSC2017 has a software reset that can be issued by loading the Setup comand with '1011 01xx' via I²C, as shown in Figure 36. After software reset, the device returns to the default configuration and all the settings in the control byte are reset to the default values (see Table 2 and Table 4).

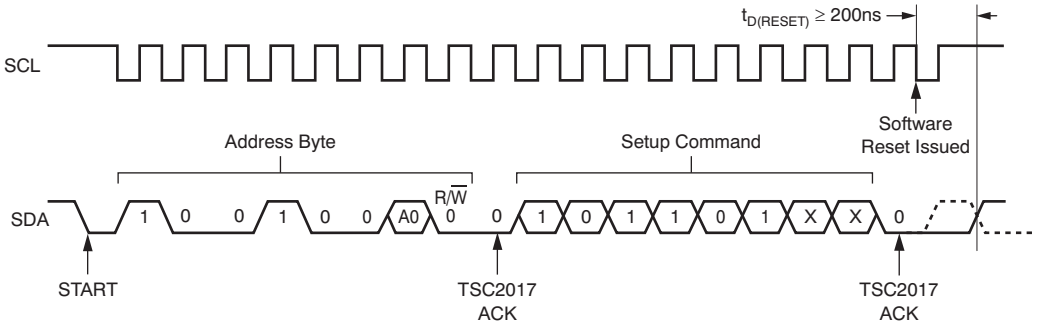

Figure 36. Software Reset Timing

Power-On Reset

During TSC2017 power-up, an internal POR is automatically implemented. The POR brings the TSC to the default working condition. The TSC2017 senses the power-up curve and decides whether or not to implement a POR. Follow the power-on/off slope and interval requirements, as provided in the Electrical Characteristics, in order to ensure a proper POR of the TSC2017.

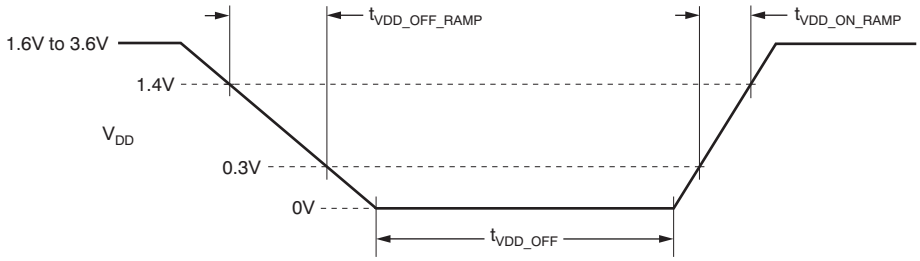

Figure 37. Power-On Reset Timing

Table 7. Timing Requirements for Figure 37

PARAMETER	TEST CONDITIONS	MIN	MAX	UNIT
V_{DD} off ramp	T_A = –40°C to +85°C	50	1,000,000	V/s
V_{DD} off time	T_A = –40°C to +85°C, V_{DD} ≤ 0.4V	20		µs
V_{DD} on ramp	T_A = –40°C to +85°C	90	1,000,000	V/s

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LAYOUT

The following layout suggestions should obtain optimum performance from the TSC2017. Keep in mind that many portable applications have conflicting requirements for power, cost, size, and weight. In general, most portable devices have fairly clean power and grounds because most of the internal components are very low power. This situation would mean less bypassing for the converter power and less concern regarding grounding. However, each situation is unique and the following suggestions should be reviewed carefully.

For optimum performance, care should be taken with the physical layout of the TSC2017 circuitry. The basic SAR architecture is sensitive to glitches or sudden changes on the power supply, reference, ground connections, and digital inputs that occur immediately before latching the output of the analog comparator. Therefore, during any single conversion for an *n*-bit SAR converter, there are *n* windows in which large external transient voltages can easily affect the conversion result. Such glitches might originate from switching power supplies, nearby digital logic, and high power devices. The degree of error in the digital output depends on the reference voltage, layout, and the exact timing of the external event. The error can change if the external event changes in time with respect to the SCL input.

With this consideration in mind, power to the TSC2017 should be clean and well-bypassed. A 0.1µF ceramic bypass capacitor should be placed as close to the device as possible. In addition, a 1µF to 10µF capacitor may also be needed if the impedance of the connection between VDD/REF and the power supply is high.

A bypass capacitor is generally not needed on the VDD/REF pin because the internal reference is buffered by an internal op amp. If an external reference voltage originates from an op amp, make sure that it can drive any bypass capacitor that is used without oscillation.

The TSC2017 architecture offers no inherent rejection of noise or voltage variation with regard to using an external reference input, which is of particular concern when the reference input is tied to the power supply. Any noise and ripple from the supply appears directly in the digital results. While high-frequency noise can be filtered out, voltage variation because of line frequency (50Hz or 60Hz) can be difficult to remove. Some package options have pins labeled as VOID. Avoid any active trace going under any pin marked as VOID unless it is shielded by a ground or power plane.

The GND pin should be connected to a clean ground point. In many cases, this point is the analog ground. Avoid connections that are too near the grounding point of a microcontroller or digital signal processor. If needed, run a ground trace directly from the converter to the power-supply entry or battery connection point. The ideal layout includes an analog ground plane dedicated to the converter and associated analog circuitry.

In the specific case of use with a resistive touch screen, care should be taken with the connection between the converter and the touch screen. Resistive touch screens have fairly low resistance; therefore, the interconnection should be as short and robust as possible. Loose connections can be a source of error when the contact resistance changes with flexing or vibrations.

As indicated previously, noise can be a major source of error in touch-screen applications (for example, applications that require a back-lit LCD panel). This electromagnetic interfence (EMI) noise can be coupled through the LCD panel to the touch screen and cause flickering of the converted A/D converter data. Several things can be done to reduce this error, such as using a touch screen with a bottom-side metal layer connected to ground, which couples the majority of noise to ground. Additionally, filtering capacitors, from Y+, Y–, X+, and X– to ground, can also help. Note, however, that the use of these capacitors increases screen settling time and requires a longer time for panel voltages to stabilize. The resistor value varies depending on the touch screen sensor used. The $\overline{\text{PENIRQ}}$ pull-up resistor (R_{IRQ}) may be adequate for most of sensors.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TSC2017IYZGR	ACTIVE	DSBGA	YZG	12	3000	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 85	TSC2017I	Samples
TSC2017IYZGT	ACTIVE	DSBGA	YZG	12	250	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 85	TSC2017I	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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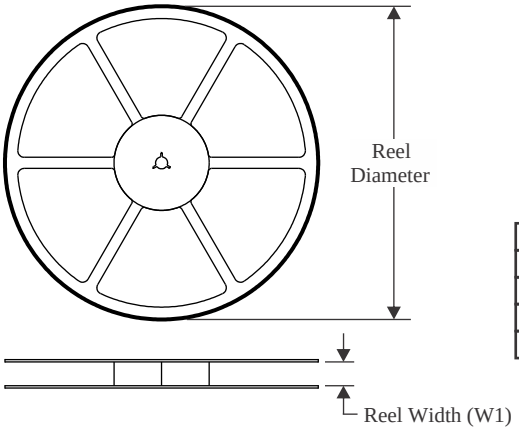
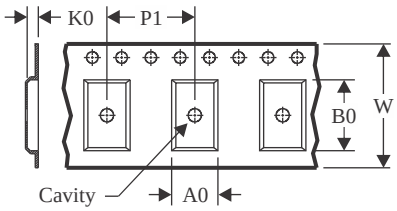
TAPE AND REEL INFORMATION

REEL DIMENSIONS

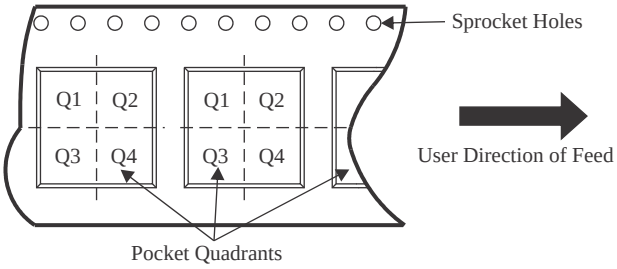


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

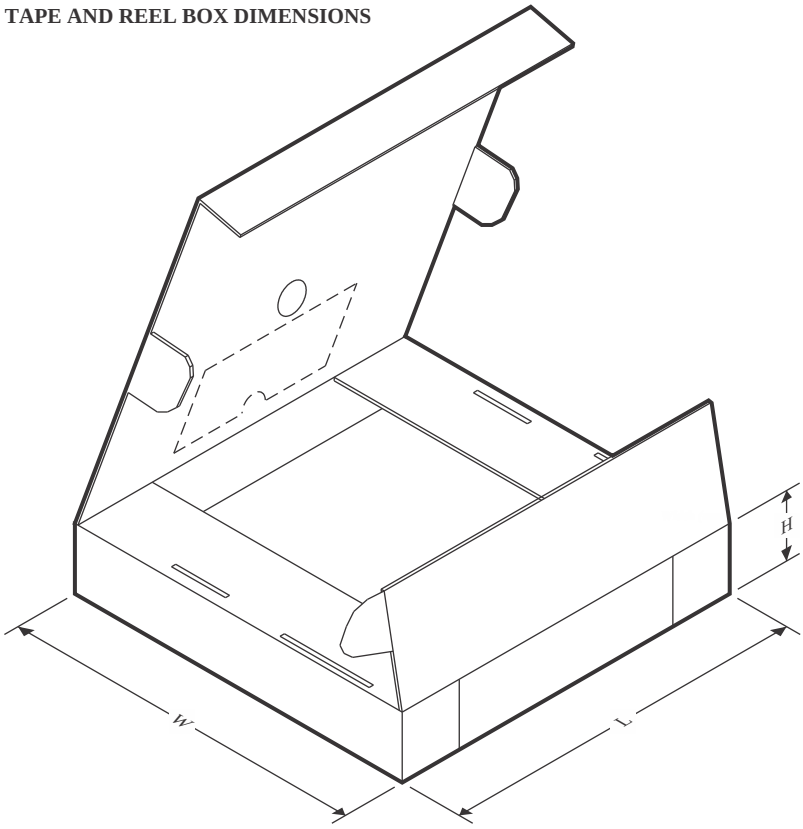
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TSC2017IYZGR	DSBGA	YZG	12	3000	180.0	8.4	1.75	2.25	0.81	4.0	8.0	Q1
TSC2017IYZGT	DSBGA	YZG	12	250	180.0	8.4	1.75	2.25	0.81	4.0	8.0	Q1

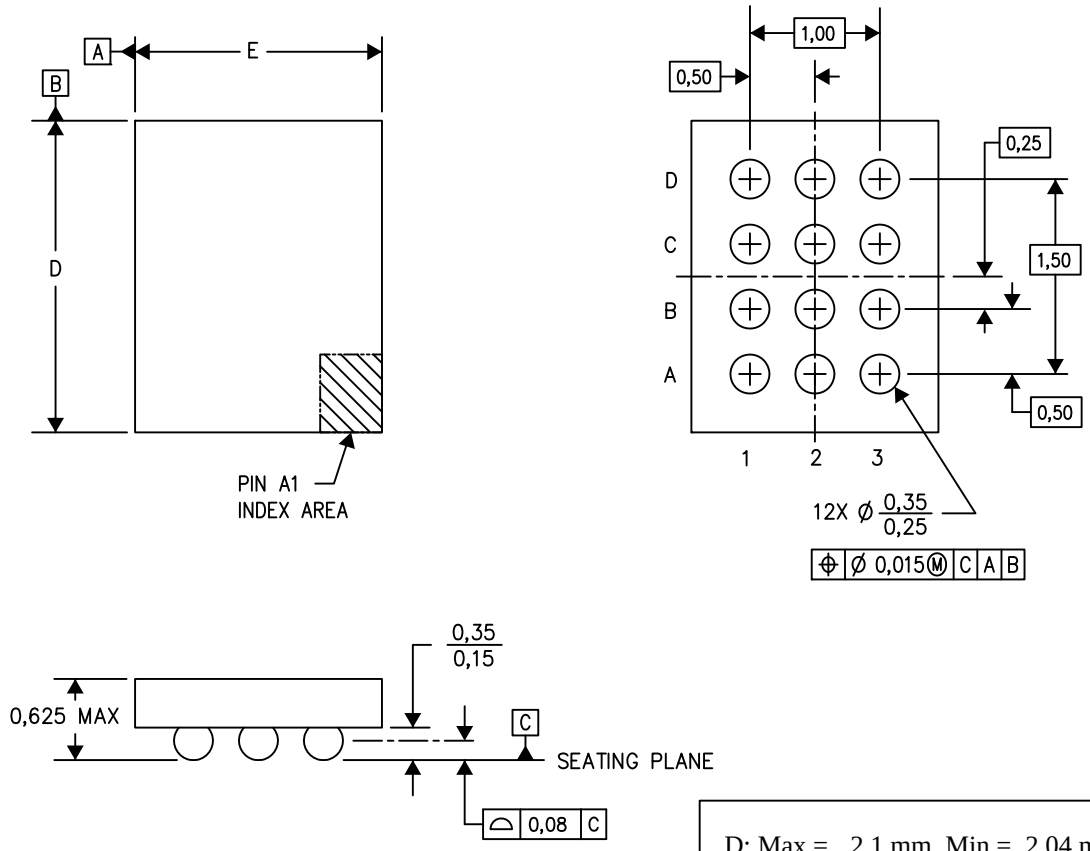
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TSC2017IYZGR	DSBGA	YZG	12	3000	182.0	182.0	20.0
TSC2017IYZGT	DSBGA	YZG	12	250	182.0	182.0	20.0

YZG (R-XBGA-N12) DIE-SIZE BALL GRID ARRAY



D: Max = 2.1 mm, Min = 2.04 mm

E: Max = 1.6 mm, Min = 1.539 mm

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NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
B. This drawing is subject to change without notice.
C. NanoFree™ package configuration.

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