1 Features

- Qualified for Automotive Applications
- AEC-Q100 Qualified With the Following Results
  - Device Temperature Grade 1: –40°C to +125°C Ambient Operating Temperature Range
  - 1.2 V to 3.6 V on A Port and 1.65 V to 5.5 V on B Port (\(V_{CCA} \leq V_{CCB}\))
- \(V_{CC}\) Isolation Feature – If Either \(V_{CC}\) Input is at GND, All Outputs are in the High-Impedance State
- OE Input Circuit Referenced to \(V_{CCA}\)
- \(I_{off}\) Supports Partial-Power-Down Mode Operation
- ESD Protection Exceeds JESD 22
  - A port
    - ±2500-V Human-Body Model (A114-B)
    - ±1000-V Charged-Device Model (C101)
  - B port
    - ±1500-V Human-Body Model (A114-B)
    - ±1000-V Charged-Device Model (C101)

2 Applications

- Automotive infotainment
- Advanced Driver Assistance System (ADAS)
- Telematics

3 Description

Voltage-level translators address the challenges posed by simultaneous use of different supply-voltage levels on the same circuit board. This 4-bit non-inverting translator uses two separate configurable power-supply rails. The A port is designed to track \(V_{CCA}\). \(V_{CCA}\) accepts any supply voltage from 1.2 V to 3.6 V. The B port is designed to track \(V_{CCB}\). \(V_{CCB}\) accepts any supply voltage from 1.65 V to 5.5 V. This allows for universal low-voltage bidirectional translation between any of the 1.2-V, 1.5-V, 1.8-V, 2.5-V, 3.3-V, and 5-V voltage nodes. \(V_{CCA}\) should not exceed \(V_{CCB}\).

When the output-enable (OE) input is low, all outputs are placed in the high-impedance state. To ensure the high-impedance state during power up or power down, OE should be tied to GND through a pulldown resistor; the minimum value of the resistor is determined by the current-sourcing capability of the driver.

The TXB0104 is designed so that the OE input circuit is supplied by \(V_{CCA}\).

This device is fully specified for partial-power-down applications using \(I_{off}\). The \(I_{off}\) circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

### Device Information\(^{(1)}\)

<table>
<thead>
<tr>
<th>PART NUMBER</th>
<th>PACKAGE</th>
<th>BODY SIZE (NOM)</th>
</tr>
</thead>
<tbody>
<tr>
<td>TXB0104-Q1</td>
<td>TSSOP (14)</td>
<td>5.00 mm x 4.40 mm</td>
</tr>
<tr>
<td></td>
<td>VQFN (14)</td>
<td>3.50 mm x 3.50 mm</td>
</tr>
<tr>
<td></td>
<td>UQFN (12)</td>
<td>2.00 mm x 1.70 mm</td>
</tr>
</tbody>
</table>

\(^{(1)}\) For all available packages, see the orderable addendum at the end of the datasheet.

![Typical Application Block Diagram for TXB010X](image-url)
# Table of Contents

1 Features .......................................................... 1
2 Applications ...................................................... 1
3 Description ....................................................... 1
4 Revision History .................................................. 2
5 Pin Configuration and Functions .............................. 3
6 Specifications ..................................................... 4
   6.1 Absolute Maximum Ratings ................................. 4
   6.2 ESD Ratings .................................................. 4
   6.3 Recommended Operating Conditions ..................... 4
   6.4 Thermal Information ......................................... 5
   6.5 Electrical Characteristics ................................. 5
   6.6 Timing Requirements: $V_{CCA} = 1.2\, \text{V}$ ....... 6
   6.7 Timing Requirements: $V_{CCA} = 1.5\, \text{V} \pm 0.1\, \text{V}$ ..... 6
   6.8 Timing Requirements: $V_{CCA} = 1.8\, \text{V} \pm 0.15\, \text{V}$ ..... 6
   6.9 Timing Requirements: $V_{CCA} = 2.5\, \text{V} \pm 0.2\, \text{V}$ ..... 6
   6.10 Timing Requirements: $V_{CCA} = 3.3\, \text{V} \pm 0.3\, \text{V}$ ..... 6
   6.11 Switching Characteristics: $V_{CCA} = 1.2\, \text{V}$ ........ 7
   6.12 Switching Characteristics: $V_{CCA} = 1.5\, \text{V} \pm 0.1\, \text{V}$ .... 7
   6.13 Switching Characteristics: $V_{CCA} = 1.8\, \text{V} \pm 0.15\, \text{V}$ .. 7
   6.14 Switching Characteristics: $V_{CCA} = 2.5\, \text{V} \pm 0.2\, \text{V}$ .... 8
   6.15 Switching Characteristics: $V_{CCA} = 3.3\, \text{V} \pm 0.3\, \text{V}$ .... 8
6.16 Operating Characteristics ................................. 9
6.17 Typical Characteristics ..................................... 9
7 Parameter Measurement Information ...................... 10
8 Detailed Description .......................................... 11
   8.1 Overview .................................................... 11
   8.2 Functional Block Diagram ................................ 11
   8.3 Feature Description ....................................... 11
   8.4 Device Functional Modes ................................. 13
9 Application and Implementation ............................. 14
   9.1 Application Information ................................. 14
   9.2 Typical Application ....................................... 14
10 Power Supply Recommendations ............................ 16
11 Layout ............................................................ 16
   11.1 Layout Guidelines ........................................ 16
   11.2 Layout Example .......................................... 16
12 Device and Documentation Support .......................... 17
   12.1 Trademarks ................................................ 17
   12.2 Electrostatic Discharge Caution ......................... 17
   12.3 Glossary .................................................. 17
13 Mechanical, Packaging, and Orderable Information ....... 17

## 4 Revision History

Changes from Original (June 2008) to Revision A

- Added ESD Ratings table, Feature Description section, Device Functional Modes, Application and Implementation section, Power Supply Recommendations section, Layout section, Device and Documentation Support section, and Mechanical, Packaging, and Orderable Information section.
## 5 Pin Configuration and Functions

### Pin Functions

<table>
<thead>
<tr>
<th>PIN</th>
<th>I/O</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>NO.</td>
<td>NAME</td>
<td>DESCRIPTION</td>
</tr>
<tr>
<td>1</td>
<td>VCCA</td>
<td>I-port supply voltage (1.2 \text{ V} \leq V_{\text{CCA}} \leq 3.6 \text{ V}) and (V_{\text{CCA}} \leq V_{\text{CCB}}).</td>
</tr>
<tr>
<td>2</td>
<td>A1</td>
<td>I/O Input/output 1. Referenced to (V_{\text{CCA}}).</td>
</tr>
<tr>
<td>3</td>
<td>A2</td>
<td>I/O Input/output 2. Referenced to (V_{\text{CCA}}).</td>
</tr>
<tr>
<td>4</td>
<td>A3</td>
<td>I/O Input/output 3. Referenced to (V_{\text{CCA}}).</td>
</tr>
<tr>
<td>5</td>
<td>A4</td>
<td>I/O Input/output 4. Referenced to (V_{\text{CCA}}).</td>
</tr>
<tr>
<td>6</td>
<td>NC</td>
<td>– No connection. Not internally connected.</td>
</tr>
<tr>
<td>7</td>
<td>GND</td>
<td>– Ground</td>
</tr>
<tr>
<td>8</td>
<td>OE</td>
<td>I 3-state output-mode enable. Pull OE low to place all outputs in 3-state mode. Referenced to (V_{\text{CCA}}).</td>
</tr>
<tr>
<td>9</td>
<td>NC</td>
<td>– No connection. Not internally connected.</td>
</tr>
<tr>
<td>10</td>
<td>B4</td>
<td>I/O Input/output 4. Referenced to (V_{\text{CCB}}).</td>
</tr>
<tr>
<td>11</td>
<td>B3</td>
<td>I/O Input/output 3. Referenced to (V_{\text{CCB}}).</td>
</tr>
<tr>
<td>12</td>
<td>B2</td>
<td>I/O Input/output 2. Referenced to (V_{\text{CCB}}).</td>
</tr>
<tr>
<td>13</td>
<td>B1</td>
<td>I/O Input/output 1. Referenced to (V_{\text{CCB}}).</td>
</tr>
<tr>
<td>14</td>
<td>VCCB</td>
<td>I B-port supply voltage (1.65 \text{ V} \leq V_{\text{CCB}} \leq 5.5 \text{ V}).</td>
</tr>
</tbody>
</table>

NC – No internal connection

For RGY, if the exposed center pad is used, it must be connected only to as a secondary ground or left electrically open.

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Product Folder Links: TXB0104-Q1
6 Specifications

6.1 Absolute Maximum Ratings (1)
over operating free-air temperature range (unless otherwise noted)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>MIN</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>VCCA</td>
<td>–0.5</td>
<td>4.6</td>
<td>V</td>
</tr>
<tr>
<td>VCCB</td>
<td>–0.5</td>
<td>6.5</td>
<td>V</td>
</tr>
<tr>
<td>VI</td>
<td>–0.5</td>
<td>4.6</td>
<td>V</td>
</tr>
<tr>
<td>VO</td>
<td>–0.5</td>
<td>6.5</td>
<td>V</td>
</tr>
<tr>
<td>VO (2)</td>
<td>–0.5</td>
<td>VCCA + 0.5</td>
<td>V</td>
</tr>
<tr>
<td>ik</td>
<td>V&lt;0</td>
<td>–50</td>
<td>mA</td>
</tr>
<tr>
<td>IO</td>
<td>V&lt;0</td>
<td>–50</td>
<td>mA</td>
</tr>
<tr>
<td>IOK</td>
<td>±50</td>
<td>mA</td>
<td></td>
</tr>
<tr>
<td>IO (2)</td>
<td>±100</td>
<td>mA</td>
<td></td>
</tr>
<tr>
<td>Tstg</td>
<td>–65</td>
<td>150</td>
<td>°C</td>
</tr>
</tbody>
</table>

(1) Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) The value of VCCA and VCCB are provided in the recommended operating conditions table.

6.2 ESD Ratings

<table>
<thead>
<tr>
<th>V(ESD)</th>
<th>Electrostatic discharge</th>
<th>VALUE</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Human-body model (HBM), per JEDEC</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>A Port</td>
<td>±2500</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td>B Port</td>
<td>±1500</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td>Charged-device model (CDM), per JEDEC</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>A Port</td>
<td>±100</td>
<td></td>
</tr>
<tr>
<td></td>
<td>B Port</td>
<td>±100</td>
<td></td>
</tr>
</tbody>
</table>

6.3 Recommended Operating Conditions (1)(2)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>VCCA</th>
<th>VCCB</th>
<th>MIN</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>VIH</td>
<td>1.2</td>
<td>3.6</td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>VIL</td>
<td>1.65</td>
<td>5.5</td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>VI</td>
<td>1.2 V to 3.6 V</td>
<td>1.65 V to 5.5 V</td>
<td>VCCA × 0.65 (3)</td>
<td>VCCA</td>
<td>V</td>
</tr>
<tr>
<td>VI OE</td>
<td>1.2 V to 3.6 V</td>
<td>1.65 V to 5.5 V</td>
<td>VCCA × 0.65 (3)</td>
<td>VCCA</td>
<td>V</td>
</tr>
<tr>
<td>VO</td>
<td>0 V</td>
<td>VCCA × 0.35 (3)</td>
<td>VCCA × 0.35 (3)</td>
<td>VCCA</td>
<td>V</td>
</tr>
<tr>
<td>VO A-port</td>
<td>1.2 V to 3.6 V</td>
<td>1.65 V to 5.5 V</td>
<td>0</td>
<td>3.6</td>
<td>V</td>
</tr>
<tr>
<td>VO B-port</td>
<td>1.2 V to 3.6 V</td>
<td>1.65 V to 5.5 V</td>
<td>0</td>
<td>5.5</td>
<td>V</td>
</tr>
<tr>
<td>ΔV/Δv</td>
<td>1.2 V to 3.6 V</td>
<td>1.65 V to 5.5 V</td>
<td>40</td>
<td>ns/V</td>
<td></td>
</tr>
<tr>
<td>TA</td>
<td>–40</td>
<td>125</td>
<td>°C</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

(1) The A and B sides of an unused data I/O pair must be held in the same state, i.e., both at VCCI or both at GND.
(2) VCCA must be less than or equal to VCCB and must not exceed 3.6 V.
(3) VCCI is the supply voltage associated with the input port.
### 6.4 Thermal Information

<table>
<thead>
<tr>
<th>THERMAL METRIC(1)</th>
<th>TXB0104-Q1</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>PW</td>
<td>RGY</td>
</tr>
<tr>
<td>(R_{\text{JA}})</td>
<td>Junction-to-ambient thermal resistance</td>
<td>121</td>
</tr>
<tr>
<td>(R_{\text{JC(top)}})</td>
<td>Junction-to-case (top) thermal resistance</td>
<td>50</td>
</tr>
<tr>
<td>(R_{\text{JB}})</td>
<td>Junction-to-board thermal resistance</td>
<td>62.8</td>
</tr>
<tr>
<td>(\psi_{\text{JT}})</td>
<td>Junction-to-top characterization parameter</td>
<td>6.4</td>
</tr>
<tr>
<td>(\psi_{\text{JB}})</td>
<td>Junction-to-board characterization parameter</td>
<td>62.2</td>
</tr>
<tr>
<td>(R_{\text{JC(bot)}})</td>
<td>Junction-to-case (bottom) thermal resistance</td>
<td>N/A</td>
</tr>
</tbody>
</table>

(1) For more information about traditional and new thermal metrics, see the IC Package Thermal Metrics application report, SPRA953.

### 6.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted) (1)(2)

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>(V_{\text{CCA}})</th>
<th>(V_{\text{CCB}})</th>
<th>(T_{\text{A}} = 25^\circ\text{C})</th>
<th>(-40^\circ\text{C} \text{ to } 125^\circ\text{C})</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>MIN</td>
<td>TYP</td>
<td>MAX</td>
<td>MIN</td>
</tr>
<tr>
<td>(V_{\text{OHA}})</td>
<td>(I_{\text{OH}} = -20 \mu \text{A})</td>
<td>1.2 V</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>1.4 V to 3.6 V</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>(V_{\text{OLA}})</td>
<td>(I_{\text{OL}} = 20 \mu \text{A})</td>
<td>1.2 V</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>1.4 V to 3.6 V</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>(V_{\text{OHB}})</td>
<td>(I_{\text{OH}} = -20 \mu \text{A})</td>
<td>1.65 V to 5.5 V</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>1.4 V to 3.6 V</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>(I_{\text{I}})</td>
<td>(OE)</td>
<td>(V_{I} = V_{\text{CCI}}) or GND</td>
<td>1.2 V to 3.6 V</td>
<td></td>
<td></td>
</tr>
<tr>
<td>(I_{\text{off}})</td>
<td>(A) port</td>
<td>(V_{I} = V_{O} = 0) to 3.6 V</td>
<td>0 V</td>
<td>0 V to 5.5 V</td>
<td></td>
</tr>
<tr>
<td></td>
<td>(B) port</td>
<td>(V_{I} = V_{O} = 0) to 5.5 V</td>
<td>0 V</td>
<td>0 V to 3.6 V</td>
<td></td>
</tr>
<tr>
<td>(I_{\text{OZ}})</td>
<td>(A) or (B) port</td>
<td>(OE = \text{GND})</td>
<td>1.2 V to 3.6 V</td>
<td>1.65 V to 5.5 V</td>
<td>±1</td>
</tr>
<tr>
<td>(I_{\text{CCA}})</td>
<td>(V_{I} = V_{\text{CCI}}) or GND, (I_{O} = 0)</td>
<td>1.2 V</td>
<td>1.65 V to 5.5 V</td>
<td>0.06</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>3.6 V</td>
<td>0 V</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>0 V</td>
<td>5.5 V</td>
<td></td>
<td></td>
</tr>
<tr>
<td>(I_{\text{CCB}})</td>
<td>(V_{I} = V_{\text{CCI}}) or GND, (I_{O} = 0)</td>
<td>1.2 V</td>
<td>1.65 V to 5.5 V</td>
<td>3.4</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>3.6 V</td>
<td>0 V</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>0 V</td>
<td>5.5 V</td>
<td></td>
<td></td>
</tr>
<tr>
<td>(I_{\text{CCA}} + I_{\text{CCB}})</td>
<td>(V_{I} = V_{\text{CCI}}) or GND, (I_{O} = 0)</td>
<td>1.2 V</td>
<td>1.65 V to 5.5 V</td>
<td>3.5</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>1.4 V to 3.6 V</td>
<td>1.65 V to 5.5 V</td>
<td>40</td>
<td></td>
</tr>
<tr>
<td>(I_{\text{CCZA}})</td>
<td>(V_{I} = V_{\text{CCI}}) or GND, (I_{O} = 0, OE = \text{GND})</td>
<td>1.2 V</td>
<td>1.65 V to 5.5 V</td>
<td>0.05</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>1.4 V to 3.6 V</td>
<td>1.65 V to 5.5 V</td>
<td>15</td>
<td></td>
</tr>
<tr>
<td>(I_{\text{CCZB}})</td>
<td>(V_{I} = V_{\text{CCI}}) or GND, (I_{O} = 0, OE = \text{GND})</td>
<td>1.2 V</td>
<td>1.65 V to 5.5 V</td>
<td>3.3</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>1.4 V to 3.6 V</td>
<td>1.65 V to 5.5 V</td>
<td>15</td>
<td></td>
</tr>
<tr>
<td>(C_{i})</td>
<td>(OE)</td>
<td>PW, RGY package</td>
<td>1.2 V to 3.6 V</td>
<td>1.65 V to 5.5 V</td>
<td>3</td>
</tr>
<tr>
<td></td>
<td></td>
<td>RUT package</td>
<td>1.2 V to 3.6 V</td>
<td>1.65 V to 5.5 V</td>
<td>4</td>
</tr>
<tr>
<td>(C_{o})</td>
<td>A port</td>
<td>PW, RGY package</td>
<td>1.2 V to 3.6 V</td>
<td>1.65 V to 5.5 V</td>
<td>5</td>
</tr>
<tr>
<td></td>
<td></td>
<td>RUT package</td>
<td>1.2 V to 3.6 V</td>
<td>1.65 V to 5.5 V</td>
<td>6</td>
</tr>
<tr>
<td></td>
<td>B port</td>
<td>PW, RGY package</td>
<td>1.2 V to 3.6 V</td>
<td>1.65 V to 5.5 V</td>
<td>11</td>
</tr>
<tr>
<td></td>
<td></td>
<td>RUT package</td>
<td></td>
<td></td>
<td>13</td>
</tr>
</tbody>
</table>

(1) \(V_{\text{CCI}}\) is the supply voltage associated with the input port.
(2) \(V_{\text{CCO}}\) is the supply voltage associated with the output port.
### 6.6 Timing Requirements: $V_{CCA} = 1.2 \text{ V}$

$T_A = 25^\circ \text{C}, V_{CCA} = 1.2 \text{ V}$

<table>
<thead>
<tr>
<th>UNIT</th>
<th>$V_{CCB} = 1.8 \text{ V}$ ± 0.15 V</th>
<th>$V_{CCB} = 2.5 \text{ V}$ ± 0.2 V</th>
<th>$V_{CCB} = 3.3 \text{ V}$ ± 0.3 V</th>
<th>$V_{CCB} = 5 \text{ V}$ ± 0.5 V</th>
<th>TYP</th>
</tr>
</thead>
<tbody>
<tr>
<td>Data rate</td>
<td>For PW, RGY, RUT package</td>
<td>20</td>
<td>20</td>
<td>20</td>
<td>20</td>
</tr>
<tr>
<td>$t_w$ Pulse duration</td>
<td>Data inputs</td>
<td>50</td>
<td>50</td>
<td>50</td>
<td>50</td>
</tr>
</tbody>
</table>

### 6.7 Timing Requirements: $V_{CCA} = 1.5 \text{ V} ± 0.1 \text{ V}$

over recommended operating free-air temperature range, $V_{CCA} = 1.5 \text{ V} ± 0.1 \text{ V}$ (unless otherwise noted)

<table>
<thead>
<tr>
<th>UNIT</th>
<th>$V_{CCB} = 1.8 \text{ V}$ ± 0.15 V</th>
<th>$V_{CCB} = 2.5 \text{ V}$ ± 0.2 V</th>
<th>$V_{CCB} = 3.3 \text{ V}$ ± 0.3 V</th>
<th>$V_{CCB} = 5 \text{ V}$ ± 0.5 V</th>
<th>TYP</th>
</tr>
</thead>
<tbody>
<tr>
<td>Data rate</td>
<td>For PW, RGY package</td>
<td>40</td>
<td>40</td>
<td>40</td>
<td>40</td>
</tr>
<tr>
<td>$t_w$ Pulse duration</td>
<td>Data inputs, For PW, RGY package</td>
<td>25</td>
<td>25</td>
<td>25</td>
<td>25</td>
</tr>
<tr>
<td>Data inputs, For RUT package</td>
<td>27</td>
<td>27</td>
<td>25</td>
<td>25</td>
<td></td>
</tr>
</tbody>
</table>

### 6.8 Timing Requirements: $V_{CCA} = 1.8 \text{ V} ± 0.15 \text{ V}$

over recommended operating free-air temperature range, $V_{CCA} = 1.8 \text{ V} ± 0.15 \text{ V}$ (unless otherwise noted)

<table>
<thead>
<tr>
<th>UNIT</th>
<th>$V_{CCB} = 1.8 \text{ V}$ ± 0.15 V</th>
<th>$V_{CCB} = 2.5 \text{ V}$ ± 0.2 V</th>
<th>$V_{CCB} = 3.3 \text{ V}$ ± 0.3 V</th>
<th>$V_{CCB} = 5 \text{ V}$ ± 0.5 V</th>
<th>TYP</th>
</tr>
</thead>
<tbody>
<tr>
<td>Data rate</td>
<td>For PW, RGY package</td>
<td>55</td>
<td>55</td>
<td>55</td>
<td>55</td>
</tr>
<tr>
<td>$t_w$ Pulse duration</td>
<td>Data inputs, For PW, RGY package</td>
<td>18</td>
<td>18</td>
<td>18</td>
<td>18</td>
</tr>
<tr>
<td>Data inputs, For RUT package</td>
<td>27</td>
<td>27</td>
<td>18</td>
<td>18</td>
<td></td>
</tr>
</tbody>
</table>

### 6.9 Timing Requirements: $V_{CCA} = 2.5 \text{ V} ± 0.2 \text{ V}$

over recommended operating free-air temperature range, $V_{CCA} = 2.5 \text{ V} ± 0.2 \text{ V}$ (unless otherwise noted)

<table>
<thead>
<tr>
<th>UNIT</th>
<th>$V_{CCB} = 2.5 \text{ V}$ ± 0.2 V</th>
<th>$V_{CCB} = 3.3 \text{ V}$ ± 0.3 V</th>
<th>$V_{CCB} = 5 \text{ V}$ ± 0.5 V</th>
<th>TYP</th>
</tr>
</thead>
<tbody>
<tr>
<td>Data rate</td>
<td>For PW, RGY package</td>
<td>75</td>
<td>80</td>
<td>100</td>
</tr>
<tr>
<td>$t_w$ Pulse duration</td>
<td>Data inputs, For PW, RGY package</td>
<td>13</td>
<td>12</td>
<td>10</td>
</tr>
<tr>
<td>Data inputs, For RUT package</td>
<td>15</td>
<td>12</td>
<td>11</td>
<td>ns</td>
</tr>
</tbody>
</table>

### 6.10 Timing Requirements: $V_{CCA} = 3.3 \text{ V} ± 0.3 \text{ V}$

over recommended operating free-air temperature range, $V_{CCA} = 3.3 \text{ V} ± 0.3 \text{ V}$ (unless otherwise noted)

<table>
<thead>
<tr>
<th>UNIT</th>
<th>$V_{CCB} = 3.3 \text{ V}$ ± 0.3 V</th>
<th>$V_{CCB} = 5 \text{ V}$ ± 0.5 V</th>
<th>TYP</th>
</tr>
</thead>
<tbody>
<tr>
<td>Data rate</td>
<td>For PW, RGY package</td>
<td>100</td>
<td>100</td>
</tr>
<tr>
<td>$t_w$ Pulse duration</td>
<td>Data inputs, For PW, RGY package</td>
<td>10</td>
<td>10</td>
</tr>
<tr>
<td>Data inputs, For RUT package</td>
<td>11</td>
<td>11</td>
<td>ns</td>
</tr>
</tbody>
</table>
### 6.11 Switching Characteristics: \( V_{CCA} = 1.2 \) V

\( T_A = 25^\circ C, \ V_{CCA} = 1.2 \) V

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>FROM (INPUT)</th>
<th>TO (OUTPUT)</th>
<th>( V_{CCB} = 1.8 ) V</th>
<th>( V_{CCB} = 2.5 ) V</th>
<th>( V_{CCB} = 3.3 ) V</th>
<th>( V_{CCB} = 5 ) V</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>( t_{pd} )</td>
<td>A</td>
<td>B</td>
<td>6.9</td>
<td>5.7</td>
<td>5.3</td>
<td>5.5</td>
<td>ns</td>
</tr>
<tr>
<td></td>
<td>B</td>
<td>A</td>
<td>7.4</td>
<td>6.4</td>
<td>6</td>
<td>5.8</td>
<td></td>
</tr>
<tr>
<td>( t_{en} )</td>
<td>OE</td>
<td>A</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>µs</td>
</tr>
<tr>
<td></td>
<td>B</td>
<td>A</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td></td>
</tr>
<tr>
<td>( t_{ds} )</td>
<td>OE</td>
<td>A</td>
<td>320</td>
<td>320</td>
<td>320</td>
<td>330</td>
<td>ns</td>
</tr>
<tr>
<td></td>
<td>B</td>
<td>A</td>
<td>150</td>
<td>110</td>
<td>150</td>
<td>110</td>
<td></td>
</tr>
<tr>
<td>( t_{A} ), ( t_{U} )</td>
<td>A-port rise and fall times</td>
<td>4.2</td>
<td>4.2</td>
<td>4.2</td>
<td>4.2</td>
<td>4.2</td>
<td>ns</td>
</tr>
<tr>
<td>( t_{B} ), ( t_{G} )</td>
<td>B-port rise and fall times</td>
<td>2.1</td>
<td>1.5</td>
<td>1.2</td>
<td>1.1</td>
<td>1.1</td>
<td>ns</td>
</tr>
</tbody>
</table>

### 6.12 Switching Characteristics: \( V_{CCA} = 1.5 \) V ± 0.1 V

over recommended operating free-air temperature range, \( V_{CCA} = 1.5 \) V ± 0.1 V (unless otherwise noted)

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>FROM (INPUT)</th>
<th>TO (OUTPUT)</th>
<th>( V_{CCB} = 1.8 ) V ± 0.15 V</th>
<th>( V_{CCB} = 2.5 ) V ± 0.2 V</th>
<th>( V_{CCB} = 3.3 ) V ± 0.3 V</th>
<th>( V_{CCB} = 5 ) V ± 0.5 V</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>( t_{pd} )</td>
<td>A</td>
<td>B</td>
<td>MIN 15.9</td>
<td>MAX 13.1</td>
<td>MIN 13</td>
<td>MAX 12.9</td>
<td>ns</td>
</tr>
<tr>
<td></td>
<td>B</td>
<td>A</td>
<td>MIN 17.2</td>
<td>MAX 15.2</td>
<td>MIN 15.3</td>
<td>MAX 16.7</td>
<td></td>
</tr>
<tr>
<td>( t_{en} )</td>
<td>OE</td>
<td>A</td>
<td>MIN 1</td>
<td>MAX 1</td>
<td>MIN 1</td>
<td>MAX 1</td>
<td>µs</td>
</tr>
<tr>
<td></td>
<td>B</td>
<td>A</td>
<td>MIN 1</td>
<td>MAX 1</td>
<td>MIN 1</td>
<td>MAX 1</td>
<td></td>
</tr>
<tr>
<td>( t_{ds} )</td>
<td>OE</td>
<td>A</td>
<td>MIN 340</td>
<td>MAX 280</td>
<td>MIN 280</td>
<td>MAX 300</td>
<td>ns</td>
</tr>
<tr>
<td></td>
<td>B</td>
<td>A</td>
<td>MIN 220</td>
<td>MAX 220</td>
<td>MIN 220</td>
<td>MAX 220</td>
<td></td>
</tr>
<tr>
<td>( t_{A} ), ( t_{U} )</td>
<td>A-port rise and fall times</td>
<td>MIN 7.1</td>
<td>MAX 7.1</td>
<td>MIN 7.1</td>
<td>MAX 7.1</td>
<td>MIN 7.1</td>
<td>ns</td>
</tr>
<tr>
<td>( t_{B} ), ( t_{G} )</td>
<td>B-port rise and fall times</td>
<td>MIN 6.5</td>
<td>MAX 5.2</td>
<td>MIN 4.8</td>
<td>MAX 4.7</td>
<td>MIN 4.7</td>
<td>ns</td>
</tr>
</tbody>
</table>

### 6.13 Switching Characteristics: \( V_{CCA} = 1.8 \) V ± 0.15 V

over recommended operating free-air temperature range, \( V_{CCA} = 1.8 \) V ± 0.15 V (unless otherwise noted)

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>FROM (INPUT)</th>
<th>TO (OUTPUT)</th>
<th>( V_{CCB} = 1.8 ) V ± 0.15 V</th>
<th>( V_{CCB} = 2.5 ) V ± 0.2 V</th>
<th>( V_{CCB} = 3.3 ) V ± 0.3 V</th>
<th>( V_{CCB} = 5 ) V ± 0.5 V</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>( t_{pd} )</td>
<td>A</td>
<td>B</td>
<td>MIN 14</td>
<td>MAX 10.7</td>
<td>MIN 9.8</td>
<td>MAX 9.5</td>
<td>ns</td>
</tr>
<tr>
<td></td>
<td>B</td>
<td>A</td>
<td>MIN 15</td>
<td>MAX 11.4</td>
<td>MIN 10.6</td>
<td>MAX 10.1</td>
<td></td>
</tr>
<tr>
<td>( t_{en} )</td>
<td>OE</td>
<td>A</td>
<td>MIN 1</td>
<td>MAX 1</td>
<td>MIN 1</td>
<td>MAX 1</td>
<td>µs</td>
</tr>
<tr>
<td></td>
<td>B</td>
<td>A</td>
<td>MIN 1</td>
<td>MAX 1</td>
<td>MIN 1</td>
<td>MAX 1</td>
<td></td>
</tr>
<tr>
<td>( t_{ds} )</td>
<td>OE</td>
<td>A</td>
<td>MIN 280</td>
<td>MAX 250</td>
<td>MIN 250</td>
<td>MAX 250</td>
<td>ns</td>
</tr>
<tr>
<td></td>
<td>B</td>
<td>A</td>
<td>MIN 220</td>
<td>MAX 220</td>
<td>MIN 220</td>
<td>MAX 220</td>
<td></td>
</tr>
<tr>
<td>( t_{A} ), ( t_{U} )</td>
<td>A-port rise and fall times</td>
<td>MIN 6.2</td>
<td>MAX 6.1</td>
<td>MIN 6.1</td>
<td>MAX 6.1</td>
<td>MIN 6.1</td>
<td>ns</td>
</tr>
<tr>
<td>( t_{B} ), ( t_{G} )</td>
<td>B-port rise and fall times</td>
<td>MIN 5.8</td>
<td>MAX 5.2</td>
<td>MIN 4.8</td>
<td>MAX 4.7</td>
<td>MIN 4.7</td>
<td>ns</td>
</tr>
</tbody>
</table>
6.14 Switching Characteristics: $V_{CCA} = 2.5 \, \text{V} \pm 0.2 \, \text{V}$
over recommended operating free-air temperature range, $V_{CCA} = 2.5 \, \text{V} \pm 0.2 \, \text{V}$ (unless otherwise noted)

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>FROM (INPUT)</th>
<th>TO (OUTPUT)</th>
<th>$V_{CCA} = 2.5 , \text{V} \pm 0.2 , \text{V}$</th>
<th>$V_{CCB} = 3.3 , \text{V} \pm 0.3 , \text{V}$</th>
<th>$V_{CCB} = 5 , \text{V} \pm 0.5 , \text{V}$</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td>MIN</td>
<td>MAX</td>
<td>MIN</td>
</tr>
<tr>
<td>$t_{pd}$</td>
<td>A</td>
<td>B</td>
<td>9.3</td>
<td>8.2</td>
<td>7.7</td>
</tr>
<tr>
<td></td>
<td>B</td>
<td>A</td>
<td>9.6</td>
<td>8.1</td>
<td>7.4</td>
</tr>
<tr>
<td>$t_{en}$</td>
<td>OE</td>
<td>A</td>
<td>1</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td></td>
<td>B</td>
<td>A</td>
<td>1</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>$t_{dis}$</td>
<td>OE</td>
<td>A</td>
<td>220</td>
<td>220</td>
<td>220</td>
</tr>
<tr>
<td></td>
<td>B</td>
<td>A</td>
<td>220</td>
<td>220</td>
<td>220</td>
</tr>
</tbody>
</table>

6.15 Switching Characteristics: $V_{CCA} = 3.3 \, \text{V} \pm 0.3 \, \text{V}$
over recommended operating free-air temperature range, $V_{CCA} = 3.3 \, \text{V} \pm 0.3 \, \text{V}$ (unless otherwise noted)

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>FROM (INPUT)</th>
<th>TO (OUTPUT)</th>
<th>$V_{CCB} = 3.3 , \text{V} \pm 0.3 , \text{V}$</th>
<th>$V_{CCB} = 5 , \text{V} \pm 0.5 , \text{V}$</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td>MIN</td>
<td>MAX</td>
</tr>
<tr>
<td>$t_{pd}$</td>
<td>A</td>
<td>B</td>
<td>7.7</td>
<td>7</td>
</tr>
<tr>
<td></td>
<td>B</td>
<td>A</td>
<td>7.9</td>
<td>6.8</td>
</tr>
<tr>
<td>$t_{en}$</td>
<td>OE</td>
<td>A</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td></td>
<td>B</td>
<td>A</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>$t_{dis}$</td>
<td>OE</td>
<td>A</td>
<td>280</td>
<td>280</td>
</tr>
<tr>
<td></td>
<td>B</td>
<td>A</td>
<td>220</td>
<td>220</td>
</tr>
<tr>
<td>$t_{A}, t_{A}$</td>
<td>A-port rise and fall times</td>
<td>4.5</td>
<td>4.5</td>
<td></td>
</tr>
<tr>
<td>$t_{B}, t_{B}$</td>
<td>B-port rise and fall times</td>
<td>4.1</td>
<td>4.7</td>
<td></td>
</tr>
</tbody>
</table>
### 6.16 Operating Characteristics\(^{(1)}\)

**\(T_A = 25°C\)**

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>(V_{CCB})</th>
<th>(V_{CCA})</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>5 V</td>
<td>1.2 V</td>
</tr>
<tr>
<td>(C_{pdA})</td>
<td>A-port input, B-port output</td>
<td><strong>TYP</strong></td>
<td>7.8</td>
</tr>
<tr>
<td></td>
<td>B-port input, A-port output</td>
<td><strong>TYP</strong></td>
<td>12</td>
</tr>
<tr>
<td>(C_{pdB})</td>
<td>A-port input, B-port output</td>
<td><strong>TYP</strong></td>
<td>&amp; 38.1</td>
</tr>
<tr>
<td></td>
<td>B-port input, A-port output</td>
<td><strong>TYP</strong></td>
<td>25.4</td>
</tr>
<tr>
<td>(C_{pdA})</td>
<td>A-port input, B-port output</td>
<td><strong>TYP</strong></td>
<td>0.01</td>
</tr>
<tr>
<td></td>
<td>B-port input, A-port output</td>
<td><strong>TYP</strong></td>
<td>0.01</td>
</tr>
<tr>
<td>(C_{pdB})</td>
<td>A-port input, B-port output</td>
<td><strong>TYP</strong></td>
<td>0.01</td>
</tr>
<tr>
<td></td>
<td>B-port input, A-port output</td>
<td><strong>TYP</strong></td>
<td>0.01</td>
</tr>
</tbody>
</table>

(1) \(C_{pd}\) parameter is the capacitance used to determine the no-load dynamic power dissipation per logic function for CMOS devices as per the formula: \(P_D = C_{pd}(V_{CC})^2 + I_{CC}V_{CC}\). For more details about the use of \(C_{pd}\) to calculate power dissipation, refer to SCAA035.

### 6.17 Typical Characteristics

- **Figure 1.** Input capacitance for OE pin (\(C_I\)) vs Power Supply (\(V_{CCA}\)) for \(V_{CCB} = 3.3\) V (RUT package)
- **Figure 2.** Capacitance for A port I/O pins (\(C_{iO}\)) vs Power Supply (\(V_{CCA}\)) for \(V_{CCB} = 3.3\) V (RUT package)
- **Figure 3.** Capacitance for B port I/O pins (\(C_{iO}\)) vs Power Supply (\(V_{CCA}\)) for \(V_{CCB} = 3.3\) V (RUT package)
7 Parameter Measurement Information

A. \( C_L \) includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR \( \leq 10 \) MHz, \( Z_0 = 50 \) \( \Omega \), \( dv/dt \geq 1 \) V/ns.
C. The outputs are measured one at a time, with one transition per measurement.
D. \( t_{PLH} \) and \( t_{PHL} \) are the same as \( t_{pd} \).
E. \( V_{CCI} \) is the \( V_C \) associated with the input port.
F. \( V_{CCO} \) is the \( V_C \) associated with the output port.
G. All parameters and waveforms are not applicable to all devices.

Figure 4. Load Circuits and Voltage Waveforms
8 Detailed Description

8.1 Overview
The TXB0104 device is a 4-bit, bi-directional voltage-level translator specifically designed for translating logic voltage levels. The A port is able to accept I/O voltages ranging from 1.2 V to 3.6 V, while the B port can accept I/O voltages from 1.65 V to 5.5 V. The device is a buffered architecture with edge-rate accelerators (one-shots) to improve the overall data rate. This device can only translate push-pull CMOS logic outputs. If for open-drain signal translation, please refer to TI's TXS010X products.

8.2 Functional Block Diagram

8.3 Feature Description

8.3.1 Architecture
The TXB0104 architecture (see Functional Block Diagram) does not require a direction-control signal to control the direction of data flow from A to B or from B to A. In a DC state, the output drivers of the TXB0104 can maintain a high or low, but are designed to be weak, so that they can be overdriven by an external driver when data on the bus starts flowing the opposite direction.
Feature Description (continued)

The output one-shots detect rising or falling edges on the A or B ports. During a rising edge, the one-shot turns on the PMOS transistors (T1, T3) for a short duration, which speeds up the low-to-high transition. Similarly, during a falling edge, the one-shot turns on the NMOS transistors (T2, T4) for a short duration which speeds up the high-to-low transition. The typical output impedance during output transition is 70 Ω at \( V_{CCO} = 1.2 \) V to 1.8 V, 50 Ω at \( V_{CCO} = 1.8 \) V to 3.3 V, and 40 Ω at \( V_{CCO} = 3.3 \) V to 5 V.

![Feature Description Diagram](image)

**Figure 5. Architecture of TXB0104 I/O Cell**

### 8.3.2 Input Driver Requirements

Typical \( I_{IN} \) vs \( V_{IN} \) characteristics of the TXB0104 are shown in **Figure 6**. For proper operation, the device driving the data I/Os of the TXB0104 must have drive strength of at least ±2 mA.

![Input Driver Requirement Diagram](image)

**Figure 6. Typical \( I_{IN} \) vs \( V_{IN} \) Curve**

A. \( V_T \) is the input threshold voltage of the TXB0104 (typically \( V_{CC}/2 \)).
B. \( V_D \) is the supply voltage of the external driver.
Feature Description (continued)

8.3.3 Output Load Considerations
TI recommends careful PCB layout practices with short PCB trace lengths to avoid excessive capacitive loading and to ensure that proper one shot (O.S.) triggering takes place. PCB signal trace-lengths should be kept short enough such that the round trip delay of any reflection is less than the one-shot duration. This improves signal integrity by ensuring that any reflection sees a low impedance at the driver. The O.S. circuits have been designed to stay on for approximately 10 ns. The maximum capacitance of the lumped load that can be driven also depends directly on the one-shot duration. With very heavy capacitive loads, the one-shot can time-out before the signal is driven fully to the positive rail. The O.S. duration has been set to best optimize trade-offs between dynamic \( I_{CC} \), load driving capability, and maximum bit-rate considerations. Both PCB trace length and connectors add to the capacitance that the TXB0104 output sees, so it is recommended that this lumped-load capacitance be considered to avoid O.S. retriggering, bus contention, output signal oscillations, or other adverse system-level affects.

8.3.4 Enable and Disable
The TXB0104 has an OE input that is used to disable the device by setting OE = low, which places all I/Os in the high-impedance (Hi-Z) state. The disable time (\( t_{\text{dis}} \)) indicates the delay between when OE goes low and when the outputs actually get disabled (Hi-Z). The enable time (\( t_{\text{en}} \)) indicates the amount of time the user must allow for the one-shot circuitry to become operational after OE is taken high.

8.3.5 Pullup or Pulldown Resistors on I/O Lines
The TXB0104 is designed to drive capacitive loads of up to 70 pF. The output drivers of the TXB0104 have low DC drive strength. If pullup or pulldown resistors are connected externally to the data I/Os, their values must be kept higher than 50 k\( \Omega \) to ensure that they do not contend with the output drivers of the TXB0104.

For the same reason, the TXB0104 should not be used in applications such as \( \text{i}^2\text{C} \) or 1-Wire where an open-drain driver is connected on the bidirectional data I/O. For these applications, use a device from the TI TXS01xx series of level translators.

8.4 Device Functional Modes
The TXB0104 device has two functional modes, enabled and disabled. To disable the device, set the OE input to low, which places all I/Os in a high impedance state. Setting the OE input to high will enable the device.
9 Application and Implementation

**NOTE**

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI’s customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The TXB0104 can be used in level-translation applications for interfacing devices or systems operating at different interface voltages with one another. It can only translate push-pull CMOS logic outputs. If for open-drain signal translation, please refer to TI TXS010X products. Any external pulldown or pullup resistors are recommended larger than 50 kΩ.

9.2 Typical Application

Figure 7. Typical Application Schematic

9.2.1 Design Requirements

For this design example, use the parameters listed in Table 1. And make sure the \( V_{CCA} \leq V_{CCB} \).

<table>
<thead>
<tr>
<th>DESIGN PARAMETERS</th>
<th>EXAMPLE VALUE</th>
</tr>
</thead>
<tbody>
<tr>
<td>Input voltage range</td>
<td>1.2 V to 3.6 V</td>
</tr>
<tr>
<td>Output voltage range</td>
<td>1.65 V to 5.5 V</td>
</tr>
</tbody>
</table>

9.2.2 Detailed Design Procedure

To begin the design process, determine the following:

- **Input voltage range**
  - Use the supply voltage of the device that is driving the TXB0104 device to determine the input voltage range. For a valid logic high the value must exceed the \( V_{IH} \) of the input port. For a valid logic low the value must be less than the \( V_{IL} \) of the input port.

- **Output voltage range**
  - Use the supply voltage of the device that the TXB0104 device is driving to determine the output voltage range.
  - It is not recommended to have the external pullup or pulldown resistors. If mandatory, it is recommended the value should be larger than 50 kΩ.

- An external pulldown or pullup resistor decreases the output \( V_{OH} \) and \( V_{OL} \). Use the below equations to draft estimate the \( V_{OH} \) and \( V_{OL} \) as a result of an external pulldown and pullup resistor.
\[ V_{OH} = V_{CCx} \times R_{PD} / (R_{PD} + 4.5 \, \text{k}\Omega) \]
\[ V_{OL} = V_{CCx} \times 4.5 \, \text{k}\Omega / (R_{PU} + 4.5 \, \text{k}\Omega) \]

where
- \( V_{CCx} \) is the output port supply voltage on either \( V_{CCA} \) or \( V_{CCB} \)
- \( R_{PD} \) is the value of the external pull down resistor
- \( R_{PU} \) is the value of the external pull up resistor
- 4.5 k\( \Omega \) is the counting the variation of the serial resistor 4 k\( \Omega \) in the I/O line

9.2.3 Application Curve

Figure 8. Example of Level Translation of a 2.5-MHz 1.8 V Signal (Green) to a 3.3 V Signal (Pink)
10 Power Supply Recommendations

During operation, ensure that $V_{CCA} \leq V_{CCB}$ at all times. During power-up sequencing, $V_{CCA} \geq V_{CCB}$ does not damage the device, so any power supply can be ramped up first. The TXB0104 has circuitry that disables all output ports when either $V_{CC}$ is switched off ($V_{CCAB} = 0$ V). The output-enable (OE) input circuit is designed so that it is supplied by $V_{CCA}$ and when the (OE) input is low, all outputs are placed in the high-impedance state. To ensure the high-impedance state of the outputs during power up or power down, the OE input pin must be tied to GND through a pulldown resistor and must not be enabled until $V_{CCA}$ and $V_{CCB}$ are fully ramped and stable. The minimum value of the pulldown resistor to ground is determined by the current-sourcing capability of the driver.

11 Layout

11.1 Layout Guidelines

To ensure reliability of the device, following common printed-circuit board layout guidelines are recommended:

- Bypass capacitors should be used on power supplies. And should be placed as close as possible to the VCCA, VCCB pin, and GND pin.
- Short trace-lengths should be used to avoid excessive loading.
- PCB signal trace-lengths must be kept short enough so that the round-trip delay of any reflection is less than the one-shot duration, approximately 10 ns, ensuring that any reflection encounters low impedance at the source driver.

11.2 Layout Example

![Figure 9. Layout Example Schematic](image-url)
12 Device and Documentation Support

12.1 Trademarks
All trademarks are the property of their respective owners.

12.2 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.3 Glossary

SLYZ022 — Ti Glossary.
This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.
### PACKAGING INFORMATION

<table>
<thead>
<tr>
<th>Orderable Device</th>
<th>Status (1)</th>
<th>Package Type</th>
<th>Package Drawing</th>
<th>Pins</th>
<th>Package Qty</th>
<th>Eco Plan (2)</th>
<th>Lead/Ball Finish (6)</th>
<th>MSL Peak Temp</th>
<th>Op Temp (°C)</th>
<th>Device Marking (4/5)</th>
<th>Samples</th>
</tr>
</thead>
<tbody>
<tr>
<td>TXB0104QPWRQ1</td>
<td>ACTIVE</td>
<td>TSSOP</td>
<td>PW</td>
<td>14</td>
<td>2000</td>
<td>Green (RoHS &amp; no Sb/Br)</td>
<td>NIPDAU</td>
<td>Level-1-260C-UNLIM</td>
<td>-40 to 125</td>
<td>YE04Q1</td>
<td>Samples</td>
</tr>
<tr>
<td>TXB0104QRGYRQ1</td>
<td>ACTIVE</td>
<td>VQFN</td>
<td>RGY</td>
<td>14</td>
<td>3000</td>
<td>Green (RoHS &amp; no Sb/Br)</td>
<td>NIPDAU</td>
<td>Level-2-260C-1 YEAR</td>
<td>-40 to 125</td>
<td>YE04Q1</td>
<td>Samples</td>
</tr>
<tr>
<td>TXB0104QRUTRQ1</td>
<td>ACTIVE</td>
<td>UQFN</td>
<td>RUT</td>
<td>12</td>
<td>3000</td>
<td>Green (RoHS &amp; no Sb/Br)</td>
<td>NIPDAUAG</td>
<td>Level-1-260C-UNLIM</td>
<td>-40 to 125</td>
<td>SIG</td>
<td>Samples</td>
</tr>
</tbody>
</table>

(1) The marketing status values are defined as follows:
- **ACTIVE**: Product device recommended for new designs.
- **LIFEBUY**: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
- **NRND**: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
- **PREVIEW**: Device has been announced but is not in production. Samples may or may not be available.
- **OBSOLETE**: TI has discontinued the production of the device.

(2) **RoHS**: TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
- **RoHS Exempt**: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
- **Green**: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) **MSL, Peak Temp.** - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a “~” will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**OTHER QUALIFIED VERSIONS OF TXB0104-Q1:**
- Catalog: TXB0104

**NOTE: Qualified Version Definitions:**
- Catalog - TI's standard catalog product
## TAPE AND REEL INFORMATION

### TAPE DIMENSIONS

<table>
<thead>
<tr>
<th>Dimension</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>A0</td>
<td>Dimension designed to accommodate the component width</td>
</tr>
<tr>
<td>B0</td>
<td>Dimension designed to accommodate the component length</td>
</tr>
<tr>
<td>K0</td>
<td>Dimension designed to accommodate the component thickness</td>
</tr>
<tr>
<td>W</td>
<td>Overall width of the carrier tape</td>
</tr>
<tr>
<td>P1</td>
<td>Pitch between successive cavity centers</td>
</tr>
</tbody>
</table>

### REEL DIMENSIONS

- Reel Diameter
- Reel Width (W1)

### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

- Q1, Q2, Q3, Q4
- Pocket Quadrants
- Sprocket Holes
- User Direction of Feed

---

### PACKAGE MATERIALS INFORMATION

<table>
<thead>
<tr>
<th>Device</th>
<th>Package Type</th>
<th>Package Drawing</th>
<th>Pins</th>
<th>SPQ</th>
<th>Reel Diameter (mm)</th>
<th>Reel Width W1 (mm)</th>
<th>A0 (mm)</th>
<th>B0 (mm)</th>
<th>K0 (mm)</th>
<th>P1 (mm)</th>
<th>W (mm)</th>
<th>Pin 1 Quadrant</th>
</tr>
</thead>
<tbody>
<tr>
<td>TXB0104QPWRQ1</td>
<td>TSSOP</td>
<td>PW</td>
<td>14</td>
<td>2000</td>
<td>330.0</td>
<td>12.4</td>
<td>5.6</td>
<td>1.6</td>
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<td>12.0</td>
<td>Q1</td>
<td></td>
</tr>
<tr>
<td>TXB0104QRGYRQ1</td>
<td>VQFN</td>
<td>RGY</td>
<td>14</td>
<td>3000</td>
<td>330.0</td>
<td>12.4</td>
<td>3.75</td>
<td>1.15</td>
<td>8.0</td>
<td>12.0</td>
<td>Q1</td>
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<tr>
<td>TXB0104QRUTRQ1</td>
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<td>RUT</td>
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<td>3000</td>
<td>180.0</td>
<td>8.4</td>
<td>2.3</td>
<td>0.75</td>
<td>4.0</td>
<td>8.0</td>
<td>Q1</td>
<td></td>
</tr>
</tbody>
</table>

*All dimensions are nominal.*
<table>
<thead>
<tr>
<th>Device</th>
<th>Package Type</th>
<th>Package Drawing</th>
<th>Pins</th>
<th>SPQ</th>
<th>Length (mm)</th>
<th>Width (mm)</th>
<th>Height (mm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>TXB0104QPWRQ1</td>
<td>TSSOP</td>
<td>PW</td>
<td>14</td>
<td>2000</td>
<td>367.0</td>
<td>367.0</td>
<td>35.0</td>
</tr>
<tr>
<td>TXB0104QRGYRQ1</td>
<td>VQFN</td>
<td>RGY</td>
<td>14</td>
<td>3000</td>
<td>367.0</td>
<td>367.0</td>
<td>35.0</td>
</tr>
<tr>
<td>TXB0104QRUTRQ1</td>
<td>UQFN</td>
<td>RUT</td>
<td>12</td>
<td>3000</td>
<td>202.0</td>
<td>201.0</td>
<td>28.0</td>
</tr>
</tbody>
</table>

*All dimensions are nominal.*

*All dimensions are nominal.*
NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
B. This drawing is subject to change without notice.
C. QFN (Quad Flatpack No-Lead) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.

Pin 1 identifiers are located on both top and bottom of the package and within the zone indicated.

The Pin 1 identifiers are either a molded, marked, or metal feature.
G. Package complies to JEDEC MO-241 variation BA.
THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal pasting, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.

NOTE: All linear dimensions are in millimeters.
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC-7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat-Pack QFN/SOIC PCB Attachment, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.
NOTES:

A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.

B. This drawing is subject to change without notice.

C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 each side.

D. Body width does not include interlead flash. Interlead flash shall not exceed 0.25 each side.

E. Falls within JEDEC MO-153
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC-7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.
NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
B. This drawing is subject to change without notice.
C. QFN (Quad Flatpack No-Lead) package configuration.
NOTES:  
A. All linear dimensions are in millimeters.  
B. This drawing is subject to change without notice.  
C. Publication IPC-7351 is recommended for alternate designs.  
D. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.  
E. Maximum stencil thickness 0.1016 mm (4 mils). All linear dimensions are in millimeters.  
F. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.  
G. Over-printing land for larger area ratio is not advised due to land width and bridging potential. Exersize extreme caution.  
H. Suggest stencils cut with lasers such as Fiber Laser that produce the greatest positional accuracy.  
I. Component placement force should be minimized to prevent excessive paste block deformation.
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