SLUS623A – SEPTEMBER 2004 – REVISED AUGUST 2006

PRIMARY-SIDE PUSH-PULL OSCILLATOR WITH DEAD-TIME CONTROL

FEATURES

- **Push-Pull Oscillator With Programmable Deadtime**
- **High-Current Totem-Pole Dual Output Stage Drives Push-Pull Configuration with 1-A Sink and 0.5-A Source Capability**
- **Can be Used in Push-Pull, Half-Bridge, or Full-Bridge Topologies**
- **Oscillator Synchronization Output**
- **Low Start-Up Current of 130 μA and 1.4-mA Typical Run Current**
- **Over-Current Shutdown**
- **Digitally Controlled Over-Current/Retry Feature**
- **Undervoltage Lockout With Hysteresis**

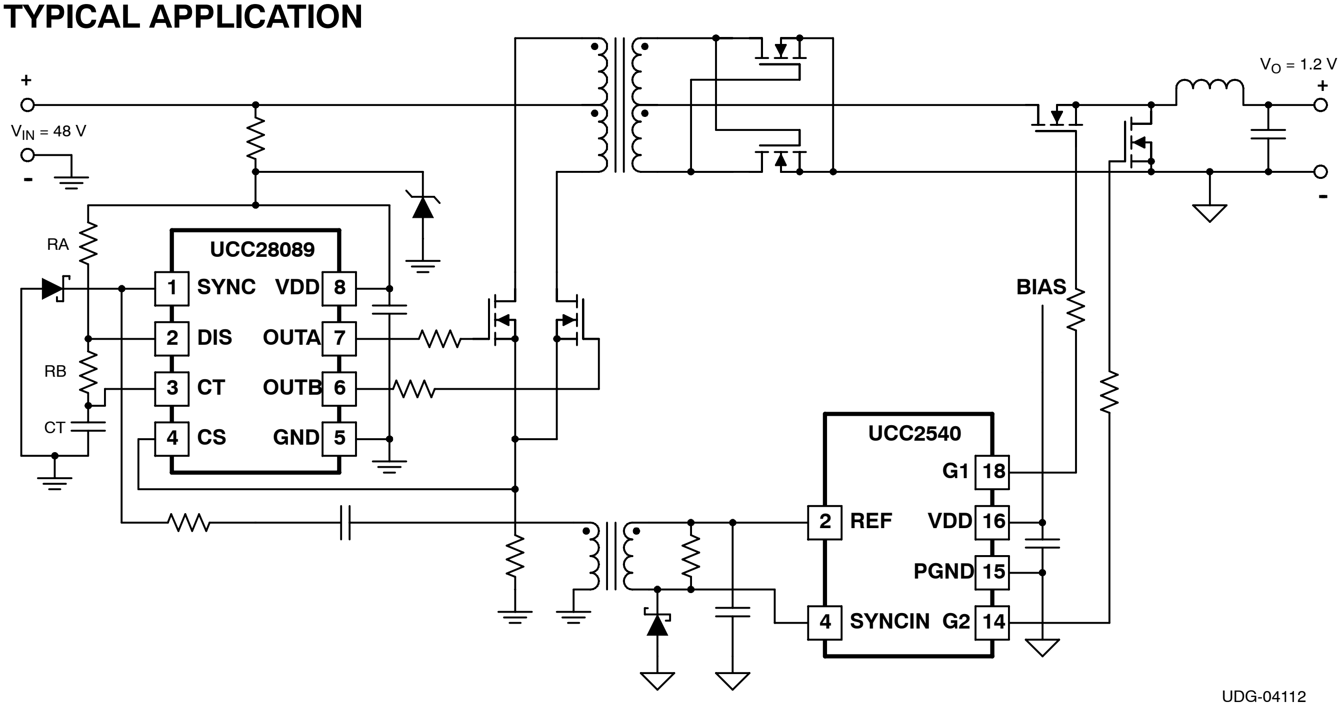
APPLICATIONS

- **High Efficiency Cascaded Converters**
- **Inverters**
- **Electronic Ballasts**
- **Uninterruptable Power Supplies (UPS)**
- **AC or DC Links**

DESCRIPTION

The UCC28089 is a versatile BiCMOS controller for dc-to-dc or off-line fixed-frequency switching power supplies. The UCC28089 has dual alternating output stages in dual-alternating push-pull configuration. Both outputs switch at half the oscillator frequency using a toggle flip-flop and duty cycle is limited to less than 50%.

TYPICAL APPLICATION



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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

DESCRIPTION (CONTINUED)

The UCC28089 is optimized for use as the primary-side companion controller for a cascaded converter that has secondary-side control. The device incorporates dead-time programming. The synchronization output also provides dead-time information. The retry and soft-start duration scales with the oscillator clock frequency for high performance fault recovery.

The UCC28089 also provides primary side under-voltage protection (UVLO), and over-current protection. Both the soft start and retry after fault durations scale with oscillator frequency for high performance. The turn-on/off UVLO thresholds are 10.5 V/8.0 V.

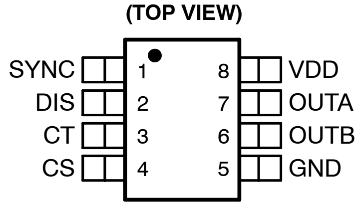
ORDERING INFORMATION

TEMPERATURE RANGE $T_A = T_J$	PACKAGED DEVICES†
	SOIC-8 (D)
–40°C to 105°C	UCC28089D

† D (SOIC–8) package is available taped and reeled. Add R suffix to device type (e.g. UCC28089DR) to order quantities of 2,500 devices per reel (for D).

CONNECTION DIAGRAM

D PACKAGE (SOIC-8)
(TOP VIEW)



ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature (unless otherwise noted)†‡

PARAMETER	SYMBOL	RATING	UNITS
Supply voltage (I_{DD} < 10 mA)	V_{DD}	15	V
Supply current	I_{DD}	20	mA
OUTA/OUTB sink current (peak)	$I_{OUT(sink)}$	1.0	A
OUTA/OUTB source current (peak)	$I_{OUT(source)}$	–0.5	
SYNC sink current (peak)		50	mA
SYNC source current (peak)		–50	
Analog inputs (DIS, CT, CS)		–0.3 to V_{DD} + 0.3, not to exceed 5	V
Power dissipation at T_A = 25°C (D package)		650	mW
Power dissipation at T_A = 25°C (DRB package)		TBD	
Junction operating temperature	T_J	–55 to 150	°C
Storage temperature	T_{stg}	–65 to 150	
Lead temperature (soldering, 10 sec.)	T_{sol}	+300	

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

‡ All voltages are with respect to GND. Currents are positive into, negative out of the specified terminal. Consult Packaging Section of the Databook for thermal limitations and considerations of packages.

RECOMMENDED OPERATION CONDITIONS

Parameter	Symbol	MIN	TYP	MAX	UNITS
Supply voltage (I_{DD} < 10 mA)	V_{DD}	8.5		14	V
SYNC sink current (peak)		0	10	25	mA
SYNC source current (peak)		–25	–10	0	
Analog inputs (DIS, CT, CS)		0		4	V
Timing capacitor range	CT	100		100,000	pF
Timing charge resistor range	RA	32		750	kΩ
Discharge resistor range	RB	0		250	
Timing charge current	$I_{CHG(RA+RB)}$	10		300	μA
Switching Frequency	f_{SW}			1000	kHz
Junction temperature	T_J	–40		105	°C

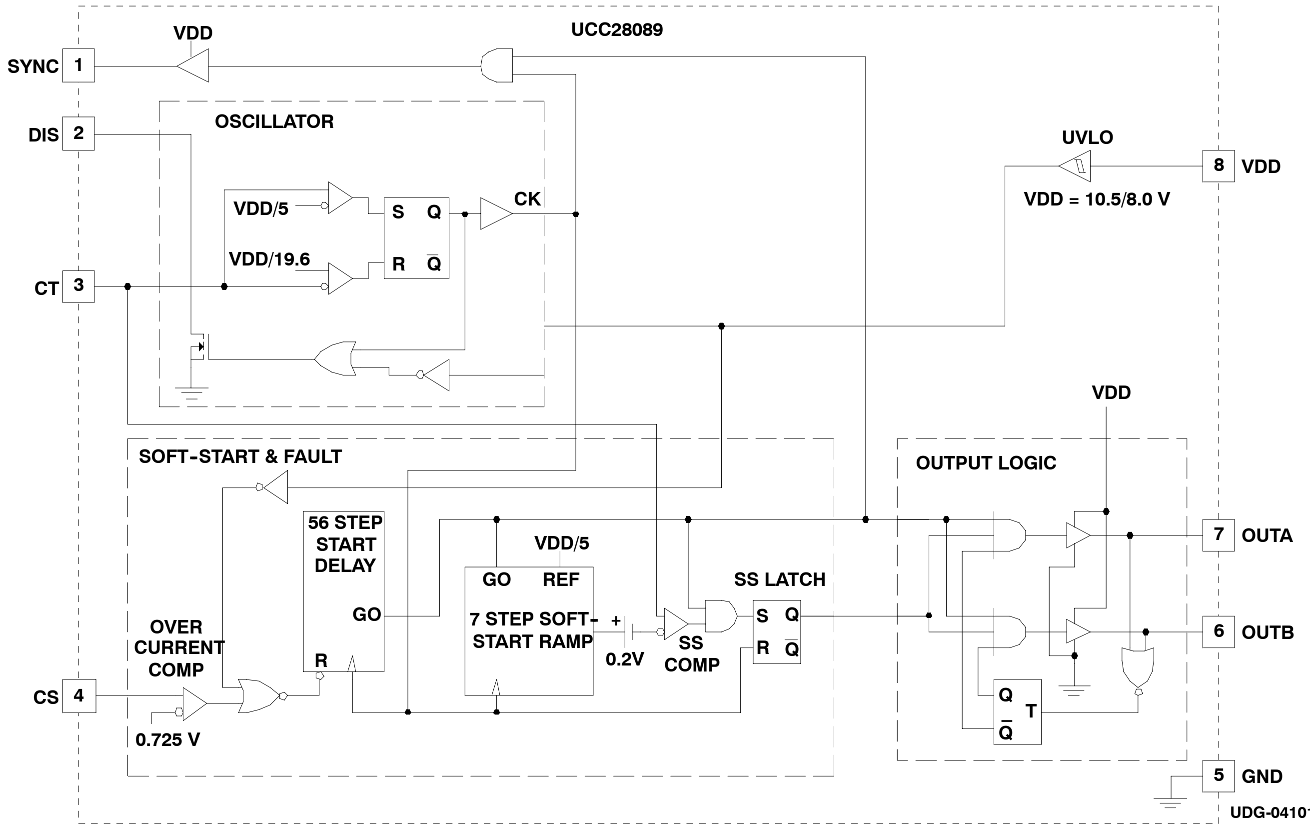
ELECTRICAL CHARACTERISTICS:

T_A = −40°C to 105°C for UCC28089, V_{DD} = 9 V (see Note 1), 1 μF capacitor from VDD to GND, RA = 110 kΩ, RB = 182 Ω, CT = 220 pF, $T_A = T_J$, (unless otherwise noted).

PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNITS
Overall Section					
Startup current	VDD < UVLO start threshold (see Note 2)		130	260	μA
Operating supply current	CS = 0 V, (see Note 1, Note 2)		1.4	2.0	mA
Undervoltage Lockout					
Start threshold	See Note 1	9.5	10.5	11.5	V
Minimum operating voltage after start		7.4	8.0	8.4	
Hysteresis		2.1	2.5	2.9	
Oscillator					
Oscillator frequency	2 x OUTx frequency, Measured at output(s)	180	200	220	kHz
Current Sense					
Current Shutdown threshold	Resetting current limit	0.650	0.725	0.800	V
CS to output delay	CS from 0 mV to 900 mV		45	100	ns
Output					
Dead Time	Measured at OUTA or OUTB	90	100	110	ns
	Over temperature	80		125	
Minimum duty cycle	CS = 0.9 V			0	%
VOL (OUTA or OUTB)	I_{OUT} = 75 mA		0.5	1	V
VOH (OUTA or OUTB)	I_{OUT} = −35 mA, (VDD – VOUT)		1.0	1.3	
Output resistance high	T_A = 25°C I_{OUT} = −1 mA (see Note 4)	70	80	90	Ω
	T_A = full range I_{OUT} = −1 mA (see Note 4)	40	80	135	
Output resistance low	T_A = 25°C I_{OUT} = 1 mA (see Note 4)	6.5	7.5	8.5	
	T_A = full range I_{OUT} = 1 mA (see Note 4)	4	7.5	14	
tr, Rise Time	C_{LOAD} = 1 nF		28	50	ns
tf, Fall Time	C_{LOAD} = 1 nF		13	30	
SYNC					
SYNC duration	Measured at SYNC pin	75	95	115	ns
tr, delay	Rising SYNC until falling OUTA or OUTB	0	8.5	30	
tf, delay	Falling SYNC until rising OUTA or OUTB	0	14	50	
SYNC V_{OH}	I_{SYNC} = −5 mA (VDD – VSYNC)		0.3	1	V
SYNC V_{OL}	I_{SYNC} = 5 mA		0.3	1	
tr, Rise Time	C_{LOAD} = 100 pF		15	30	ns
tf, Fall Time	C_{LOAD} = 100 pF		15	30	
Soft Start & Fault					
OUTA/OUTB start delay time	Cycles as measured at CT pin	57	59	62	cycles
OUTA/OUTB soft start duration	First output stage cycle to first full output stage cycle, CS ≤ 0.6 V	4	5	7	

NOTES:
1. Set VDD above the start threshold before setting at 9V.
2. Does not include current of the external oscillator network.
3. Ensured by design. Not 100% tested in production.
4. The pullup / pulldown circuits of the driver are bipolar and MOSFET transistors in parallel. The output resisstance is the RDS(ON) of the MOSFET transistor when the voltage of the driver output is less than the saturation voltage of the bipolar transistor.

FUNCTIONAL BLOCK DIAGRAM



PIN #	NAME	I/O	FUNCTION
1	SYNC	O	Active when OUTA and OUTB are active, logic LO at all other times such as during under-voltage lock-out and over-current shutdown. When active, SYNC is logic HI (VDD) during the discharge time of the oscillator and logic LO (GND) at all other times. The pulse occur during the dead time.
2	DIS	I	Separate oscillator timing capacitor discharge pin that allows the dead time to be externally programmed.
3	CT	I	Oscillator timing capacitor connection.
4	CS	I	Current sense pin. An over current shutdown event is triggered when the voltage of this pin rises above 0.75 V.
5	GND	–	Ground pin. Analog and digital signals reference this pin and output drivers return current through this pin
6	OUTB	O	Driver output, capable of sinking 1 A and sourcing 0.5 A. OUTB signal alternates with OUTA.
7	OUTA	O	Driver output, capable of sinking 1 A and sourcing 0.5 A. OUTA signal alternates with OUTB.
8	VDD	I	Power input connection for this device.

APPLICATION INFORMATION

UCC28089 is an alternating dual-driver output oscillator with over-current and under-voltage fault protection. This feature set is ideal as a start-up controller for isolated power systems where the majority of control functions are performed on the secondary side. This device is especially useful for dc link for topologies such as the cascaded buck converter [1], ac link inverter topologies [2], and inexpensive modified square wave inverters. The UCC28089 has a brief 5 to 7 cycle leading-edge modulated soft-start cycle so that it will not interfere with secondary-side controlled soft start. Both systems with off-line self bias and auxiliary bias supplies are more fault tolerant with the UCC28089 because it consistently responds to a fault with a delay of at least 56 oscillator cycles before retry.

Detailed Functional Description

VDD: Power input connection for this device. Although quiescent VDD current is very low, total supply current is higher, depending on OUTA and OUTB current and the programmed oscillator frequency. During fault response, the current drops to a lower level because the oscillator is disabled.

In order to avoid noise problems, position a 1-μF ceramic bypass capacitor, connected from VDD to GND, as close to the chip as possible. The ceramic bypass capacitor is in addition to any energy storage capacitance that would be used to hold up the VDD voltage during start-up transients.

GND: Ground pin. Analog signals reference this pin and output drivers return current through this pin. For best results, use this pin as a local ground point in a star ground configuration.

OUTA and OUTB: Output drivers capable of sinking 1 A and sourcing 0.5 A. The output pulse alternates between OUTA and OUTB. In addition, a T latch forces the output pulses to alternate in order to reduce flux build up in a transformer during low duty ratio operation. Each output is capable of driving the gate of a power MOSFET.

CT and DIS: Oscillator timing capacitor pin and timing capacitor discharge pin. The UCC28089 oscillator tracks VDD and GND internally in order to minimize oscillator frequency changes due to variations in the voltage of VDD. Figure 1 shows the oscillator block diagram.

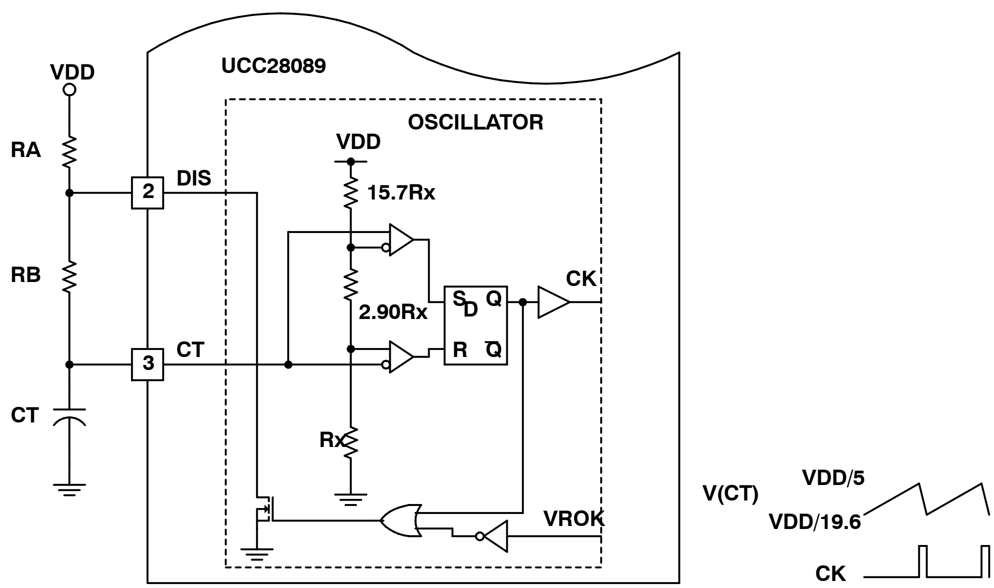


Figure 1. Block Diagram for Oscillator

APPLICATION INFORMATION

The recommended oscillator frequency range is up to 1 MHz. In order to avoid noise issues, R_A and R_B should be small enough for the oscillator to have at least 10 μA of current. There are two sets of oscillator programming equations that model the oscillator over its wide programming range. Measure the charge and the discharge times at the SYNC pin in order to avoid affecting the oscillator with probe impedances or output driver delays.

The approximate first order equations in the table are adequate for switching frequencies below 50 kHz and/or discharge times that are greater than 1 μs. The specific requirements for using the first order equations versus the second order equations are related to the timing capacitor size and the discharge resistor. Keep in mind that the 1st order equations and 2nd order equations are merely approximations that are typically within +/–20% of the actual operating point. The frequency, charge and discharge times are relatively insensitive to temperature but larger values of C_T and R_B exhibit the least sensitivity to temperature. Incidentally, the second order equations apply for the operating conditions that are in the Electrical Characteristics table. The oscillator frequency is set according to the following equations:

	1^{ST} ORDER EQUATIONS	2^{ND} ORDER EQUATIONS
Condition	$R_A > 300\ k\Omega$ AND $C_T > 300\ pF$	$32\ k\Omega < R_A < 300\ k\Omega$ OR $100\ pF < C_T < 300\ pF$
T_{CHARGE}	$0.169\left(R_A + R_B\right)C_T$	$0.175\left(R_A + R_B\right)\left(C_T + 40\ pF\right) + 20\ ns$
$T_{DISCHARGE}$	$1.36\ R_B\ C_T$	$(1.37)\left(R_B + 44\right)\left(C_T + 14\ pF\right) + 20\ ns$
f_{OSC}	$\dfrac{5.9}{\left(R_A + 8.0\ R_B\right)C_T}$	$\dfrac{1}{T_{CHARGE} + T_{DISCHARGE}}$

Where R_A and R_B are in Ohms; C_T is in Farads; f_{OSC} is in Hz; t_{CHARGE} and $t_{DISCHARGE}$ are in seconds.

The oscillator is optimized for a C_T timing capacitor range from 100 pF to 1000 nF and R_B more than 100 Ω. If the shortest discharge time possible is desired, it is permissible to short DIS to C_T for all recommended C_T values (100 pF to 0.100 μF).

SYNC: This SYNC pin produces an output pulse from 0 to VDD that can be used to synchronize a secondary side-buck controller to the free running isolating power stage. The proper timing of this signal enables zero voltage switching on the primary side MOSFETs. The clean signal also solves a problem of getting a synchronization signal from the secondary side of the transformer, which can have leakage inductance voltage spikes that may cause false triggering. The SYNC pulse width is the oscillator discharge time, which is approximately equal to the dead time. Pulse frequency is the oscillator frequency. During fault conditions, the SYNC pulses are terminated and the SYNC output is held low for at least 56 oscillator cycles. During soft start, SYNC precedes the first output pulse by at least one oscillator cycle.

CS: Connect the current sense device to this pin. A voltage threshold of 0.725 V triggers a shutdown sequence.

An over-current fault triggers an immediate shutdown. After the fault clears, a total of 64 oscillator cycles are required for an entire soft start sequence to occur. First, the outputs and SYNC are kept OFF for at least 56 oscillator cycles. Next, after one or two SYNC pulses, the soft start progressively increases the output duty ratio over the next five to seven oscillator cycles.

APPLICATION INFORMATION

Using the UCC28089 as the Primary-Side start-up Controller in a Cascaded Push-Pull Buck Two-Stage Converter

The cascaded push-pull topology is ideal for converting from moderate bus voltages, such as 48-V telecom buses, to sub 2-V output voltages. The general topology is shown in Figure 2 using the UCC28089 as the primary-side start-up controller and the UCC2540 as the secondary-side regulator [3].

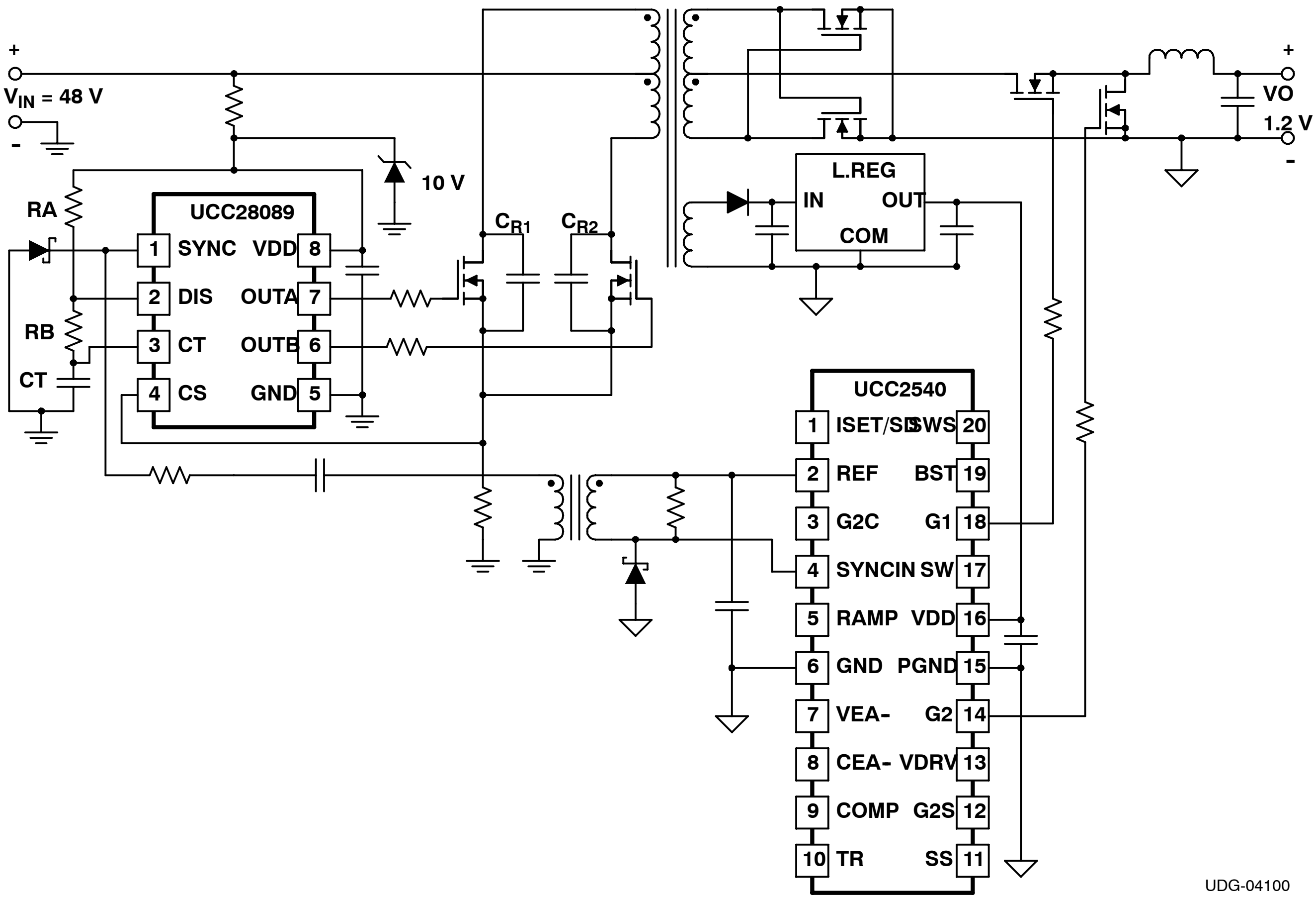


Figure 2. Cascaded Push-Pull Buck Two-Stage Converter

APPLICATION INFORMATION

Program the oscillator frequency of the UCC28089 to equal the desired switching frequency of the output post regulator. The secondary-side controller may also need corresponding switching frequency programming, such as RAMP and G2C capacitor values for the UCC2540. Program the dead time to be approximately 1/4 of the resonant period of the equivalent parasitic L−C circuit that is established by the primary leakage inductance of the transformer and the total drain-source capacitance of the primary-side power MOSFET transistors (C_{OSS} + stray capacitances). Remember that C_{OSS} predictably varies over input line voltage. If the variation is too great and/or 1/4 the resonant period is less than 100 ns, connect additional capacitance (C_{R1} and C_{R2} in Figure 2) between the drain and source of the primary transistors, which stabilizes the capacitance and raise the total capacitance value.

If the secondary-side controller is compatible with pulse edges, the pulse edge transformer circuit in Figure 3 can provide an isolated pulse edge signal on the secondary side using a transformer core that is 6-mm diameter or less. The recommended transformer (COEV #MGBBT−0001101) is compatible with all switching frequencies and it is smaller than many opto-isolators.

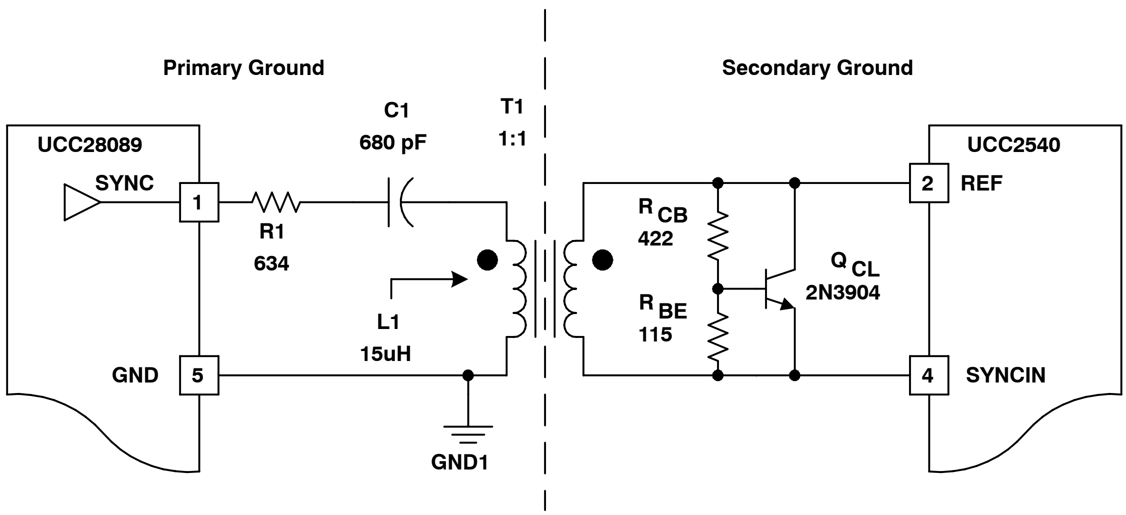


Figure 3. Isolation and clamping the SYNC signal for Cascaded Buck Converters

Notice that the peak-pulse voltage is proportional to the UCC28089 bias voltage. The circuit in Figure 3 is well suited to the full VDD bias voltage range of the UCC28089 bias voltage because it has a clamp circuit. The clamp circuit in Figure 3 (R_{CB}, R_{BE} and Q_{CL}) is a V_{BE} clamp rather than a Zener diode. A V_{BE} clamp is used here because it has much lower capacitance than typical Zener diodes so that the clamp does not affect the narrow 50-ns pulse width. The clamp may be replaced by a single resistor in applications, as in Figure 2, where the VDD bias voltage of the UCC28089 is regulated within a +/−5% window.

APPLICATION INFORMATION

Synchronization of Multiple UCC28089 Controllers to an External Signal

In systems where multiple UCC28089 parts need to be synchronized to a common clock, a 3.3-V logic-level signal can be directly applied to the CT pin (the SYNC pin on UCC28089 only provides output sync signals). As shown in Figure 4, the externally supplied sync pulse width determines the frequency and the dead time between OUT A and OUT B. In this configuration, the discharge pin DIS should be grounded since it is not used. The external sync signal should exceed the oscillator trip level of $V_{DD}/5$ when high, and pull CT below $V_{DD}/20$ when low.

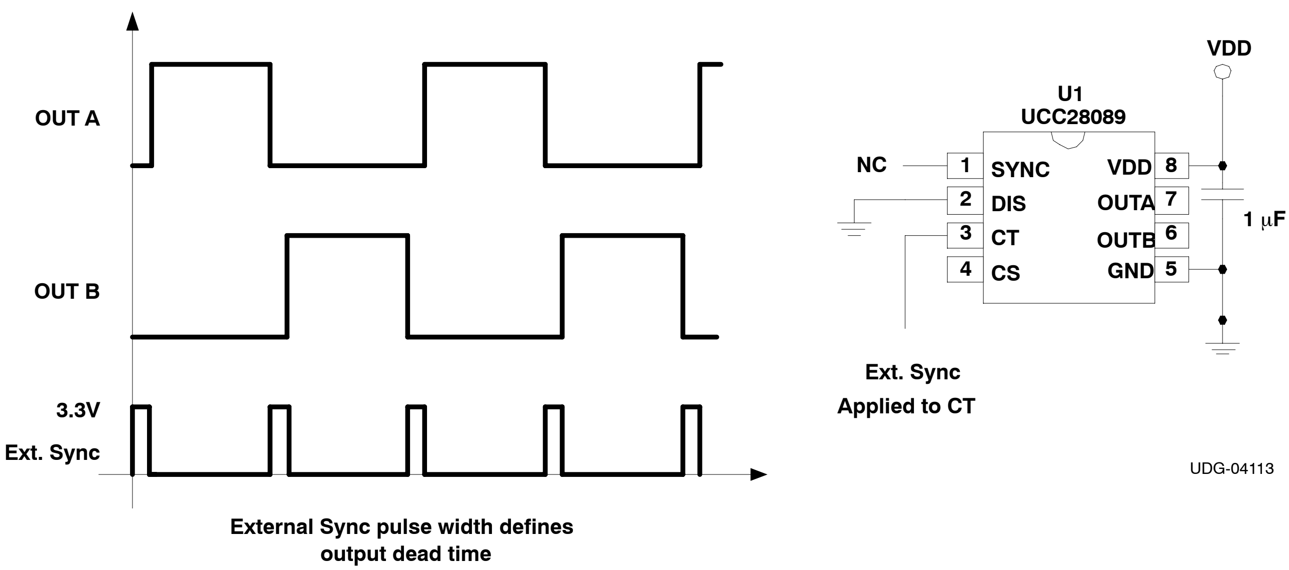
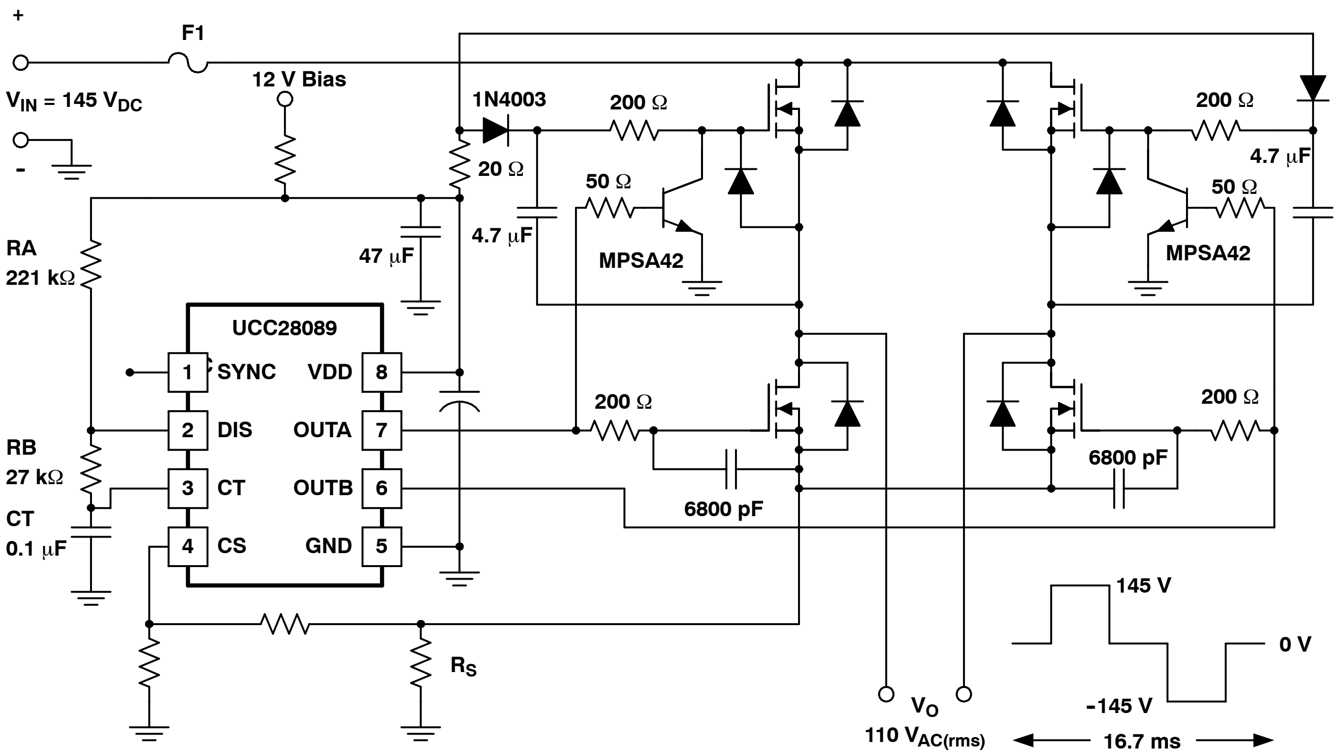


Figure 4. Synchronizing the UCC28089 to an External Signal

APPLICATION INFORMATION

Using the UCC28089 as a Modified Square Wave Inverter

Remote or dc-only power systems often require a limited amount of 60-Hz ac line power to supply small appliances. Compatible loads include universal motors, incandescent lamps, and other electronic devices with switched mode power supplies to convert the 110-V_{AC} to lower dc voltages. Many of these devices do not require a perfect sinusoidal line voltage, and acceptable performance can be obtained with a modified square wave voltage. Using the circuit in Figure 5, the UCC28089 can provide the appropriate waveform along with primary side over-current protection. Components RA, RB, and CT are selected to program the desired modified square waveform with the appropriate dead time.



NOTE: CS signal should be selected to limit peak inrush current to acceptable levels. UDG-04105

Figure 5. Modified Square Wave Inverter

The high-side gate drives of the inverter in Figure 5 are suitable for low frequency applications with relatively constant duty ratio. The NPN transistors and the charge pump diodes on the high-side gate drives must be rated for high voltage (at least 145 V + VDD). The gates are protected from excessive negative voltage by the diodes shown from gate to source.

APPLICATION INFORMATION

If desired, the 60-Hz modified square wave inverter frequency could be programmed using an external sync signal that might originate from a separate oscillator or digital controller. The following diagram in Figure 6 shows a 50% duty cycle square wave fed into the CT pin, with a frequency of 120 Hz, and the resulting OUTA/OUTB wave shapes.

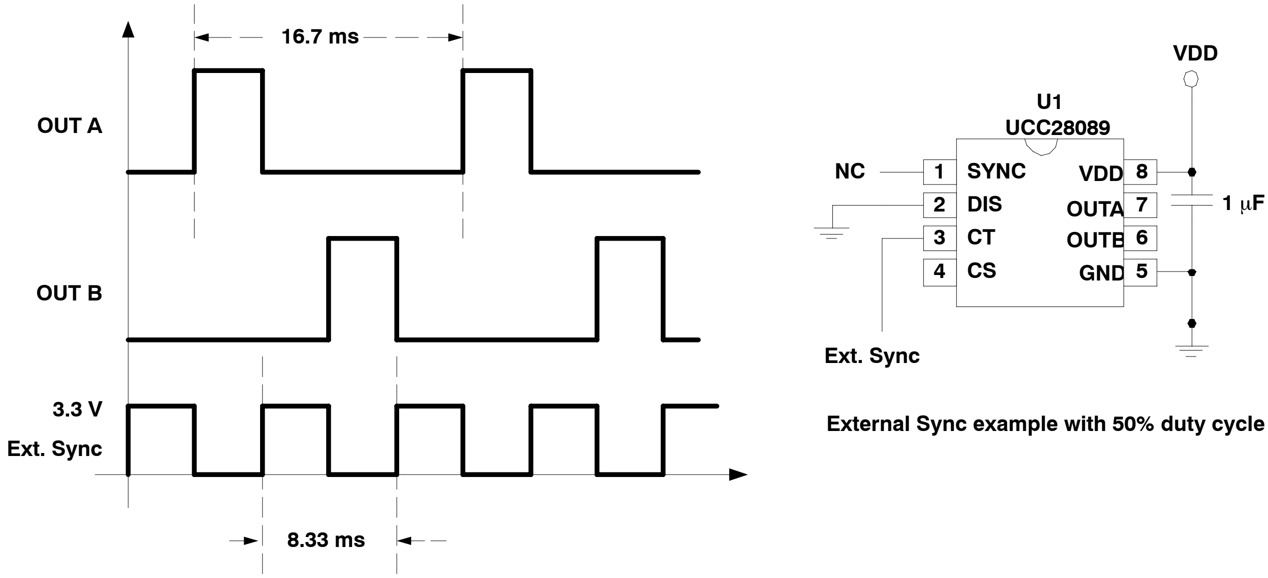


Figure 6. External Synchronization Example with 50% Duty Cycle Square Wave

RELATED PRODUCTS

DEVICE	DESCRIPTION
UCC2540	High-Efficiency Secondary-Side Synchronous-Buck PWM Controller

TYPICAL CHARACTERISTICS

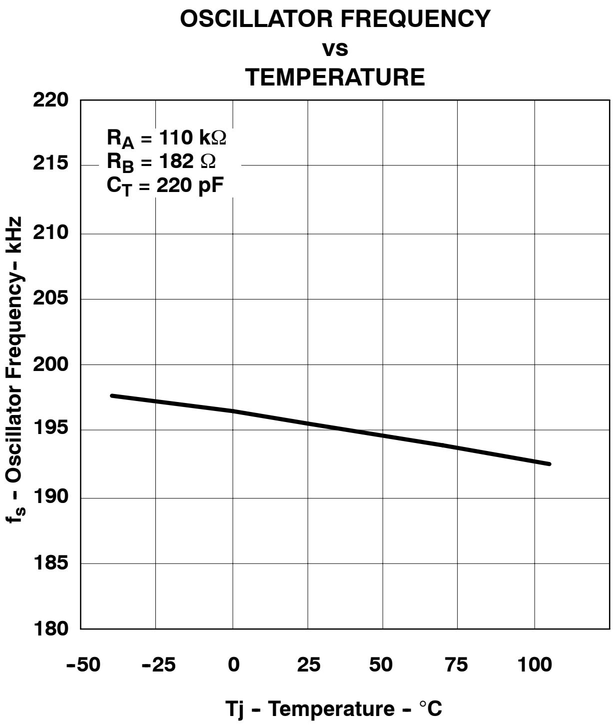


Figure 7

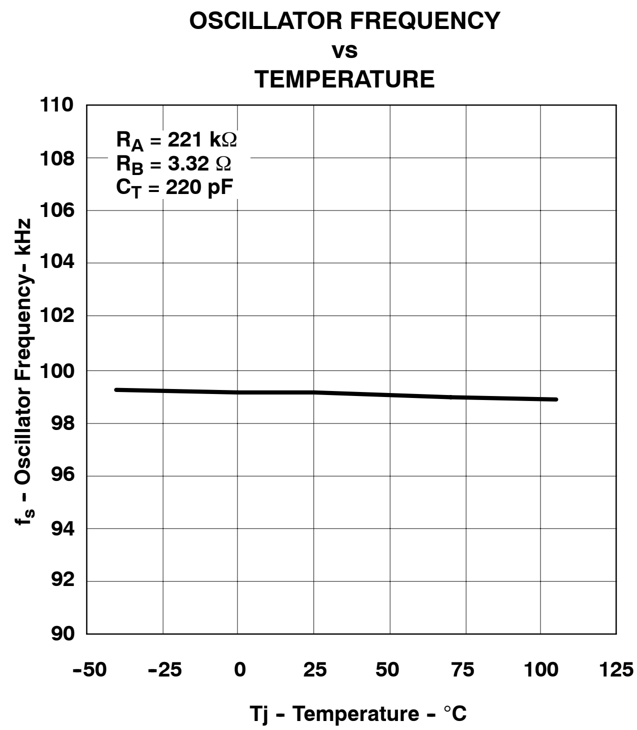


Figure 8

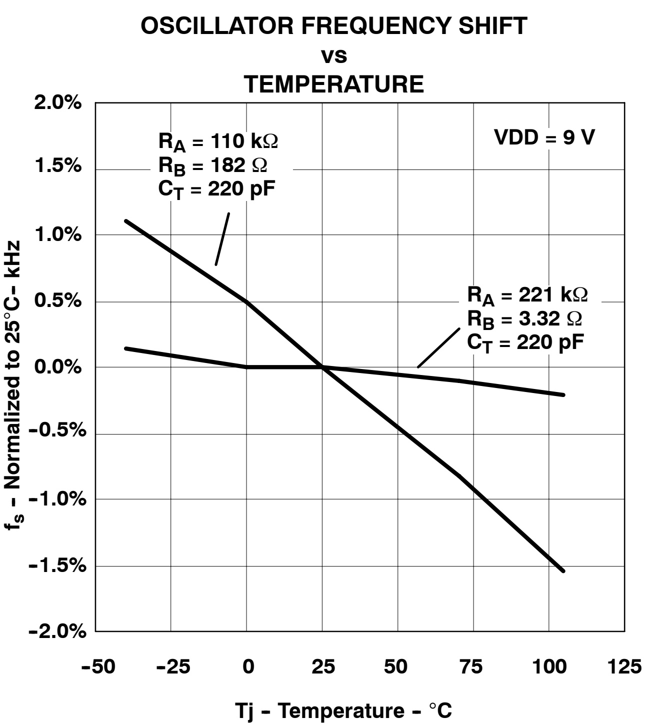


Figure 9

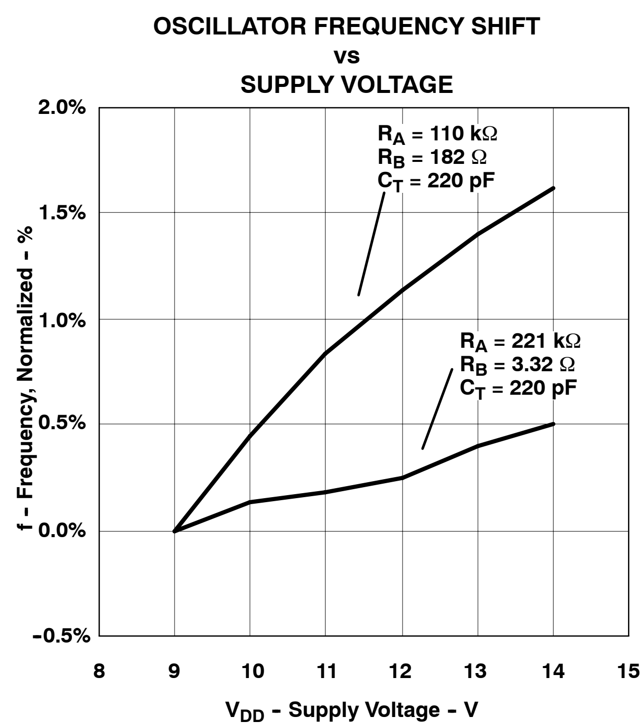


Figure 10

TYPICAL CHARACTERISTICS

OSCILATOR FREQUENCY
vs
RA x CT

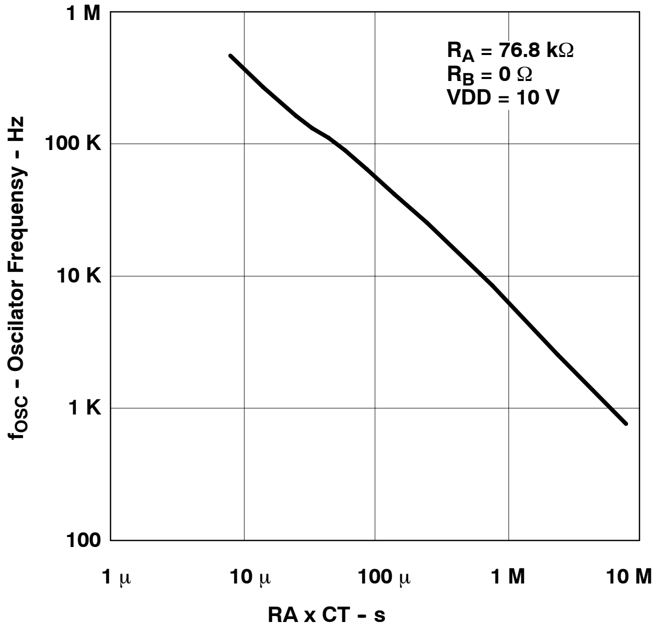


Figure 11

DISCHARGE TIME
vs
CT

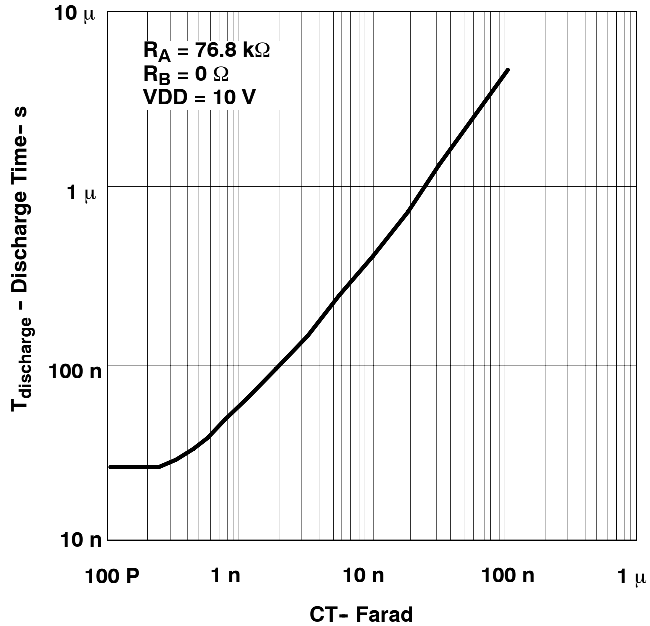


Figure 12

SYNC PULSE WIDTH
vs
TEMPERATURE

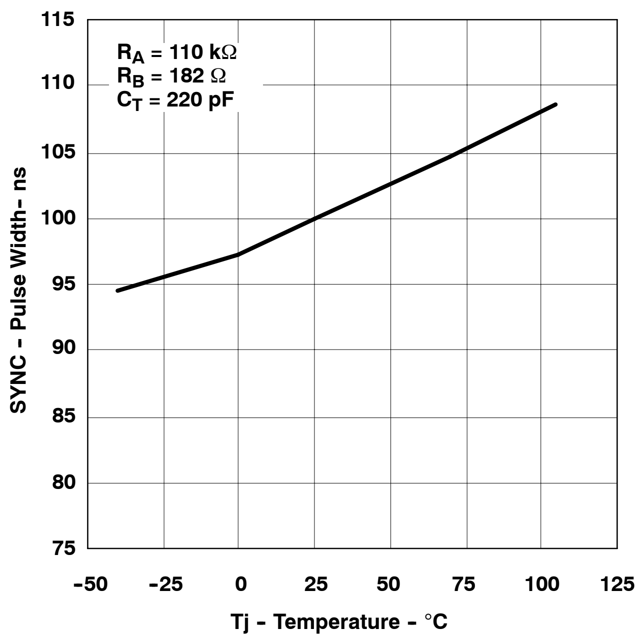


Figure 13

OUTPUT DEAD TIME
vs
TEMPERATURE

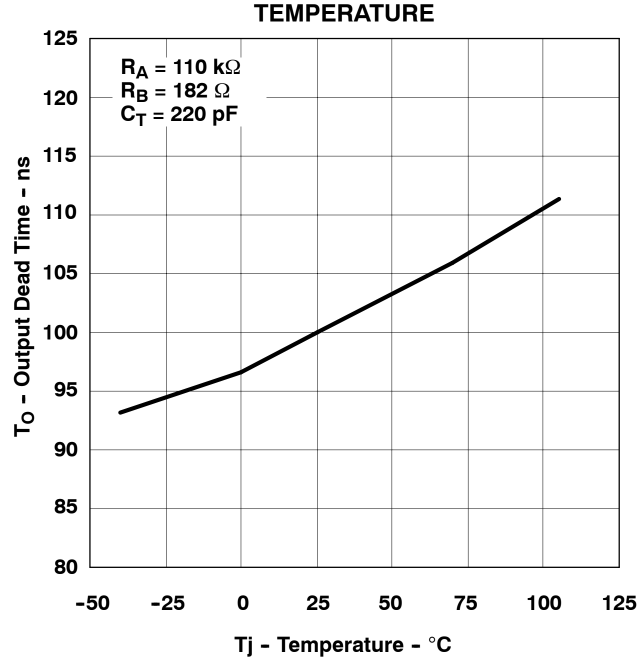


Figure 14

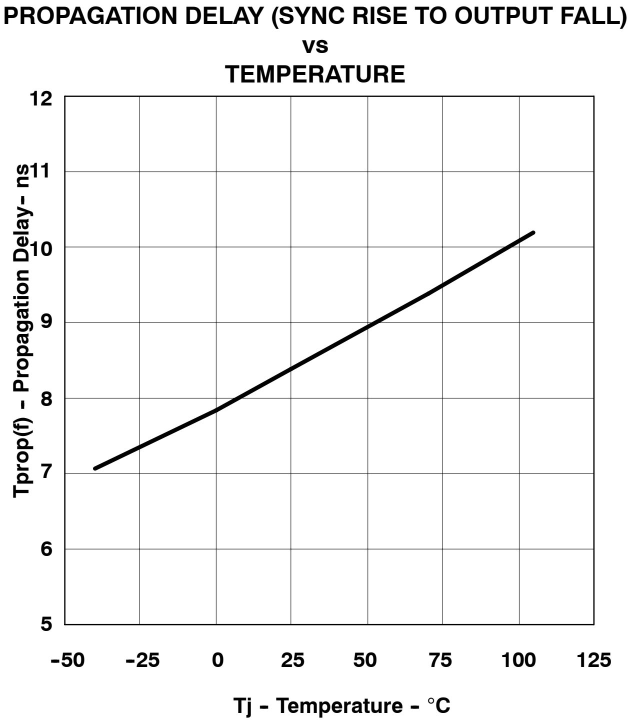


Figure 15

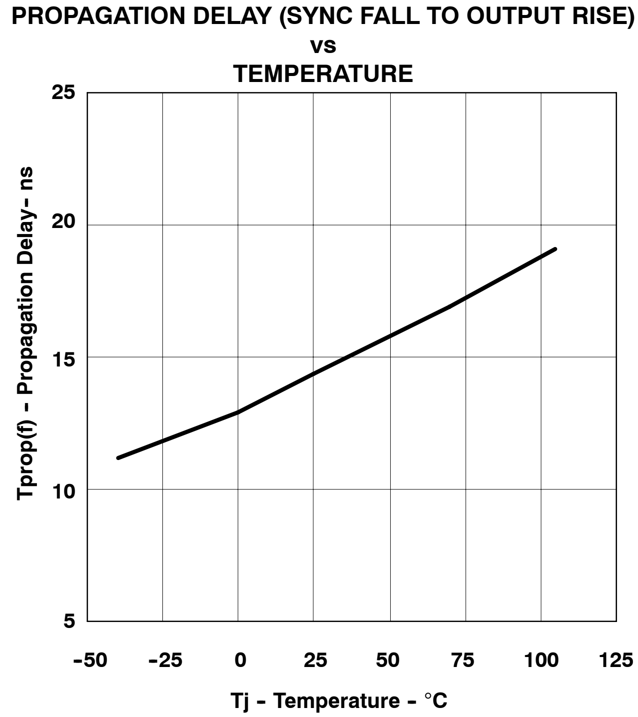


Figure 16

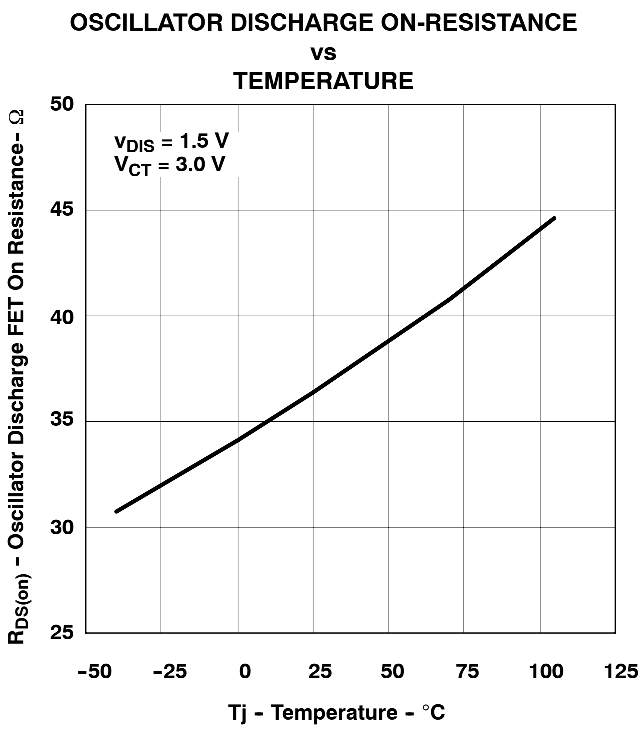


Figure 17

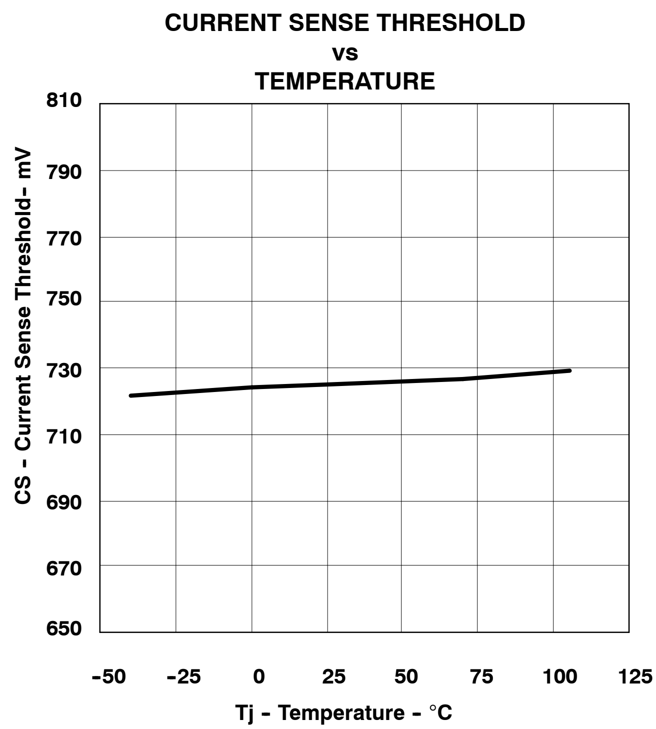


Figure 18

TYPICAL CHARACTERISTICS

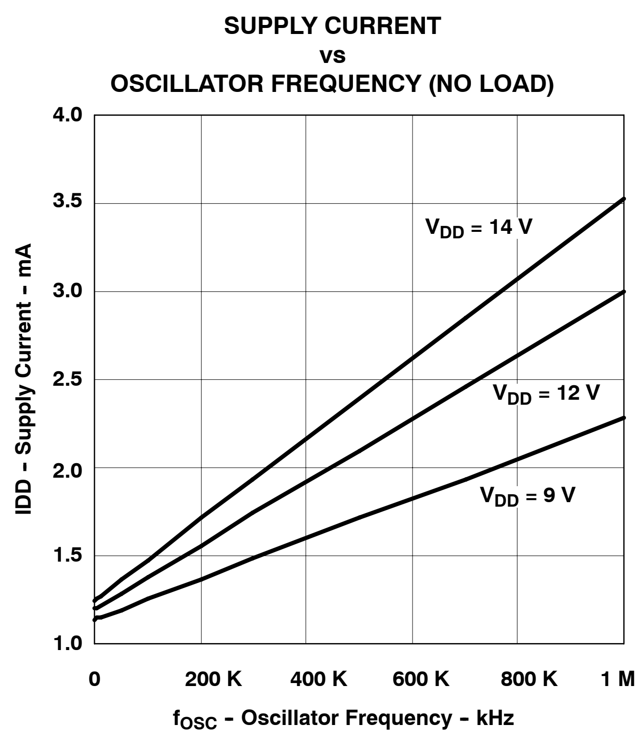


Figure 19

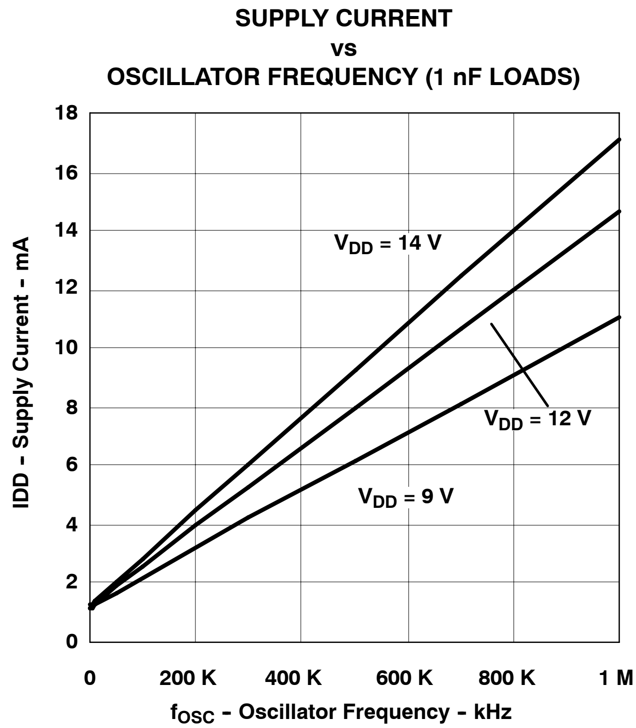


Figure 20

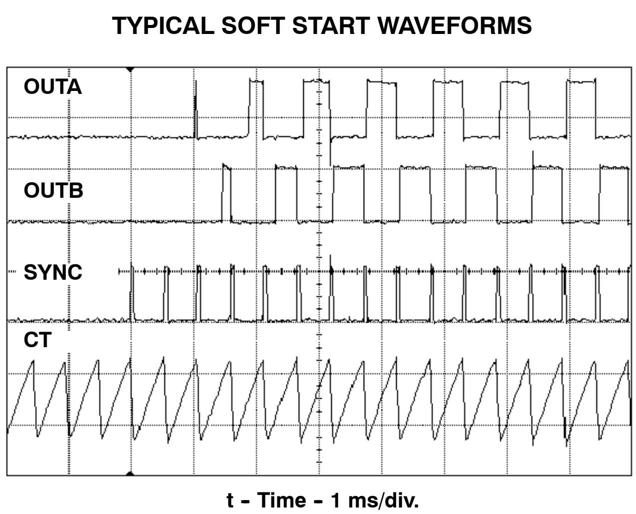


Figure 21

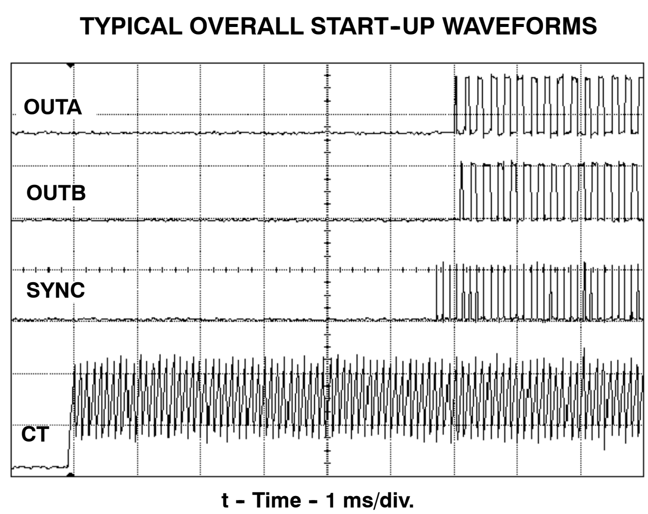


Figure 22

REFERENCES

1. Power Supply Seminar SEM–1300 Topic 1: *Unique Cascaded Power Converter Topology for High Current Low Output Voltage Applications*, by L. Balogh, C. Bridge and B. Andreycak, Texas Instruments Literature No. SLUP133

2. *Low Cost Inverter Suitable for Medium-Power Fuel Cell Sources*, by P.T. Krein and R Balog, IEEE Power Electronics Specialists Conference Proceedings, 2002, vol. 1, pp. 321–326.

3. Datasheet, UCC2540 *High-Efficiency Secondary-Side Synchronous-Buck PWM Controller*, Texas Instruments Literature No. SLUS539

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
UCC28089D	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 105	28089	Samples
UCC28089DR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 105	28089	Samples
UCC28089DRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 105	28089	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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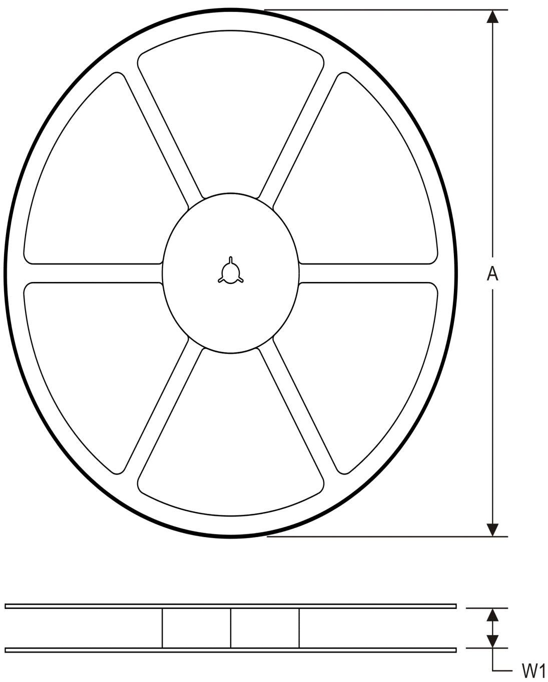
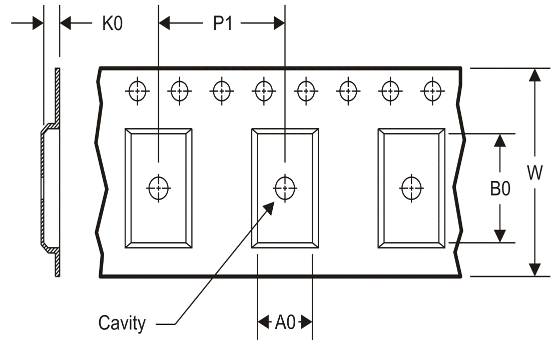
TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



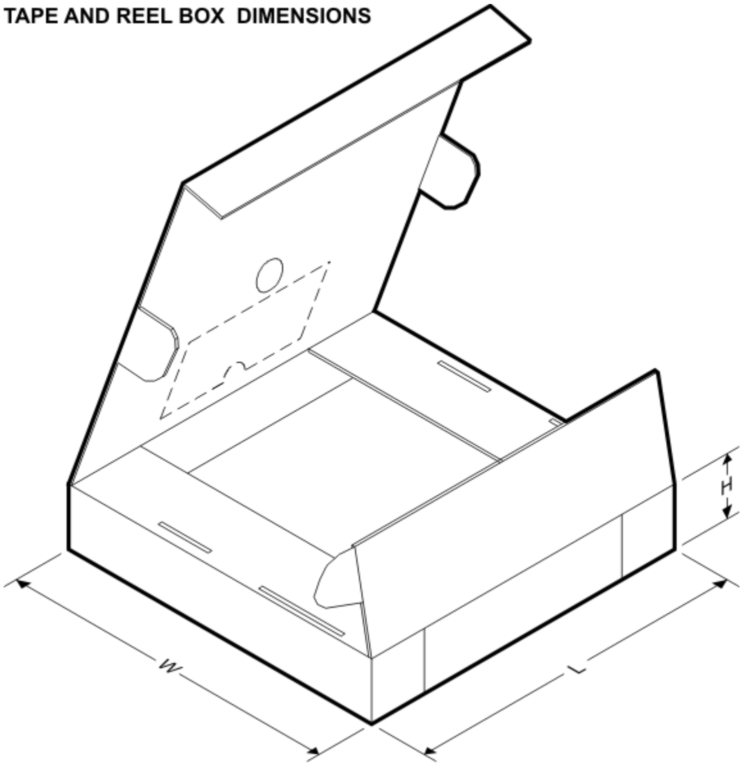
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

TAPE AND REEL INFORMATION

*All dimensions are nominal

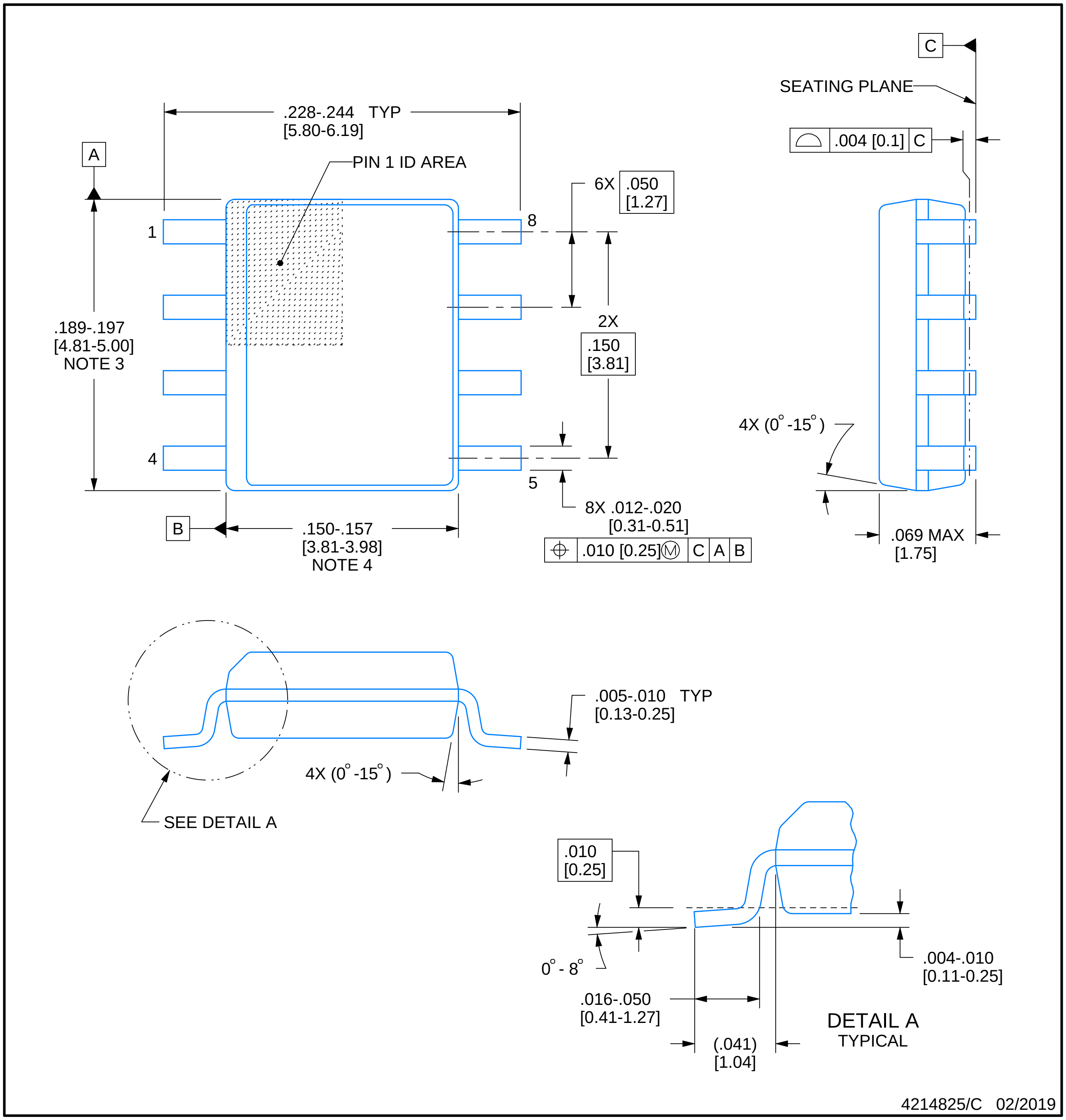
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
UCC28089DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



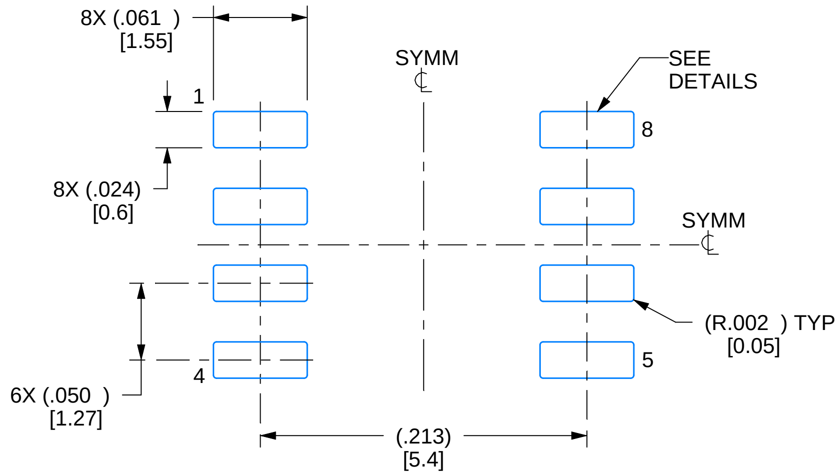
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
UCC28089DR	SOIC	D	8	2500	367.0	367.0	35.0

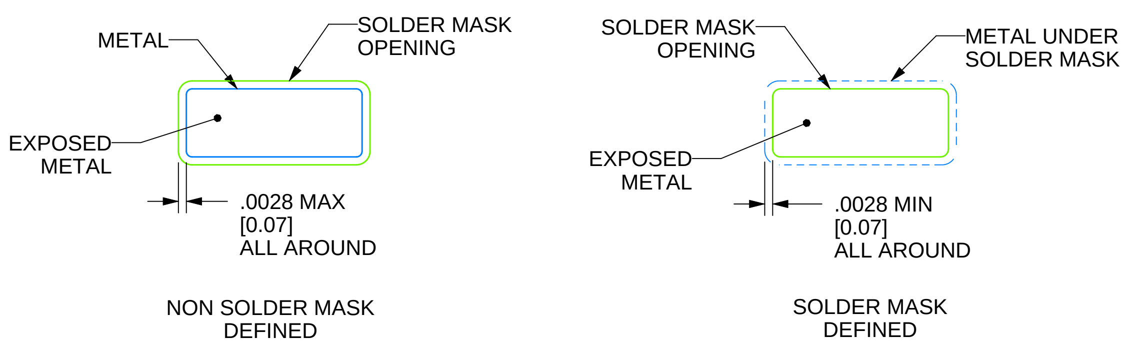


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

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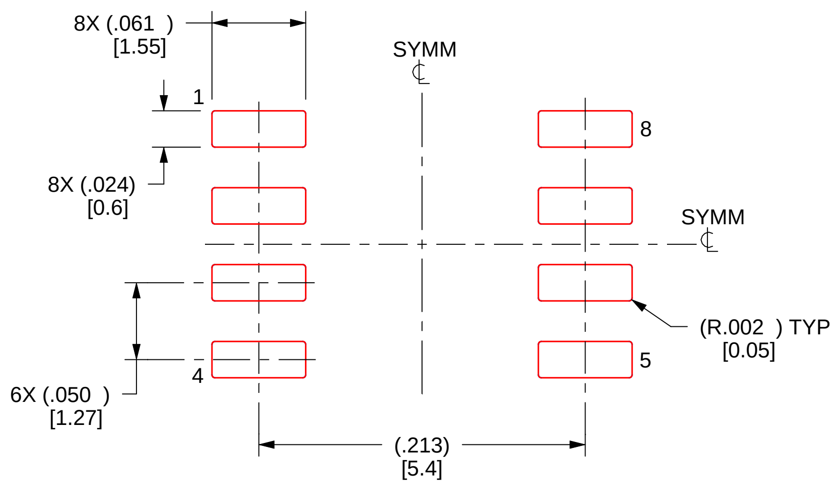
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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