

## DUAL CHANNEL SYNCHRONIZED CURRENT-MODE PWM

 Check for Samples: [UCC3810-DIE](#)

### FEATURES

- **Single Oscillator Synchronizes Two PWMs**
- **Startup Supply Current**
- **Operating Supply Current**
- **Internal Soft-Start**
- **Full-Cycle Fault Restart**
- **Internal Leading-Edge Blanking of the Current Sense Signal**
- **75-ns Typical Response from Current Sense to Output**
- **1.5% Tolerance Voltage Reference**

### DESCRIPTION

The UCC3810-DIE is a high-speed BiCMOS controller integrating two synchronized pulse width modulators for use in off-line and dc-to-dc power supplies. The UCC3810-DIE provides perfect synchronization between two PWMs by using the same oscillator. The oscillator's sawtooth waveform can be used for slope compensation if required.

Using a toggle flip-flop to alternate between modulators, the UCC3810-DIE ensures that one PWM does not slave, interfere, or otherwise affect the other PWM. This toggle flip-flop also ensures that each PWM is limited to 50% maximum duty cycle, insuring adequate off-time to reset magnetic elements.

### ORDERING INFORMATION<sup>(1)</sup>

PRODUCT	PACKAGE DESIGNATOR	PACKAGE	ORDERABLE PART NUMBER	PACKAGE QUANTITY
UCC3810	TD	Bare die in waffle pack <sup>(2)</sup>	UCC3810TD1	100
			UCC3810TD2	10

- (1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at [www.ti.com](http://www.ti.com).
- (2) Processing is per the Texas Instruments commercial production baseline and is in compliance with the Texas Instruments Quality Control System in effect at the time of manufacture. Electrical screening consists of DC parametric and functional testing at room temperature only. Unless otherwise specified by Texas Instruments AC performance and performance over temperature is not warranted. Visual Inspection is performed in accordance with MIL-STD-883 Test Method 2010 Condition B at 75X minimum.



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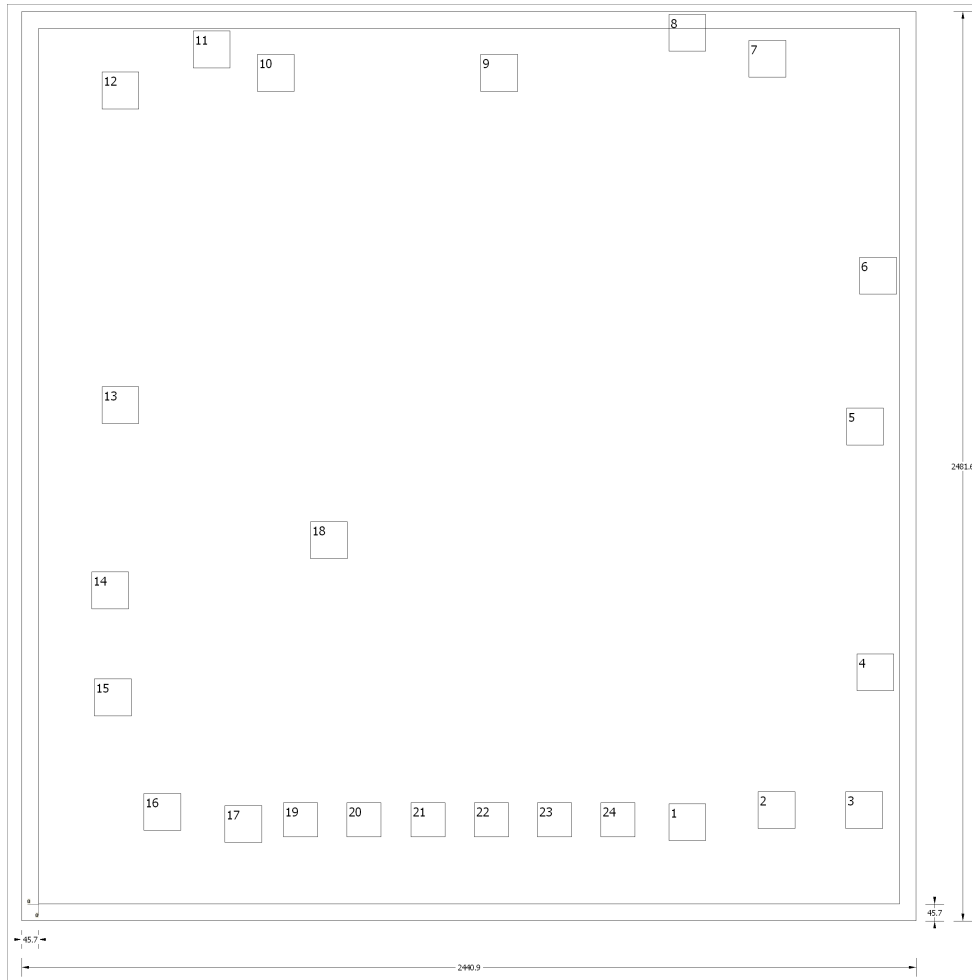


This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

**BARE DIE INFORMATION**

DIE THICKNESS	BACKSIDE FINISH	BACKSIDE POTENTIAL	BOND PAD METALLIZATION COMPOSITION	BOND PAD THICKNESS
10.5 mils.	Silicon with backgrind	Floating	ALCU(0.5%)	1200 nm



**Table 1. Bond Pad Coordinates in Microns**

DESCRIPTION	PAD NUMBER	X MIN	Y MIN	X MAX	Y MAX
SYNC	1	1719.58	172.72	1821.18	274.32
CT	2	1963.42	205.74	2065.02	307.34
RT	3	2202.18	205.74	2303.78	307.34
FB1	4	2232.66	581.66	2334.26	683.26
COMP1	5	2204.72	1252.22	2306.32	1353.82
CS1	6	2240.28	1663.7	2341.88	1765.3
OUT1	7	1938.02	2255.52	2039.62	2357.12
GND	8	1719.58	2326.64	1821.18	2428.24
GND	9	1206.5	2217.42	1308.1	2319.02
PWRGND	10	596.9	2217.42	698.5	2319.02
OUT2	11	421.64	2280.92	523.24	2382.52
CS2	12	172.72	2169.16	274.32	2270.76
COMP2	13	172.72	1310.64	274.32	1412.24
FB2	14	144.78	805.18	246.38	906.78
ENABLE2	15	152.4	513.08	254	614.68
REF	16	287.02	200.66	388.62	302.26
VCC	17	508	167.64	609.6	269.24
VCC	18	741.68	942.34	843.28	1043.94
N/C	19	668.02	182.88	762	276.86
N/C	20	840.74	182.88	934.72	276.86
N/C	21	1016	182.88	1109.98	276.86
N/C	22	1188.72	182.88	1282.7	276.86
N/C	23	1361.44	182.88	1455.42	276.86
N/C	24	1534.16	182.88	1628.14	276.86

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
UCC3810TD1	ACTIVE			0	100	TBD	Call TI	N / A for Pkg Type	25 to 25		<a href="#">Samples</a>
UCC3810TD2	ACTIVE			0	10	TBD	Call TI	N / A for Pkg Type	25 to 25		<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

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(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

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(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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