

DLP3000, DLPC300 DLP® 0.3 WVGA Chipset

Data Manual



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DLP[®] 0.3 WVGA Chipset

Check for Samples: [DLP3000](#), [DLPC300](#)

1 Introduction

1.1 Features

- **Enables High-Performance Optical Imaging With DMD**
 - 0.3-Inch (7.62-mm) Micromirror Diagonal Array
 - 608 × 684 Array of Aluminum Micromirrors, 7.6- μ m Pitch
 - $\pm 12^\circ$ Micromirror Tilt Angle
 - Side Illumination for Optimized Efficiency
 - Highly Efficient in Visible Light (420 nm–700 nm):
 - Window Transmission 97% (Single Pass, Through Two Window Surfaces)
 - Micromirror Reflectivity, 88%
 - Array Diffraction Efficiency, 86%
 - Array Fill Factor, 92%
- **Multi-Mode, 24-Bit Input Port:**
 - Supports Parallel RGB With Pixel Clock up to 33.5 MHz and 3 Input-Color Bit-Depth Options:
 - 24-bit RGB888 or 4:4:4 YCrCb888
 - 18-bit RGB666 or 4:4:4 YCrCb666
 - 16-bit RGB565 or 4:2:2 YCrCb
 - Supports 8-Bit BT.565 Bus Mode With Pixel Clock up to 33.5 MHz
- **Pattern Input Mode**
 - One-to-One Mapping of Input Data to Micromirrors
 - 1-Bit Binary Pattern Rates up to 4000-Hz
 - 8-Bit Grayscale Pattern Rates up to 120-Hz
- **Video Input Mode with Pixel Data Processing**
 - Supports 1Hz to 60Hz Frame Rates
 - Programmable Degamma
 - Spatial-Temporal Multiplexing (Dithering)
 - Automatic Gain Control
 - Color Space Conversion
- **Output Trigger Signal for Synchronizing with Camera, Sensor, or Other Peripherals**
- **External Memory Support:**
 - 166-MHz Mobile DDR SDRAM
 - 33.3-MHz Serial FLASH
- **Solid-State Illumination Interface (LED):**
 - Supports Three Independent Channels, E.g., Red, Green, and Blue LEDs
- **System Control:**
 - I²C Interface for Device Control
 - Programmable Splash Screens
 - Programmable LED Current and Sync Control
 - Integrated DMD Reset Driver Circuitry to Simplify System Design

1.2 Applications

- Machine Vision
- Industrial Inspection
- 3D Modeling/Design
- Automated Fingerprint Identification
- Facial Recognition
- Dental Scanning
- Orthopaedics
- Prosthetics
- Augmented Reality
- Embedded Display
- Interactive Display
- Information Overlay
- Photo-Stimulation
- Virtual Gauges

1.3 Purpose

This document provides a description of the 0.3 WVGA chipset components and function, interconnect information for the individual chipset components, and system-level design guidelines to ensure proper function of the 0.3 WVGA chipset components.



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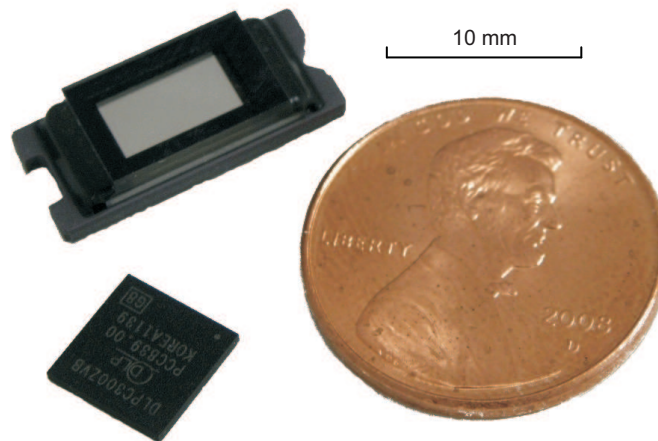
1.4 Related Documents

DOCUMENT	TI LITERATURE NUMBER
<i>DLP3000 0.3 WVGA Series 220 DMD data sheet</i>	DLPS022
<i>DLPC300 Digital Controller for the DLP3000 data sheet</i>	DLPS023
<i>DLPC300 Programmer's Guide</i>	DLPU004

2 Glossary

DDR	Double data rate
LVDS	Low-voltage differential signaling
DLP®	Digital light processing
DMD	Digital micromirror device
DVI	Digital video interface
WVGA	Wide VGA (video graphics array), 854 × 480 resolution
PROM	Programmable read-only memory
PWM	Pulse width modulation
SDRAM	Synchronous dynamic random-access memory
SPI	Serial peripheral interface
USB	Universal serial bus
I²C	Inter-Integrated circuit bus, multi-master serial communication bus invented by Philips
EDID	Extended Display Identification Data
mDDR	Mobile Double-Data Rate RAM
RGB	Red, green, and blue
PCB	Printed circuit board

3 Device Description



The DLP 0.3 WVGA chipset consists of two individual components:

- [DLP3000](#) – 0.3 WVGA series 220 DMD
- [DLPC300](#) – DLP3000 controller

Plus two additional components:

- SPI serial configuration flash loaded with the DLPC300 Configuration and Support Firmware
- Mobile DDR SDRAM

Detailed specifications for the components can be found in the individual component data sheets.

Figure 3-1 illustrates the connectivity between the individual components in the chipset, which include the following internal chipset interfaces:

- DLPC300 to DLP3000 data and control interface (DMD pattern data)
- DLPC300 to DLP3000 micromirror array reset control interface
- DLPC300 to mobile DDR SDRAM
- DLPC300 to SPI serial flash

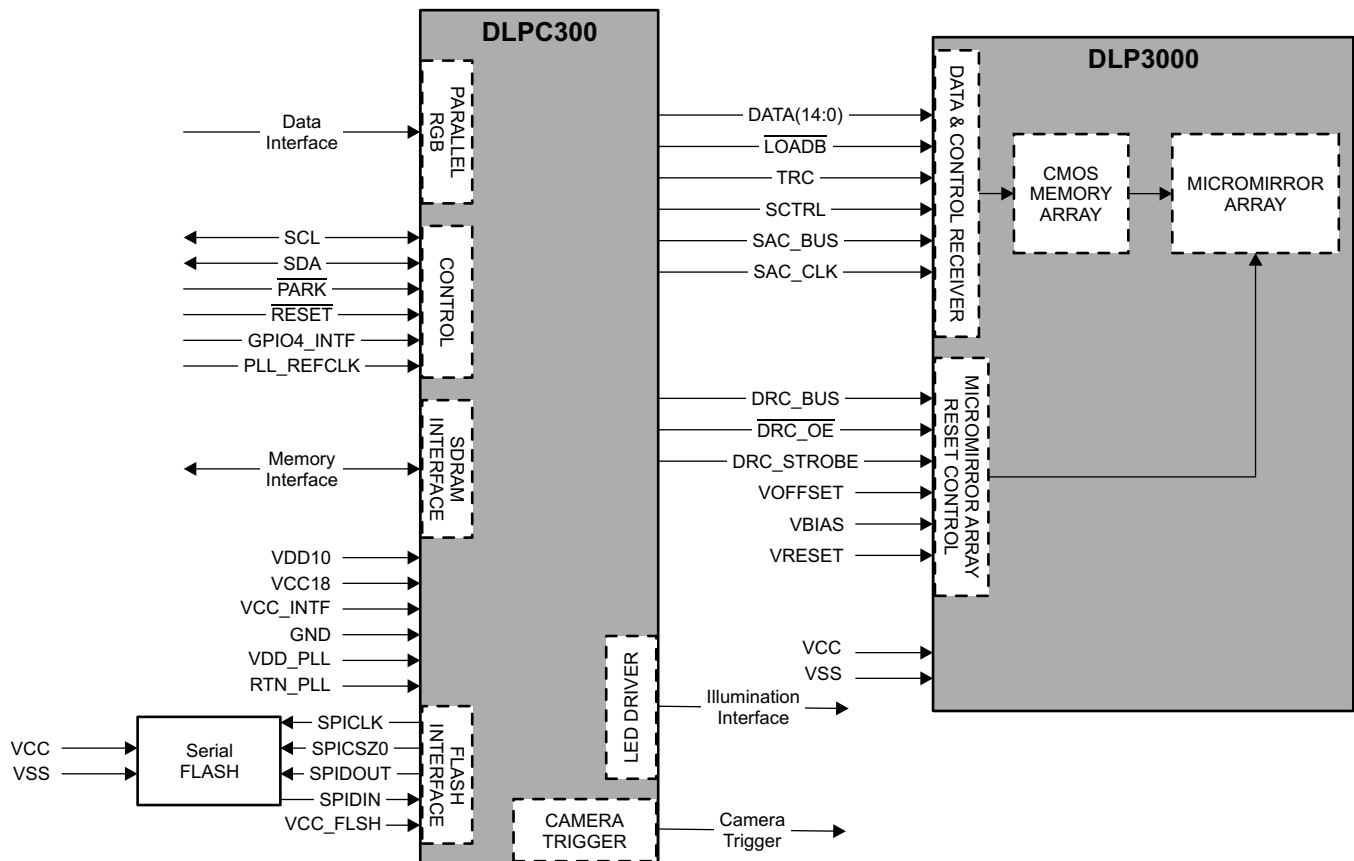


Figure 3-1. Chipset Block Diagram

Figure 3-2 illustrates the connectivity between the chipset and other key system-level components, which include the following external chipset interfaces:

- Data Interface, consisting of:
 - 24-bit data bus (PDATA[23:0])
 - Vertical sync signal (VSYNC)
 - Horizontal sync signal (HSYNC)
 - Data valid signal (DATAEN)
 - Data clock signal (PCLK)
 - Data mask (PDM)
- Control Interface, consisting of:
- I²C signals (SCL and SDA)
 - Park signal (PARK)
 - Reset signal (RESET)
 - Oscillator signals (PLL_REFCLK)
- Mobile DDR SDRAM interface (mDDR)

- Serial configuration flash interface
- Illumination driver control interface

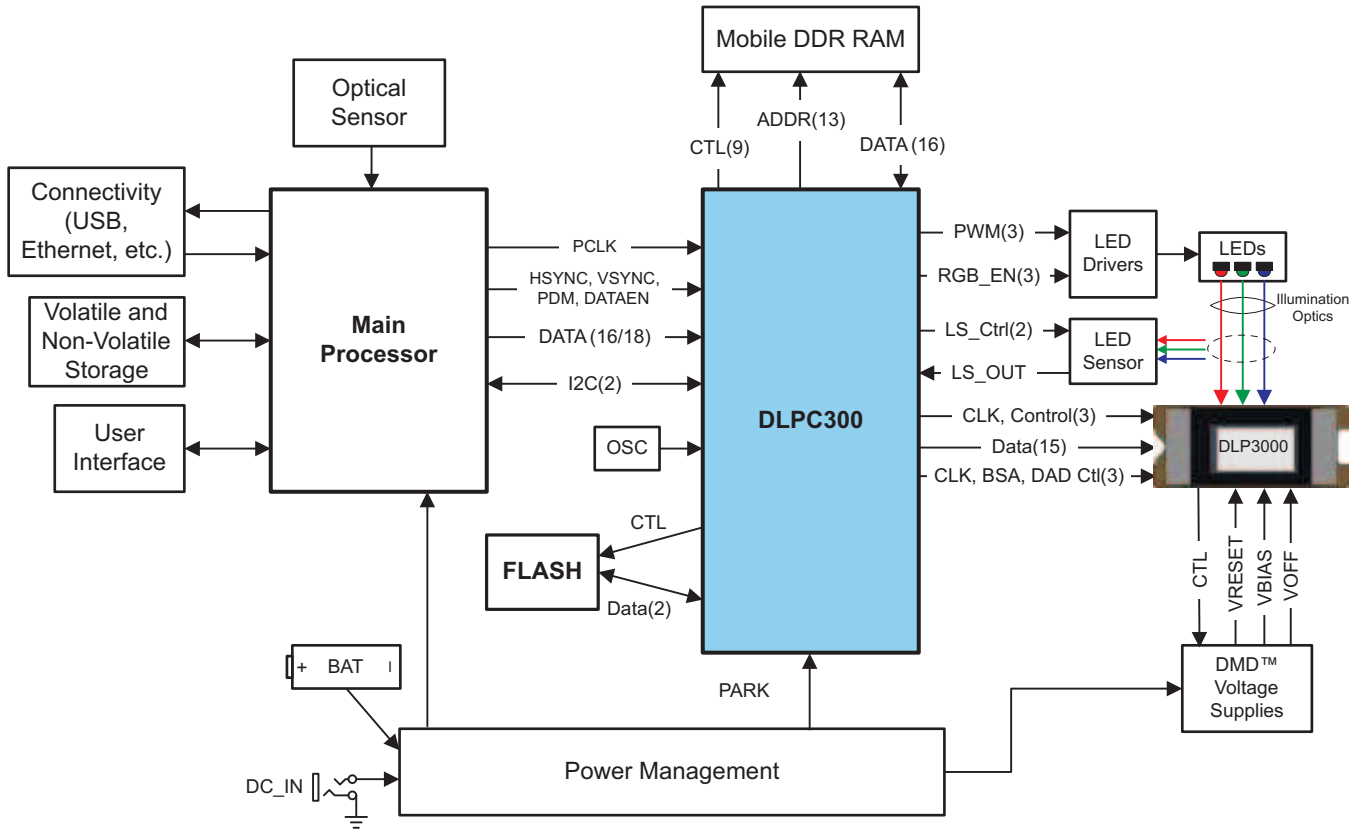


Figure 3-2. System Block Diagram

4 Control Interface

The 0.3 WVGA chipset is supported by a set of I²C commands to control its operation. The I²C commands allow users to control in real-time or configure the 0.3 WVGA chipset. For example, the I²C commands have functions to set the LED drive current or display splash screens stored in serial flash memory.

For more details about the specific functions and features, see the *DLPC300 Programmers Guide*, TI literature number [DLPU004](#). Other related documents are listed in [Section 1.4](#).

5 System Input Interfaces

The 0.3 WVGA Chipset supports a single 24-bit parallel RGB interface for data transfers from another device. The system input also requires that proper configuration of the $\overline{\text{PARK}}$ and $\overline{\text{RESET}}$ inputs to ensure reliable operation.

See the DLPC300 data sheet (TI literature number [DLPS023](#)) for detailed specifications for each of the following interfaces.

5.1 Data Interface

The data Interface is a digital video input port with up to 24-bit RGB, and has a nominal I/O voltage of 3.3 V. The data interface also supports a 24-bit BT656 video interface. As shown in [Figure 3-2](#) (system block diagram), the data Interface can be configured to connect to a video decoder device or an external processor through an 8-, 16-, 18-, or 24-bit parallel interface.

[Table 5-1](#) provides a description of the signals associated with the data interface.

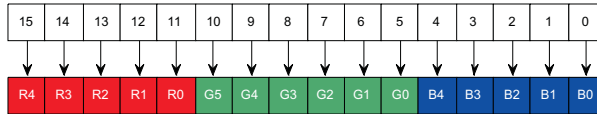
Table 5-1. Active Signals – Data Interface

SIGNAL NAME	DESCRIPTION
PDATA(0:23)	24-bit data inputs (8 bits for each of the red, green, and blue channels)
PCLK	Pixel clock; all input signals on data interface are synchronized with this clock.
VSYNC	Vertical sync
HSYNC	Horizontal sync
DATAEN	Input data valid
PDM	Parallel data mask

Maximum and minimum input timing specifications are provided in the Parallel Interface Timing Requirements of the DLPC300 data sheet. The mapping of the red-, green-, and blue-channel data bits is shown in Figure 5-1.

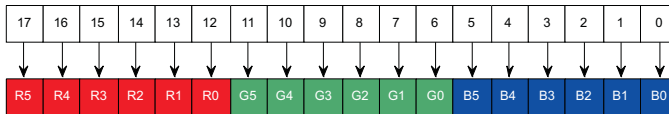
Parallel Bus Mode – RGB 4:4:4 Source

PDATA(15:0) – RGB565 Mapping to RGB888



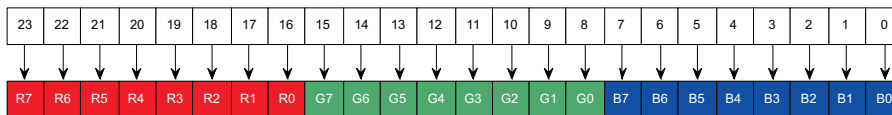
PDATA(15:0) of the Input Pixel data bus
 Bus Assignment Mapping
 Data bit mapping on the DLPC300

PDATA(17:0) – RGB666 Mapping to RGB888



PDATA(17:0) of the Input Pixel data bus
 Bus Assignment Mapping
 Data bit mapping on the DLPC300

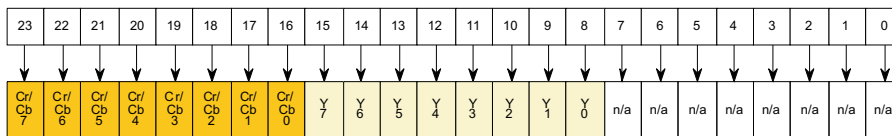
PDATA(23:0) – RGB888 Mapping



PDATA(23:0) of the Input Pixel data bus
 Bus Assignment Mapping
 Data bit mapping on the DLPC300

Parallel Bus Mode - YCrCb 4:2:2 Source

PDATA(23:0) – Cr/CbY880 Mapping

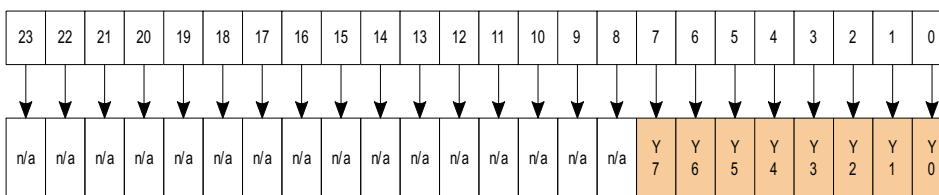


PDATA(23:0) of the Input Pixel data bus
 Bus Assignment Mapping
 Data bit mapping on the pins of the DLPC300

Figure 5-1. Parallel Interface Mode Bit Mapping

BT.656 Bus Mode - YCrCb 4:2:2 Source

PDATA(23:0) - BT.656 Mapping



PDATA(7:0) of the Input Pixel data bus
 Bus Assignment Mapping
 Data bit mapping on the pins of the ASIC

Figure 5-2. BT.656 Interface Mode Bit Mapping

5.2 Control Interface

The 0.3 WVGA chipset supports I²C commands through the control interface. The control interface allows another master processor to send commands to the 0.3 WVGA chipset to query system status or perform real-time operations, such as, LED driver current settings. The DLPC300 offers two different slave addresses. The I2C_ADDR_SEL pin provides the ability to select an alternate set of 7-bit I²C slave address. If I2C_ADDR_SEL is low, then the DLPC300 slave address is 1Bh. If I2C-ADDR_SEL pin is high, then the DLPC300 slave address is 1Dh. See the *DLPC300 Programmer's Guide* (TI literature number [DLPA014](#)) for detailed information about these operations.

Table 5-2 provides a description for active signals used by the DLPC300 to support the I²C interface.

Table 5-2. Active Signals – I²C Interface

SIGNAL NAME	DESCRIPTION
SCL	I ² C clock. Bidirectional open-drain signal
SDA	I ² C data. Bidirectional open-drain signal

6 System Output Interfaces

There are two primary output interfaces: illumination driver control interface and sync outputs.

6.1 Illumination Interface

An illumination interface is provided that supports up to a three (3) channel LED driver.

The illumination interface provides signals that support: LED driver enable, LED enable, LED enable select, and PWM signals to control the LED current. [Table 6-1](#) describes the active signals for the illumination interface.

Table 6-1. Active Signals – Illumination Interface

SIGNAL NAME	DESCRIPTION
LED_ENABLE	LED enable
LEDDRIV_ON	LED driver master enable
LED_SEL(1:0)	Red, Green, or Blue LED enable select
RED_EN	Red LED enable
GREEN_EN	Green LED enable
BLUE_EN	Blue LED enable
RPWM	Red LED PWM signal used to control the LED current
GPWM	Green LED PWM signal used to control the LED current
BPWM	Blue LED PWM signal used to control the LED current

7 System Support Interfaces

There are three system support interfaces provided by the 0.3 WVGA chipset:

- Mobile DDR synchronous DRAM (mDDR)
- Serial configuration non-volatile FLASH
- System reference clock

7.1 DLPC300 Reference Clock

The DLPC300 requires a 16.667-MHz 1.8-V external input from an oscillator. This signal is the 0.3 WVGA chipset reference clock from which the majority of the interfaces derive their timing. This includes mDDR SDRAM, DMD interfaces, and serial interfaces.

See the DLPC300 data sheet (TI literature number DLPS023) for reference clock specifications.

7.2 Mobile DDR Synchronous DRAM (mDDR)

The 0.3 WVGA chipset relies on the use of mobile DDR SDRAM to store DMD formatted patterns. The SDRAM interface is a 16-bit wide bus and nominally operates at a frequency of 166 MHz. The data bus is routed in a point-to-point fashion between the DLPC300 and the mDDR devices, where each data line only makes a single connection between the DLPC300 and the mDDR device.

Listed below are the compatibility requirements for the mDDR:

SDRAM memory Type: Mobile DDR

Size: 128 M-bit minimum. DLPC300 can only address 128 Mb . Use of larger memories requires bit A13 to be grounded

Organization: N x 16-bits wide with 4 equally sized banks

Burst Length: 4

Refresh period: ≥ 64 ms

Speed Grade t_{CK} : 6 ns max

CAS Latency (C_L): 3 clocks

t_{RCD} : 3 clocks

t_{RP} : 3 clocks

Table 7-1 describes the signals for the SDRAM interface.

Table 7-1. Active Signals – Mobile DDR Synchronous DRAM (mDDR)

SIGNAL NAME	DESCRIPTION
MEM_A(0:12)	13-bit address bus
MEM_BA(0:1)	Bank select signals
MEM_CKE	Clock enable
MEM_CAS	Column address strobe
MEM_RAS	Row address strobe
MEM_CS	Chip select
MEM_WE	Write enable
MEM_LDQS	R/W data strobe for lower byte
MEM_LDM	Write data mask for lower byte
MEM_UDQS	R/W data strobe for upper byte
MEM_UDM	Write data mask for upper byte
MEM_DQ(0:15)	16-bit data bus
MEM_CLK_N	Negative signal of the differential clock pair
MEM_CLK_P	Positive signal of the differential clock pair

7.3 DLPC300 Serial Configuration Flash PROM

The DLPC300 requires configuration information to be available at each system power up. The serial configuration FLASH PROM stores the system design configuration default settings of the 0.3 WVGA chipset. The actual configuration file can be downloaded from [DLPR300 product folder](#). This configuration file is for a 64-Mbit serial FLASH PROM.

The serial FLASH PROM can be programmed by holding the DLPC300 in reset (driving DLPC300's $\overline{\text{RESET}}$ pin low). When the DLPC300 is in reset, the SPI interface is tri-stated, allowing another device to drive the SPI signals to program the serial FLASH PROM.

DLPC300 uses a fixed SPI clock and does not support the normal (slow) read opcode. The DLPC300 also assumes the SPI FLASH supports address auto-incrementing for all read operations. The DLPC300 does not have any specific page, block or sector size requirements.

The DLPC300 does not drive the HOLD (active-low hold) or WP (active-low write protect) pins on the flash device, and thus these pins should be tied to a logic high on the PCB via an external pullup.

The DLPC300 supports 1.8-, 2.5- or 3.3-V serial FLASH devices with a separate supply for the FLASH interface, VCC_FLASH. Therefore, VCC_FLASH must be supplied with the corresponding voltage.

[Table 7-2](#) describes the signals used to support this interface.

Table 7-2. Active Signals – DLPC300 Serial Configuration Flash PROM

SIGNAL NAME	DESCRIPTION
SPIDOUT	Serial configuration flash data output (from DLPC300 to flash)
SPIDIN	Serial configuration flash data input (from flash to DLPC300)
SPICLK	Serial configuration flash clock
$\overline{\text{SPICSO}}$	Serial configuration flash chip select

See [Figure 3-1](#) for detailed connection between the DLPC300 and serial flash PROM.

7.4 DLPC300 Reference Clock

The DLPC300 requires a 16.667-MHz, 1.8-V crystal for its reference clock. This is the 0.3 WVGA chipset reference clock from which the majority of interfaces derive their clock, including mDDR and DMD interfaces.

See the DLPC300 data sheet (TI literature number [DLPS023](#)) for reference clock specifications.

8 DMD Interfaces

8.1 DLPC300 to DLP3000 Digital Data

The DLPC300 provides the DMD pattern data to the DMD over a double data rate (DDR) interface.

[Table 8-1](#) describes the signals used for this interface.

Table 8-1. Active Signals – DLPC300-to-DLP3000 Digital Data Interface

DLPC300 SIGNAL NAME	DLP3000 SIGNAL NAME
DMD_D(14:0)	DATA(14:0)
DMD_DCLK	DCLK

8.2 DLPC300-to-DLP3000 Control Interface

The DLPC300 provides the control data to the DMD over a serial bus.

[Table 8-2](#) describes the signals used for this interface.

Table 8-2. Active Signals – DLPC300 to DLP3000 Control Interface

DLPC300 SIGNAL NAME	DLP3000 SIGNAL NAME	DESCRIPTION
DMD_SAC_BUS	SAC_BUS	DMD stepped-address control (SAC) bus data
DMD_SAC_CLK	SAC_CLK	DMD stepped-address control (SAC) bus clock
$\overline{\text{DMD_LOADB}}$	$\overline{\text{LOADB}}$	DMD data load signal
DMD_SCTRL	SCTRL	DMD data serial control signal
DMD_TRC	TRC	DMD data toggle rate control

8.3 DLPC300-to-DLP3000 Micromirror Reset Control Interface

The DLPC300 controls the micromirror clock pulses in a manner to ensure proper and reliable operation of the DMD.

[Table 8-3](#) describes the signals used for this interface.

Table 8-3. Active Signals – DLPC300-to-DLP3000 Micromirror Reset Control Interface

DLPC300 SIGNAL NAME	DLP3000 SIGNAL NAME	DESCRIPTION
DMD_DRC_BUS	DRC_BUS	DMD reset control serial bus
$\overline{\text{DMD_DRC_OE}}$	$\overline{\text{DRC_OE}}$	DMD reset control output enable
DMD_DRC_STRB	DRC_STRB	DMD reset control strobe

9 Printed Circuit Board (PCB) System Design Considerations for mDDR and DMD Interfaces

The 0.3 WVGA chipset is a high-performance (high-frequency and high-bandwidth) set of components. This section provides PCB guidelines to ensure proper operation of the 0.3 WVGA chipset with respect to the mobile DDR memory and the DMD interface.

9.1 Printed Circuit Board Design Guidelines

The PCB design may vary depending on system design. The following table provides general recommendations on the PCB design.

Table 9-1. PCB General Recommendations for mDDR and DMD Interfaces

DESCRIPTION	RECOMMENDATION
Configuration	Asymmetric dual stripline
Etch thickness (T)	0.5-oz. (0.18-mm thick) copper
Single-ended signal impedance	50 Ω (\pm 10%)
Differential signal impedance	100 Ω differential (\pm 10%)

9.2 Printed Circuit Board Layer Stackup Geometry

The PCB layer stack may vary depending on system design. However, careful attention is required in order to meet design considerations listed in the following sections. [Table 9-2](#) provides general guidelines for the mDDR and DMD interface stackup geometry.

Table 9-2. PCB Layer Stackup Geometry for mDDR and DMD Interfaces

PARAMETER	DESCRIPTION	RECOMMENDATION
Reference plane 1	Ground plane for proper return	
Er	Dielectric FR4	4.2 (nominal)
H1	Signal trace distance to reference plane 1	5 mil (0.127 mm)
H2	Signal trace distance to reference plane 2	34.2 mil (0.869 mm)
Reference plane 2	I/O power plane or ground	

9.3 Signal Layers

The PCB signal layers should follow these recommendations:

- Layer changes should be minimized for single-ended signals.
- Individual differential pairs can be routed on different layers, but the signals of a given pair should not change layers.
- Stubs should be avoided.
- Only voltage or low-frequency signals should be routed on the outer layers, except as noted previously in this document.
- Double data rate signals should be routed first.

9.4 Routing Constraints

In order to meet the specifications listed in the following tables, typically the PCB designer must route these signals manually (not using automated PCB routing software). In case of length matching requirements, the longer signals should be routed in a serpentine fashion, keeping the number of turns to a minimum and the turn angles no sharper than 45 degrees. Avoid routing long traces all around the PCB.

Table 9-3. Signal Length Routing Constraints for mDDR and DMD Interfaces

SIGNALS	MAX SIGNAL SINGLE-BOARD ROUTING LENGTH	MAX SIGNAL MULTI-BOARD ROUTING LENGTH
DMD_D(14:0), DMD_CLK, DMD_TRC, DMD_SCTRL, DMD_LOADB, DMD_OE, DMD_DRC_STRB, DMD_DRC_BUS, DMD_SAC_CLK, and DMD_SAC_BUS	4 in (10.15 cm)	3.5 in (8.8891 cm)
MEM_CLK_P, MEM_CLK_N, MEM_A(12:0), MEM_BA(1:0), MEM_CKE, MEM_CS, MEM_RAS, MEM_CAS, and MEM_WE	2.5 in (6.35 cm)	Not recommended
MEM_DQ(15:0), MEM_LDM, MEM_UDM, MEM_LDQS, MEM_UDQS	1.5 in (3.81 cm)	Not recommended

Each high-speed, single-ended signal must be routed in relation to its reference signal, such that a constant impedance is maintained throughout the routed trace. Avoid sharp turns and layer switching while keeping lengths to a minimum. The following signals should follow these signal matching requirements.

Table 9-4. High-Speed Signal Matching Requirements for mDDR and DMD Interfaces

SIGNALS	REFERENCE SIGNAL	MAX MISMATCH	UNIT
DMD_D(14:0), DMD_TRC, DMD_SCTRL, DMD_LOADB, DMD_OE,	DMD_DCLK	±500 (12.7)	mil (mm)
DMD_DRC_STRB, DMD_DRC_BUS	DMD_DCLK	±750 (19.05)	mil (mm)
DMD_SAC_CLK	DMD_DCLK	±500 (12.7)	mil (mm)
DMD_SAC_BUS	DMD_SAC_CLK	±750 (19.05)	mil (mm)
MEM_CLK_P	MEM_CLK_N	±150 (3.81)	mil (mm)
MEM_DQ(7:0), MEM_LDM	MEM_LDQS	±300 (7.62)	mil (mm)
MEM_DQ(15:8), MEM_UDM	MEM_UDQS	±300 (7.62)	mil (mm)
MEM_A(12:0), MEM_BA(1:0), MEM_CKE, MEM_CS, MEM_RAS, MEM_CAS, MEM_WE	MEM_CLK_P, MEM_CLK_N	±1000 (25.4)	mil (mm)
MEM_LDQS, MEM_UDQS	MEM_CLK_P, MEM_CLK_N	±300 (7.62)	mil (mm)

9.5 Termination Requirements

Table 9-5 lists the termination requirements for the DMD and mDDR interfaces.

For applications where the routed distance of the mDDR or DMD signal can be kept less than 0.75 inches, then this signal is short enough not to be considered a transmission line and should not need a series terminating resistor.

Table 9-5. Termination Requirements for mDDR and DMD Interfaces

SIGNALS	SYSTEM TERMINATION
DMD_D(14:0), DMD_CLK, DMD_TRC, DMD_SCTRL, DMD_LOADB, DMD_DRC_STRB, DMD_DRC_BUS, DMD_SAC_CLK, and DMD_SAC_BUS	Terminated at source with 10-Ω to 30-Ω series resistor. 30 Ω is recommended for most applications as this minimizes over/under-shoot and reduces EMI.
MEM_CLK_P and MEM_CLK_N	Terminated at source with 30-Ω series resistor. The pair should also be terminated with an external 100-Ω differential termination across the two signals as close to the mDDR as possible.

Table 9-5. Termination Requirements for mDDR and DMD Interfaces (continued)

SIGNALS	SYSTEM TERMINATION
MEM_DQ(15:0), MEM_LDM, MEM_UDM, MEM_LDQS, MEM_UDQS	Terminated with 30-Ω series resistor located midway between the two devices
MEM_A(12:0), MEM_BA(1:0), MEM_CKE, MEM_CS, MEM_RAS, MEM_CAS, and MEM_WE	Terminated at the source with a 30-Ω series resistor

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