

MSP432P401Y Device Erratasheet

The revision of the device can be identified by the revision letter on the [Package Markings](#) or by the [HW_ID](#) located inside the TLV structure of the device

1 Functional Errata Revision History

Errata impacting device's operation, function or parametrics.

✓ The check mark indicates that the issue is present in the specified revision.

Errata Number	Rev A
PORT31	✓
PORT32	✓
PORT34	✓
USCI42	✓
USCI45	✓
USCI47	✓
USCI50	✓
USCI51	✓

2 Preprogrammed Software Errata Revision History

Errata impacting pre-programmed software into the silicon by Texas Instruments.

✓ The check mark indicates that the issue is present in the specified revision.

Errata Number	Rev A
UDMA2	✓

3 Debug only Errata Revision History

Errata only impacting debug operation.

✓ The check mark indicates that the issue is present in the specified revision.

The device doesn't have Debug errata.

4 Fixed by Compiler Errata Revision History

Errata completely resolved by compiler workaround. Refer to specific erratum for IDE and compiler versions with workaround.

✓ The check mark indicates that the issue is present in the specified revision.

The device doesn't have Compiler-Fixed errata.

5 Package Markings


PZ100

LQFP (PZ) 100 Pin

<div style="display: flex; align-items: center;"> <div style="margin-right: 10px;">○</div> <div style="text-align: left;"> <p>MSP432™</p> <p>Pxxxx</p> <p>TI NNN #</p> <p>NNNN <u>G4</u></p> </div> </div>	<table style="border: none;"> <tr> <td>#</td> <td>= Die revision</td> </tr> <tr> <td>○</td> <td>= Pin 1 location</td> </tr> <tr> <td>N</td> <td>= Lot trace code</td> </tr> </table>	#	= Die revision	○	= Pin 1 location	N	= Lot trace code
#	= Die revision						
○	= Pin 1 location						
N	= Lot trace code						

RGC64

QFN (RGC), 64 pin

<div style="display: flex; align-items: center;"> <div style="margin-right: 10px;">  </div> <div style="text-align: left;"> <p>NNNNNNNG4</p> <p>MSP432xxxx</p> <p>Rev #</p> </div> </div> <div style="margin-top: 10px;">○</div>	<table style="border: none;"> <tr> <td>#</td> <td>= Die revision</td> </tr> <tr> <td>○</td> <td>= Pin 1 location</td> </tr> <tr> <td>N</td> <td>= Lot trace code</td> </tr> </table>	#	= Die revision	○	= Pin 1 location	N	= Lot trace code
#	= Die revision						
○	= Pin 1 location						
N	= Lot trace code						

6 Memory-Mapped Hardware Revision (TLV Structure)

Die Revision	TLV Hardware Revision
Rev A	41h

Further guidance on how to locate the TLV structure and read out the HW_ID can be found in the device User's Guide.

7 Detailed Bug Description

PORT31	<i>PORT Module</i>
Category	Functional
Function	Fast transient noise on GPIOs may result in a constant high current
Description	<p>GPIOs subject to fast transient noise (e.g. electromagnetic noise) may see a high constant current. The constant high current is a result of the fast transient noise triggering the internal ESD protection structure and it persists as long as the internal or external current driver sustains the current.</p> <ol style="list-style-type: none"> 1. When using in Input mode (PxDIR = 0), all GPIOs are impacted by this issue. A fast transient noise on the pin configured as an input or on an adjacent pin could cause a constant high current that is sustained as long as the external driver is present. 2. When using in Output mode (PxDIR = 1), only the high drive GPIOs (P2.0,P2.1,P2.2 and P2.3) are impacted by this issue. If the affected GPIOs are configured in high drive mode (PxDS register) and they (or adjacent pins) are subject to fast transient noise, it could cause a constant high current. Note that this issue is not seen in GPIOs configured in the output direction with the regular drive strength setting since the high drive mode is required to sustain the high current. <p>If the GPIO configuration is reset by a power cycle, the constant high current is no longer sustained.</p>
Workaround	<ol style="list-style-type: none"> 1. For GPIOs configured as input, ensure that they are driven by a current-limited source < 30mA (up to Tj=85C) or 20mA (up to Tj=125C, if allowed for device. See device specific datasheet for maximum allowed operating junction temperature) OR use a series resistance >100 ohm (up to Tj=85C) or 150 ohm (up to Tj=125C, if allowed for device. See device specific datasheet for maximum allowed operating junction temperature) to limit the current. 2. For high drive GPIOs configured as output, ensure adequate protection from fast transients is provided to both the high drive IOs and any adjacent pins. 3. In general, it is recommended to terminate any unused GPIOs in the output direction, driving low to minimize the occurrence of this issue. 4. For guidelines on ESD considerations refer to the document: MSP430 System-level ESD Considerations SLAA530
PORT32	<i>PORT Module</i>
Category	Functional
Function	Sucessive writes to port registers may cause interrupt to pend incorrectly
Description	<p>Writing to the PxIES register sets the corresponding PxIFG bit. The PxIFG bit can be cleared by writing '0' to it (clearing the register).</p> <p>However if the PxIFG bit is cleared immediately (next instruction cycle) after writing to the PxIES register, the interrupt flag does not clear and stays pending.</p>
Workaround	Insert a NOP or <code>__no_operation()</code> ; instruction after writing to the PxIES register and before clearing the PxIFG register.
PORT34	<i>PORT Module</i>
Category	Functional

Function	Timer_A1 & A2 outputs and EUSCIB3 pins should not be used simultaneously
Description	<p>The following pin functions cannot be simultaneously active on the device at any pin:</p> <ol style="list-style-type: none"> 1) TA1.0 and UCB3STE 2) TA2.0 and UCB3CLK 3) TA2.3 and UCB3SIMO 4) TA2.4 and UCB3SOMI <p>Attempting to use both pin's secondary functions will cause functional conflicts and abnormal behavior of the peripherals. For example, using Timer_A2.3 output will prevent proper operation of EUSCIB3SIMO.</p>
Workaround	None.
<hr/>	
UDMA2	<i>DMA Module</i>
Category	Software in ROM
Function	UDMA driver library versions < 4.20.00.03 (SimpleLink MSP432P4 SDK versions < 2.10.00.14) do not support use case where increment size and transfer size are different.
Description	UDMA driver library APIs with versions < 4.20.00.03 (SimpleLink MSP432P4 SDK versions < 2.10.00.14) do not support use cases where increment size and transfer sizes are different for either the source or destination. The addresses computation are performed wrongly and this result in erroneous data transfers.
Workaround	<p>This is fixed in driver library API versions \geq 4.20.00.03 (SimpleLink MSP432P4 SDK versions \geq 2.10.00.14).</p> <ul style="list-style-type: none"> - For TI Drivers users, update to SDK version 2.10.00.14 and TI Drivers based applications automatically leverage the bug fix. - For Driver Library users, update to SDK version 2.10.00.14 and ensure that the application code uses MAP_DMA_ function calls for Driverlib DMA [instead of direct DMA_API calls].
<hr/>	
USCI42	<i>eUSCI Module</i>
Category	Functional
Function	UART asserts UCTXCPITIFG after each byte in multi-byte transmission
Description	UCTXCPTIFG flag is triggered at the last stop bit of every UART byte transmission, independently of an empty buffer, when transmitting multiple byte sequences via UART. The erroneous UART behavior occurs with and without DMA transfer.
Workaround	None.
<hr/>	
USCI45	<i>eUSCI Module</i>
Category	Functional
Function	Unexpected SPI clock stretching possible when UCxCLK is asynchronous to MCLK
Description	In rare cases, during SPI communication, the clock high phase of the first data bit may be stretched significantly. The SPI operation completes as expected with no data loss. This issue only occurs when the USCI SPI module clock (UCxCLK) is asynchronous to the system clock (MCLK).

Workaround	Ensure that the USCI SPI module clock (UCxCLK) and the CPU clock (MCLK) are synchronous to each other.
USCI47	<i>eUSCI Module</i>
Category	Functional
Function	eUSCI SPI slave with clock phase UCCKPH = 1
Description	<p>The eUSCI SPI operates incorrectly under the following conditions:</p> <ol style="list-style-type: none"> 1. The eUSCI_A or eUSCI_B module is configured as a SPI slave with clock phase mode UCCKPH = 1 <p>AND</p> <ol style="list-style-type: none"> 2. The SPI clock pin is not at the appropriate idle level (low for UCCKPL = 0, high for UCCKPL = 1) when the UCSWRST bit in the UCxxCTLW0 register is cleared. <p>If both of the above conditions are satisfied, then the following will occur:</p> <p>eUSCI_A: the SPI will not be able to receive a byte (UCAxRXBUF will not be filled and UCRXIFG will not be set) and SPI slave output data will be wrong (first bit will be missed and data will be shifted).</p> <p>eUSCI_B: the SPI receives data correctly but the SPI slave output data will be wrong (first byte will be duplicated or replaced by second byte).</p>
Workaround	<p>Use clock phase mode UCCKPH = 0 for MSP SPI slave if allowed by the application.</p> <p>OR</p> <p>The SPI master must set the clock pin at the appropriate idle level (low for UCCKPL = 0, high for UCCKPL = 1) before SPI slave is reset (UCSWRST bit is cleared).</p> <p>OR</p> <p>For eUSCI_A: to detect communication failure condition where UCRXIFG is not set, check both UCRXIFG and UCTXIFG. If UCTXIFG is set twice but UCRXIFG is not set, reset the MSP SPI slave by setting and then clearing the UCSWRST bit, and inform the SPI master to resend the data.</p>
USCI50	<i>eUSCI Module</i>
Category	Functional
Function	Data may not be transmitted correctly from the eUSCI when operating in SPI 4-pin master mode with UCSTEM = 0
Description	When the eUSCI is used in SPI 4-pin master mode with UCSTEM = 0 (STE pin used as an input to prevent conflicts with other SPI masters), data that is moved into UCxTXBUF while the UCxSTE input is in the inactive state may not be transmitted correctly. If the eUSCI is used with UCSTEM = 1 (STE pin used to output an enable signal), data is transmitted correctly.
Workaround	When using the STE pin in conflict prevention mode (UCSTEM = 0), only move data into UCxTXBUF when UCxSTE is in the active state. If an active transfer is aborted by UCxSTE transitioning to the master-inactive state, the data must be rewritten into UCxTXBUF to be transferred when UCxSTE transitions back to the master-active state.
USCI51	<i>eUSCI Module</i>
Category	Functional

Function	UART could lose bytes while transmitting with DMA
Description	Accessing the RXIFG (which is at the same address as the TXIFG) while transmitting with the DMA, could cause a second interrupt for the DMA and overwrite the transmit buffer, before moving to the Shift register.
Workaround	Clear pending UART RX-interrupt flags with dummy read and enable RX-interrupt as the below example code: <pre>volatile uint8_t temp; temp = EUSCI_A_CMSIS(EUSCI_A2_BASE)->RXBUF; MAP_UART_enableInterrupt(EUSCI_A2_BASE, EUSCI_A_UART_RECEIVE_INTERRUPT);</pre>

8 Document Revision History

Changes from device specific erratasheet to document Revision A.

1. Device name changed from "XMS" to "MSP430"
2. BSL17 was removed from the errata documentation.
3. TA23 was removed from the errata documentation.
4. USCI44 was removed from the errata documentation.
5. SYSCTLA1 was removed from the errata documentation.
6. COMP11 was removed from the errata documentation.
7. RTC14 was removed from the errata documentation.
8. USCI43 was removed from the errata documentation.
9. USCI47 was added to the errata documentation.

Changes from document Revision A to Revision B.

1. PORT34 was added to the errata documentation.
2. USCI50 was added to the errata documentation.
3. Function for USCI45 was updated.
4. Workaround for PORT31 was updated.

Changes from document Revision B to Revision C.

1. Erratasheet format update.
2. Added errata category field to "Detailed bug description" section

Changes from document Revision C to Revision D.

1. UDMA2 was added to the errata documentation.

Changes from document Revision D to Revision E.

1. USCI51 was added to the errata documentation.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to TI's Terms of Sale (www.ti.com/legal/termsofsale.html) or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2019, Texas Instruments Incorporated