TMS320LF2407

DSP Controller

Silicon Errata

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TEXAS INSTRUMENTS

Contents

1 Introduction

This document describes the silicon updates to the functional specifications for the TMS320LF2407 DSP Controller, silicon revisions 1.0 ,1.1, 1.2, 1.3, 1.4, and 1.6. The updates are applicable to:

- TMS320LF2407 (144-pin LQFP, PGE suffix)

1.1 Quality and Reliability Conditions

TMX Definition

Texas Instruments (TI) does not warranty either (1) electrical performance to specification, or (2) product reliability for products classified as “TMX.” By definition, the product has not completed data sheet verification or reliability performance qualification according to TI Quality Systems Specifications.

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TMS Definition

Fully-qualified production device.

1.2 Revision Identification

The device revision can be determined by the lot trace code marked on the top of the package. The location of the lot trace code for the PGE package is shown in Figure 1.

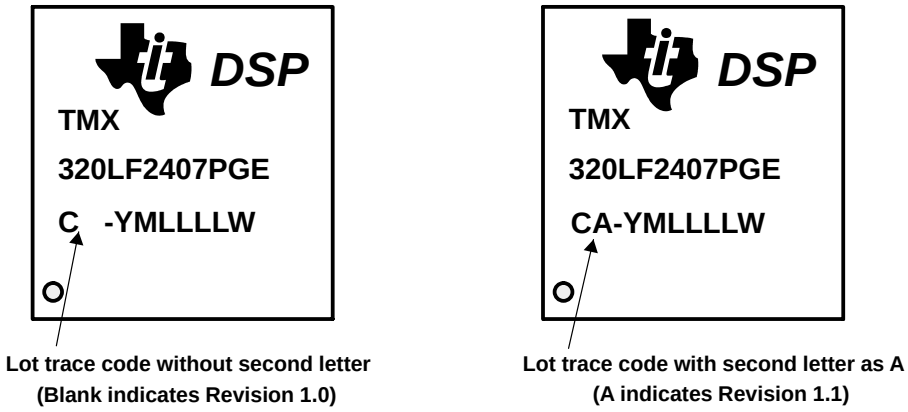

Figure 1. Example, Lot Trace Code for TMX320LF2407 (PGE)

Second Letter in Prefix of Lot Trace Code	Silicon Revision	Comments
Blank (no second letter in prefix)	Indicates Revision 1.0	This silicon revision is available as TMX only.
A (second letter in prefix is an “A”)	Indicates Revision 1.1	This silicon revision is available as TMX only.
B (second letter in prefix is a “B”)	Indicates Revision 1.2	This silicon revision is available as TMX only.
C (second letter in prefix is a “C”)	Indicates Revision 1.3	This silicon revision is available as TMS.
D (second letter in prefix is a “D”)	Indicates Revision 1.4	This silicon revision is available as TMS.
F (second letter in prefix is a “F”)	Indicates Revision 1.6	This silicon revision is available as TMS.

NOTE: There is no Revision 1.5 silicon.

2 Known Design Marginality/Exceptions to Functional Specifications

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Advisory *Internal Oscillator*

Revision(s) Affected: 1.0, 1.1, 1.2, 1.3, 1.4, and 1.6

Details: The internal oscillator of the 2407 device has a design marginality that may prevent the internal oscillator from starting upon power-up under certain conditions pertaining to board layout, ground bounce, and power-supply ramp rate. This is a concern only when the internal oscillator is used in conjunction with an external quartz crystal/ceramic resonator and not with an external oscillator.

Workaround: Use of a 1M-Ω resistor in parallel with the crystal across the XTAL1 and XTAL2 pins removes this condition.

Advisory *ADC – Calibration*

Revision(s) Affected: 1.0, 1.1, 1.2, 1.3, 1.4, and 1.6

Details: The automatic calibration feature of the 240x ADC module exhibits occasional inconsistencies and hence should be avoided. The calibration feature can still be used with the restriction that the three internal reference points (V_{REFLO}, V_{REFHI}, and midpoint) should not be used. Therefore, bits 3, 2, and 1 of the ADCTRL1 register should be treated as reserved and must always be written with zeroes. The functionality of bit 14 of the ADCTRL2 register is now restricted to RST_SEQ1 (i.e., to reset sequencer 1).

Workaround: The calibration feature should only be used in a “manual” configuration. The user should connect the signal of interest (whose value is known), for which the offset needs to be determined. Once the offset is determined, it can be written into the CALIBRATION register. All subsequent conversion results will be adjusted by the offset as before. There is no need to be in the calibration mode to be able to write to the CALIBRATION register.

Advisory *ADC – Self-Test*

Revision(s) Affected: 1.0, 1.1, 1.2, 1.3, 1.4, and 1.6

Details: The **self-test mode** of the ADC yields inconsistent results.

Workaround: The self-test mode should not be used. Bit 0 of ADCTRL1 should be treated as reserved and must always be written with zero.

Advisory	*ADC – Start of Conversion*

Revision(s) Affected: 1.0, 1.1, 1.2, 1.3, 1.4, and 1.6

Details: The **start of conversion** is unreliable when the Conversion Clock Prescale (CPS) bit in the ADCTRL1 register is 1, **and** when the acquisition prescaler is 0 (both conditions met). When CPS = 0, the ADC operation is not affected.

This bug only affects the ADC operation when the CPS bit is set (ADCCLK = CLKOUT ÷ 2). The bug causes the START signal, which is going to the analog portion of the A/D, to start a half-cycle of ADCCLK early and end a full cycle early. Thus, the acquisition window (which is the START signal plus one ADCCLK cycle) is a half-cycle shorter than it should be.

For the ACQ_PS3 to ACQ_PS0 bits (where ACQ_PSn = 1 through 15), this only affects the conversion time and source impedance. However, when ACQ_PSn = 0, a half-cycle shorter START bit causes the START signal to be active for only a half-cycle ... not long enough to ensure that a conversion will occur.

Workaround: ACQ_PS = 0 should **not** be used in conjunction with CPS = 1. This will be fixed in the 240xA silicon.

Advisory	*CAN – AME and AAM Bits Get Corrupted Upon Reception*

Revision(s) Affected: 1.0, 1.1, 1.2, 1.3, 1.4, and 1.6

Details: This problem surfaces only when “message filtering” or “automatic answer mode” is used. It applies to any mailbox configured for reception or for mailboxes configured for “automatic reply” to remote requests. It affects the AAM and AME bits of a mailbox after a data frame (or a remote frame) is received in that mailbox and leads to a possible corruption of these bits.

This corruption is experienced *only* when a CPU read/write access of any mailbox RAM is executed in the system clock cycle prior to the first write access (to the receive mailbox RAM) of the received data. The AAM and AME bits flip to the state of the CPU accessed data, thereby changing from their original values. A typical scenario is when bits 13 and 14 of any mailbox RAM were read/written as zero exactly one clock cycle prior to the reception of data in a receive mailbox. This will change bits 13 and 14 of the MSGID register of the mailbox that just received the data to zero. Therefore, the AAM and AME bits have to be considered corrupt after any reception.

Problem Effect:
AME bit corruption: When the AME bit of a receive mailbox is unintentionally changed to zero, it effectively shuts down that particular mailbox, since the acceptance mask filtering criterion will not be satisfied anymore. With time, this phenomenon could take place in other receive mailboxes and shut them down as well, effectively preventing the CAN module from receiving any further messages.

CAN – AME and AAM Bits Get Corrupted Upon Reception (Continued)

AAM bit corruption: When the AAM bit of a mailbox is unintentionally changed to zero, it prevents the CAN node from automatically responding to a “remote request”. For a mailbox configured for “automatic answer mode” (i.e., for a mailbox configured as a transmit-mailbox with the AAM bit set), this may prevent the CAN module from responding to a remote request.

Workaround: Reinitialize these bits to the appropriate value after every reception. This will be fixed in the 240xA silicon.

Advisory *CAN – Method to Service Multiple Interrupts Through the Existing Two-Interrupt Structure*

Revision(s) Affected: 1.0, 1.1, 1.2, 1.3, 1.4, and 1.6

Details: A CAN module interrupt will not assert a core-level interrupt if a CAN_IFR bit (set by any previous CAN interrupt) still remains set at the time of occurence of the new interrupt. For example, when a new CAN interrupt is asserted before the processor has had a chance to clear the CAN_IFR bit that caused the interrupt to happen, the CAN module does not assert a core-level CPU interrupt (INTn) for the new interrupt and may “lose” interrupts. However, the occurence of any interrupt-causing event will always set the appropriate flag bit in the CAN_IFR register.

Workaround: The CAN_IFR bit that causes an interrupt must be cleared as early as possible within the ISR. This can be done by copying the CAN_IFR register to a memory variable and then clearing the set bit. The memory variable can then be examined to determine which interrupt was asserted. If all CAN_IFR bits are cleared (i.e., zero) when a “new” interrupt is asserted, the “new” interrupt will be recognized and serviced by the core.

Advisory *CAN – CAN Bit Timing*

Revision(s) Affected: 1.0, 1.1, 1.2, 1.3, 1.4, and 1.6

Details: When the SBG bit (bit 10 of the BCR1 register) is set to 1, the “high” bit may be one TQ shorter/longer than it should be.

Workaround: Set SBG = 0.

Advisory *EV – CAPn Input*

Revision(s) Affected: 1.0, 1.1, 1.2, 1.3, 1.4, and 1.6

Details: If a CAPn input is high while the capture units are being enabled, it triggers spurious captures. The CAPFIFO status bits would indicate that there are two words in the FIFO, when in reality, no capture was triggered. If the capture interrupt is enabled, it will trigger the capture interrupt as well.

Workaround: Initialize the CAPFIFO status bits (and enable the capture interrupt) after configuring the capture units.

Advisory *EV – $\overline{\text{PDPINTx}}$ Pin Operation*

Revision(s) Affected: 1.0, 1.1, 1.2, 1.3, 1.4, and 1.6

Details: If the $\overline{\text{PDPINTx}}$ pin is active during a device reset, it prevents the recognition of valid PDPINTx interrupts in the future.

Workaround: To overcome this problem, bit PIRQR0.0 (for $\overline{\text{PDPINTA}}$) and bit PIRQR2.0 (for $\overline{\text{PDPINTB}}$) need to be cleared to zero. This can be achieved by writing a zero to these bits or by writing a one to the corresponding PIACKRn.0 bits. In addition to this, the EVAIFRA.0 bit (or EVBIFRA.0 bit) should be cleared as appropriate.

The PIRQRn and PIACKRn registers are ***not*** intended to be used in user applications. The workaround mentioned herein is a special case during the initialization of the device. After initialization, these registers should not be used by the user code.

Advisory	*EV – QEP Circuit*

Revision(s) Affected: 1.0, 1.1, 1.2, 1.3, 1.4, and 1.6

Details: After a DSP reset, the QEP module fails to detect the first transition that occurs on QEP input pins. Therefore, if the first transition occurs after a GP Timer has been initialized and enabled as the QEP counter (i.e., to use QEP as source of clock), the first transition will not be counted by the GP Timer. The result is an error of one count in the GP Timer out of a total of 1024 counts for a 256-line encoder, or 4096 counts for a 1024-line encoder. However, the issue is not a concern under any of the following conditions:

1. *The first transition happens **before** the GP Timer is initialized and enabled as QEP counter.* This ensures that all transitions are counted after initialization.
2. *After the first index pulse is received and if the index pulse is used to recalibrate the GP Timer (through capture interrupt).* The recalibration corrects the error in the GP Timer; therefore, from the time the first index pulse is received, the QEP counter becomes accurate.

Workaround(s):

1. Make the first transition happen before the GP timer is initialized and enabled as QEP counter. This is usually the case because typically the rotor shaft is locked to a known position before the GP Timer is initialized. Locking the rotor shaft will generate transitions on QEP input pins, unless the rotor shaft is exactly aligned to the known position (which is a rare case). Disturbing the rotor shaft on purpose takes care of the rare case.
2. Use the index pulse of the encoder to recalibrate the GP Timer used as QEP counter.

Advisory	*Phantom Interrupts While Using the Real-Time Monitor*

Revision(s) Affected: 1.0, 1.1, 1.2, 1.3, 1.4, and 1.6

Details: When the real-time monitor (RTM) is used, phantom interrupts may be occasionally seen—i.e., the PIVR register is loaded with 0000h when an interrupt is asserted. This problem is seen **only while debugging with the RTM** and is not applicable in actual applications.

Workaround: Check the PIVR value in the ISR. If a phantom interrupt is detected, return to the main code.

Advisory *SCI – SCI TX_EMPTY*

Revision(s) Affected: 1.0, 1.1, 1.2, 1.3, 1.4, and 1.6

Details: The TX_EMPTY bit (bit 6 in the SCICTL2 register) is supposed to get set when the transmit buffer and the shift register are ***both*** empty. However, this bit may occasionally be read as being set even when there is data in the transmit buffer.

Assuming two characters are being written back-to-back to the SCI, the TX_EMPTY bit is expected to go high after the second character is shifted out of the SCITXD pin. Occasionally, the TX_EMPTY bit goes high right after the first character is shifted out (i.e., when the second character is still in the transmit buffer). If the TX_EMPTY bit is polled to check the end-of-transmission of all characters, it may provide incorrect information about the status of the transmission.

Workaround: Follow these steps:

1. Read the TX_EMPTY bit.
2. If set, execute 2 NOPs and proceed to Step 3. Else, repeat Step 1.
3. Read the TX_EMPTY bit again.
4. If the bit is still set, then there are no more characters to be transmitted. If the bit is not set, it indicates transmission is not complete. Proceed to Step 1.

This will be fixed in the 240xA silicon.

Advisory *SCSR1 – ILLADR Bit*

Revision(s) Affected: 1.0, 1.1, 1.2, 1.3, 1.4, and 1.6

Details: The ILLADR bit in the SCSR1 register may be set even though no illegal address access took place.

Workaround: This is a problem with the debugger-hardware interaction. This bit may be set on an emulation suspend such as a breakpoint or while single stepping. However, this bit works correctly in run time (i.e., this bit works correctly when the program is free-run without the JTAG connector being connected). This can be easily verified by writing a test code (running out of Flash) that copies the status of this bit to the XF bit and then monitoring the status of the XF pin using an oscilloscope.

Advisory — *SCSR1 – OSC FAIL FLAG and OSC FAIL RESET Bits*

Revision(s) Affected: 1.0, 1.1, 1.2, 1.3, 1.4, and 1.6

Details: These bits do not work as intended. They will be marked as “reserved” in all future documentation.

Workaround: None

Advisory — *SPI – $\overline{\text{SPISTE}}$ Timing Anomaly*

Revision(s) Affected: 1.0, 1.1, 1.2, 1.3, 1.4, and 1.6

Details: The $\overline{\text{SPISTE}}$ signal has a timing anomaly due to which, it goes high sooner than it should (i.e., before the last bit has ended). This results in unreliable read of the last bit of the word by both the master and the slave. Following is a summary of the bug description depending on which SPI clocking scheme is used:

- CLOCK POLARITY = 0, PHASE = 0
  The $\overline{\text{SPISTE}}$ signal goes high 3 CPU clock cycles after the falling edge of the SPICLK for the last bit of transmission.
- CLOCK POLARITY = 0, PHASE = 1
  The $\overline{\text{SPISTE}}$ signal goes high 3 CPU clock cycles after the rising edge of the SPICLK for the last bit of transmission.
- CLOCK POLARITY = 1, PHASE = 0
  The $\overline{\text{SPISTE}}$ signal goes high 3 CPU clock cycles after the rising edge of the SPICLK for the last bit of transmission.
- CLOCK POLARITY = 1, PHASE = 1
  The $\overline{\text{SPISTE}}$ signal goes high 3 CPU clock cycles after the falling edge of the SPICLK for the last bit of transmission.

Note that the timing issue is aggravated when PHASE = 1, since the time window for which the $\overline{\text{SPISTE}}$ signal is valid for the last bit gets reduced further.

Workaround: The $\overline{\text{SPISTE}}$ pin should be used in its GPIO configuration. This pin can then be manipulated manually in software. Note that this workaround does not require any hardware change.

Advisory *WDCR – WDFLAG Bit (in WDCR Register)*

Revision(s) Affected: 1.0, 1.1, 1.2, 1.3, 1.4, and 1.6

Details: The power-on reset (POR) state of the WDFLAG bit is undefined. This could cause confusion if the user code attempts to differentiate a watchdog-initiated reset from a power-on reset.

Workaround: If an application implements a mechanism to differentiate a POR from other types of reset, the WDFLAG bit must be cleared after a POR. Once this is done, the WDFLAG bit can be set only by a watchdog reset.

Advisory *Flash Specification for Write/Erase Cycles*

Revision(s) Affected: 1.3

Details: The minimum specification for endurance for the flash array (N_f) is 50 Write/Erase cycles.

Workaround: This will be fixed in revision 1.4 of the silicon.

Advisory *Additional Wait-State During Flash Memory Access*

Revision(s) Affected: 1.0, 1.1, and 1.2

Details: The DSP adds one wait state for every read access fo the Flash (i.e., CPU accesses to Flash memory are always at one wait-state. As a result of this, a program executed off Flash may take twice as long compared to external RAM. This affects *only* the Flash memory access time and does not affect DARAM, SARAM, external memory interface or peripheral registers.

Workaround: This will be fixed in revision 1.3 of the silicon.

Advisory *SPI – SPI Double Transmission*

Revision(s) Affected: 1.0, 1.1, and 1.2

Details: The problem appears when two LF240x devices communicate with each other using the master/slave mode. The first character transmitted by the slave board is sent twice. Subsequent transmissions do not exhibit this problem. This problem appears when the slave code is run from Flash memory and does not appear when run from RAM.

Workaround: This has been fixed in revision 1.3 of the silicon.

Advisory *Test Conditions*

Revision(s) Affected: 1.0, 1.1, and 1.2

Table 2. Test Conditions

			NOM	MAX	UNIT
T_A	Operating free-air temperature (excluding flash programming)	DSP Core	25	85	°C
		System and Peripherals	25		
V_{DD},V_{DDO}	Supply voltage (3.3 V ±10%)	3.3-V operation	3.3		V
f_{CLKOUT}	Device clock frequency			30	MHz

Advisory *CLKOUT*

Revision(s) Affected: 1.0

Details: The 2407 CLKOUT rates differ from the data sheet specifications. The CLKOUT output has an additional ÷2 after the PLL module. CLKOUT is the same as the CPU clock.

Workaround: For *Silicon Revision 1.0*, use the crystal/resonator/oscillator with twice the specified frequency. For example, if 30-MHz CLKOUT is desired, use 15-MHz input clock instead of 7.5 MHz. Note that the PLL multiplication factor should be ×4 to derive a 30-MHz CLKOUT from a 15-MHz input clock due to this bug. This will be fixed in the next revision of the silicon.

Table 3 shows the 3-bit ratio selection for various PLL output clock frequencies in *Silicon Revision 1.0*. These register bits are located in the SCSR1 register.

Table 3. Ratio Selection for Various PLL Output Clock Frequencies

CLK PS2	CLK PS1	CLK PS0	CPU Clock Frequency (CLKOUT) (F_{in} is input clock frequency)
0	0	0	2 * F_{in}
0	0	1	F_{in}
0	1	0	0.67 * F_{in}
0	1	1	0.5 * F_{in}
1	0	0	0.4 * F_{in}
1	0	1	0.33 * F_{in}
1	1	0	0.29 * F_{in}
1	1	1	0.25 * F_{in}

Advisory *Emulation and Debugger*

Revision(s) Affected: 1.0

Details: In reference to the CLKOUT problem mentioned in the *CLKOUT* advisory, prototype boards or EVMs built for *Silicon Revision 1.0* may have debugger start-up problems.

Workaround: To avoid this problem, it is suggested that the device always be powered up in the *boot enable* mode (BOOT_EN pin low at reset). The boot code resets the watchdog and helps the debugger come up reliably. Once the debugger is up, the boot ROM can be disabled by writing a 0 to bit 3, the BOOT_EN bit, in the SCSR2 register. Debugging then works as normal.

This will be fixed in the next revision of the silicon.

Advisory *SARAM*

Revision(s) Affected: 1.0

Details: On-chip SARAM is available in both program space (8000h) and data space (0800h). This mapping is controlled by the PON and DON bits (bits 0 and 1, respectively) in the SCSR2 register. At reset, these bits are set to 1, and SARAM is available in both spaces.

In *Silicon Revision 1.0*, SARAM will be demapped in program space under two conditions:

- Any write to the SCSR2 register (disables the PON bit which demaps the SARAM).
- Programming the on-chip wait-state generator to 07F8h (enables zero wait-state access to external program memory).

Workaround: None. This will be fixed in the next revision of the silicon.

Revision(s) Affected: 1.0

Details: If the ENA_144 pin is low at reset, SARAM is **not** available in program space (8000h). It is available only in data space (0800h).

Workaround: None. This will be fixed in the next revision of the silicon.

Revision(s) Affected: 1.0

Details: If set to 1, the DON bit enables SARAM in internal data space between 800h and FFFh. If DON is cleared, SARAM will be demapped from internal data space. However, addresses 800h to FFFh will not be available in external data memory. The external data memory is available only between 8000h and FFFFh, i.e., SARAM space in data memory (800h to FFFh) will not be available externally, even if DON is cleared.

Workaround: This is applicable for the 2407 device only and is a correction to the data sheet specification.

Advisory	*Watchdog Disable (WDDIS) Bit*

Revision(s) Affected: 1.0

Details: At reset, the watchdog override bit (WD OVERRIDE, bit 5 in the SCSR2 register) is set to 1. This allows the user to disable the watchdog by writing a 1 to the WDDIS bit (WDDIS, bit 6 in the WDCR register). Ideally, if the WD OVERRIDE bit is cleared by writing a 1, the user will not be able to disable the watchdog, even after writing a 1 to the WDDIS bit. In *Silicon Revision 1.0*, this feature does not work, i.e., the watchdog can be disabled by writing to the WDDIS bit, even if the WD OVERRIDE bit has been cleared.

Workaround: None. This will be fixed in the next revision of the silicon.

3 Documentation Support

For device-specific data sheets and related documentation, visit the TI web site at: **http://www.ti.com**

To access documentation on the web site:

1. Go to **http://www.ti.com**
2. Click on **DSP Product Tree**
3. Click on the **C2000** tab
4. Click on **TMS320C24x DSP Generation**
5. Click on a device name and then click on the documentation type you prefer.

For further information regarding the TMS320LF2407, please refer to the following publications:

- *TMS320LF/LC240xA DSP Controllers Reference Guide: System and Peripherals* (literature number SPRU357)
- Manual Update Sheet for *TMS320LF/LC240xA DSP Controllers Reference Guide: System and Peripherals* (SPRU357B) [literature number SPRZ015]
- *TMS320F/C24x DSP Controllers Reference Guide: CPU and Instruction Set* (literature number SPRU160)
- *3.3V DSP for Digital Motor Control* application report (literature number SPRA550)
- *TMS320LF2407, TMS320LF2406, TMS320LF2402 DSP Controllers* data sheet (literature number SPRS094)

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