66AK2G0x Multicore DSP+ARM KeyStone II System-on-Chip (SoC) Silicon Revision 1.0

This document describes the known exceptions to the functional specifications (advisories). This document may also contain usage notes. Usage notes describe situations where the device's behavior may not match presumed or documented behavior. This may include behaviors that affect device performance or functional correctness.

Topic **Page**

1 Usage Notes and Advisories Matrices

Table 1 lists all usage notes and the applicable silicon revision(s). Table 2 lists all advisories, modules affected, and the applicable silicon revision(s).

Table 1. Usage Notes Matrix

ID	DESCRIPTION	SILICON REVISIONS AFFECTED
		1.0
KeyStoneII.BTS_errata_usagenote.10	Section 3.1.1, I2C: I2C Bus Hang After Master Reset	Yes

Table 2. Advisories Matrix

MODULE	DESCRIPTION	SILICON REVISIONS AFFECTED
		1.0
PCIe®	KeyStoneII.BTS_errata_advisory.21 — PCIe: Descriptors Placed in PCIe Memory Space Can Cause Problems	Yes
PCIe	KeyStoneII.BTS_errata_advisory.43 — PCIe: SerDes Fails to Adapt BOOST Equalization	Yes
PCIe, Control Module	KeyStoneII.BTS_errata_advisory.44 — PCIe, Control Module: PCIe Hot Reset Not Honored by ROM Code	Yes
BOOT, GMAC_SW	KeyStoneII.BTS_errata_advisory.45 — BOOT, GMAC_SW: Ethernet Boot Failure on RESETn	Yes
BOOT, GPMC	KeyStoneII.BTS_errata_advisory.46 — BOOT, GPMC: GPMC XIP Boot Failure	Yes
Control Module	KeyStoneII.BTS_errata_advisory.48 — Control Module: Internal Oscillator Does Not Always Start Reliably	Yes
PADCONFIG, Control Module	KeyStoneII.BTS_errata_advisory.49 — PADCONFIG, Control Module: Unexpected Write Operation to BOOTCFG_PADCFG194 and BOOTCFG_PADCFG202	Yes

2 Nomenclature, Package Symbolization, and Revision Identification

2.1 Device and Development-Support Tool Nomenclature

To designate the stages in the product development cycle, TI assigns prefixes to the part numbers of all microprocessors (MPUs) and support tools. Each device has one of three prefixes: X, P, or null (no prefix) (for example, 66AK2G02). Texas Instruments recommends two of three possible prefix designators for its support tools: TMDX and TMDS. These prefixes represent evolutionary stages of product development from engineering prototypes (X/TMDX) through fully qualified production devices and tools (null/TMDS).

Device development evolutionary flow:

X — Experimental device that is not necessarily representative of the final device's electrical specifications and may not use production assembly flow.

P — Prototype device that is not necessarily the final silicon die and may not necessarily meet final electrical specifications.

null— Production version of the silicon die that is fully qualified.

Support tool development evolutionary flow:

TMDX — Development-support product that has not yet completed Texas Instruments internal qualification testing.

TMDS — Fully-qualified development-support product.

X and P devices and TMDX development-support tools are shipped against the following disclaimer:

"Developmental product is intended for internal evaluation purposes."

Production devices and TMDS development-support tools have been characterized fully, and the quality and reliability of the device have been demonstrated fully. TI's standard warranty applies.

Predictions show that prototype devices (X or P) have a greater failure rate than the standard production devices. Texas Instruments recommends that these devices not be used in any production system because their expected end-use failure rate still is undefined. Only qualified production devices are to be used.

For additional information how to read the complete device name for any 66AK2G0x device, see the device Data Manual (SPRS932).

2.2 Devices Supported by This Document

This document supports the following devices:

- 66AK2G01
- 66AK2G02

2.3 Package Symbolization and Revision Identification

Figure 1 and Table 3 describe package symbolization and device revision codes.

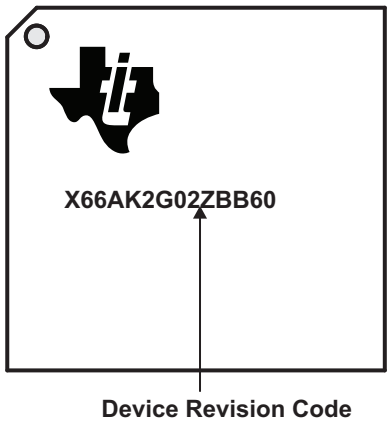

Figure 1. Package Symbolization

Table 3. Revision Identification

DEVICE REVISION CODE	SILICON REVISION	COMMENTS
BLANK	1.0	Available as null.

3 Silicon Revision 1.0 Usage Notes and Advisories

This section lists the usage notes and advisories for this silicon revision.

3.1 Silicon Revision 1.0 Usage Notes

3.1.1 I²C: I²C Bus Hang After Master Reset

On 66AK2G0x silicon revision 1.0, the I²C bus can hang if an I²C master is removed from the bus in the middle of a data read. This can occur because the I²C protocol does not mandate a minimum clock rate. Therefore, if a master is reset in the middle of a read while a slave is driving the data line low, the slave will continue driving the data line low while it waits for the next clock edge. This prevents bus masters from initiating transfers.

If this condition is detected, the following three steps will clear the bus hang condition:

1. An I²C master must generate up to 9 clock cycles.
2. After each clock cycle, the data pin must be observed to determine whether it has gone high while the clock is high.
3. As soon as the data pin is observed high, the master can initiate a start condition.

3.2 Silicon Revision 1.0 Advisories

Table 4. Silicon Revision 1.0 Advisory List

KeyStoneII.BTS_errata_advisory.21

PCIe: Descriptors Placed in PCIe Memory Space Can Cause Problems

Revision(s) Affected: 1.0

Details: Packet DMA can generate write transactions with partial byte enables when trying to access descriptors. This can cause problems if the descriptors are stored in PCIe memory space since PCIe cannot handle partial byte enables. Here, partial byte enables means that the transactions are accessing memory that is not a full 32-bit word.

Workaround(s): As long as host-mode descriptors are used and these descriptors are located in a memory space that can properly handle partial byte enables (such as L2 SRAM, DDR3 or MSMC), the issue will not affect Packet DMA accesses to PCIe memory space. As mentioned earlier, data buffers can be stored in PCIe memory space without any problems.

KeyStoneII.BTS_errata_advisory.43

PCIe: SerDes Fails to Adapt RX BOOST Equalization

Revision(s) Affected: 1.0

Details:

NOTE: The advisory does not impact 10GbE operation.

The SerDes on PCIe will not automatically adapt its RX equalization when provided with certain data encodings common to that peripheral's electrical standard.

The TI SerDes contains an adaptation algorithm that allows the RX equalization blocks to adapt their parameters to the SerDes data channel. The adaptation algorithm sets the optimal values for the ATT, BOOST, and DFE blocks in order to equalize the signal, maximize margin, and minimize channel distortion. For higher data rates (that is 5Gbps and greater), the high frequency gain provided by the BOOST block is generally considered necessary to compensate for the low-pass characteristics of data channels and widen the data eye.

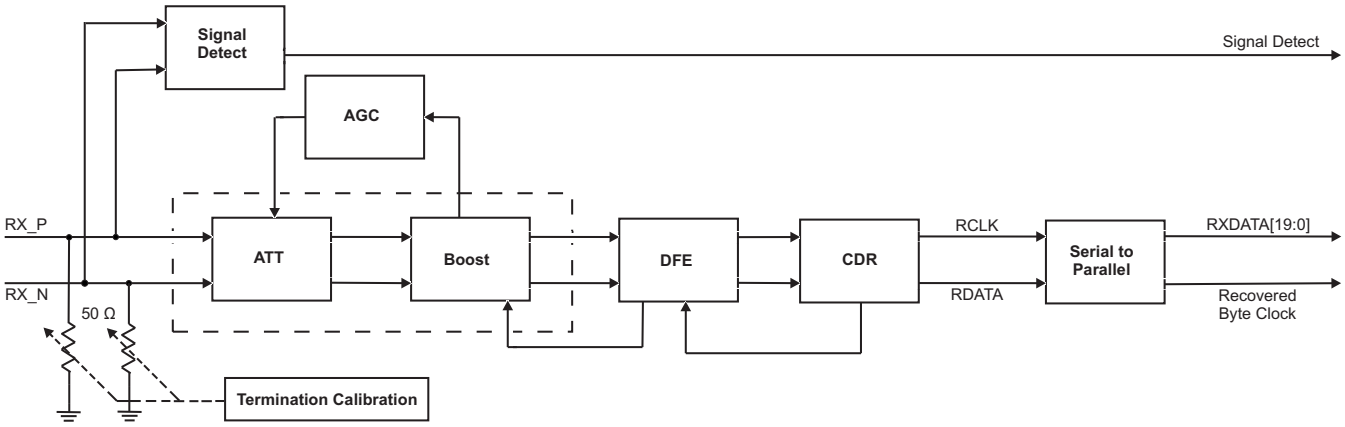

Figure 2. RX Path Block Diagram

The SerDes BOOST block was designed to require a specific set of patterns in order to best adapt its parameters to the channel. If these patterns are not found, the BOOST adaptation algorithm will not update the internal block settings and/or may incorrectly update these settings. The required data pattern is a series of six 0'-s followed by a 101 pattern. This pattern must occur numerous times on both odd and even bit alignments. This data pattern is not present in the 8b/10b coded symbols that are sent over many of the high speed peripheral links.

The data pattern is present in longer length PRBS patterns such as PRBS-23, and PRBS-31 used by the SerDes internal BIST hardware used during BER testing. The data pattern that is required is not present in the symbols used in PCIe SerDes interfaces during data transport.

If the BOOST has not been properly adapted for the received signal, then there is a chance that the SerDes will be unable to recover the RX data or the error rate may be higher than expected.

Workaround(s): The recommended workaround is to not use the RX equalization auto-adaptation mechanism with the impacted interfaces at higher data rates. As an alternative, a user can hardcode the optimal ATT and BOOST values for their channel. These optimal ATT and BOOST values must be determined by the user through one of two options:

- Perform BER test with PRBS sequence and sweep across all values of ATT/BOOST

while using a fixed set of TX parameters that have already been optimized. Use optimal ATT and BOOST value permutation that has the most margin. This is the value permutation that is both error-free and "farthest" from permutations with errors.

  - The SerDes DIAG tests can be found under <TI_PDK_INSTALL_DIR>\packages\ti\diag\serdes_diag in the latest CSL/PDK release and can be configured to perform this test.

- Perform a test where a PRBS data pattern is presented to the RX and the ATT/BOOST are allowed to auto-adapt. This method can also be used to identify the optimal ATT and BOOST value permutation that has the most margin.

The optimal ATT and BOOST values found by one of the two above methods can be hardcoded into the SerDes upon initialization.

KeyStoneII.BTS_errata_advisory.44

PCIe, Control Module: PCIe Hot Reset Not Honored by ROM Code

Revision(s) Affected: 1.0

Details: When receiving a PCI-Express (PCIe) Hot Reset request during the PCIe boot process, the PCI-Express Subsystem (PCIESS) will disable the Link Training and Status State Machine (LTSSM) and suspend the PCIe bus in the Detect.Quiet state. With the LTSSM disabled, there will be no subsequent transition from Detect.Quiet to Detect.Active and the PCIe boot process will fail.

Workaround(s):

1. Prevent the PCIe Root Complex (RC) from issuing PCIe Hot Reset during the PCIe boot process
   or
2. Do not use PCIe as the primary boot mode. Use an alternative boot mode and post boot application software or secondary boot loader implement the PCIe hot reset handling to appropriately communicate with the root complex host.
   The interrupt handling support in bootloader depends on its software architecture. Note that many bootloaders like U-Boot (http://www.denx.de/wiki/U-Boot) do not support interrupt handling on ARM architecture.

KeyStoneII.BTS_errata_advisory.45

BOOT, GMAC_SW: Ethernet Boot Failure on RESETn

Revision(s) Affected: 1.0

Details: On hard/soft resets (for example, RESETn pin) the boot ROM incorrectly configures the internal Ethernet switch. This causes a boot failure if the configuration happens while packets are traversing the switch.

Workaround(s): Only RESETFULLn or PORn reliably allow Ethernet boot mode to work.

KeyStoneII.BTS_errata_advisory.46

BOOT, GMPC: GPMC XIP Boot Failure

Revision(s) Affected: 1.0

Details: General-Purpose Memory Controller (GPMC) eXecute in Place (XIP) boot fails with default timing value.

Workaround(s): The default timing value is too aggressive for the currently available flash devices. To work around this issue, the boot pins should select a PLL reference clock frequency that is higher than the actual reference clock frequency. For example, if the actual reference clock frequency is 24 MHz, then the boot pins need to select a 100 MHz reference clock

frequency. The XIP boot then will succeed and the PLLs can be reconfigured along with the XP timing to continue the booting process.

KeyStoneII.BTS_errata_advisory.48

Control Module: Internal Oscillator Does Not Always Start Reliably

Revision(s) Affected: 1.0

Details: The default state of the internal HF Oscillator is not always set correctly. If this condition occurs, the internal HF Oscillator will not start causing the SoC to remain in the reset state.

This issue is only observed if the SYSCLKSEL is set low to select the internal HF OSC. If the problem occurs, no oscillation will be observed at the SYSOSC_OUT pin and the part will not exit reset. JTAG access will not be possible either.

Workaround(s): This state can be avoided by setting RSV6 to a high state while PORn is low for a minimum of 5msec after the power supplies are stable. Setting the RSV6 high will cause the HF OSC to initialize correctly allowing it to oscillate. RSV6 must then be set low a minimum of 1msec before PORn is set high. From that time on, RSV6 must be held low for proper operation.

Figure 3 shows the power sequencing diagram when HF OSC.

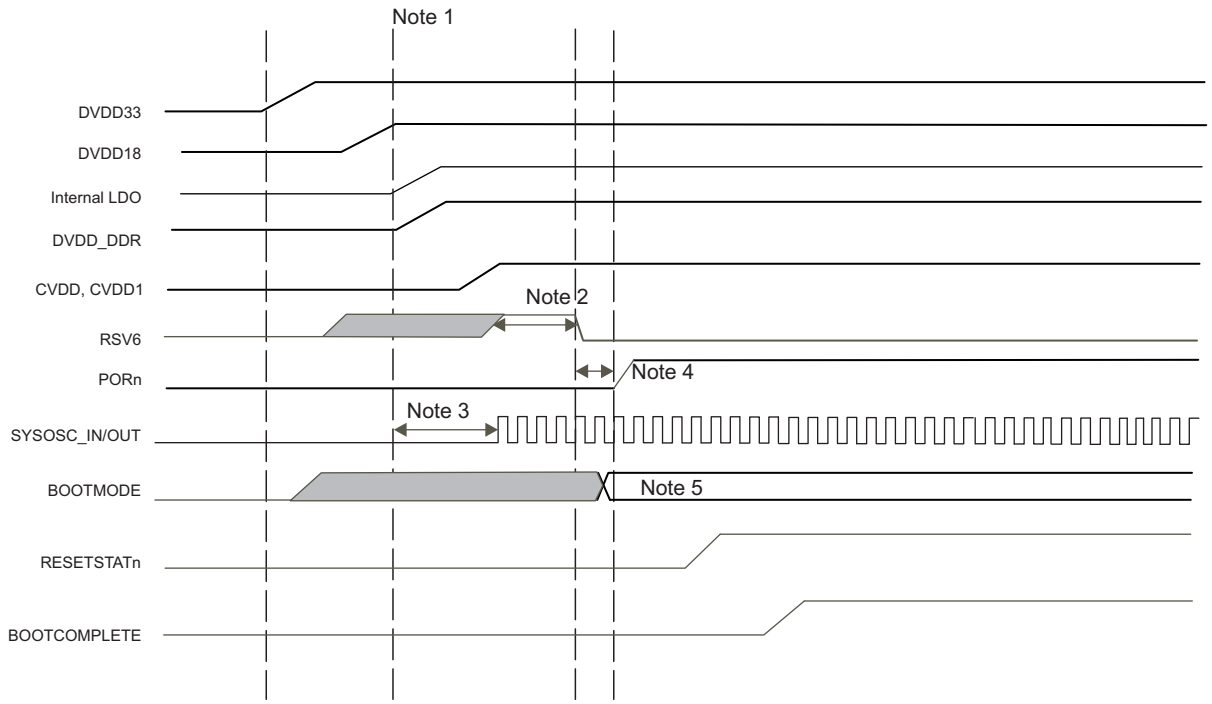

Figure 3. Power System Sequence when SYSCLKSEL is Low

Note 1 – Power-up begins by enabling the DVDD33 supply first.
Note 2 – Once DVDD33 is present, RSV6 is set high and must remain high for 5msec after all supplies have ramped.
Note 3 – Oscillator Power-up time once DVDD18 is present and RSV6 is high (approx. 1-2msec).
Note 4 – PORn must be held low until all supplies have ramped and for a minimum of 1msec after RSV6 is brought low. RSV6 must remain low after PORn is set high.
Note 5 – BOOTMODE pins are latched at the rising edge of PORn (synchronously using SYSOSC_IN/OUT).

KeyStoneII.BTS_errata_advisory.49

PADCONFIG, Control Module: Unexpected Write Operation to BOOTCFG_PADCFG194 and BOOTCFG_PADCFG202

Revision(s) Affected: 1.0

Details:

A logic error in the BOOTCFG_RSTMUX0 and BOOTCFG_RSTMUX8 lock circuit has unexpected side effects on writes to the BOOTCFG_PADCFG194 and BOOTCFG_PADCFG202 registers.

The BOOTCFG_RSTMUX0 and BOOTCFG_RSTMUX8 lock circuit uses the respective RSTMUX_LOCK bit and the lower 12 bits of the address bus to select one of two data sources that will be written into the respective register during a write operation. When the lock bit is not set, data is sourced from the master performing the write operation. When the lock bit is set, data is sourced from the respective register. This effectively locks the contents of the register since it can only be updated with its own value once the lock bit is set.

The multiplexer used in the lock circuit to select the data source was inserted in the path of all BOOTCFG registers.

Any writes to BOOTCFG_PADCFG194 or BOOTCFG_PADCFG202 when the lock bit of the corresponding BOOTCFG_RSTMUX0 or BOOTCFG_RSTMUX8 register is set will cause the respective BOOTCFG_PADCFG194 or BOOTCFG_PADCFG202 register to be updated with the contents of the corresponding BOOTCFG_RSTMUX0 or BOOTCFG_RSTMUX8 register during a write operation since the address decode logic in the lock circuit only uses the lower 12 address bits.

Workaround(s):

There are two workaround options.

1. The BOOTCFG_PADCFG194 and BOOTCFG_PADCFG202 registers can be configured to any value required by the application before setting the lock bit in the corresponding BOOTCFG_RSTMUX0 or BOOTCFG_RSTMUX8 register. Any attempt to write a new value to the BOOTCFG_PADCFG194 and BOOTCFG_PADCFG202 registers after the lock bit has been set will change its value to the current value of the corresponding BOOTCFG_RSTMUX0 or BOOTCFG_RSTMUX8 register. Therefore, dynamic pin multiplexing is not supported for the pins associated with the BOOTCFG_PADCFG194 and BOOTCFG_PADCFG202 registers when the application requires the corresponding BOOTCFG_RSTMUX0 or BOOTCFG_RSTMUX8 register to be locked. In this use case, the BOOTCFG_PADCFG194 and BOOTCFG_PADCFG202 registers must be configured before locking the corresponding BOOTCFG_RSTMUX0 or BOOTCFG_RSTMUX8 registers and never change the contents of the BOOTCFG_PADCFG194 and BOOTCFG_PADCFG202 registers.
2. If the application requires BOOTCFG_PADCFG194 and BOOTCFG_PADCFG202 registers to be changed after being configured to their initial value, the corresponding BOOTCFG_RSTMUX0 or BOOTCFG_RSTMUX8 registers should never be locked.

4 Modules Affected

Table 5 shows the module(s) that are affected by each advisory.

Table 5. Advisories by Modules

Module name	Silicon Advisories, Limitations, and Cautions
BOOT	KeyStoneII.BTS_errata_advisory.45 — BOOT, GMAC_SW: Ethernet Boot Failure on RESETn
	KeyStoneII.BTS_errata_advisory.46 — BOOT, GPMC: GPMC XIP Boot Failure
Control Module	KeyStoneII.BTS_errata_advisory.44 — PCIe, Control Module: PCIe Hot Reset Not Honored by ROM Code
	KeyStoneII.BTS_errata_advisory.48 — Control Module: Internal Oscillator Does Not Always Start Reliably
	KeyStoneII.BTS_errata_advisory.49 — PADCONFIG, Control Module: Unexpected Write Operation to BOOTCFG_PADCFG194 and BOOTCFG_PADCFG202
GMAC_SW	KeyStoneII.BTS_errata_advisory.45 — BOOT, GMAC_SW: Ethernet Boot Failure on RESETn
GPMC	KeyStoneII.BTS_errata_advisory.46 — BOOT, GPMC: GPMC XIP Boot Failure
PADCONFIG	KeyStoneII.BTS_errata_advisory.49 — PADCONFIG, Control Module: Unexpected Write Operation to BOOTCFG_PADCFG194 and BOOTCFG_PADCFG202
PCIe	KeyStoneII.BTS_errata_advisory.21 — PCIe: Descriptors Placed in PCIe Memory Space Can Cause Problems
	KeyStoneII.BTS_errata_advisory.43 — PCIe: SerDes Fails to Adapt BOOST Equalization
	KeyStoneII.BTS_errata_advisory.44 — PCIe, Control Module: PCIe Hot Reset Not Honored by ROM Code

Table 6 shows the module(s) that are affected by each usagenote.

Table 6. Usagenote by Modules

MODULE NAME	SILICON ADVISORY
I2C	KeyStoneII.BTS_errata_usagenote.10 — I2C: I2C Bus Hang After Master Reset

Revision History

Changes from B Revision (February 2017) to C Revision **Page**

- The book is aligned to new errata standards 1
- Section 3.2: Added KeyStoneII.BTS_errata_advisory.49, BOOT: Unexpected Write Operation to BOOTCFG_PADCFG194 and BOOTCFG_PADCFG202 9

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