CD74AC251 8-Input Multiplexer, Three-State

1 Features

- Buffered inputs
- Typical propagation delay
  - 6ns at V_{CC} = 5V, T_A = 25°C, C_L = 50pF
- Exceeds 2kV ESD protection MIL-STD-883, method 3015
- SCR-latchup-resistant CMOS process and circuit design
- Speed of bipolar FAST™/AS/S with significantly reduced power consumption
- Balanced propagation delays
- AC types feature 1.5V to 5.5V operation and balanced noise immunity at 30% of the supply
- ±24mA output drive current
  - Fanout to 15 FAST™ ICs
  - Drives 50Ω transmission lines

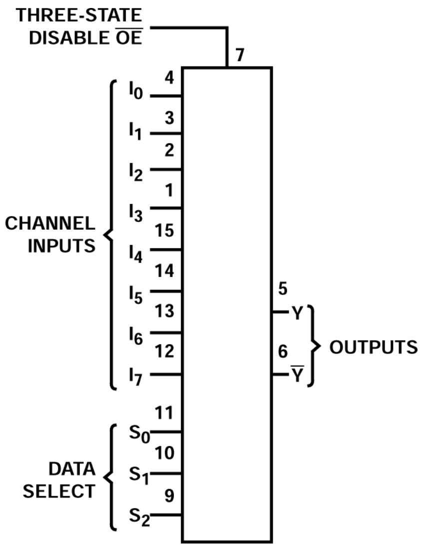
2 Description

The CD74AC251 8-input multiplexers that utilize the Harris Advanced CMOS Logic technology. This multiplexer features both true (Y) and complement ($\overline{Y}$) outputs as well as an Output Enable ($\overline{OE}$) input. The OE must be at a LOW logic level to enable this device. When the $\overline{OE}$ input is HIGH, both outputs are in the high-impedance state. When enabled, address information on the data select inputs determines which data input is routed to the Y and $\overline{Y}$ outputs.

Package Information

PART NUMBER	PACKAGE(1)	PACKAGE SIZE(2)	BODY SIZE(3)
CD74AC251	D (SOIC, 16)	9.9mm × 6mm	9.9mm × 3.9mm

(1) For more information, see Section 10.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.
(3) The body size (length × width) is a nominal value and does not include pins.



Functional Diagram

Table of Contents

3 Pin Configuration and Functions

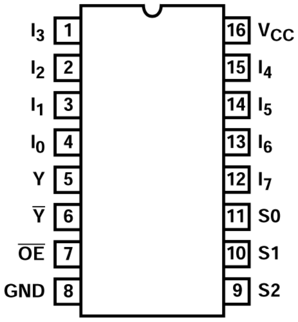


Figure 3-1. CD74AC251 D Package, 16-Pin SOIC (Top View)

PIN		TYPE[1]	DESCRIPTION
NAME	NO.		
I_3	1	I	Input 3
I_2	2	I	Input 2
I_1	3	I	Input 1
I_0	4	I	Input 0
Y	5	I	Output
$\overline{Y}$	6	I	Inverted Output
$\overline{OE}$	7	O	Output Enable
GND	8	G	Ground
S2	9	O	Input Select 2
S1	10	O	Input Select 1
S0	11	O	Input Select 0
I_7	12	O	Input 7
I_6	13	O	Input 6
I_5	14	O	Input 5
I_4	15	O	Input 4
V_{CC}	16	P	Positive Supply

1. Signal Types: I = Input, O = Output, I/O = Input or Output.

4 Specifications

4.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_{CC}	Supply voltage		-0.5	6	V
I_{IK}	Input diode current	($V_I < -0.5V$ or $V_I > V_{CC} + 0.5V$)		±20	mA
I_{OK}	Output diode current	($V_I < -0.5V$ or $V_I > V_{CC} + 0.5V$)		±50	mA
I_O	Output source or sink current per output pin	$V_O < -0.5V$ or $V_O > V_{CC} + 0.5V$		±50	mA
	V_{CC} or ground current, ICC or IGND (2)			±100	mA
T_J	Maximum junction temperature (plastic package)			150	°C
T_{stg}	Storage temperature		-65	150	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

(2) For up to 4 outputs per device, add ±25mA for each additional output.

4.2 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_{CC} (1)	Supply voltage	1.5	1.5	
V_I, V_O	Input or output voltage	0	V_{CC}	V
dt/dv	Input rise and fall slew rate			
	AC types, 1.5V to 3V		50	ns
	AC types, 3.6V to 5.5V		20	ns
T_A	Temperature range	-55	125	°C

(1) Unless otherwise specified, all voltages are referenced to ground.

4.3 Thermal Information

		CD74AC251	
		D (SOIC)	
THERMAL METRIC		16 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance(1)	119.9	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

4.4 Electrical Characteristics

SYMBOL	PARAMETER	TEST CONDITIONS		V_{CC} (V)	25°C		-40°C TO 85°C		-55°C TO 125°C		UNIT
		V_I (V)	I_O (mA)		MIN	MAX	MIN	MAX	MIN	MAX	
V_{IH}	High level input voltage	-	-	1.5	1.2	-	1.2	-	1.2	-	V
				3	2.1	-	2.1	-	2.1	-	V
				5.5	3.85	-	3.85	-	3.85	-	V
V_{IL}	Low level input voltage	-	-	1.5	-	0.3	-	0.3	-	0.3	V
				3	-	0.9	-	0.9	-	0.9	V
				5.5	-	1.65	-	1.65	-	1.65	V

SYMBOL	PARAMETER	TEST CONDITIONS		V_{CC} (V)	25°C		-40°C TO 85°C		-55°C TO 125°C		UNIT
		V_I (V)	I_O (mA)		MIN	MAX	MIN	MAX	MIN	MAX	
V_{OH}	High level output voltage	V_{IH} or V_{IL}	-0.05	1.5	1.4	-	1.4	-	1.4	-	V
			-0.05	3	2.9	-	2.9	-	2.9	-	V
			-0.05	4.5	4.4	-	4.4	-	4.4	-	V
			-4	3	2.58	-	2.48	-	2.4	-	V
			-24	4.5	3.94	-	3.8	-	3.7	-	V
			-75 (1), (2)	5.5	-	-	3.85	-	-	-	V
			-50 (1), (2)	5.5	-	-	-	-	3.85	-	V
V_{OL}	Low level output voltage	V_{IH} or V_{IL}	0.05	1.5	-	0.1	-	0.1	-	0.1	V
			0.05	3	-	0.1	-	0.1	-	0.1	V
			0.05	4.5	-	0.1	-	0.1	-	0.1	V
			12	3	-	0.36	-	0.44	-	0.5	V
			24	4.5	-	0.36	-	0.44	-	0.5	V
			75 (1), (2)	5.5	-	-	-	1.65	-	-	V
			50(1), (2)	5.5	-	-	-	-	-	1.65	V
I_I	Input leakage current	V_{CC} or GND	-	5.5	-	±0.1	-	±1	-	±1	µA
I_{OZ}	Three-state leakage current	V_{IH} or V_{IL} V_O = V_{CC} or GND	-	5.5	-	±0.5	-	±5	-	±10	µA
I_{CC}	Quiescent supply current MSI	V_{CC} or GND	0	5.5	-	8	-	80	-	160	µA

(1) Test one output at a time for a 1-second maximum duration. Measurement is made by forcing current and measuring voltage to minimize power dissipation.

(2) Test verifies a minimum 50Ω transmission-line-drive capability at 85°C, 75Ω at 125°C.

Table 4-1. ACT Input Load Table

INPUT	UNIT LOAD
S0, S1, S3	1
OE	1
I_0 - I_7	1

Note

Unit load is ΔI_{CC} limit specified in DC Electrical Specifications Table, e.g., 2.4mA max at 25°C.

4.5 Switching Characteristics

Input t_r, t_f = 3ns, C_L = 50pF (Worst Case)

SYMBOL	PARAMETER	V_{CC} (V)	-40°C TO 85°C			-55°C TO 125°C			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
t_{PLH}, t_{PHL}	Propagation delay, data to Y output	1.5	-	-	153	-	-	169	ns
		3.3(1)	4.9	-	17.2	4.7	-	18.9	ns
		5(2)	3.5	-	12.3	3.4	-	13.5	ns
t_{PLH}, t_{PHL}	Propagation delay, data to $\overline{Y}$ output	1.5	-	-	169	-	-	186	ns
		3.3	5.4	-	19	5.2	-	20.9	ns
		5	3.8	-	13.5	3.7	-	14.9	ns

Input t_r, t_f = 3ns, C_L = 50pF (Worst Case)

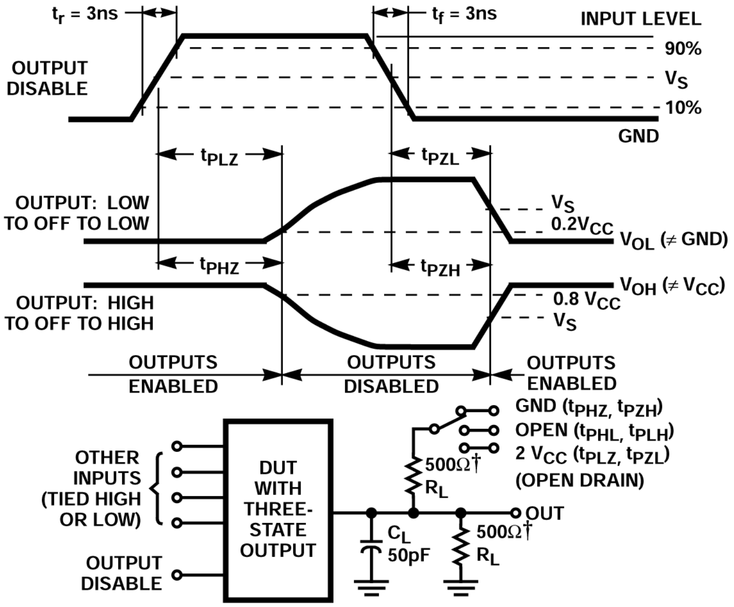
SYMBOL	PARAMETER	V_{CC} (V)	-40°C TO 85°C			-55°C TO 125°C			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
t_{PLH}, t_{PHL}	Propagation delay, select to Y output	1.5	-	-	207	-	-	228	ns
		3.3	6.6	-	23.2	6.4	-	25.5	ns
		5	4.7	-	16.5	4.6	-	18.2	ns
t_{PLH}, t_{PHL}	Propagation Delay, Select to $\overline{Y}$ Output	1.5	-	-	223	-	-	245	ns
		3.3	7.1	-	24.9	6.9	-	27.4	ns
		5	5.1	-	17.8	4.9	-	19.6	ns
t_{PZH}, t_{PZL}, t_{PHZ}, t_{PLZ}	Propagation delay, output enable and output disable to output	1.5	-	-	155	-	-	169	ns
		3.3	5.2	-	18.7	5.1	-	20.3	ns
		5	3.5	-	12.3	3.4	-	13.5	ns
C_O	Three-state output capacitance	-	-	-	15	-	-	15	pF
C_I	Input capacitance	-	-	-	10	-	-	10	pF
C_{PD} (3)	Power dissipation capacitance	-	-	120	-	-	120	-	pF

(1) 3.3V Min is at 3.6V, Max is at 3V.
(2) 5V Min is at 5.5V, Max is at 4.5V.
(3) C_{PD} is used to determine the dynamic power consumption per device.

Note

$P_D = V_{CC}{}^2 f_i (C_{PD} + C_L)$ where f_i = input frequency, C_L = output load capacitance, V_{CC} = supply voltage.

5 Parameter Measurement Information



†FOR AC SERIES ONLY: WHEN V_{CC} = 1.5V, R_L = 1kΩ

[†]

Figure 5-1. Three-state Propagation Delay Waveforms and Test Circuit

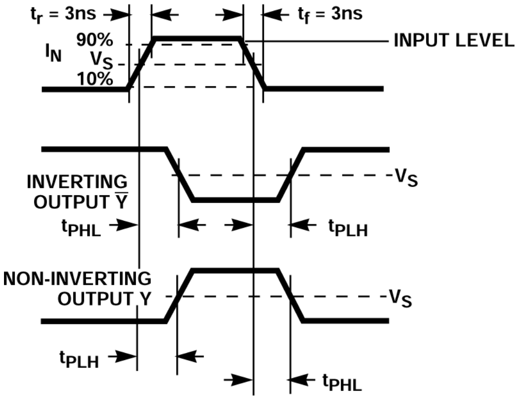
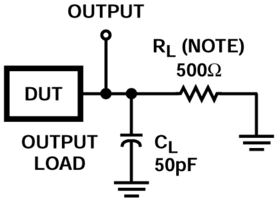


Figure 5-2. Propagation Delay Times



A. For AC Series Only: When V_{CC} = 1.5V, R_L = 1kΩ.

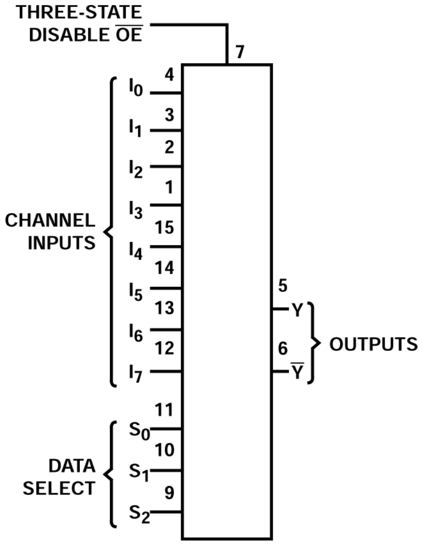
Figure 5-3. Propagation Delay Times

	CD74AC
Input Level	V_{CC}
Input Switching Voltage, V_S	0.5 V_{CC}
Output Switching Voltage, V_S	0.5 V_{CC}

[†] FOR AC SERIES ONLY: WHEN V_{CC} = 1.5V, R_L = 1kΩ

6 Detailed Description

6.1 Functional Block Diagram



6.2 Device Functional Modes

Table 6-1. Truth Table

INPUTS				OUTPUTS	
SELECT					
S2	S1	S0	OUTPUT ENABLE $\overline{OE}$	Y	$\overline{Y}$
X	X	X	H	Z	Z
L	L	L	L	I_0	$\overline{I}_0$
L	L	H	L	I_1	$\overline{I}_1$
L	H	L	L	I_2	$\overline{I}_2$
L	H	H	L	I_3	$\overline{I}_3$
H	L	L	L	I_4	$\overline{I}_4$
H	L	H	L	I_5	$\overline{I}_5$
H	H	L	L	I_6	$\overline{I}_6$
H	H	H	L	I_7	$\overline{I}_7$

7 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

7.1 Power Supply Recommendations

The power supply can be any voltage between the MIN and MAX supply voltage rating located in the *Section 4.2* table.

Each V_{CC} pin should have a good bypass capacitor to prevent power disturbance. For devices with a single supply, 0.1 μf is recommended; if there are multiple V_{CC} pins, then 0.01 μf or 0.022 μf is recommended for each power pin. It is acceptable to parallel multiple bypass caps to reject different frequencies of noise. A 0.1 μf and a 1 μf are commonly used in parallel. The bypass capacitor should be installed as close to the power pin as possible for best results.

7.2 Layout

7.2.1 Layout Guidelines

When using multiple-bit logic devices, inputs should never float.

In many cases, functions or parts of functions of digital logic devices are unused, for example, when only two inputs of a triple-input AND gate are used or only 3 of the 4 buffer gates are used. Such input pins should not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. Layout Diagram specifies the rules that must be observed under all circumstances. All unused inputs of digital logic devices must be connected to a high or low bias to prevent them from floating. The logic level that should be applied to any particular unused input depends on the function of the device. Generally they will be tied to GND or V_{CC}, whichever makes more sense or is most convenient. It is generally acceptable to float outputs, unless the part is a transceiver. If the transceiver has an output enable pin, it will disable the output section of the part when asserted. This will not disable the input section of the I/Os, so they cannot float when disabled.

8 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

8.1 Documentation Support (Analog)

8.1.1 Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
CD74AC251	Click here	Click here	Click here	Click here	Click here

8.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

8.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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8.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

8.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

9 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (August 1998) to Revision A (August 2024) **Page**

- Deleted references to CD74ACT251 throughout the data sheet.......... 1
- Added *Package Information* table, *Pin Functions* table, *ESD Ratings* table, *Thermal Information* table, *Device Functional Modes,*Application and Implementation section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section 1
- Added RθJA value: D = 119.9, all values in °C/W.......... 4

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10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGE OPTION ADDENDUM

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
CD74AC251M96	Active	Production	SOIC (D) | 16	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	AC251M
CD74AC251M96.A	Active	Production	SOIC (D) | 16	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	AC251M

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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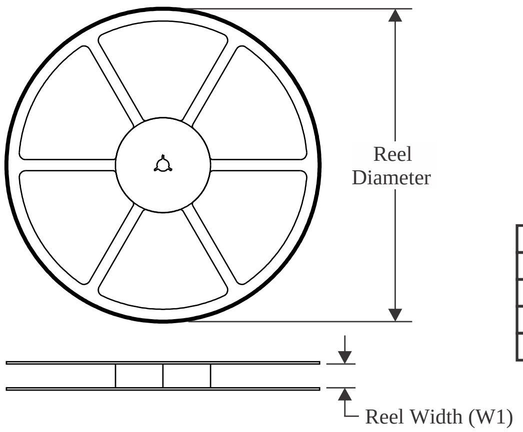
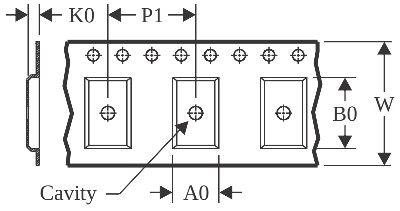
TAPE AND REEL INFORMATION

REEL DIMENSIONS

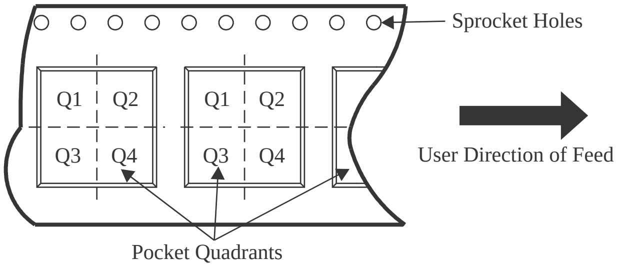


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

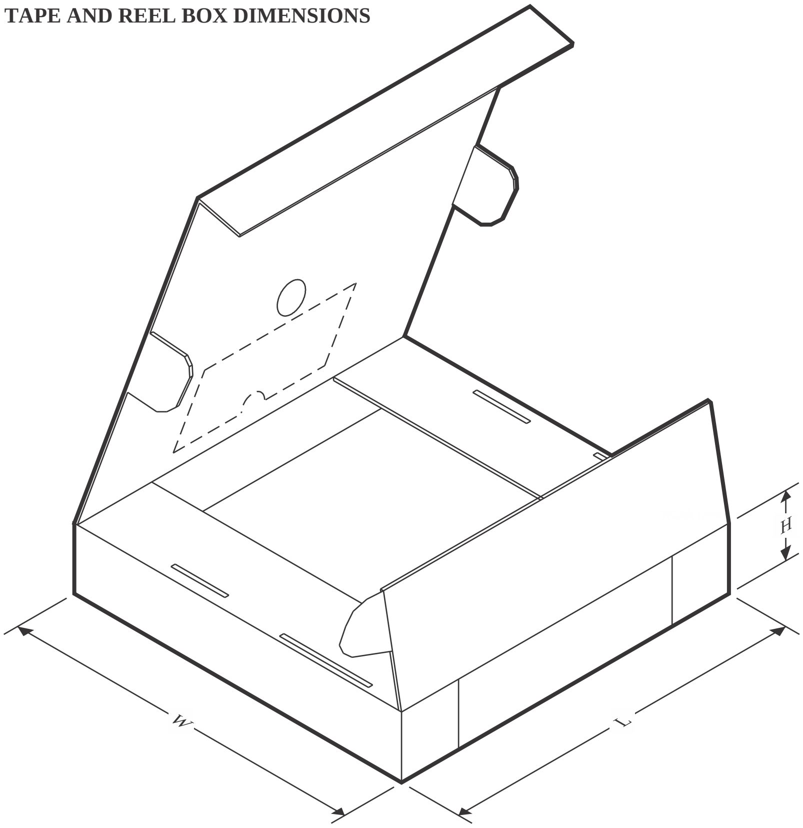
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CD74AC251M96	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1

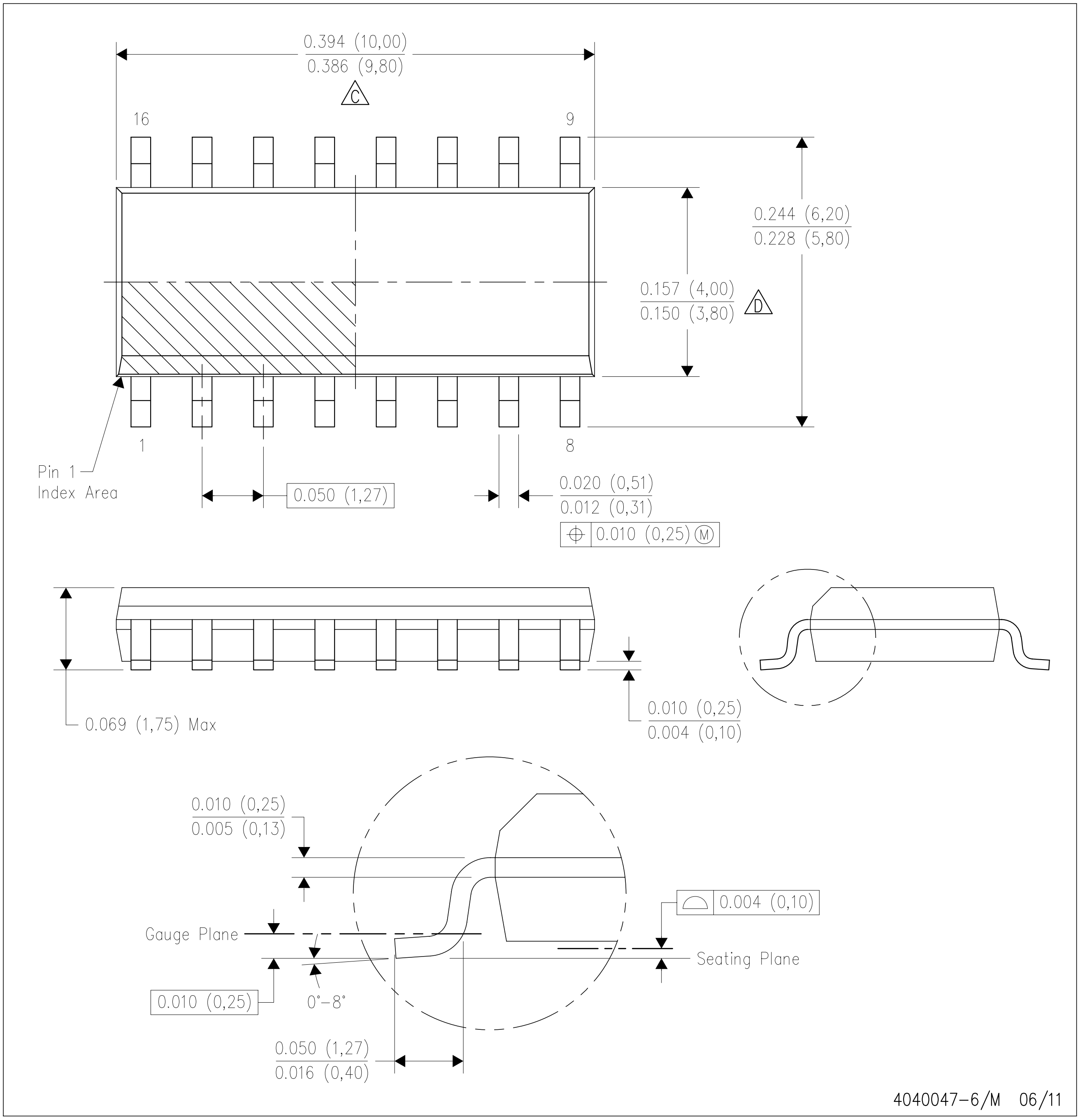
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CD74AC251M96	SOIC	D	16	2500	353.0	353.0	32.0

D (R–PDSO–G16) PLASTIC SMALL OUTLINE



NOTES:
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
- D Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
- E. Reference JEDEC MS–012 variation AC.

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