



SCCS027B - August 1994 - Revised September 2001

# CY74FCT16240T CY74FCT162240T

## 16-Bit Buffers/Line Drivers

### Features

- $I_{off}$  supports partial-power-down mode operation
- Edge-rate control circuitry for significantly improved noise characteristics
- Typical output skew < 250 ps
- ESD > 2000V
- TSSOP (19.6-mil pitch) and SSOP (25-mil pitch) packages
- Industrial temperature range of  $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$
- $V_{CC} = 5\text{V} \pm 10\%$

#### CY74FCT16240T Features:

- 64 mA sink current, 32 mA source current
- Typical  $V_{OLP}$  (ground bounce)  
<1.0V at  $V_{CC} = 5\text{V}$ ,  $T_A = 25^{\circ}\text{C}$

#### CY74FCT162240T Features:

- Balanced output drivers: 24 mA
- Reduced system switching noise
- Typical  $V_{OLP}$  (ground bounce)  
<0.6V at  $V_{CC} = 5\text{V}$ ,  $T_A = 25^{\circ}\text{C}$

### Functional Description

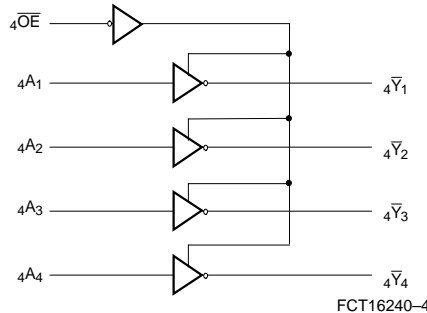
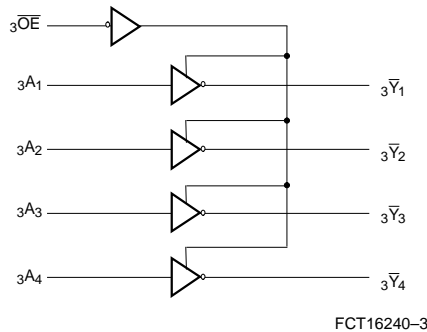
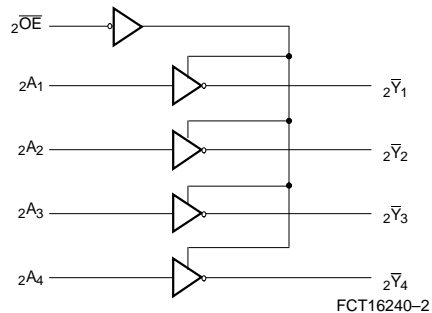
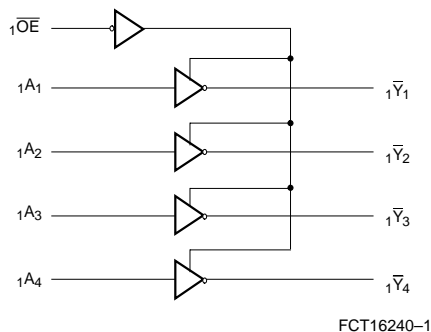
These 16-bit buffer/line drivers are used in memory driver, clock driver, or other bus interface applications, where high speed and low power are required. With flow-through pinout and small shrink packaging, board layout is simplified. The three-state controls are designed to allow 4-, 8-, or 16-bit operation.

This device is fully specified for partial-power-down applications using  $I_{off}$ . The  $I_{off}$  circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

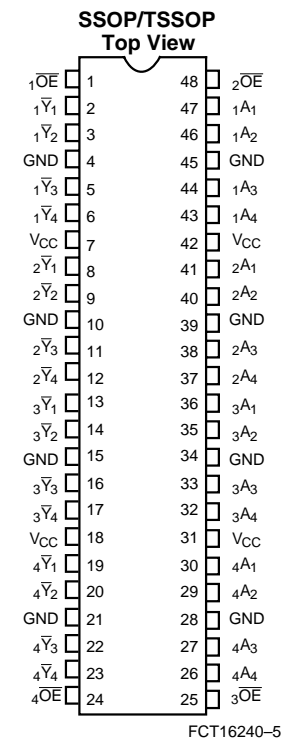
The CY74FCT16240T is ideally suited for driving high-capacitance loads and low-impedance backplanes.

The CY74FCT162240T has 24-mA balanced output drivers with current limiting resistors in the outputs. This reduces the need for external terminating resistors and provides for minimal undershoot and reduced ground bounce. The CY74FCT162240T is ideal for driving transmission lines.

### Logic Block Diagrams



### Pin Configuration



## Pin Summary

Name	Description
OE	Three-State Output Enable Inputs (Active LOW)
A	Data Inputs
Y	Three-State Outputs

## Function Table<sup>[1]</sup>

Inputs		Outputs
OE	A	Y
L	L	H
L	H	L
H	X	Z

## Maximum Ratings<sup>[2, 3]</sup>

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature .....Com'l. -55°C to +125°C

Ambient Temperature with

Power Applied.....Com'l. -55°C to +125°C

DC Input Voltage ..... -0.5V to +7.0V

DC Output Voltage..... -0.5V to +7.0V

DC Output Current

(Maximum Sink Current/Pin) ..... -60 to +120 mA

Power Dissipation ..... 1.0W

Static Discharge Voltage

(per MIL-STD-883, Method 3015) ..... >2001V

## Operating Range

Range	Ambient Temperature	V <sub>CC</sub>
Industrial	-40°C to +85°C	5V ± 10%

## Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions	Min.	Typ. <sup>[4]</sup>	Max.	Unit
V <sub>IH</sub>	Input HIGH Voltage		2.0			V
V <sub>IL</sub>	Input LOW Voltage				0.8	V
V <sub>H</sub>	Input Hysteresis <sup>[5]</sup>			100		mV
V <sub>IK</sub>	Input Clamp Diode Voltage	V <sub>CC</sub> = Min., I <sub>IN</sub> = -18 mA		-0.7	-1.2	V
I <sub>IH</sub>	Input HIGH Current	V <sub>CC</sub> = Max., V <sub>I</sub> = V <sub>CC</sub>			±1	μA
I <sub>IH</sub>	Input HIGH Current	V <sub>CC</sub> = Max., V <sub>I</sub> = V <sub>CC</sub>			±1	μA
I <sub>IL</sub>	Input LOW Current	V <sub>CC</sub> = Max., V <sub>I</sub> = GND			±1	μA
I <sub>IL</sub>	Input LOW Current	V <sub>CC</sub> = Max., V <sub>I</sub> = GND			±1	μA
I <sub>OZH</sub>	High Impedance Output Current (Three-State Output pins)	V <sub>CC</sub> = Max., V <sub>OUT</sub> = 2.7V			±1	μA
I <sub>OZL</sub>	High Impedance Output Current (Three-State Output pins)	V <sub>CC</sub> = Max., V <sub>OUT</sub> = 0.5V			±1	μA
I <sub>OS</sub>	Short Circuit Current <sup>[6]</sup>	V <sub>CC</sub> = Max., V <sub>OUT</sub> = GND	-80	-140	-200	mA
I <sub>O</sub>	Output Drive Current <sup>[6]</sup>	V <sub>CC</sub> = Max., V <sub>OUT</sub> = 2.5V	-50		-180	mA
I <sub>OFF</sub>	Power-Off Disable	V <sub>CC</sub> = 0V, V <sub>OUT</sub> ≤ 4.5V <sup>[7]</sup>			±1	μA

## Output Drive Characteristics for CY74FCT16240T

Parameter	Description	Test Conditions	Min.	Typ. <sup>[4]</sup>	Max.	Unit
V <sub>OH</sub>	Output HIGH Voltage	V <sub>CC</sub> = Min., I <sub>OH</sub> = -3 mA	2.5	3.5		V
		V <sub>CC</sub> = Min., I <sub>OH</sub> = -15 mA	2.4	3.5		V
		V <sub>CC</sub> = Min., I <sub>OH</sub> = -32 mA	2.0	3.0		V
V <sub>OL</sub>	Output LOW Voltage	V <sub>CC</sub> = Min., I <sub>OL</sub> = 64 mA		0.2	0.55	V

### Notes:

1. H = HIGH Voltage Level. L = LOW Voltage Level. X = Don't Care. Z = High Impedance.
2. Operation beyond the limits set forth may impair the useful life of the device. Unless noted, these limits are over the operating free-air temperature range.
3. Unused inputs must always be connected to an appropriate logic voltage level, preferably either V<sub>CC</sub> or ground.
4. Typical values are at V<sub>CC</sub> = 5.0V, T<sub>A</sub> = +25°C ambient.
5. This parameter is specified but not tested.
6. Not more than one output should be shorted at a time. Duration of short should not exceed one second. The use of high-speed test apparatus and/or sample and hold techniques are preferable in order to minimize internal chip heating and more accurately reflect operational values. Otherwise prolonged shorting of a high output may raise the chip temperature well above normal and thereby cause invalid readings in other parametric tests. In any sequence of parameter tests, I<sub>OS</sub> tests should be performed last.
7. Tested at +25°C.

**Output Drive Characteristics for CY74FCT162240T**

Parameter	Description	Test Conditions	Min.	Typ. <sup>[4]</sup>	Max.	Unit
$I_{ODL}$	Output LOW Current <sup>[6]</sup>	$V_{CC} = 5V$ , $V_{IN} = V_{IH}$ or $V_{IL}$ , $V_{OUT} = 1.5V$	60	115	150	mA
$I_{ODH}$	Output HIGH Current <sup>[6]</sup>	$V_{CC} = 5V$ , $V_{IN} = V_{IH}$ or $V_{IL}$ , $V_{OUT} = 1.5V$	-60	-115	-150	mA
$V_{OH}$	Output HIGH Voltage	$V_{CC} = \text{Min.}$ , $I_{OH} = -24 \text{ mA}$	2.4	3.3		V
$V_{OL}$	Output LOW Voltage	$V_{CC} = \text{Min.}$ , $I_{OL} = 24 \text{ mA}$		0.3	0.55	V

**Capacitance<sup>[5]</sup>** ( $T_A = +25^\circ\text{C}$ ,  $f = 1.0 \text{ MHz}$ )

Parameter	Description	Test Conditions	Typ. <sup>[4]</sup>	Max.	Unit
$C_{IN}$	Input Capacitance	$V_{IN} = 0V$	4.5	6.0	pF
$C_{OUT}$	Output Capacitance	$V_{OUT} = 0V$	5.5	8.0	pF

**Power Supply Characteristics**

Parameter	Description	Test Conditions		Typ. <sup>[4]</sup>	Max.	Unit
I <sub>CC</sub>	Quiescent Power Supply Current	V <sub>CC</sub> =Max.	V <sub>IN</sub> ≤0.2V, V <sub>IN</sub> ≥V <sub>CC</sub> −0.2V	5	500	μA
ΔI <sub>CC</sub>	Quiescent Power Supply Current (TTL inputs HIGH)	V <sub>CC</sub> =Max.	V <sub>IN</sub> =3.4V <sup>[8]</sup>	0.5	1.5	mA
I <sub>CCD</sub>	Dynamic Power Supply Current <sup>[9]</sup>	V <sub>CC</sub> =Max., One Input Toggling, 50% Duty Cycle, Outputs Open, $\overline{OE}$ =GND	V <sub>IN</sub> =V <sub>CC</sub> or V <sub>IN</sub> =GND	60	100	μA/MHz
I <sub>C</sub>	Total Power Supply Current <sup>[10]</sup>	V <sub>CC</sub> =Max., f <sub>1</sub> =10 MHz, 50% Duty Cycle, Outputs Open, One Bit Toggling, $\overline{OE}$ =GND	V <sub>IN</sub> =V <sub>CC</sub> or V <sub>IN</sub> =GND	0.6	1.5	mA
			V <sub>IN</sub> =3.4V or V <sub>IN</sub> =GND	0.9	2.3	mA
		V <sub>CC</sub> =Max., f <sub>1</sub> =2.5 MHz, 50% Duty Cycle, Outputs Open, Sixteen Bits Toggling, $\overline{OE}$ =GND	V <sub>IN</sub> =V <sub>CC</sub> or V <sub>IN</sub> =GND	2.4	4.5 <sup>[11]</sup>	mA
			V <sub>IN</sub> =3.4V or V <sub>IN</sub> =GND	6.4	16.5 <sup>[11]</sup>	mA

**Notes:**

8. Per TTL driven input ( $V_{IN} = 3.4V$ ); all other inputs at  $V_{CC}$  or GND.
9. This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
10.  $I_C = I_{\text{QUIESCENT}} + I_{\text{INPUTS}} + I_{\text{DYNAMIC}}$   
 $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_0/2 + f_1 N_1)$   
 $I_{CC}$  = Quiescent Current with CMOS input levels  
 $\Delta I_{CC}$  = Power Supply Current for a TTL HIGH input ( $V_{IN} = 3.4V$ )  
 $D_H$  = Duty Cycle for TTL inputs HIGH  
 $N_T$  = Number of TTL inputs at  $D_H$   
 $I_{CCD}$  = Dynamic Current caused by an input transition pair (HLH or LHL)  
 $f_0$  = Clock frequency for registered devices, otherwise zero  
 $f_1$  = Input signal frequency  
 $N_1$  = Number of inputs changing at  $f_1$   
 All currents are in milliamps and all frequencies are in megahertz.
11. Values for these conditions are examples of the  $I_{CC}$  formula. These limits are specified but not tested.

**Switching Characteristics** Over the Operating Range<sup>[12]</sup>

Parameter	Description	CY74FCT16240AT		CY74FCT162240CT		Unit	Fig. No. <sup>[13]</sup>
		Min.	Max.	Min.	Max.		
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay Data to Output	1.5	4.8	1.5	4.3	ns	1, 2
t <sub>PZH</sub> t <sub>PZL</sub>	Output Enable Time	1.5	6.2	1.5	5.8	ns	1, 7, 8
t <sub>PHZ</sub> t <sub>PLZ</sub>	Output Disable Time	1.5	5.6	1.5	5.2	ns	1, 7, 8
t <sub>SK(O)</sub>	Output Skew <sup>[14]</sup>		0.5		0.5	ns	—

**Note:**

12. Minimum limits are specified but not tested on Propagation Delays.

13. See "Parameter Measurement Information" in the General Information section.

14. Skew between any two outputs of the same package switching in the same direction. This parameter is ensured by design.

**Ordering Information CY74FCT16240**

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
4.8	CY74FCT16240ATPVC/PVCT	O48	48-Lead (300-Mil) SSOP	Industrial

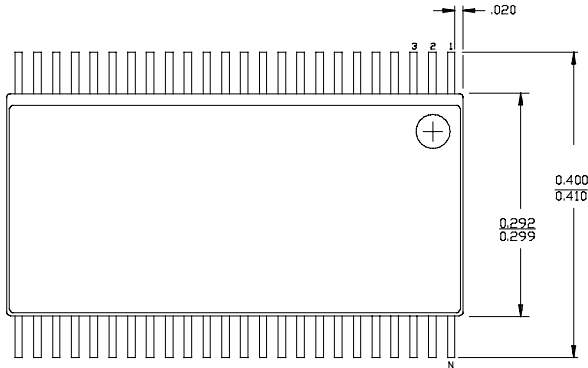
**Ordering Information CY74FCT162240**

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
4.3	74FCT162240CTPACT	Z48	48-Lead (240-Mil) TSSOP	Industrial
	CY74FCT162240CTPVC	O48	48-Lead (300-Mil) SSOP	
	74FCT162240CTPVCT	O48	48-Lead (300-Mil) SSOP	

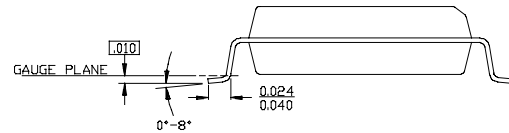
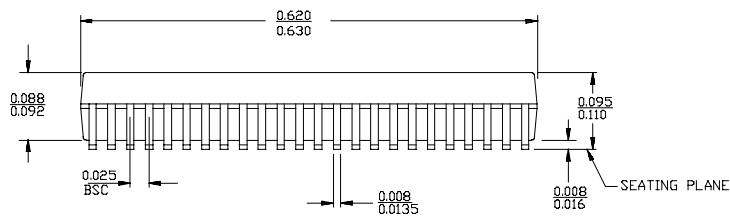
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**Package Diagrams**

**48-Lead Shrunk Small Outline Package O48**

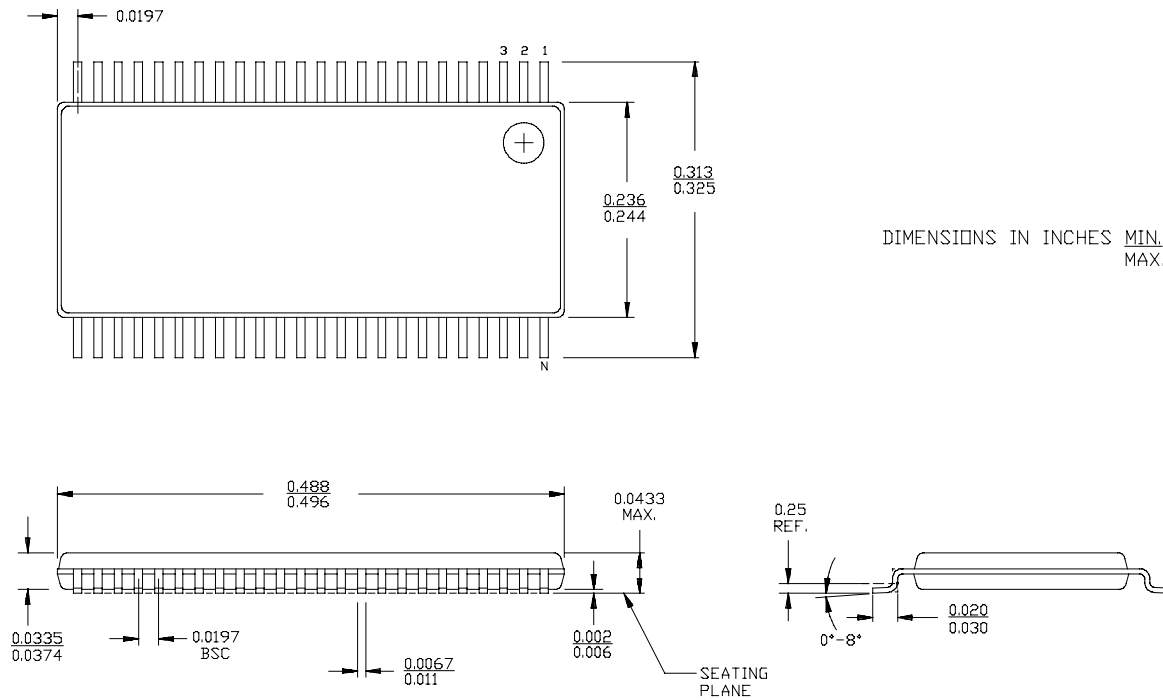


DIMENSIONS IN INCHES MIN.  
MAX.



**Package Diagrams**

**48-Lead Thin Shrink Small Outline Package**



## PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package   Pins	Package qty   Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
<a href="#">74FCT162240ATPACT</a>	Obsolete	Production	TSSOP (DGG)   48	-	-	Call TI	Call TI	-40 to 85	FCT162240A
<a href="#">74FCT162240CTPVCT</a>	Obsolete	Production	SSOP (DL)   48	-	-	Call TI	Call TI	-40 to 85	FCT162240C
<a href="#">CY74FCT16240ATPACT</a>	Obsolete	Production	TSSOP (DGG)   48	-	-	Call TI	Call TI	-40 to 85	FCT16240A
<a href="#">CY74FCT16240ATPVC</a>	Obsolete	Production	SSOP (DL)   48	-	-	Call TI	Call TI	-40 to 85	FCT16240A
<a href="#">CY74FCT16240ATPVCT</a>	Obsolete	Production	SSOP (DL)   48	-	-	Call TI	Call TI	-40 to 85	FCT16240A

<sup>(1)</sup> **Status:** For more details on status, see our [product life cycle](#).

<sup>(2)</sup> **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

<sup>(3)</sup> **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

<sup>(4)</sup> **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

<sup>(5)</sup> **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

<sup>(6)</sup> **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

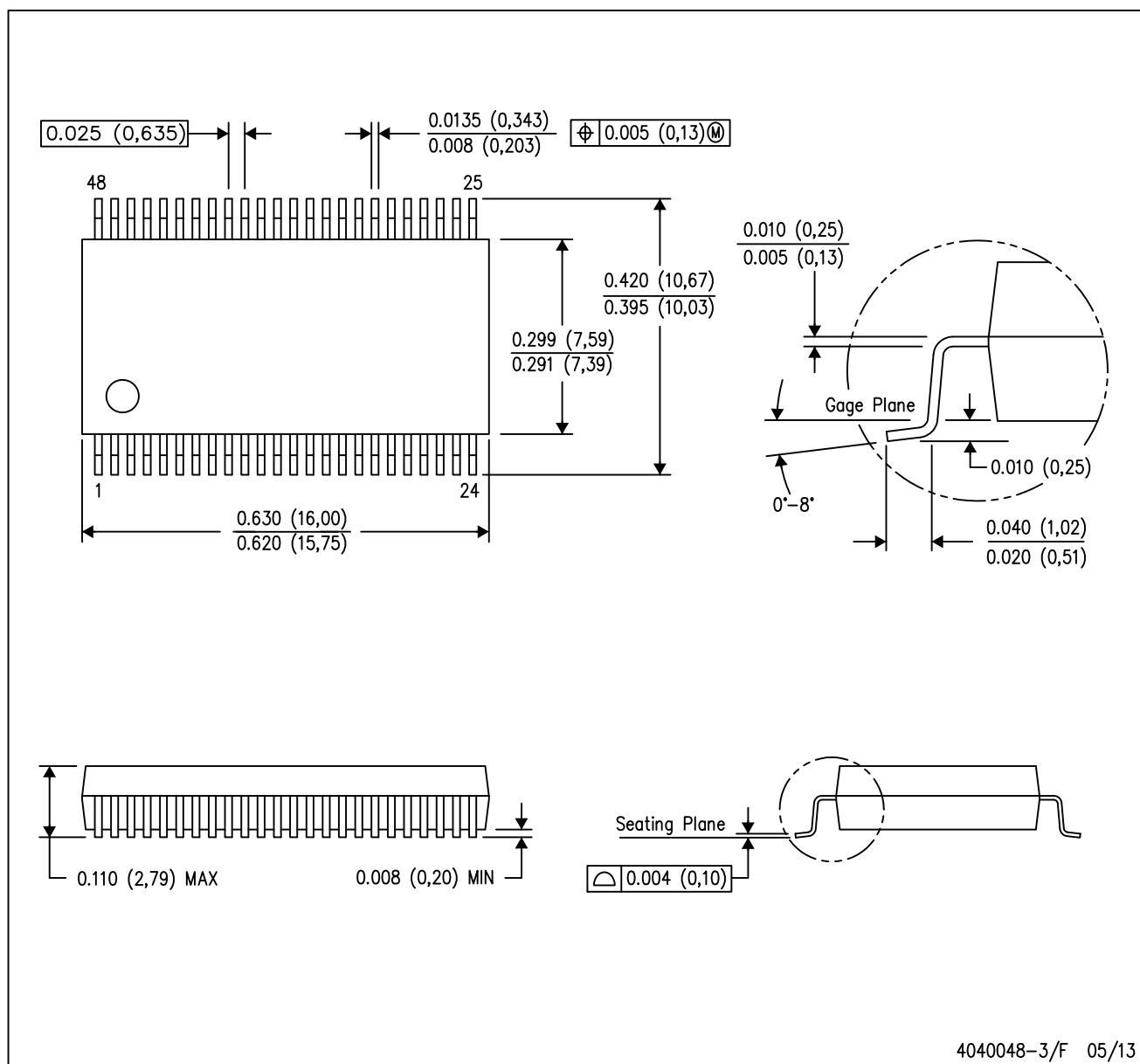
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## MECHANICAL DATA

DL (R-PDSO-G48)

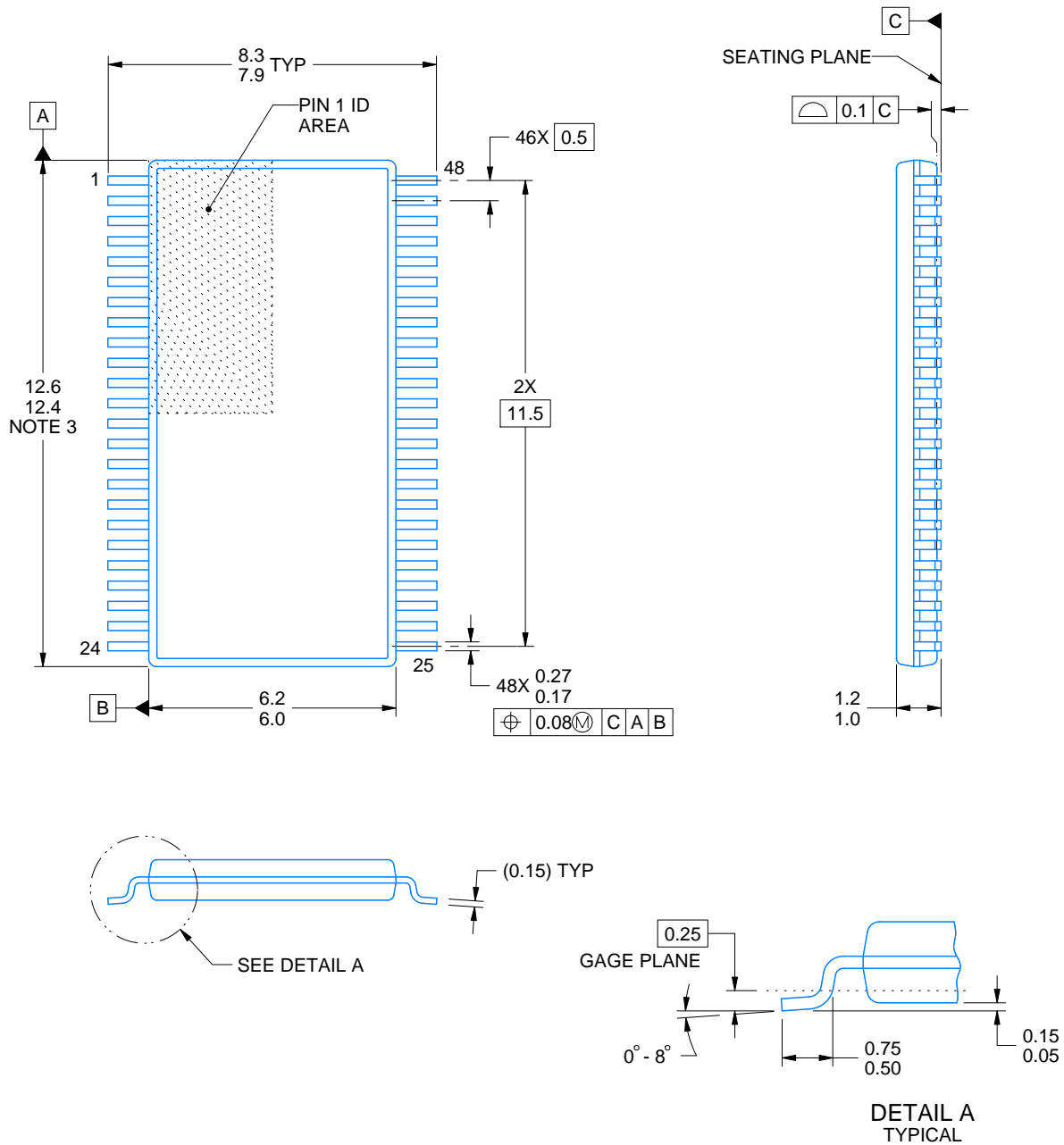
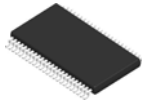
# PLASTIC SMALL-OUTLINE PACKAGE



- NOTES: A. All linear dimensions are in inches (millimeters).  
B. This drawing is subject to change without notice.  
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).  
D. Falls within JEDEC MO-118

**PowerPAD is a trademark of Texas Instruments.**





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## NOTES:

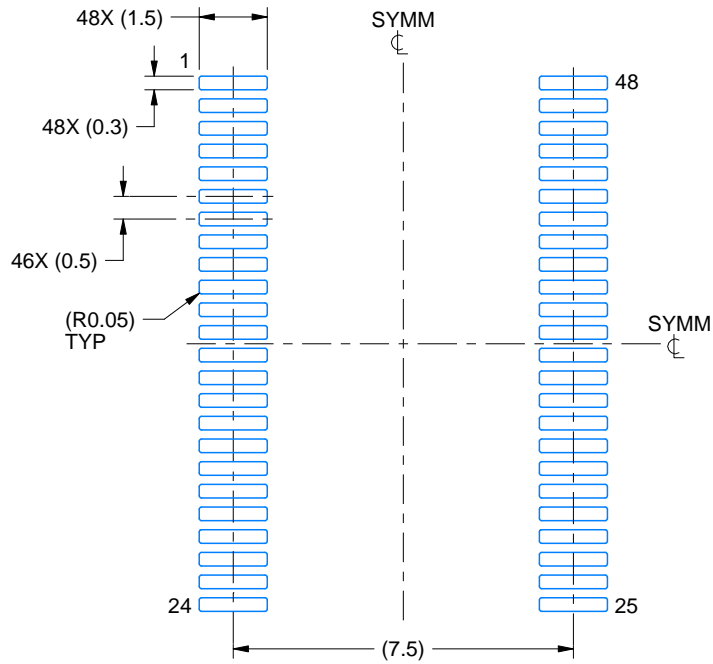
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-153.

# EXAMPLE BOARD LAYOUT

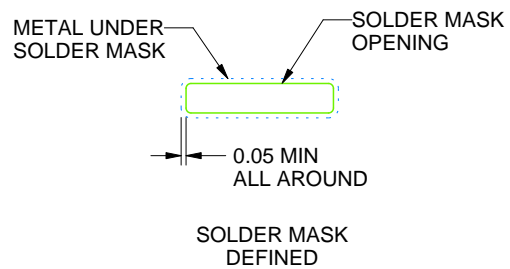
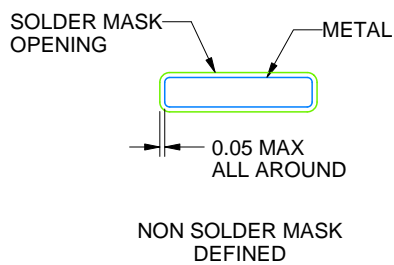
DGG0048A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
SCALE:6X



SOLDER MASK DETAILS

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NOTES: (continued)

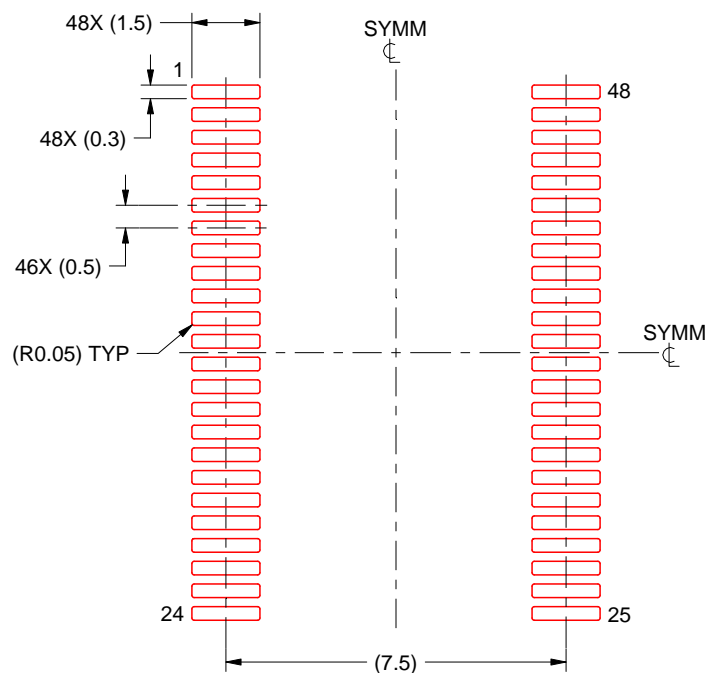
5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

DGG0048A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:6X

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NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

## DGG (R-PDSO-G\*\*)

## PLASTIC SMALL-OUTLINE PACKAGE

48 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold protrusion not to exceed 0,15.  
 D. Falls within JEDEC MO-153

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