LMH6723/LMH6724 Single/Dual/Quad 370-MHz, 1-mA Current Feedback Operational Amplifier

1 Features

- Large Signal Bandwidth and Slew Rate 100% Tested
- 370 MHz Bandwidth (A_V = 1, V_{OUT} = 0.5 V_{PP}) −3 dB BW
- 260 MHz (A_V = +2 V/V, V_{OUT} = 0.5 V_{PP}) −3 dB BW
- 1 mA Supply Current
- 110 mA Linear Output Current
- 0.03%, 0.11° Differential Gain, Phase
- 0.1 dB Gain Flatness to 100 MHz
- Fast Slew Rate: 600 V/µs
- Unity Gain Stable
- Single Supply Range of 4.5 to 12V
- Improved Replacement for CLC450, CLC452, (LMH6723)

2 Applications

- Line Driver
- Portable Video
- A/D Driver
- Portable DVD

3 Description

The LMH6723/LMH6724 provides a 260 MHz small signal bandwidth at a gain of +2 V/V and a 600 V/µs slew rate while consuming only 1 mA from ±5V supplies.

The LMH6723/LMH6724 supports video applications with its 0.03% and 0.11° differential gain and phase for NTSC and PAL video signals, while also offering a flat gain response of 0.1 dB to 100 MHz. Additionally, the LMH6723/LMH6724 can deliver 110 mA of linear output current. This level of performance, as well as a wide supply range of 4.5 to 12V, makes the LMH6723/LMH6724 an ideal op amp for a variety of portable applications. With small packages (SOIC and SOT-23), low power requirement, and high performance, the LMH6723/LMH6724 serves a wide variety of portable applications.

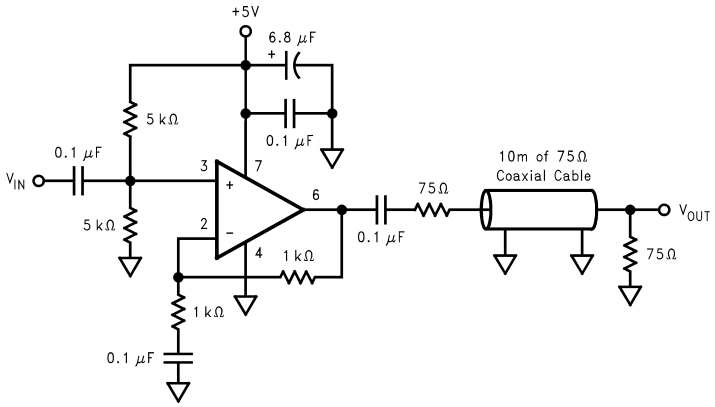
The LMH6723/LMH6724 is manufactured in Texas Instruments' VIP10 complimentary bipolar process.

Device Information[1]

PART NUMBER	PACKAGE	BODY SIZE (NOM)
LMH6723	SOT-23 (5)	2.90 mm × 1.60 mm
LMH6723	SOIC (8)	4.90 mm × 3.91 mm
LMH6724	SOIC (8)	4.90 mm × 3.91 mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.

Typical Application



An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

Table of Contents

4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision H (April 2013) to Revision I **Page**

- Changed data sheet structure and organization. Added, updated, or renamed the following sections: Device Information Table, Application and Implementation; Power Supply Recommendations; Device and Documentation Support; Mechanical, Packaging, and Ordering Information. Removed "LMH6725" from title and document. ... 1
- Deleted "Channel Matching" and "Crosstalk" plots. ... 8
- Changed Figure 11 ... 9
- Changed Figure 12 ... 9
- Changed Figure 29 ... 11
- Changed Figure 30 ... 11
- Deleted sentence beginning "These evaluation boards..." ... 13
- Deleted sentence beginning, "Although the example..." ... 17
- Deleted sentence beginning "The SOIC-14 has ..." ... 19

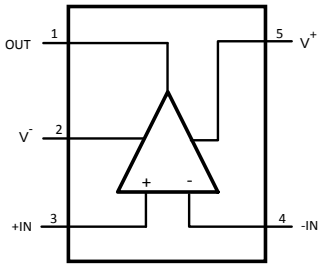
Changes from Revision G (April 2013) to Revision H **Page**

- Changed layout of National Data Sheet to TI format ... 19

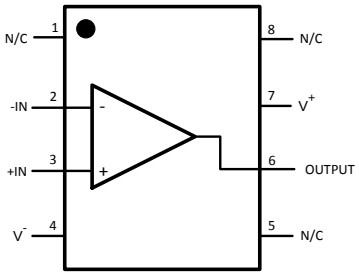
Copyright © 2003–2014, Texas Instruments Incorporated

5 Pin Configuration and Functions

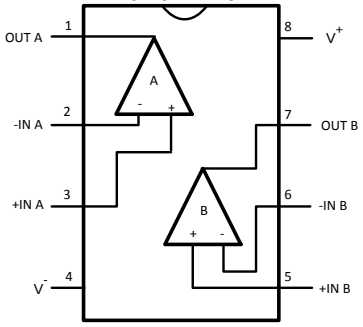
**5-Pin SOT-23 (LMH6723)
Package DBV
(Top View)**



**8-Pin SOIC Package (LMH6723)
Package D08A
(Top View)**



**8-Pin SOIC Package (LMH6724)
Package D08A
(Top View)**



Pin Functions

PIN				I/O	DESCRIPTION
NAME	NUMBER				
	LMH6723 (DBV)	LMH6723 (D08A)	LMH6724 (D08A)		
-IN	4	2		I	Inverting Input
+IN	3	3		I	Non-inverting Input
-IN A			2	I	ChA Inverting Input
+IN A			3	I	ChA Non-inverting Input
-IN B			6	I	ChB Inverting Input
+IN B			5	I	ChB Non-inverting Input
N/C		1,5,8		–	–
OUT A			1	O	ChA Output
OUT B			7	O	ChB Output
OUTPUT	1	6		O	Output
V -	2	4	4	I	Negative Supply
V+	5	7	8	I	Positive Supply

Copyright © 2003–2014, Texas Instruments Incorporated

6 Specifications

6.1 Absolute Maximum Ratings[1][2][3]

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_{CC} (V^+ - V^-)			±6.75	V
I_{OUT}			120[4]	mA
Common Mode Input Voltage			$\pm V_{CC}$	V
Maximum Junction Temperature			+150	°C
Soldering Information	Infrared or Convection (20 sec)		235	°C
	Wave Soldering (10 sec)		260	°C

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not ensured. For ensured specifications, see the Electrical Characteristics tables.
(2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/Distributors for availability and specifications.
(3) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(4) The maximum continuous output current (I_{OUT}) is determined by device power dissipation limitations. See *Power Supply Recommendations* for more details.

6.2 Handling Ratings

			MIN	MAX	UNIT
T_{stg}	Storage temperature range		−65	+150	°C
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins[1][2]		2000	V
		Machine Model (MM), per JEDEC specification JESD22-C101, all pins[2][3]		200	

(1) JEDEC document JEP155 states that 2000-V HBM allows safe manufacturing with a standard ESD control process.
(2) Human Body Model, 1.5 kΩ in series with 100 pF. Machine Model, 0Ω In series with 200 pF.
(3) JEDEC document JEP157 states that 200-V MM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions[1]

over operating free-air temperature range (unless otherwise noted)

	MIN	NOM	MAX	UNIT
Operating Temperature Range	−40		+85	°C
Nominal Supply Voltage	4.5		12	V

(1) The maximum continuous output current (I_{OUT}) is determined by device power dissipation limitations. See *Power Supply Recommendations* for more details.

6.4 Thermal Information

THERMAL METRIC[1]		SOT-23	SOIC	UNIT
		DBV	D08A	
		5 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	230°C/W	166°C/W	°C/W

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

Copyright © 2003–2014, Texas Instruments Incorporated

6.5 ±5V Electrical Characteristics

Unless otherwise specified, A_V = +2, R_F = 1200Ω, R_L = 100Ω. **Boldface** limits apply at temperature extremes.(1)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
FREQUENCY DOMAIN RESPONSE							
SSBW	−3 dB Bandwidth Small Signal	V_{OUT} = 0.5 V_{PP}			260		MHz
LSBW	−3dB Bandwidth Large Signal	V_{OUT} = 4.0 V_{PP}		90	110		MHz
				85	95		
UGBW	−3 dB Bandwidth Unity Gain	V_{OUT} = .2 V_{PP} A_V = 1 V/V			370		MHz
.1dB BW	.1 dB Bandwidth	V_{OUT} = 0.5 V_{PP}			100		MHz
DG	Differential Gain	R_L = 150Ω, 4.43 MHz			0.03%		
DP	Differential Phase	R_L = 150Ω, 4.43 MHz			0.11		deg
TIME DOMAIN RESPONSE							
TRS	Rise and Fall Time	4V Step			2.5		ns
TSS	Settling Time to 0.05%	2V Step			30		ns
SR	Slew Rate	4V Step		500	600		V/µs
DISTORTION and NOISE RESPONSE							
HD2	2nd Harmonic Distortion	2 V_{PP}, 5 MHz			−65		dBc
HD3	3rd Harmonic Distortion	2 V_{PP}, 5 MHz			−63		dBc
EQUIVALENT INPUT NOISE							
VN	Non-Inverting Voltage Noise	>1 MHz			4.3		nV/√Hz
NICN	Inverting Current Noise	>1 MHz			6		pA/√Hz
ICN	Non-Inverting Current Noise	>1 MHz			6		pA/√Hz
STATIC, DC PERFORMANCE							
V_{IO}	Input Offset Voltage				1	±3 **±3.7**	mV
I_{BN}	Input Bias Current	Non-Inverting			−2	±4 **±5**	µA
I_{BI}	Input Bias Current	Inverting			0.4	±4 **±5**	µA
PSRR	Power Supply Rejection Ratio	DC, 1V Step	LMH6723	59 **57**	64		dB
			LMH6724	59 **55**	64		
CMRR	Common Mode Rejection Ratio	DC, 1V Step	LMH6723	57 **55**	60		dB
			LMH6724	57 **53**	60		
I_{CC}	Supply Current (per amplifier)	R_L = ∞			1	1.2 **1.4**	mA

(1) Electrical Table values apply only for factory testing conditions at the temperature indicated. Factory testing conditions result in very limited self-heating of the device such that $T_J = T_A$. No ensured specification of parametric performance is indicated in the electrical tables under conditions of internal self heating where $T_J > T_A$. See *Application and Implementation* for information on temperature derating of this device. Min/Max ratings are based on product characterization and simulation. Individual parameters are tested as noted.

Copyright © 2003–2014, Texas Instruments Incorporated

±5V Electrical Characteristics (continued)

Unless otherwise specified, A_V = +2, R_F = 1200Ω, R_L = 100Ω. **Boldface** limits apply at temperature extremes.(1)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
MISCELLANEOUS PERFORMANCE							
R_{IN+}	Input Resistance	Non-Inverting			100		kΩ
R_{IN-}	Input Resistance (Output Resistance of Input Buffer)	Inverting			500		Ω
C_{IN}	Input Capacitance	Non-Inverting			1.5		pF
R_{OUT}	Output Resistance	Closed Loop			0.01		Ω
V_O	Output Voltage Range	R_L = ∞	LMH6723	±4 **±3.9**	±4.1		V
			LMH6724	±4 **±3.85**	±4.1		
V_{OL}	Output Voltage Range, High	R_L = 100Ω		3.6 **3.5**	3.7		V
	Output Voltage Range, Low	R_L = 100Ω		−3.25 **−3.1**	−3.45		
CMVR	Input Voltage Range	Common Mode, CMRR > 50 dB		±4.0			V
I_O	Output Current	Sourcing, V_{OUT} = 0		95 **70**	110		mA
		Sinking, V_{OUT} = 0		−80 **−70**	110		

6.6 ±2.5V Electrical Characteristics

Unless otherwise specified, A_V = +2, R_F = 1200Ω, R_L = 100Ω. **Boldface** limits apply at temperature extremes.(1)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
FREQUENCY DOMAIN RESPONSE						
SSBW	−3 dB Bandwidth Small Signal	V_{OUT} = 0.5 V_{PP}		210		MHz
LSBW	−3 dB Bandwidth Large Signal	V_{OUT} = 2.0 V_{PP}	95	125		MHz
UGBW	−3 dB Bandwidth Unity Gain	V_{OUT} = 0.5 V_{PP}, A_V = 1 V/V		290		MHz
.1dB BW	.1 dB Bandwidth	V_{OUT} = 0.5 V_{PP}		100		MHz
DG	Differential Gain	R_L = 150Ω, 4.43 MHz		.03%		
DP	Differential Phase	R_L = 150Ω, 4.43 MHz		0.1		deg
TIME DOMAIN RESPONSE						
TRS	Rise and Fall Time	2V Step		4		ns
SR	Slew Rate	2V Step	275	400		V/µs
DISTORTION AND NOISE RESPONSE						
HD2	2nd Harmonic Distortion	2 V_{PP}, 5 MHz		−67		dBc
HD3	3rd Harmonic Distortion	2 V_{PP}, 5 MHz		−67		dBc
EQUIVALENT INPUT NOISE						
VN	Non-Inverting Voltage	>1 MHz		4.3		nV/√Hz
NICN	Inverting Current	>1MHz		6		pA/√Hz
ICN	Non-Inverting Current	>1MHz		6		pA/√Hz

(1) Electrical Table values apply only for factory testing conditions at the temperature indicated. Factory testing conditions result in very limited self-heating of the device such that $T_J = T_A$. No ensured specification of parametric performance is indicated in the electrical tables under conditions of internal self heating where $T_J > T_A$. See *Application and Implementation* for information on temperature derating of this device. Min/Max ratings are based on product characterization and simulation. Individual parameters are tested as noted.

Copyright © 2003–2014, Texas Instruments Incorporated

±2.5V Electrical Characteristics (continued)

Unless otherwise specified, A_V = +2, R_F = 1200Ω, R_L = 100Ω. **Boldface** limits apply at temperature extremes.(1)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
STATIC, DC PERFORMANCE							
V_{IO}	Input Offset Voltage				−0.5	±3 **±3.4**	mV
I_{BN}	Input Bias Current	Non-Inverting			−2.7	±4 **±5**	µA
I_{BI}	Input Bias Current	Inverting			−0.7	±4 **±5**	µA
PSRR	Power Supply Rejection Ratio	DC, 0.5V Step	LMH6723	59 **57**	62		dB
			LMH6724	58 **55**	62		
CMRR	Common Mode Rejection Ratio	DC, 0.5V Step	LMH6723	57 **53**	59		dB
			LMH6724	55 **52**	59		
I_{CC}	Supply Current (per amplifier)	R_L = ∞			0.9	1.1 **1.3**	mA
MISCELLANEOUS PERFORMANCE							
R_{IN+}	Input Resistance	Non-Inverting			100		kΩ
R_{IN-}	Input Resistance (Output Resistance of Input Buffer)	Inverting			500		Ω
C_{IN}	Input Capacitance	Non-Inverting			1.5		pF
R_{OUT}	Output Resistance	Closed Loop			0.02		Ω
V_O	Output Voltage Range	R_L = ∞		±1.55 **±1.4**	±1.65		V
V_{OL}	Output Voltage Range, High	R_L = 100Ω	LMH6723	1.35 **1.27**	1.45		V
			LMH6724	1.35 **1.26**	1.45		
	Output Voltage Range, Low	R_L = 100Ω	LMH6723	−1.25 **−1.15**	−1.38		V
			LMH6724	−1.25 **−1.15**	−1.38		
CMVR	Input Voltage Range	Common Mode, CMRR > 50 dB		±1.45			V
I_O	Output Current	Sourcing		70 **60**	90		mA
		Sinking		−30 **−30**	−60		

Copyright © 2003–2014, Texas Instruments Incorporated

6.7 Typical Performance Characteristics

A_V = 2, R_F = 1200Ω, R_L = 100Ω, unless otherwise specified.

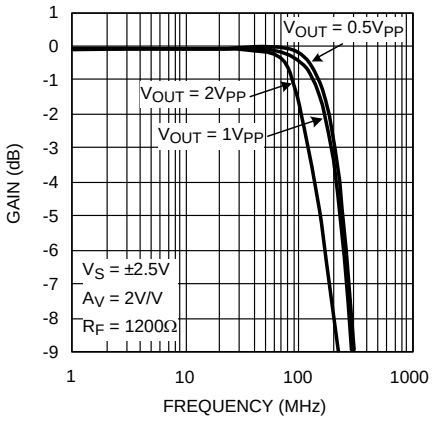


Figure 1. Frequency Response vs. V_{OUT}, A_V = 2

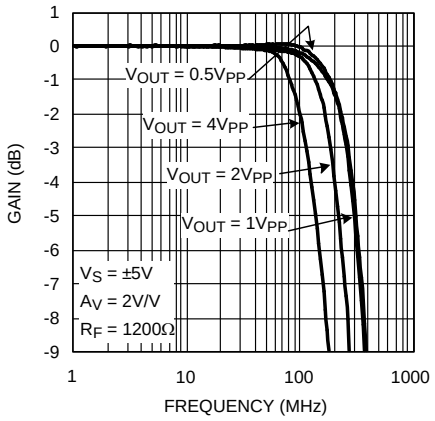


Figure 2. Frequency Response vs. V_{OUT}, A_V = 2

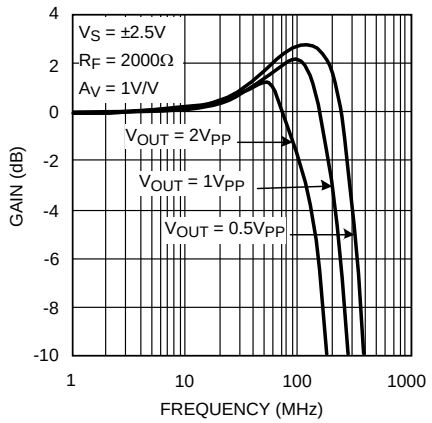


Figure 3. Frequency Response vs. V_{OUT}, A_V = 1

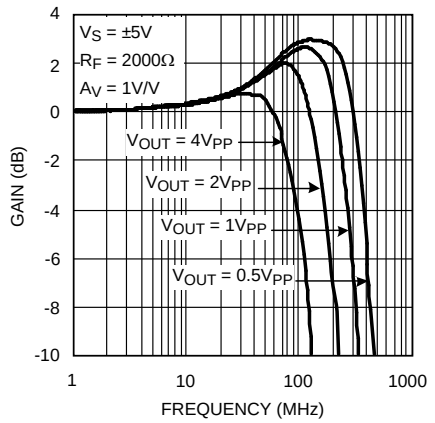


Figure 4. Frequency Response vs. V_{OUT}, A_V = 1

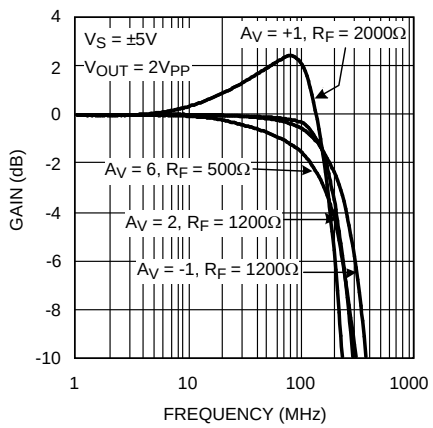


Figure 5. Large Signal Frequency Response

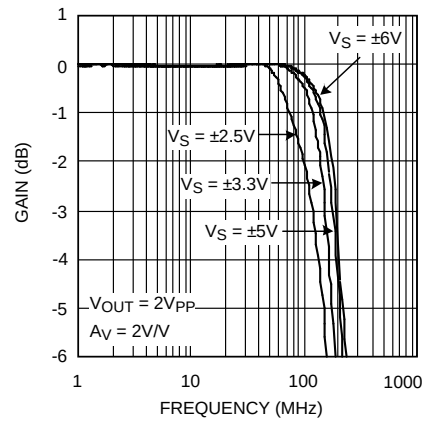


Figure 6. Frequency Response vs. Supply Voltage

Copyright © 2003–2014, Texas Instruments Incorporated

Typical Performance Characteristics (continued)

A_V = 2, R_F = 1200Ω, R_L = 100Ω, unless otherwise specified.

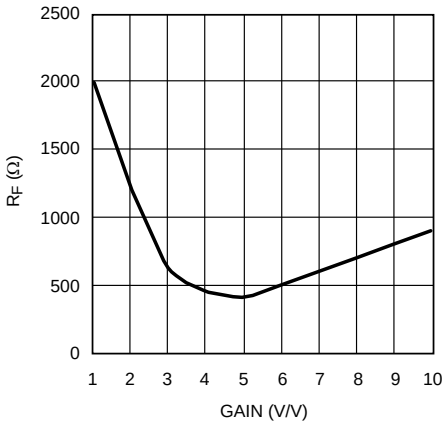


Figure 7. Suggested R_F vs. Gain Non-Inverting

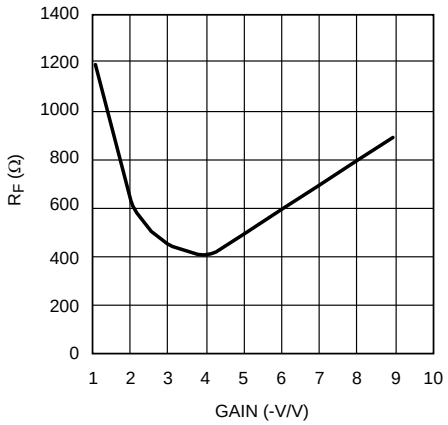


Figure 8. Suggested R_F vs. Gain Inverting

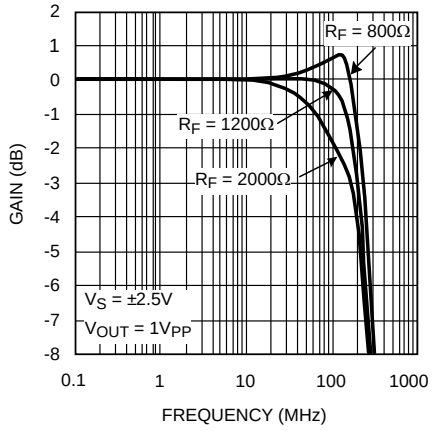


Figure 9. Frequency Response vs. R_F

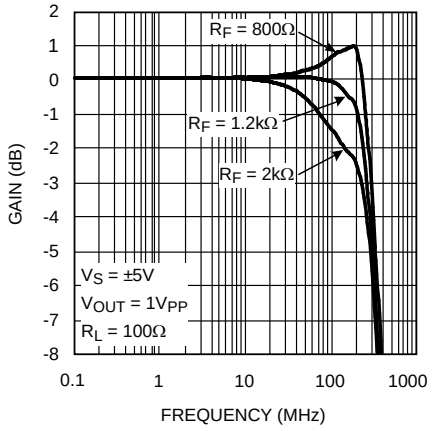


Figure 10. Frequency Response vs. R_F

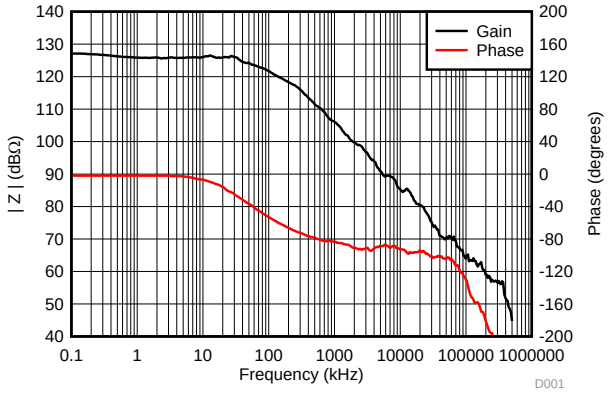


Figure 11. Open Loop Gain & Phase

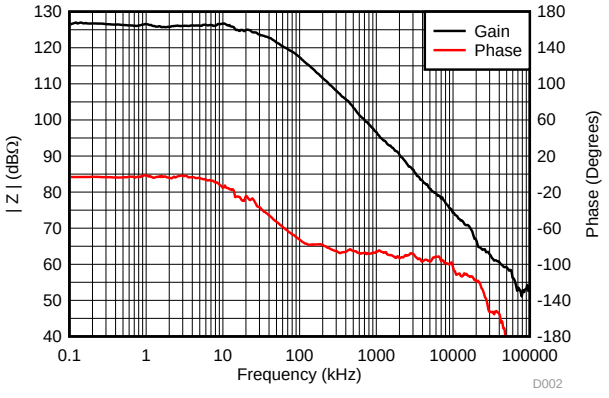


Figure 12. Open Loop Gain & Phase

Typical Performance Characteristics (continued)

A_V = 2, R_F = 1200Ω, R_L = 100Ω, unless otherwise specified.

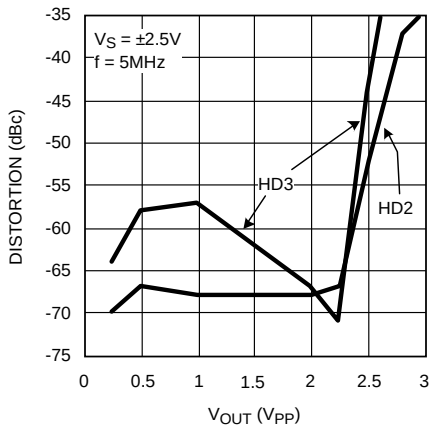


Figure 13. HD2 & HD3 vs. V_{OUT}

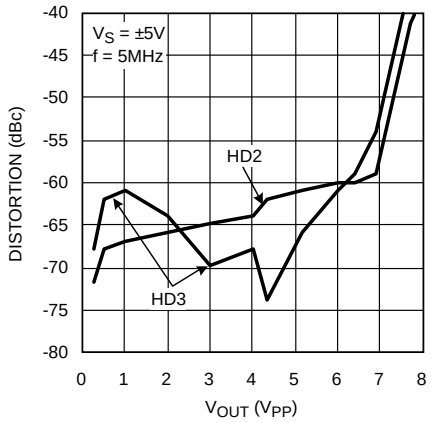


Figure 14. HD2 & HD3 vs. V_{OUT}

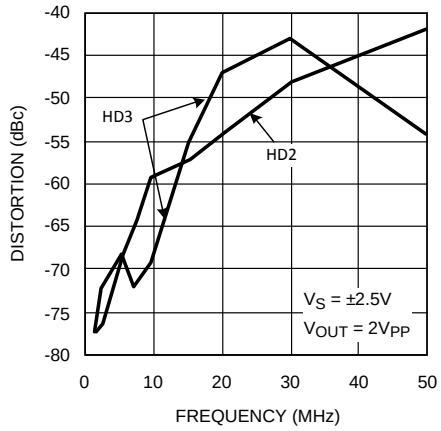


Figure 15. HD2 & HD3 vs. Frequency

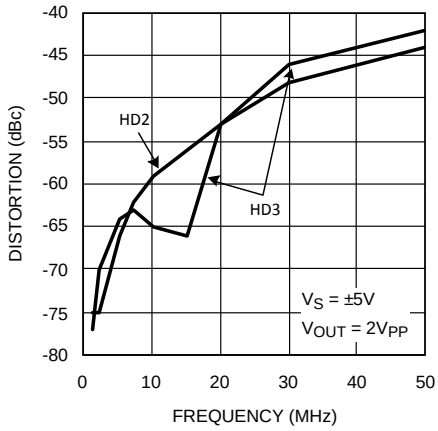


Figure 16. HD2 & HD3 vs. Frequency

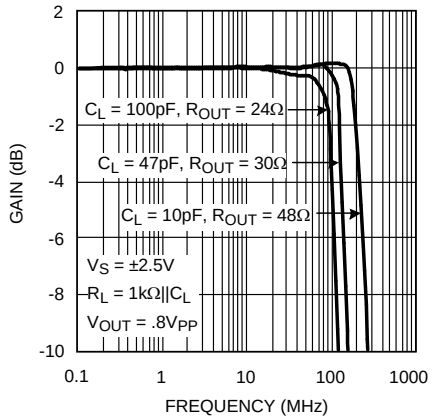


Figure 17. Frequency Response vs. C_L

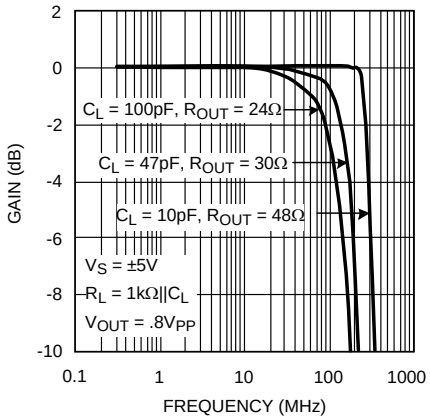


Figure 18. Frequency Response vs. C_L

Copyright © 2003–2014, Texas Instruments Incorporated

Typical Performance Characteristics (continued)

A_V = 2, R_F = 1200Ω, R_L = 100Ω, unless otherwise specified.

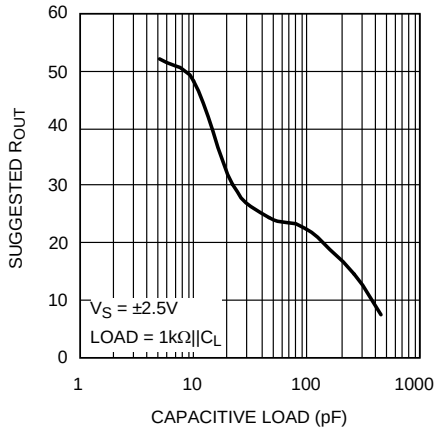


Figure 19. Suggested R_{OUT} vs. C_L

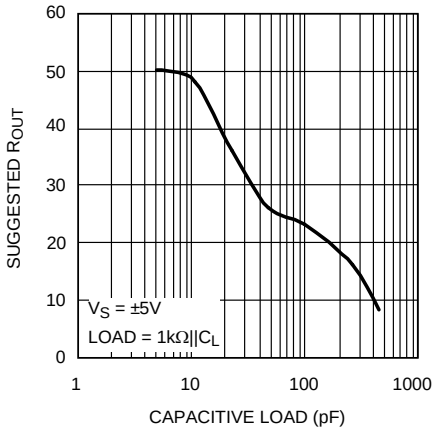


Figure 20. Suggested R_{OUT} vs. C_L

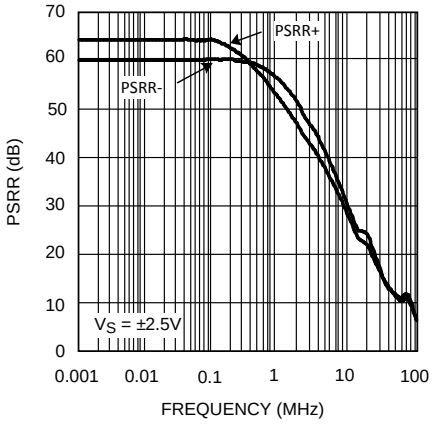


Figure 21. PSRR vs. Frequency

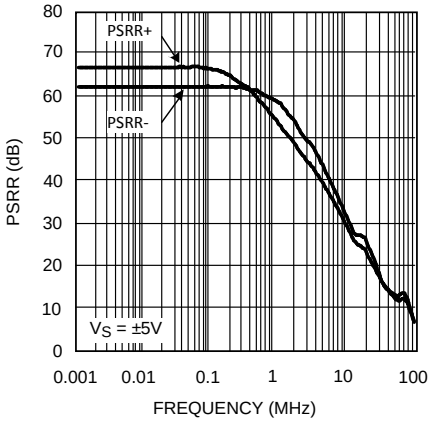


Figure 22. PSRR vs. Frequency

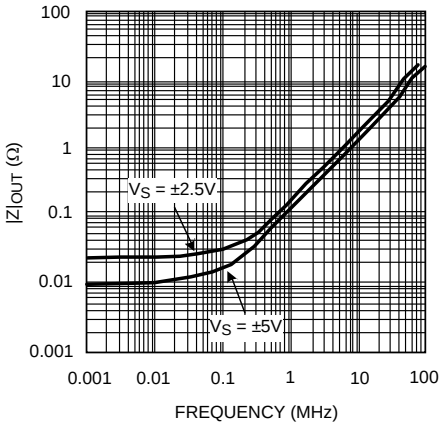


Figure 23. Closed Loop Output Resistance

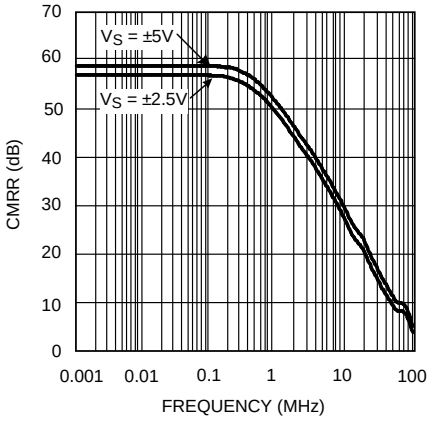


Figure 24. CMRR vs. Frequency

Typical Performance Characteristics (continued)

A_V = 2, R_F = 1200Ω, R_L = 100Ω, unless otherwise specified.

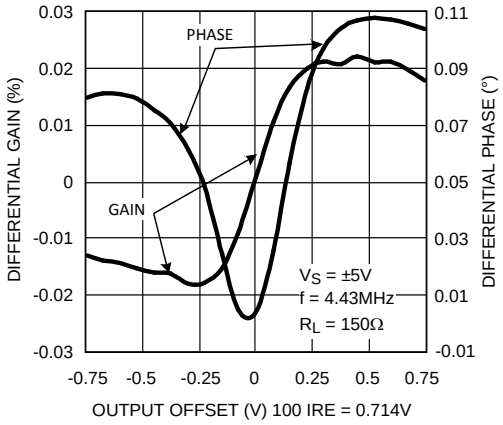


Figure 25. Differential Gain & Phase

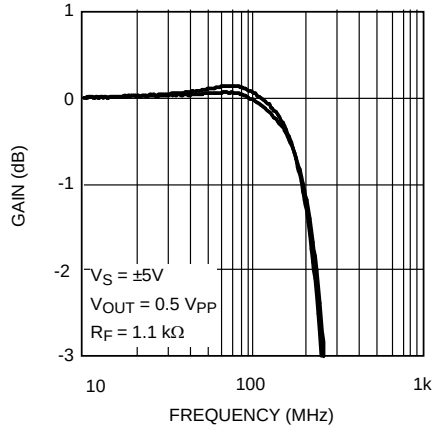


Figure 26. Channel Matching (LMH6724)

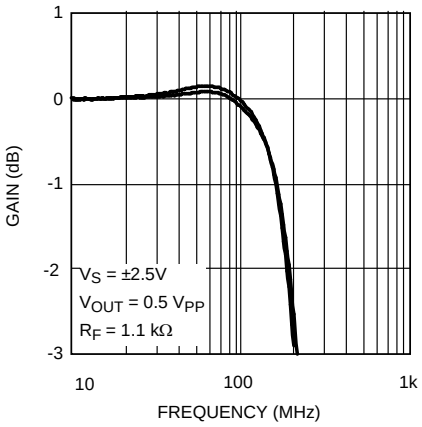


Figure 27. Channel Matching (LMH6724)

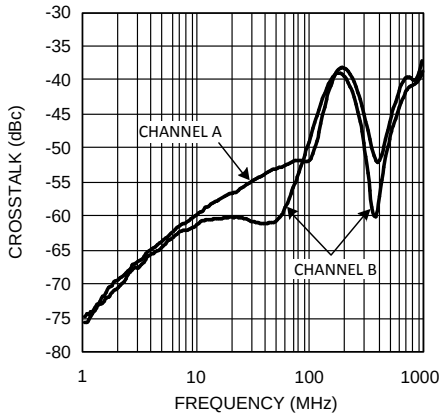


Figure 28. Crosstalk (LMH6724)

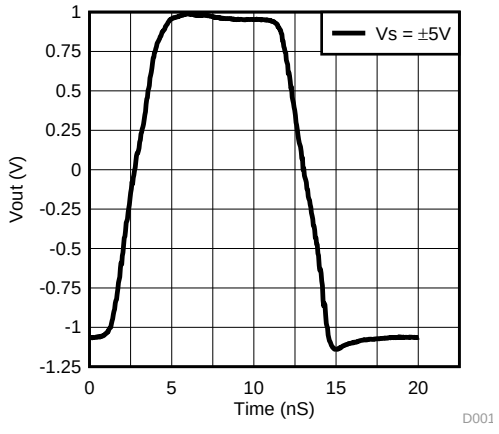


Figure 29. Output Small Signal Pulse Response

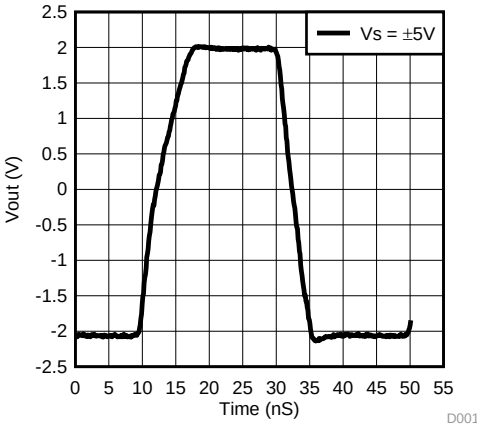


Figure 30. Output Large Signal Pulse Response

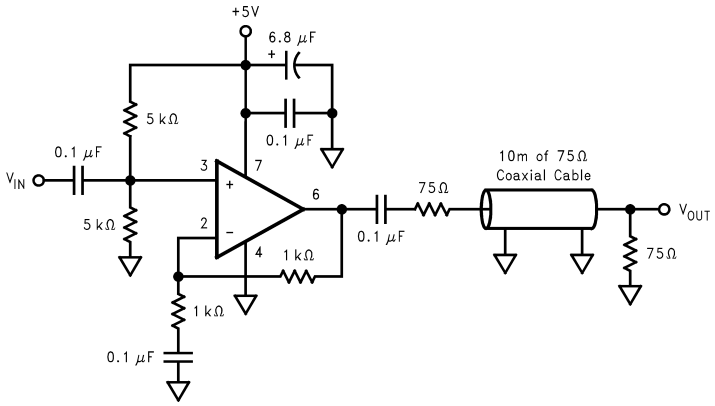
Copyright © 2003–2014, Texas Instruments Incorporated

7 Application and Implementation

7.1 Application Information

The LMH6723/LMH6724 is a high speed current feedback amplifier manufactured on Texas Instruments' VIP10 (Vertically Integrated PNP) complimentary bipolar process. LMH6723/LMH6724 offers a unique combination of high speed and low quiescent supply current making it suitable for a wide range of battery powered and portable applications that require high performance. This amplifier can operate from 4.5V to 12V nominal supply voltages and draws only 1 mA of quiescent supply current at 10V supplies (±5V typically). The LMH6723/LMH6724 has no internal ground reference so single or split supply configurations are both equally useful.

7.2 Typical Application



7.3 Evaluation Boards

Texas Instruments provides the following evaluation boards as a guide for high frequency layout and as an aid in device testing and characterization. Many of the datasheet plots were measured with these boards.

DEVICE	PACKAGE	BOARD PART NUMBER
LMH6723MA	SOIC-8	LMH730227
LMH6723MF	SOT-23	LMH730216
LMH6724MA	SOIC-8	LMH730036

Copyright © 2003–2014, Texas Instruments Incorporated

7.4 Feedback Resistor Selection

One of the key benefits of a current feedback operational amplifier is the ability to maintain optimum frequency response independent of gain by using appropriate values for the feedback resistor (R_F). The Electrical Characteristics and Typical Performance plots were generated with an R_F of 1200Ω, a gain of +2V/V and ±5V or ±2.5V power supplies (unless otherwise specified). Generally, lowering R_F from its recommended value will peak the frequency response and extend the bandwidth; however, increasing the value of R_F will cause the frequency response to roll off faster. Reducing the value of R_F too far below it's recommended value will cause overshoot, ringing, and eventually, oscillation.

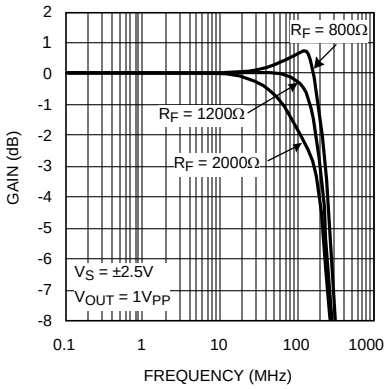


Figure 31. Frequency Response vs. R_F

Figure 31 shows the LMH6723/LMH6724's frequency response as R_F is varied (R_L = 100Ω, A_V = +2). This plot shows that an R_F of 800Ω results in peaking. An R_F of 1200Ω gives near maximal bandwidth and gain flatness with good stability. Since each application is slightly different, it is worth experimenting to find the optimal R_F for a given circuit. In general, a value of R_F that produces ~0.1 dB of peaking is the best compromise between stability and maximal bandwidth. Note that it is not possible to use a current feedback amplifier with the output shorted directly to the inverting input. The buffer configuration of the LMH6723/LMH6724 requires a 2000-Ω feedback resistor for stable operation. For other gains see the charts Figure 32 and Figure 33. These charts provide a good place to start when selecting the best feedback resistor value for a variety of gain settings.

Copyright © 2003–2014, Texas Instruments Incorporated

Feedback Resistor Selection (continued)

For more information see Application Note OA-13 which describes the relationship between R_F and closed-loop frequency response for current feedback operational amplifiers. The value for the inverting input impedance for the LMH6723/LMH6724 is approximately 500 Ω. The LMH6723/LMH6724 is designed for optimum performance at gains of +1 to +5V/V and −1 to −4V/V. Higher gain configurations are still useful; however, the bandwidth will fall as gain is increased, much like a typical voltage feedback amplifier.

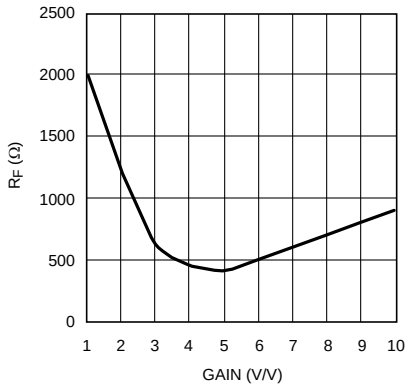


Figure 32. RF vs. Non-Inverting Gain

Figure 32 and Figure 33 show the value of R_F versus gain. A higher R_F is required at higher gains to keep R_G from decreasing too far below the input impedance of the inverting input. This limitation applies to both inverting and non-inverting configurations. For the LMH6723/LMH6724 the input resistance of the inverting input is approximately 500Ω and 100Ω is a practical lower limit for R_G. The LMH6723/LMH6724 begins to operate in a gain bandwidth limited fashion in the region where R_F must be increased for higher gains. Note that the amplifier will operate with R_G values well below 100 Ω; however, results will be substantially different than predicted from ideal models. In particular, the voltage potential between the Inverting and Non-Inverting inputs cannot be expected to remain small.

For inverting configurations the impedance seen by the source is R_G || R_T. For most sources this limits the maximum inverting gain since R_F is determined by the desired gain as shown in Figure 33. The value of R_G is then R_F/Gain. Thus for an inverting gain of −4 V/V the input impedance is equal to 100Ω. Using a termination resistor, this can be brought down to match a 50-Ω or 75-Ω source; however, a 150Ω source cannot be matched without a severe compromise in R_F.

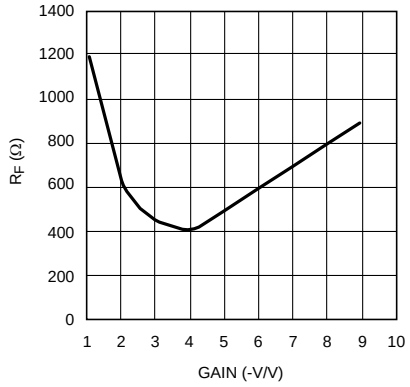


Figure 33. R_F vs. Inverting Gain

Copyright © 2003–2014, Texas Instruments Incorporated

7.5 Active Filters

When using any current feedback operational amplifier as an active filter it is necessary to be careful using reactive components in the feedback loop. Reducing the feedback impedance, especially at higher frequencies, will almost certainly cause stability problems. Likewise capacitance on the inverting input should be avoided. See Application Notes OA-07 and OA-26 for more information on Active Filter applications for Current Feedback Op Amps.

When using the LMH6723/LMH6724 as a low-pass filter the value of R_F can be substantially reduced from the value recommended in the R_F vs. Gain charts. The benefit of reducing R_F is increased gain at higher frequencies, which improves attenuation in the stop band. Stability problems are avoided because in the stop band additional device bandwidth is used to cancel the input signal rather than amplify it. The benefit of this change depends on the particulars of the circuit design. With a high pass filter configuration reducing R_F will likely result in device instability and is not recommended.

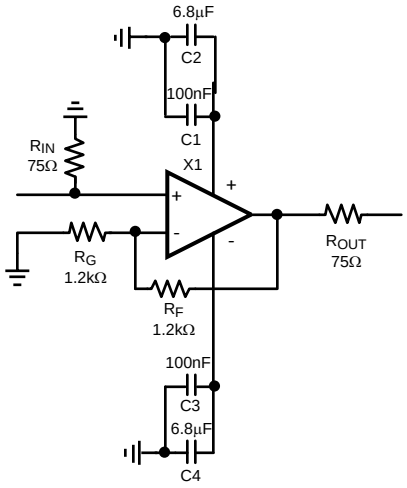


Figure 34. Typical Application with Suggested Supply Bypassing

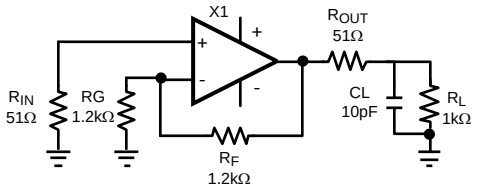


Figure 35. Decoupling Capacitive Loads

7.6 Driving Capacitive Loads

Capacitive output loading applications will benefit from the use of a series output resistor as shown in Figure 35. The charts "Suggested R_{OUT} vs. Cap Load" give a recommended value for selecting a series output resistor for mitigating capacitive loads. The values suggested in the charts are selected for .5 dB or less of peaking in the frequency response. This gives a good compromise between settling time and bandwidth. For applications where maximum frequency response is needed and some peaking is tolerable, the value of R_{OUT} can be reduced slightly from the recommended values.

There will be amplitude lost in the series resistor unless the gain is adjusted to compensate; this effect is most noticeable with heavy loads (R_L < 150Ω).

Copyright © 2003–2014, Texas Instruments Incorporated

Driving Capacitive Loads (continued)

An alternative approach is to place R_{OUT} inside the feedback loop as shown in Figure 36. This will preserve gain accuracy, but will still limit maximum output voltage swing.

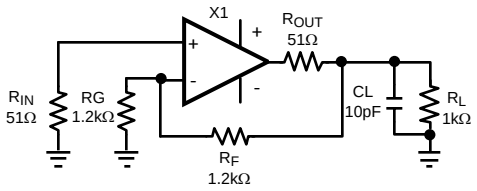


Figure 36. Series Output Resistor Inside Feedback Loop

7.7 Inverting Input Parasitic Capacitance

Parasitic capacitance is any capacitance in a circuit that was not intentionally added. It is produced through electrical interaction between conductors and can be reduced but never entirely eliminated. Most parasitic capacitances that cause problems are related to board layout or lack of termination on transmission lines. See *Layout Considerations* for hints on reducing problems due to parasitic capacitances on board traces. Transmission lines should be terminated in their characteristic impedance at both ends.

High speed amplifiers are sensitive to capacitance between the inverting input and ground or power supplies. This shows up as gain peaking at high frequency. The capacitor raises device gain at high frequencies by making R_G appear smaller. Capacitive output loading will exaggerate this effect.

One possible remedy for this effect is to slightly increase the value of the feedback (and gain set) resistor. This will tend to offset the high frequency gain peaking while leaving other parameters relatively unchanged. If the device has a capacitive load as well as inverting input capacitance, using a series output resistor as described in *Driving Capacitive Loads* will help.

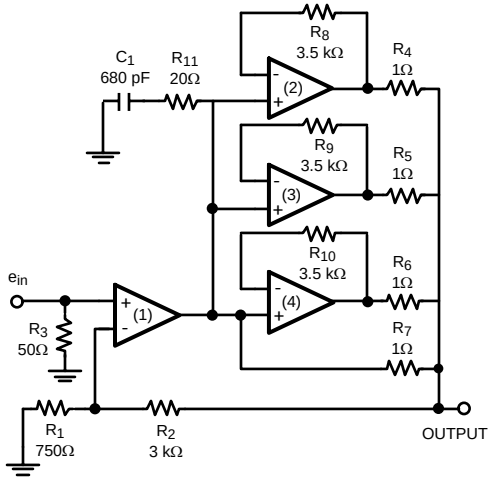


Figure 37. High Output Current Composite Amplifier

When higher currents are required than a single amplifier can provide, the circuit of Figure 37 can be used. Careful attention to a few key components will optimize performance from this circuit. The first thing to note is that the buffers need slightly higher value feedback resistors than if the amplifiers were individually configured. As well, R_{11} and C_1 provide mid circuit frequency compensation to further improve stability. The composite amplifier has approximately twice the phase delay of a single circuit. The larger values of R_8, R_9 and R_{10}, as well as the high frequency attenuation provided by C_1 and R_{11}, ensure that the circuit does not oscillate.

Copyright © 2003–2014, Texas Instruments Incorporated

Inverting Input Parasitic Capacitance (continued)

Resistors R_4, R_5, R_6, and R_7 are necessary to ensure even current distribution between the amplifiers. Since they are inside the feedback loop they have no effect on the gain of the circuit. The circuit shown in Figure 37 has a gain of 5. The frequency response of this circuit is shown in Figure 38.

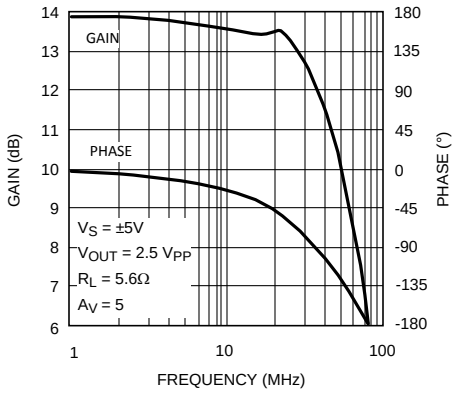


Figure 38. Composite Amplifier Frequency Response

7.8 Layout Considerations

Whenever questions about layout arise, use the evaluation board as a guide. Evaluation boards are shipped with sample requests.

To reduce parasitic capacitances ground and power planes should be removed near the input and output pins. Components in the feedback loop should be placed as close to the device as possible. For long signal paths controlled impedance lines should be used, along with impedance matching at both ends.

Bypass capacitors should be placed as close to the device as possible. Bypass capacitors from each rail to ground are applied in pairs. The larger electrolytic bypass capacitors can be located anywhere on the board; however, the smaller ceramic capacitors should be placed as close to the device as possible.

7.9 Video Performance

The LMH6723/LMH6724 has been designed to provide good performance with both PAL and NTSC composite video signals. The LMH6723/LMH6724 is specified for PAL signals. Typically, NTSC performance is marginally better due to the lower frequency content of the signal. Performance degrades as the loading is increased; therefore, best performance will be obtained with back terminated loads. The back termination reduces reflections from the transmission line and effectively masks transmission line and other parasitic capacitances from the amplifier output stage. Figure 34 shows a typical configuration for driving a 75Ω cable. The amplifier is configured for a gain of 2 to make up for the 6dB of loss in R_{OUT}.

7.10 Single 5-V Supply Video

With a 5V supply the LMH6723/LMH6724 is able to handle a composite NTSC video signal, provided that the signal is AC coupled and level shifted so that the signal is centered around $V_{CC}/2$.

7.10.1 Application Curves

See Figure 31 through Figure 33 and Figure 38.

Copyright © 2003–2014, Texas Instruments Incorporated

8 Power Supply Recommendations

Follow these steps to determine the maximum power dissipation for the LMH6723/LMH6724:

1. Calculate the quiescent (no-load) power: $P_{AMP} = I_{CC} * (V_S)$

   where $V_S = V^+ - V^-$
2. Calculate the RMS power dissipated in the output stage: P_D (rms) = rms $((V_S-V_{OUT})*I_{OUT})$ where V_{OUT} and I_{OUT} are the voltage and current of the external load and V_s is the supply voltage.
3. Calculate the total RMS power: $P_T = P_{AMP} + P_D$

The maximum power that the LMH6723/LMH6724 package can dissipate at a given temperature can be derived with the following equation:

$$P_{MAX} = (150^o - T_{AMB})/ R_{\theta JA} \quad (1)$$

where

- T_{AMB} = Ambient temperature (°C)
- $R_{\theta JA}$ = Thermal resistance, from junction to ambient, for a given package (°C/W)

For the SOIC-8 package $R_{\theta JA}$ is 166°C/W and for the SOT-23-5 it is 230°C/W.

8.1 ESD Protection

The LMH6723/LMH6724 is protected against electrostatic discharge (ESD) on all pins. The LMH6723 will survive 2000V Human Body Model or 200V Machine Model events.

Under closed loop operation the ESD diodes have no effect on circuit performance. There are occasions, however, when the ESD diodes will be evident. If the LMH6723/LMH6724 is driven into a slewing condition the ESD diodes will clamp large differential voltages until the feedback loop restores closed loop operation. Also, if the device is powered down and a large input signal is applied, the ESD diodes will conduct.

Copyright © 2003–2014, Texas Instruments Incorporated

9 Device and Documentation Support

9.1 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 1. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
LMH6723	Click here	Click here	Click here	Click here	Click here
LMH6724	Click here	Click here	Click here	Click here	Click here

9.2 Trademarks

All trademarks are the property of their respective owners.

9.3 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

9.4 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

Copyright © 2003–2014, Texas Instruments Incorporated

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LMH6723 MWC	ACTIVE	WAFERSALE	YS	0	1	TBD	Call TI	Call TI	-40 to 85		Samples
LMH6723MA	LIFEBUY	SOIC	D	8	95	Non-RoHS & Green	Call TI	Level-1-235C-UNLIM	-40 to 85	LMH67 23MA	
LMH6723MA/NOPB	ACTIVE	SOIC	D	8	95	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 85	LMH67 23MA	Samples
LMH6723MAX/NOPB	ACTIVE	SOIC	D	8	2500	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 85	LMH67 23MA	Samples
LMH6723MF/NOPB	ACTIVE	SOT-23	DBV	5	1000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 85	AB1A	Samples
LMH6723MFX	LIFEBUY	SOT-23	DBV	5	3000	Non-RoHS & Green	Call TI	Level-1-260C-UNLIM	-40 to 85	AB1A	
LMH6723MFX/NOPB	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 85	AB1A	Samples
LMH6724MA/NOPB	ACTIVE	SOIC	D	8	95	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 85	LMH67 24MA	Samples
LMH6724MAX/NOPB	ACTIVE	SOIC	D	8	2500	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 85	LMH67 24MA	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

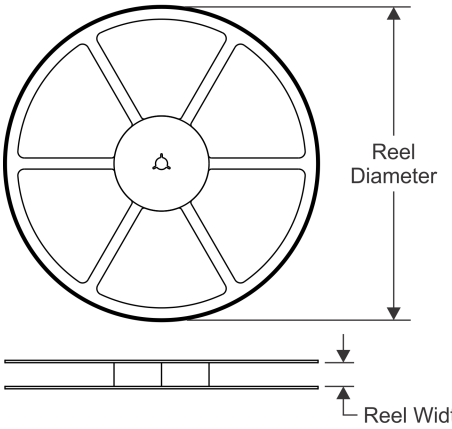
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

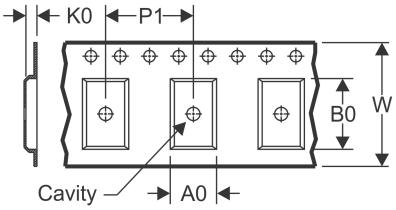
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

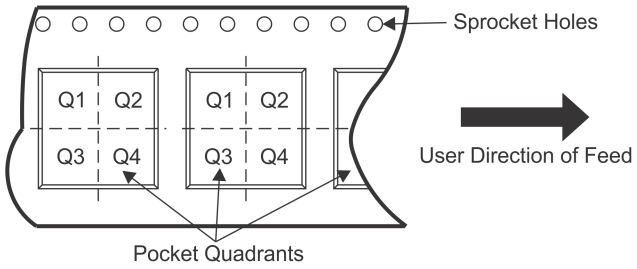


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

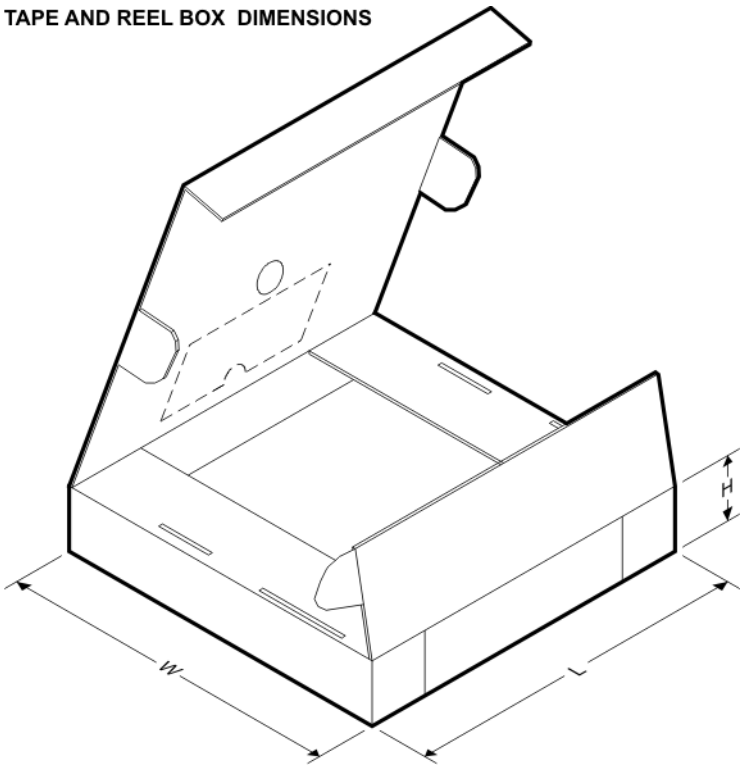
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LMH6723MAX/NOPB	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1
LMH6723MF/NOPB	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LMH6723MFX	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LMH6723MFX/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LMH6724MAX/NOPB	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1

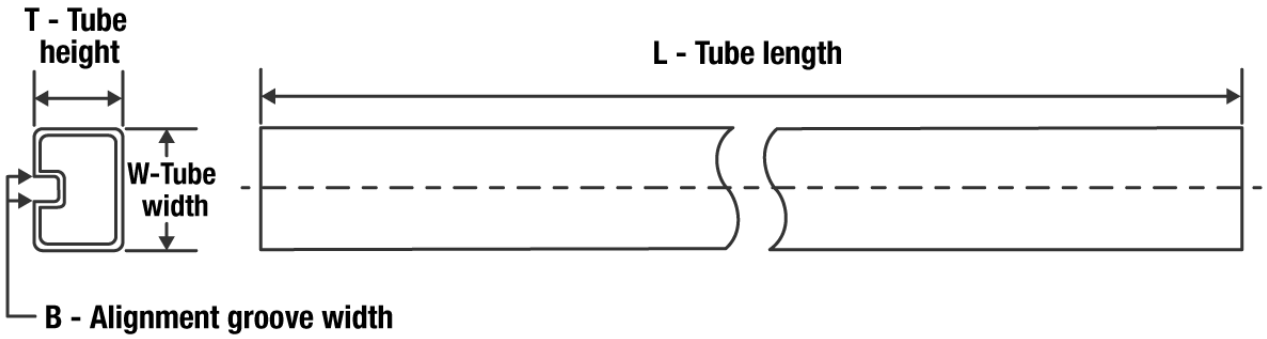
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LMH6723MAX/NOPB	SOIC	D	8	2500	356.0	356.0	35.0
LMH6723MF/NOPB	SOT-23	DBV	5	1000	208.0	191.0	35.0
LMH6723MFX	SOT-23	DBV	5	3000	208.0	191.0	35.0
LMH6723MFX/NOPB	SOT-23	DBV	5	3000	208.0	191.0	35.0
LMH6724MAX/NOPB	SOIC	D	8	2500	356.0	356.0	35.0

TUBE



*All dimensions are nominal

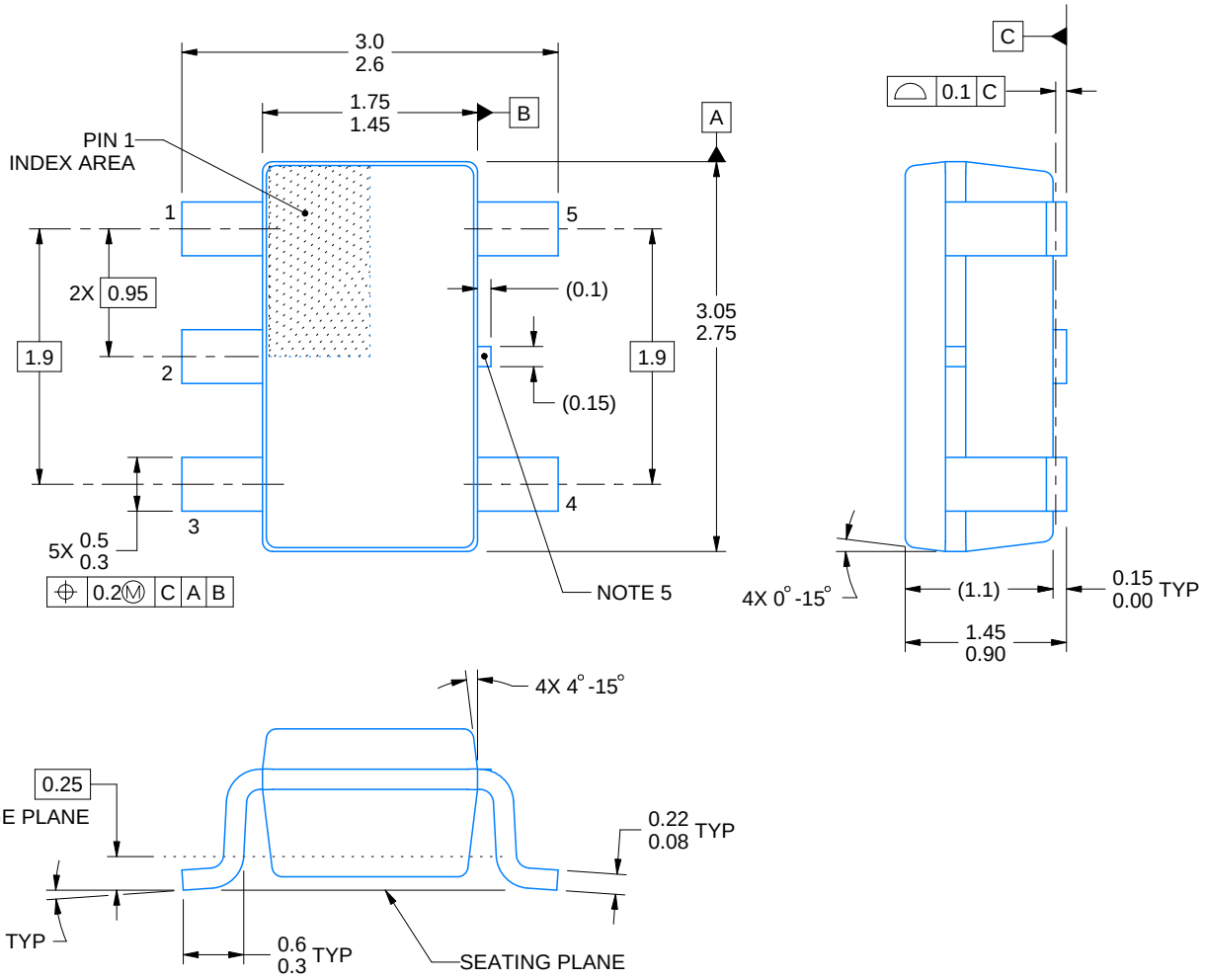
Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
LMH6723MA	D	SOIC	8	95	495	8	4064	3.05
LMH6723MA	D	SOIC	8	95	495	8	4064	3.05
LMH6723MA/NOPB	D	SOIC	8	95	495	8	4064	3.05
LMH6724MA/NOPB	D	SOIC	8	95	495	8	4064	3.05

PACKAGE OUTLINE

DBV0005A

SOT-23 - 1.45 mm max height

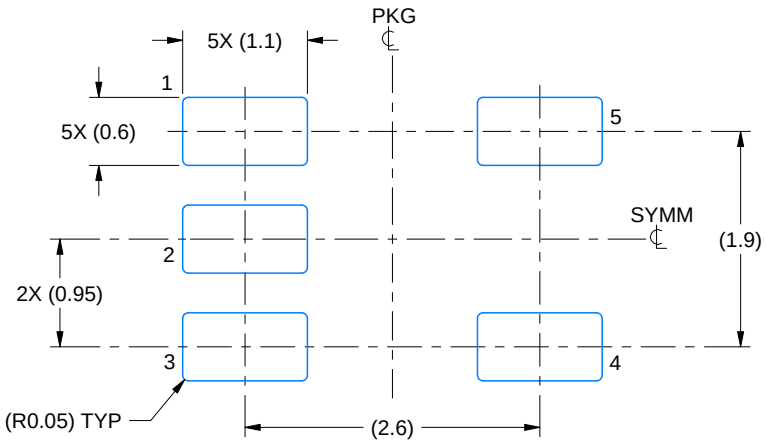
SMALL OUTLINE TRANSISTOR



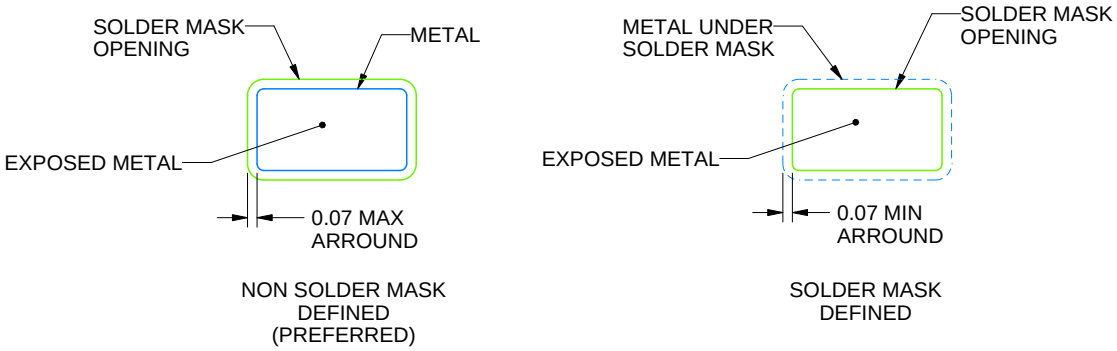
4214839/K 08/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.
5. Support pin may differ or may not be present.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

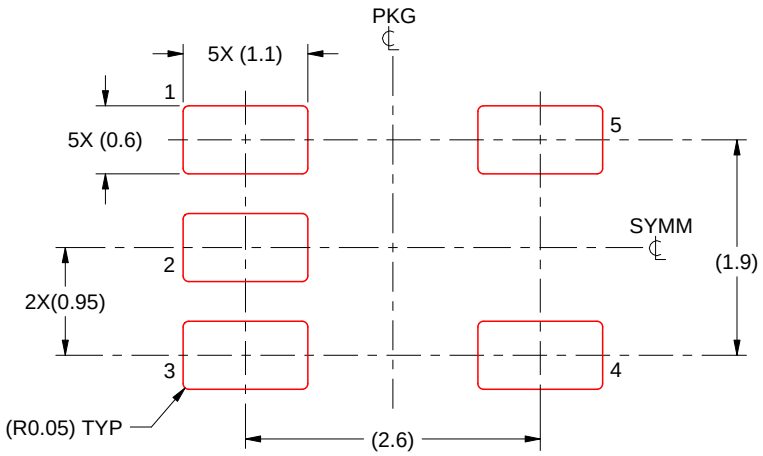


SOLDER MASK DETAILS

4214839/K 08/2024

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

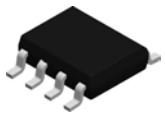


SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/K 08/2024

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

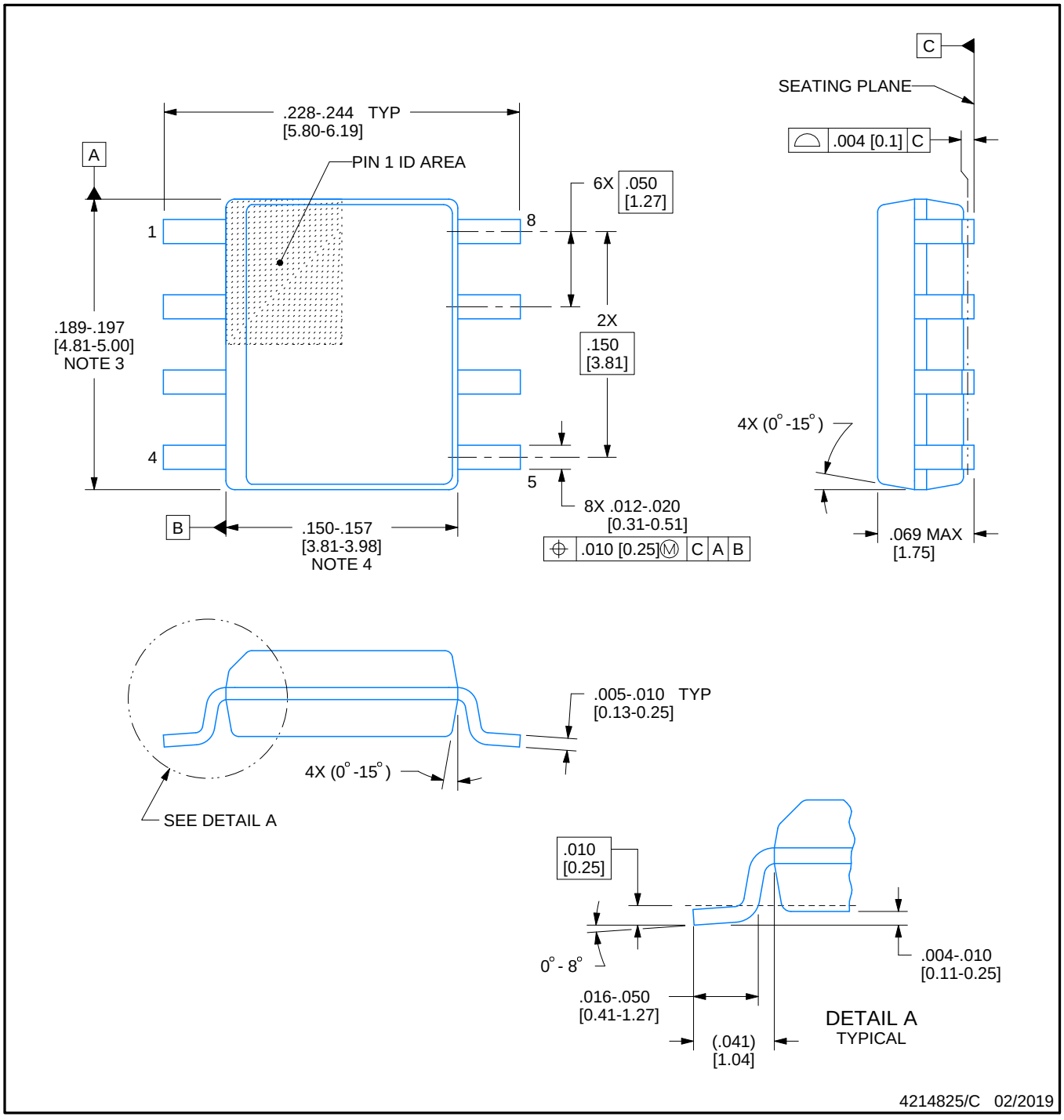


PACKAGE OUTLINE

D0008A

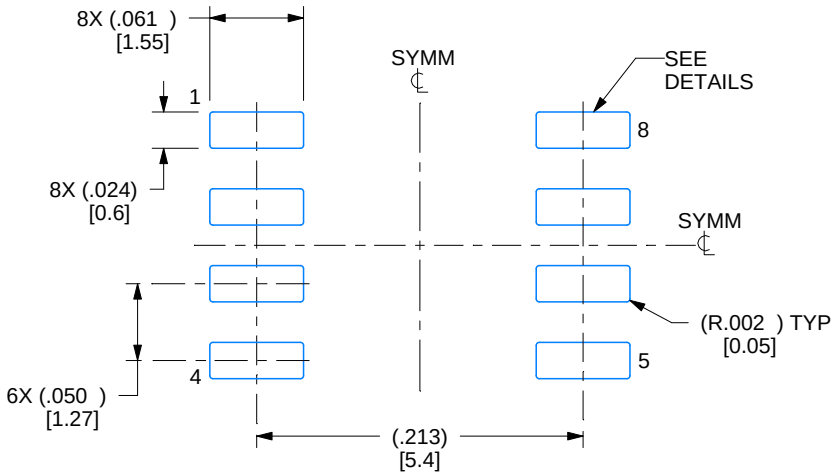
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

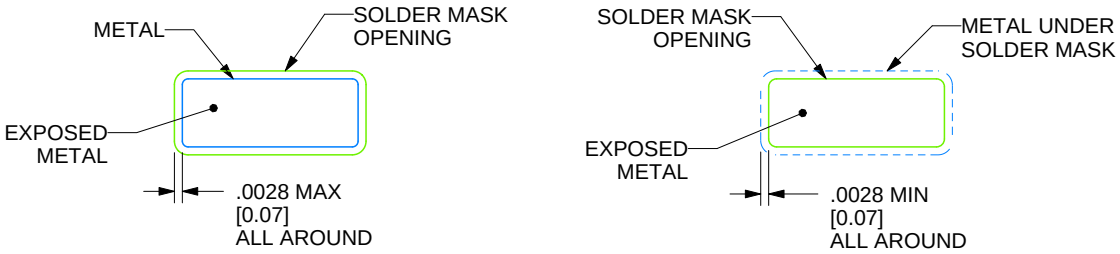


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

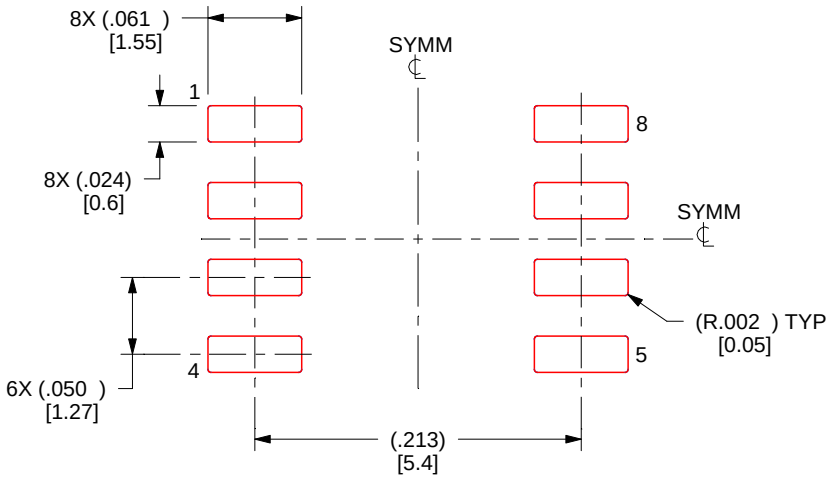
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2024, Texas Instruments Incorporated