MAX3243 3V to 5.5V Multichannel RS-232 Line Driver and Receiver With ±15kV ESD (HBM) Protection

1 Features

- Operates with 3V to 5.5V V_{CC} supply
- Single-chip and single-supply interface for IBM™ PC/AT™ serial port
- RS-232 Bus-pin ESD protection of ±15kV Using Human-Body Model (HBM)
- Meets or exceeds the requirements of TIA/EIA-232-F and ITU V.28 standards
- Three drivers and five receivers
- Operates up to 250kbit/s
- Low active current: 300µA typical
- Low standby current: 1µA typical
- External capacitors: 4 × 0.1µF
- Accepts 5V logic input with 3.3V supply
- Always-active noninverting receiver output (ROUT2B)
- Operating temperature
  - MAX3243C: 0°C to 70°C
  - MAX3243I: –40°C to 85°C
- Serial-mouse driveability
- Auto-powerdown feature to disable driver outputs when no valid RS-232 signal is sensed

2 Applications

- Battery-powered systems
- Tablets
- Notebooks
- Laptops
- Hand-held equipment

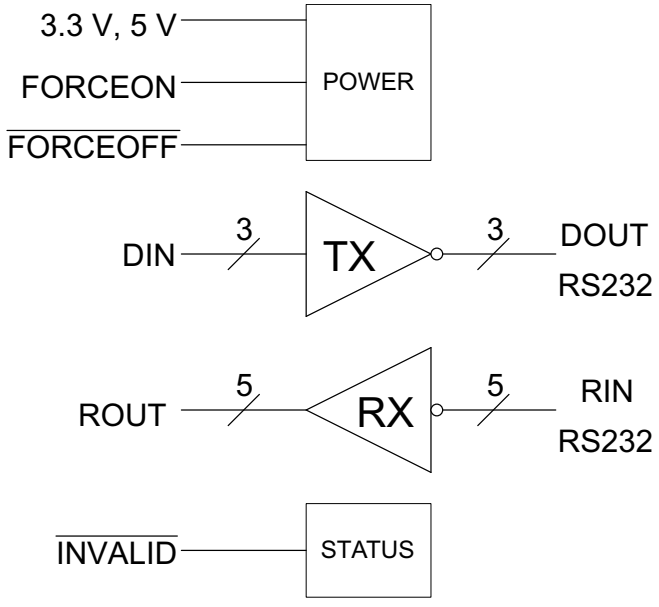
3 Description

The MAX3243 device consists of three line drivers, five line receivers which is ideal for DE-9 DTE interface. ±15kV ESD (HBM) protection pin to pin (serial- port connection pins, including GND). Flexible power features saves power automatically. Special outputs ROUT2B and INVALID are always enabled to allow checking for ring indicator and valid RS232 input.

Package Information

PART NUMBER	PACKAGE(1)	PACKAGE SIZE(2)
MAX3243	SSOP (28)	10.2mm × 7.8mm
	SOIC (28)	17.9mm × 10.3mm
	TSSOP (28)	9.7mm × 6.4mm

(1) For more information, see Section 11.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.



Simplified Diagram

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4 Pin Configuration and Functions

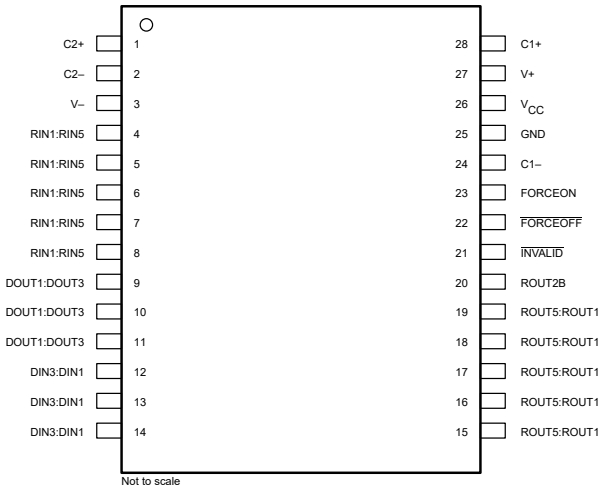


Figure 4-1. DB, DW, or PW Package (Top View)

Table 4-1. Pin Functions

PIN		TYPE	DESCRIPTION
NAME	NO.		
C2+	1	—	Positive lead of C2 capacitor
C2–	2	—	Negative lead of C2 capacitor
V–	3	O	Negative charge pump output for storage capacitor only
RIN1:RIN5	4, 5, 6, 7, 8	I	RS232 line data input (from remote RS232 system)
DOUT1:DOUT3	9, 10, 11	O	RS232 line data output (to remote RS232 system)
DIN3:DIN1	12, 13, 14	I	Logic data input (from UART)
ROUT5:ROUT1	15, 16, 17, 18, 19	O	Logic data output (to UART)
ROUT2B	20	O	Always Active non-inverting output for RIN2 (normally used for ring indicator)
$\overline{\text{INVALID}}$	21	O	Active low output when all RIN are unpowered
$\overline{\text{FORCEOFF}}$	22	I	Low input forces DOUT1-5, ROUT1-5 high Z per *Section 7.4*
FORCEON	23	I	High forces drivers on. Low is automatic mode per *Section 7.4*
C1–	24	—	Negative lead on C1 capacitor
GND	25	—	Ground
V_{CC}	26	—	Supply Voltage, Connect to 3V to 5.5V power supply
V+	27	O	Positive charge pump output for storage capacitor only
C1+	28	—	Positive lead of C1 capacitor

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)

			MIN	MAX	UNIT
V_{CC}	Supply voltage range(2)		–0.3	6	V
V+	Positive output supply voltage range(2)		–0.3	7	V
V–	Negative output supply voltage range(2)		0.3	–7	V
V+ – V–	Supply voltage difference(2)			13	V
V_I	Input voltage range	Driver, $\overline{\text{FORCEOFF}}$, FORCEON	–0.3	6	V
		Receiver	–25	25	
V_O	Output voltage range	Driver	–13.2	13.2	V
		Receiver, $\overline{\text{INVALID}}$	–0.3	V_{CC} + 0.3	
T_J	Operating virtual junction temperature			150	°C
T_{stg}	Storage temperature range		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Section 5.3* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages are with respect to network GND.

5.2 ESD Ratings

			MAX	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 RIN , DOUT, and GND pins (1)	15000	V
		Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 All other pins(1)	3000	
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2)	1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

(1) (See Figure 8-1)

				MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		V_{CC} = 3.3 V	3	3.3	3.6	V
			V_{CC} = 5 V	4.5	5	5.5	
V_{IH}	Driver and control high-level input voltage	DIN, $\overline{\text{FORCEOFF}}$, FORCEON	V_{CC} = 3.3 V	2		5.5	V
			V_{CC} = 5 V	2.4		5.5	
V_{IL}	Driver and control low-level input voltage	DIN, $\overline{\text{FORCEOFF}}$, FORCEON		0		0.8	V
V_I	Driver and control input voltage	DIN, $\overline{\text{FORCEOFF}}$, FORCEON		0		5.5	V
V_I	Receiver input voltage			–25		25	V
T_A	Operating free-air temperature		MAX3243C	0		70	°C
			MAX3243I	–40		85	

(1) Test conditions are C1–C4 = 0.1 µF at V_{CC} = 3.3 V ± 0.3 V; C1 = 0.047 µF, C2–C4 = 0.33 µF at V_{CC} = 5 V ± 0.5 V.

5.4 Thermal Information

THERMAL METRIC[1]		DB	DW	PW	UNIT
		28 PINS	28 PINS	28 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	76.1	59.0	70.3	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	35.8	28.8	21.0	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	37.4	30.3	29.2	°C/W
ψ_{JT}	Junction-to-top characterization parameter	7.4	7.8	1.3	°C/W
ψ_{JB}	Junction-to-board characterization parameter	37.0	30.0	28.8	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report (SPRA953).

5.5 Electrical Characteristics — Auto Power Down

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)[1] (see Figure 8-1)

PARAMETER		TEST CONDITIONS	MIN	TYP[1]	MAX	UNIT
I_{CC}	Supply current Auto-powerdown disabled	No load, $\overline{FORCEOFF}$ and FORCEON at V_{CC}. T_A = 25°C For DB and PW package		0.3	1.2	mA
	Supply current Auto-powerdown disabled	No load, $\overline{FORCEOFF}$ and FORCEON at V_{CC}. T_A = 25°C For DW package		0.3	1	mA
	Supply current Powered off	No load, $\overline{FORCEOFF}$ at GND. T_A = 25°C		1	10	µA
	Supply current Auto-powerdown enabled	No load, $\overline{FORCEOFF}$ at V_{CC}, FORCEON at GND, All RIN are open or grounded, All DIN are grounded. T_A = 25°C		1	10	µA
I_I	Input leakage current of $\overline{FORCEOFF}$, FORCEON	V_I = V_{CC} or V_I at GND		±0.01	±1	µA
V_{IT+}	Receiver input threshold for $\overline{INVALID}$ high-level output voltage	FORCEON = GND, $\overline{FORCEOFF}$ = V_{CC}			2.7	V
V_{IT-}	Receiver input threshold for $\overline{INVALID}$ high-level output voltage	FORCEON = GND, $\overline{FORCEOFF}$ = V_{CC}	–2.7			V
V_T	Receiver input threshold for $\overline{INVALID}$ low-level output voltage	FORCEON = GND, $\overline{FORCEOFF}$ = V_{CC}	–0.3		0.3	V
V_{OH}	$\overline{INVALID}$ high-level output voltage	I_{OH} = -1 mA, FORCEON = GND, $\overline{FORCEOFF}$ = V_{CC}	V_{CC} – 0.6			V
V_{OL}	$\overline{INVALID}$ low-level output voltage	I_{OL} = 1.6 mA, FORCEON = GND, $\overline{FORCEOFF}$ = V_{CC}			0.4	V

(1) Test conditions are C1–C4 = 0.1 µF at V_{CC} = 3.3 V ± 0.3 V; C1 = 0.047 µF, C2–C4 = 0.33 µF at V_{CC} = 5 V ± 0.5 V.

5.6 Electrical Characteristics — Driver

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)(1) (see Figure 8-1)

PARAMETER		TEST CONDITIONS			MIN	TYP(2)	MAX	UNIT
V_{OH}	High-level output voltage	All DOUT at R_L = 3 kΩ to GND			5	5.4		V
V_{OL}	Low-level output voltage	All DOUT at R_L = 3 kΩ to GND			–5	–5.4		V
V_O	Output voltage (mouse driveability)	DIN1 = DIN2 = GND, DIN3 = V_{CC}, 3-kΩ to GND at DOUT3, DOUT1 = DOUT2 = 2.5 mA			±5			V
I_{IH}	High-level input current	$V_I = V_{CC}$				±0.01	±1	µA
I_{IL}	Low-level input current	V_I at GND				±0.01	±1	µA
V_{hys}	Input hysteresis						±1	V
I_{OS}	Short-circuit output current(3)	V_{CC} = 3.6 V,	V_O = 0 V			±35	±60	mA
		V_{CC} = 5.5 V,	V_O = 0 V					
r_o	Output resistance	V_{CC}, V+, and V– = 0 V,	V_O = ±2 V		300	10M		Ω
I_{off}	Output leakage current	$\overline{FORCEOFF}$ = GND,	V_O = ±12 V,	V_{CC} = 3 to 3.6 V			±25	µA
			V_O = ±10 V,	V_{CC} = 4.5 to 5.5 V			±25	

(1) Test conditions are C1–C4 = 0.1 µF at V_{CC} = 3.3 V ± 0.3 V; C1 = 0.047 µF, C2–C4 = 0.33 µF at V_{CC} = 5 V ± 0.5 V.
(2) All typical values are at V_{CC} = 3.3 V or V_{CC} = 5 V, and T_A = 25°C.
(3) Short-circuit durations should be controlled to prevent exceeding the device absolute power dissipation ratings, and not more than one output should be shorted at a time.

5.7 Electrical Characteristics — Receiver

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)(1) (see Figure 8-1)

PARAMETER		TEST CONDITIONS	MIN	TYP(2)	MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = –1 mA	V_{CC} – 0.6	V_{CC} – 0.1		V
V_{OL}	Low-level output voltage	I_{OH} = 1.6 mA			0.4	V
V_{IT+}	Positive-going input threshold voltage	V_{CC} = 3.3 V		1.6	2.4	V
		V_{CC} = 5 V		1.9	2.4	
$V_{IT–}$	Negative-going input threshold voltage	V_{CC} = 3.3 V	0.6	1.1		V
		V_{CC} = 5 V	0.8	1.4		
V_{hys}	Input hysteresis ($V_{IT+} – V_{IT–}$)			0.5		V
I_{off}	Output leakage current (except ROUT2B)	$\overline{FORCEOFF}$ = 0 V		±0.05	±10	µA
r_I	Input resistance	V_I = ±3 V or ±25 V	3	5	7	kΩ

(1) Test conditions are C1–C4 = 0.1 µF at V_{CC} = 3.3 V ± 0.3 V; C1 = 0.047 µF, C2–C4 = 0.33 µF at V_{CC} = 5 V ± 0.5 V.
(2) All typical values are at V_{CC} = 3.3 V or V_{CC} = 5 V, and T_A = 25°C.

5.8 Switching Characteristics — Auto Power Down

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 6-5)

PARAMETER		TEST CONDITIONS	TYP(1)	UNIT
t_{valid}	Propagation delay time, low- to high-level output	V_{CC} = 5 V	1	µs
$t_{invalid}$	Propagation delay time, high- to low-level output	V_{CC} = 5 V	30	µs
t_{en}	Supply enable time	V_{CC} = 5 V	100	µs

(1) All typical values are at V_{CC} = 3.3 V or V_{CC} = 5 V, and T_A = 25°C.

5.9 Switching Characteristics — Driver

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)(2) (see Figure 8-1)
MAX3243C, MAX3243I

PARAMETER		TEST CONDITIONS		MIN	TYP(1)	MAX	UNIT
	Maximum data rate	R_L = 3 kΩ One DOUT switching,	C_L = 1000 pF See Figure 6-1	150	250		kbit/s
$t_{sk(p)}$	Pulse skew(3)	R_L = 3 kΩ to 7 kΩ	C_L = 150 pF to 2500 pF See Figure 6-3		100		ns
SR(tr)	Slew rate, transition region (see Figure 6-1)	V_{CC} = 3.3 V, R_L = 3 kΩ to 7 kΩ	C_L = 150 pF to 1000 pF	6		30	V/µs
			C_L = 150 pF to 2500 pF	4		30	

(1) All typical values are at V_{CC} = 3.3 V or V_{CC} = 5 V, and T_A = 25°C.
(2) Test conditions are C1–C4 = 0.1 µF at V_{CC} = 3.3 V + 0.3 V; C1 = 0.047 µF, C2–C4 = 0.33 µF at V_{CC} = 5 V ± 0.5 V.
(3) Pulse skew is defined as $|t_{PLH} - t_{PHL}|$ of each channel of the same device.

5.10 Switching Characteristics — Receiver

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)(2)

PARAMETER		TEST CONDITIONS	TYP(1)	UNIT
t_{PLH}	Propagation delay time, low- to high-level output	C_L = 150 pF, See Figure 6-3	150	ns
t_{PHL}	Propagation delay time, high- to low-level output		150	ns
t_{en}	Output enable time	C_L = 150 pF, R_L = 3 kΩ, See Figure 6-4	200	ns
t_{dis}	Output disable time		200	ns
$t_{sk(p)}$	Pulse skew(3)	See Figure 6-3	50	ns

(1) All typical values are at V_{CC} = 3.3 V or V_{CC} = 5 V, and T_A = 25°C.
(2) Test conditions are C1–C4 = 0.1 µF at V_{CC} = 3.3 V ± 0.3 V; C1 = 0.047 µF, C2–C4 = 0.33 µF at V_{CC} = 5 V ± 0.5 V.
(3) Pulse skew is defined as $|t_{PLH} - t_{PHL}|$ of each channel of the same device.

5.11 Typical Characteristics

V_{CC} = 3.3 V

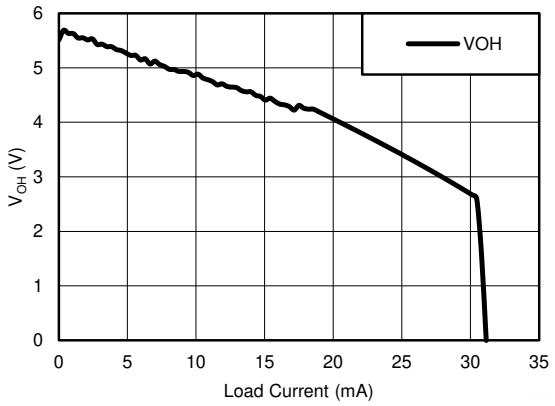


Figure 5-1. DOUT VOH vs Load Current

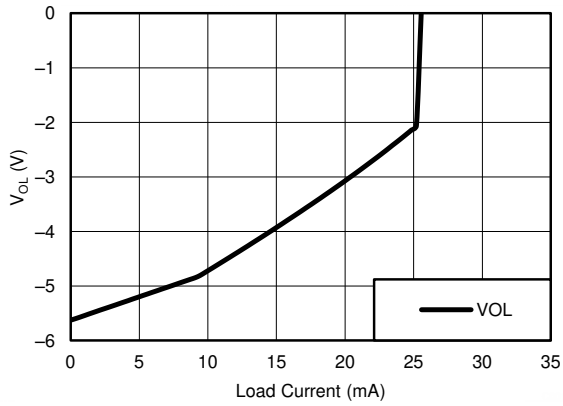
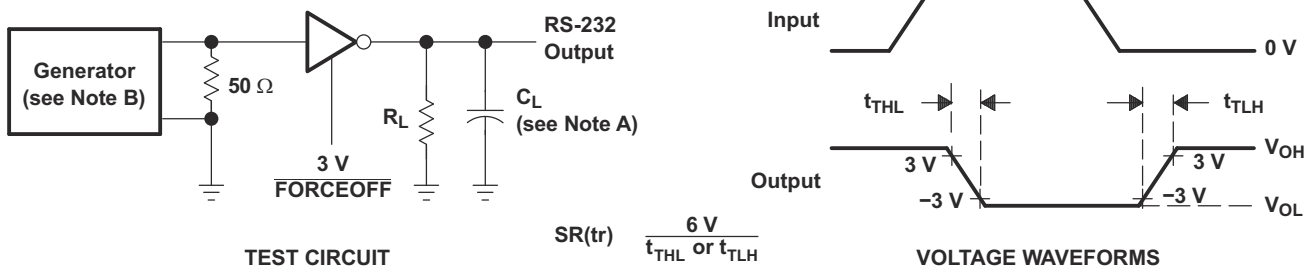


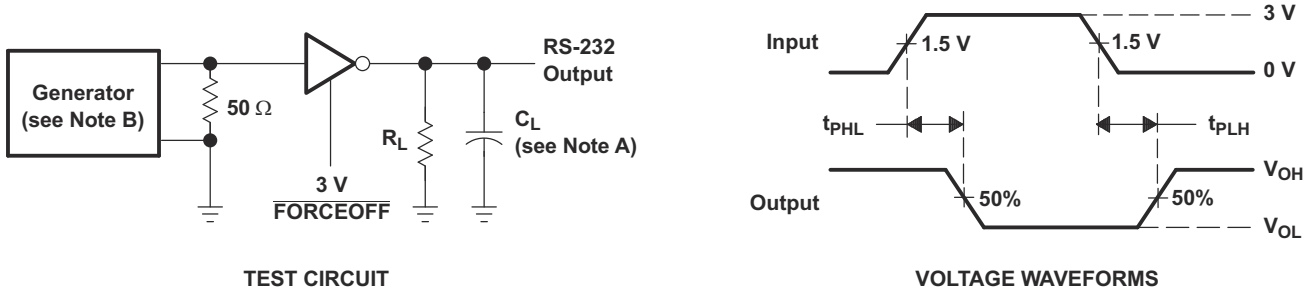
Figure 5-2. DOUT VOL vs Load Current

6 Parameter Measurement Information



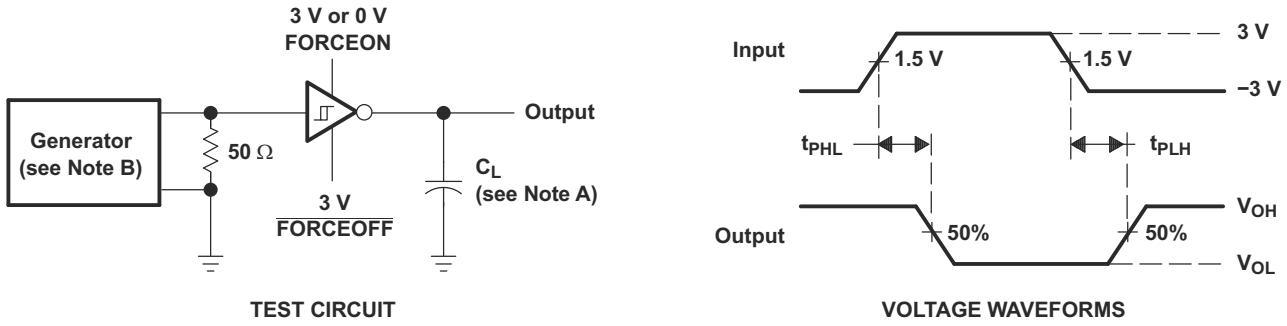
NOTES: A. C_L includes probe and jig capacitance.
B. The pulse generator has the following characteristics: PRR = 250 kbit/s (MAX3243C/I) and 1 Mbit/s (MAX3243FC/I), Z_O = 50 Ω, 50% duty cycle, t_r ≤ 10 ns, t_f ≤ 10 ns.

Figure 6-1. Driver Slew Rate



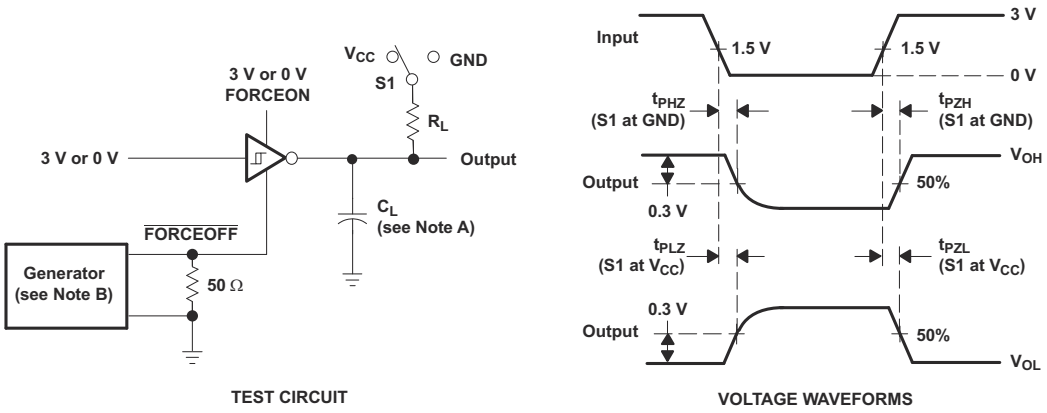
NOTES: A. C_L includes probe and jig capacitance.
B. The pulse generator has the following characteristics: PRR = 250 kbit/s (MAX3243C/I) and 1 Mbit/s (MAX3243FC/I), Z_O = 50 Ω, 50% duty cycle, t_r ≤ 10 ns, t_f ≤ 10 ns.

Figure 6-2. Driver Pulse Skew



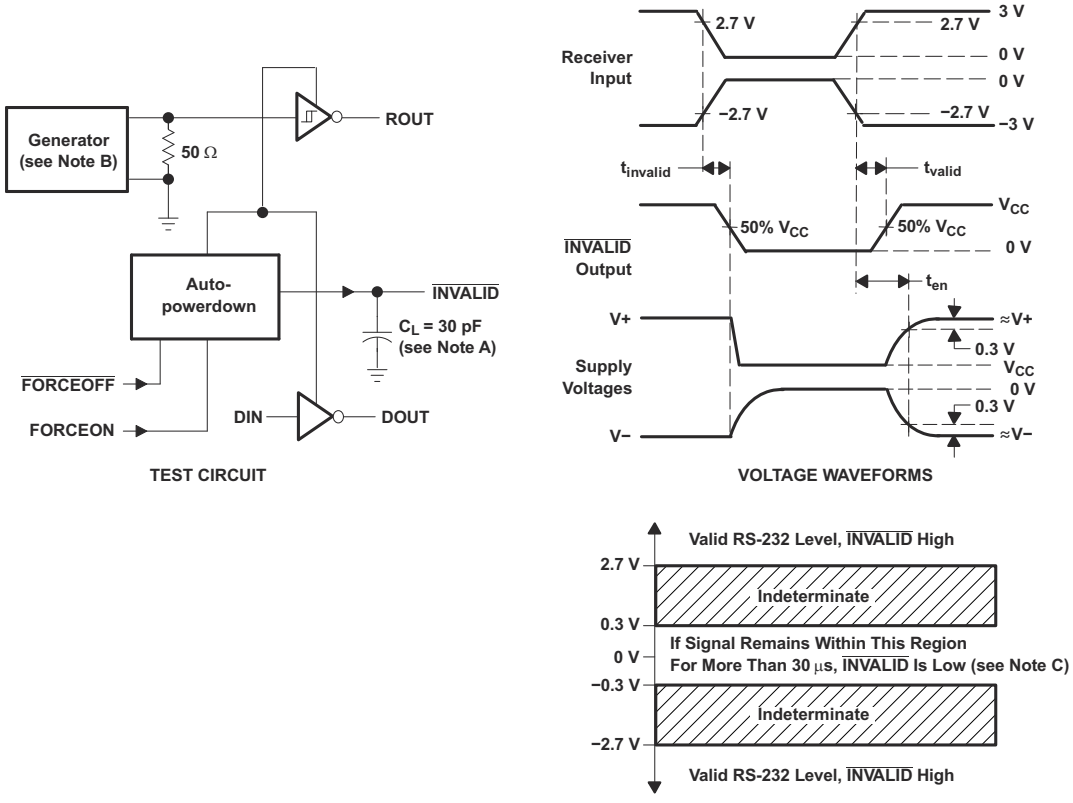
NOTES: A. C_L includes probe and jig capacitance.
B. The pulse generator has the following characteristics: Z_O = 50 Ω, 50% duty cycle, t_r ≤ 10 ns, t_f ≤ 10 ns.

Figure 6-3. Receiver Propagation Delay Times



NOTES: A. C_L includes probe and jig capacitance.
B. The pulse generator has the following characteristics: Z_O = 50 Ω, 50% duty cycle, $t_r \le 10$ ns, $t_f \le 10$ ns.
C. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
D. t_{PZL} and t_{PZH} are the same as t_{en}.

Figure 6-4. Receiver Enable and Disable Times



NOTES: A. C_L includes probe and jig capacitance.
B. The pulse generator has the following characteristics: PRR = 5 kbit/s, Z_O = 50 Ω, 50% duty cycle, $t_r \le 10$ ns, $t_f \le 10$ ns.
C. Auto-powerdown disables drivers and reduces supply current to 1 μA.

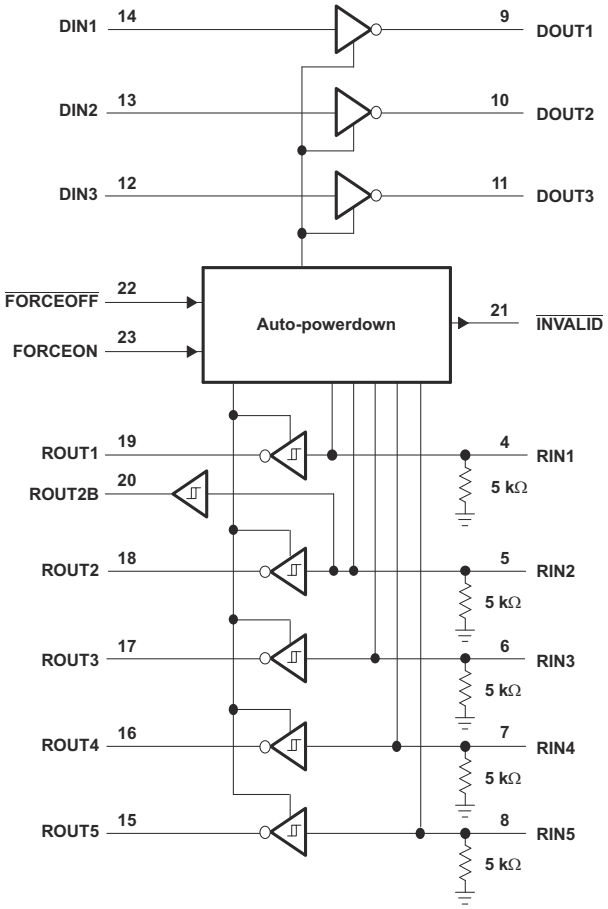
Figure 6-5. $\overline{\text{INVALID}}$ Propagation Delay Times and Supply Enabling Time

7 Detailed Description

7.1 Overview

The MAX3243 device consists of three line drivers, five line receivers, and a dual charge-pump circuit with ±15kV ESD (HBM) protection pin to pin (serial- port connection pins, including GND). The device meets the requirements of TIA/EIA-232-F and provides the electrical interface between an asynchronous communication controller and the serial-port connector. This combination of drivers and receivers matches that needed for the typical serial port used in an IBM PC/AT, or compatible. The charge pump and four small external capacitors allow operation from a single 3V to 5.5V supply. In addition, the device includes an always-active noninverting output (ROUT2B), which allows applications using the ring indicator to transmit data while the device is powered down. Flexible control options for power management are available. when the serial port is inactive. The auto-power-down feature functions when FORCEON is low and FORCEOFF is high. During this mode of operation, if the device does not sense a valid RS-232 signal, the driver outputs are disabled. If FORCEOFF is set low, both drivers and receivers (except ROUT2B) are shut off, and the supply current is reduced to 1µA. Disconnecting the serial port or turning off the peripheral drivers causes the auto-powerdown condition to occur. Auto-powerdown can be disabled when FORCEON and FORCEOFF are high and should be done when driving a serial mouse. With auto-powerdown enabled, the device is activated automatically when a valid signal is applied to any receiver input. The INVALID output is used to notify the user if an RS-232 signal is present at any receiver input. INVALID is high (valid data) if any receiver input voltage is greater than 2.7V or less than –2.7V or has been between –0.3V and 0.3V for less than 30µs. INVALID is low (invalid data) if all receiver input voltages are between –0.3V and 0.3V for more than 30µs.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Auto-Power-Down

Auto-Power-Down can be used to automatically save power when the receivers are unconnected or connected to a powered down remote RS232 port. FORCEON being high will override Auto power down and the drivers will be active. $\overline{\text{FORCEOFF}}$ being low will override FORCEON and will power down all outputs except for ROUT2B and $\overline{\text{INVALID}}$.

7.3.2 Charge Pump

The charge pump increases, inverts, and regulates voltage at V+ and V– pins and requires four external capacitors.

7.3.3 RS232 Driver

Three drivers interface standard logic level to RS232 levels. All DIN inputs must be valid high or low.

7.3.4 RS232 Receiver

Five receivers interface RS232 levels to standard logic levels. An open input will result in a high output on ROUT. Each RIN input includes an internal standard RS232 load.

7.3.5 ROUT2B Receiver

ROUT2B is an always-active noninverting output of RIN2 input, which allows applications using the ring indicator to transmit data while the device is powered down.

7.3.6 Invalid Input Detection

The $\overline{\text{INVALID}}$ output goes active low when all RIN inputs are unpowered. The $\overline{\text{INVALID}}$ output goes inactive high when any RIN input is connected to an active RS232 voltage level.

7.4 Device Functional Modes

Table 7-1. Each Driver (1)

INPUTS				OUTPUT	DRIVER STATUS
DIN	FORCEON	$\overline{\text{FORCEOFF}}$	VALID RIN RS-232 LEVEL	DOUT	
X	X	L	X	Z	Powered off
L	H	H	X	H	Normal operation with auto-powerdown disabled
H	H	H	X	L	
L	L	H	YES	H	Normal operation with auto-powerdown enabled
H	L	H	YES	L	
X	L	H	NO	Z	Power off by auto-powerdown feature

(1) H = high level, L = low level, X = irrelevant, Z = high impedance, YES = any RIN valid, NO = all RIN invalid

Table 7-2. Each Receiver (1)

INPUTS			OUTPUTS	RECEIVER STATUS
RIN	FORCEON	$\overline{\text{FORCEOFF}}$	ROUT	
X	X	L	Z	Powered off
L	X	H	H	Normal operation
H	X	H	L	
Open	X	H	H	

(1) H = high level, L = low level, X = irrelevant, Z = high impedance (off), Open = input disconnected or connected driver off

Table 7-3. $\overline{\text{INVALID}}$ and ROUT2B Outputs (1)

INPUTS				OUTPUTS		OUTPUT STATUS
VALID RIN RS-232 LEVEL	RIN2	FORCEON	$\overline{\text{FORCEOFF}}$	$\overline{\text{INVALID}}$	ROUT2B	
YES	L	X	X	H	L	Always Active
YES	H	X	X	H	H	
YES	OPEN	X	X	H	L	Always Active
NO	OPEN	X	X	L	L	

(1) H = high level, L = low level, X = irrelevant, Z = high impedance (off),
OPEN = input disconnected or connected driver off, YES = any RIN valid, NO = all RIN invalid

8 Application and Implementation

Note

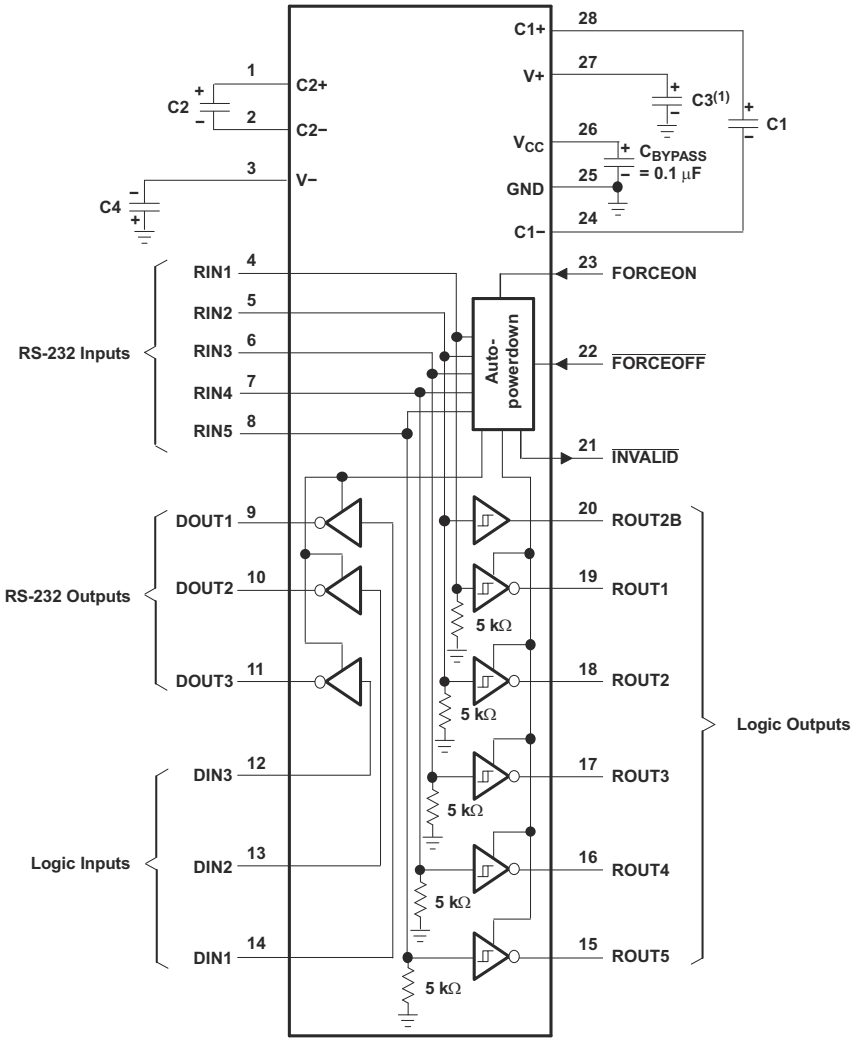
Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

It is recommended to add capacitors as shown in Figure 8-1.

8.2 Typical Application

ROUT and DIN connect to UART or general purpose logic lines. RIN and DOUT lines connect to a RS232 connector or cable.



(1) C3 can be connected to V_{CC} or GND.

NOTES: A. Resistor values shown are nominal.

B. Nonpolarized ceramic capacitors are acceptable. If polarized tantalum or electrolytic capacitors are used, they should be connected as shown.

V_{CC} vs CAPACITOR VALUES

V_{CC}	C1	C2, C3, and C4
3.3 V ± 0.3 V	0.1 µF	0.1 µF
5 V ± 0.5 V	0.047 µF	0.33 µF
3 V to 5.5 V	0.1 µF	0.47 µF

Figure 8-1. Typical Operating Circuit and Capacitor Values

8.2.1 Design Requirements

- V_{CC} minimum is 3 V and maximum is 5.5V.
- Maximum recommended bit rate is 250 kbit/s.

8.2.2 Detailed Design Procedure

- All DIN, $\overline{\text{FORCEOFF}}$ and FORCEON inputs must be connected to valid low or high logic levels.
- Select capacitor values based on V_{CC} level for best performance.

8.2.3 Application Curves

V_{CC}= 3.3 V

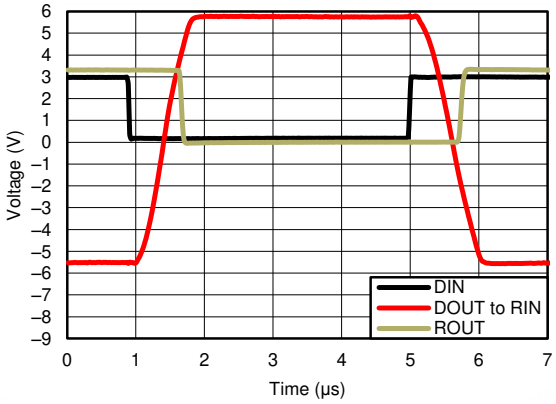


Figure 8-2. Driver to Receiver Loopback Timing Waveform

8.3 Power Supply Recommendations

V_{CC} should be between 3V and 5.5V. Charge pump capacitors should be chosen using table in Figure 8-1.

8.4 Layout

8.4.1 Layout Guidelines

Keep the external capacitor traces short. This is more important on C1 and C2 nodes that have the fastest rise and fall times.

In the *Layout Example* diagram, only critical layout sections are shown. Input and output traces will vary in shape and size depending on the customer application. FORCEON and $\overline{\text{FORCEOFF}}$ should be pulled up to VCC or GND via a pullup resistor, depending on which configuration the user desires upon power-up.

8.4.2 Layout Example

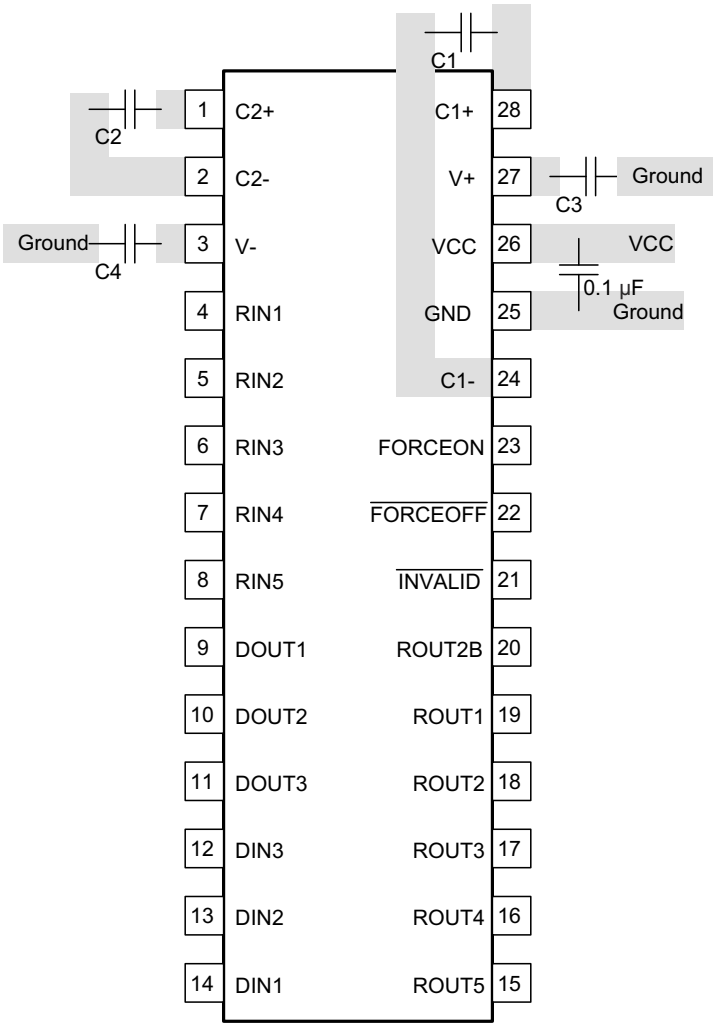


Figure 8-3. Layout Diagram

9 Device and Documentation Support

9.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.2 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

9.3 Trademarks

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TI E2E™ is a trademark of Texas Instruments.
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9.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.5 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

10 Revision History

Changes from Revision P (October 2022) to Revision Q (August 2024)	Page
• Changed the Device Information table to *Package Information* table	1
• Changed 16 PINS to 28 PINS in the *Thermal Information* table	5

Changes from Revision O (January 2015) to Revision P (October 2022)	Page
• Changed the *Thermal Information* table	5
• Changed the MAX value of I_{CC} Supply current auto-powerdown disabled from 1 mA to 1.2 mA in *Electrical Characteristics—Auto Power Down*	5

Changes from Revision N (May 2009) to Revision O (January 2015)	Page
• Added *Applications*, *Device Information* table, *Pin Functions* table, *ESD Ratings* table, *Thermal Information* table, *Typical Characteristics*, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section	1
• Deleted *Ordering Information* table	1

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
MAX3243CDBR	Active	Production	SSOP (DB) | 28	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	MAX3243C
MAX3243CDBR.A	Active	Production	SSOP (DB) | 28	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	MAX3243C
MAX3243CDBR.B	Active	Production	SSOP (DB) | 28	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	MAX3243C
MAX3243CDBRE4	Active	Production	SSOP (DB) | 28	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	MAX3243C
MAX3243CDBRG4	Active	Production	SSOP (DB) | 28	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	MAX3243C
MAX3243CDW	Obsolete	Production	SOIC (DW) | 28	-	-	Call TI	Call TI	0 to 70	MAX3243C
MAX3243CDWR	Active	Production	SOIC (DW) | 28	1000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	MAX3243C
MAX3243CDWR.A	Active	Production	SOIC (DW) | 28	1000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	MAX3243C
MAX3243CDWRG4	Active	Production	SOIC (DW) | 28	1000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	MAX3243C
MAX3243CPWR	Active	Production	TSSOP (PW) | 28	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	MA3243C
MAX3243CPWR.A	Active	Production	TSSOP (PW) | 28	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	MA3243C
MAX3243CPWR.B	Active	Production	TSSOP (PW) | 28	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	MA3243C
MAX3243CPWRG4	Active	Production	TSSOP (PW) | 28	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	MA3243C
MAX3243IDBR	Active	Production	SSOP (DB) | 28	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	MAX3243I
MAX3243IDBR.A	Active	Production	SSOP (DB) | 28	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	MAX3243I
MAX3243IDBR.B	Active	Production	SSOP (DB) | 28	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	MAX3243I
MAX3243IDBRG4	Active	Production	SSOP (DB) | 28	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	MAX3243I
MAX3243IDBRG4.A	Active	Production	SSOP (DB) | 28	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	MAX3243I
MAX3243IDBRG4.B	Active	Production	SSOP (DB) | 28	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	MAX3243I
MAX3243IDW	Active	Production	SOIC (DW) | 28	20 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	MAX3243I
MAX3243IDW.A	Active	Production	SOIC (DW) | 28	20 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	MAX3243I
MAX3243IDWR	Active	Production	SOIC (DW) | 28	1000 | LARGE T&R	Yes	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 85	MAX3243I
MAX3243IDWR.A	Active	Production	SOIC (DW) | 28	1000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	MAX3243I
MAX3243IDWR1G4	Active	Production	SOIC (DW) | 28	1000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	MAX3243I
MAX3243IDWR1G4.A	Active	Production	SOIC (DW) | 28	1000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	MAX3243I
MAX3243IPWR	Active	Production	TSSOP (PW) | 28	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	MB3243I
MAX3243IPWR.A	Active	Production	TSSOP (PW) | 28	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	MB3243I
MAX3243IPWR.B	Active	Production	TSSOP (PW) | 28	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	MB3243I
MAX3243IPWRE4	Active	Production	TSSOP (PW) | 28	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	MB3243I

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

OTHER QUALIFIED VERSIONS OF MAX3243 :

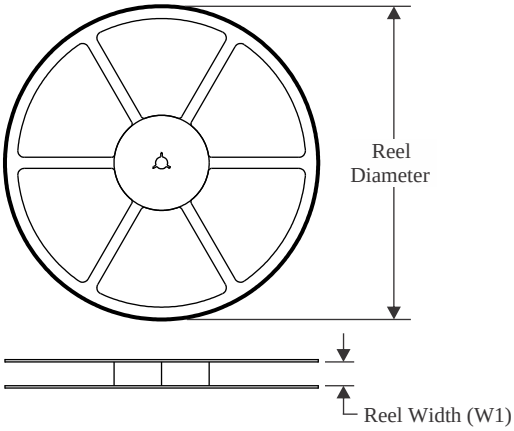
- Enhanced Product : MAX3243-EP

NOTE: Qualified Version Definitions:

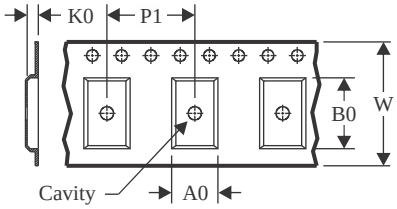
- Enhanced Product - Supports Defense, Aerospace and Medical Applications

TAPE AND REEL INFORMATION

REEL DIMENSIONS

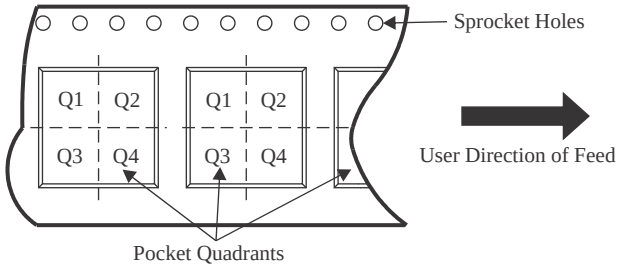


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

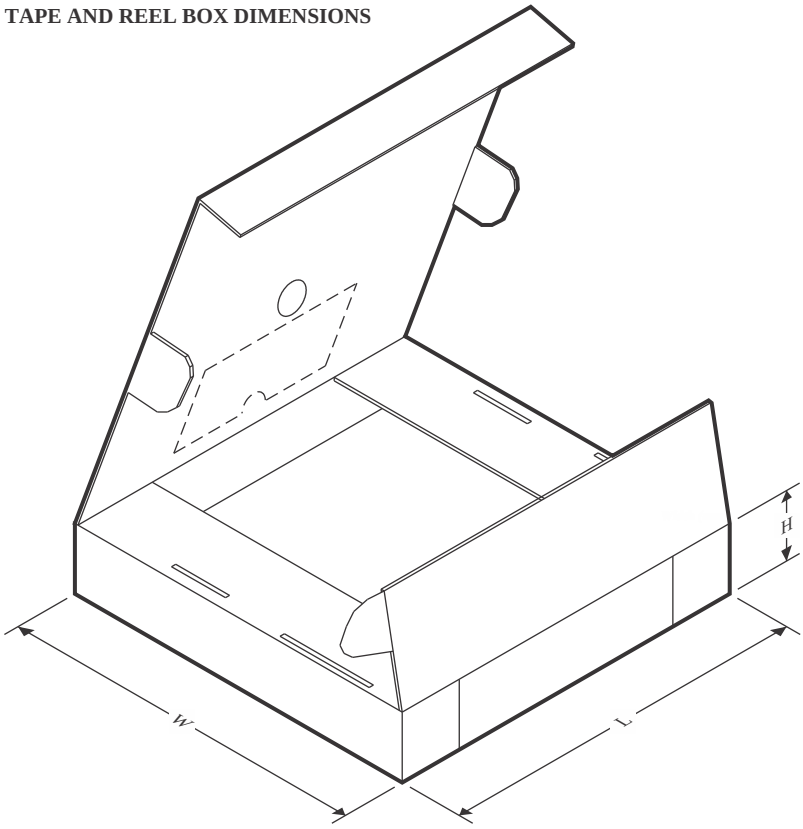
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
MAX3243CDBR	SSOP	DB	28	2000	330.0	16.4	8.45	10.55	2.5	12.0	16.2	Q1
MAX3243CDWR	SOIC	DW	28	1000	330.0	32.4	11.35	18.67	3.1	16.0	32.0	Q1
MAX3243CPWR	TSSOP	PW	28	2000	330.0	16.4	6.75	10.1	1.8	12.0	16.0	Q1
MAX3243IDBR	SSOP	DB	28	2000	330.0	16.4	8.45	10.55	2.5	12.0	16.2	Q1
MAX3243IDBRG4	SSOP	DB	28	2000	330.0	16.4	8.45	10.55	2.5	12.0	16.2	Q1
MAX3243IDWR	SOIC	DW	28	1000	330.0	32.4	11.35	18.67	3.1	16.0	32.0	Q1
MAX3243IDWR1G4	SOIC	DW	28	1000	330.0	32.4	11.35	18.67	3.1	16.0	32.0	Q1
MAX3243IPWR	TSSOP	PW	28	2000	330.0	16.4	6.75	10.1	1.8	12.0	16.0	Q1

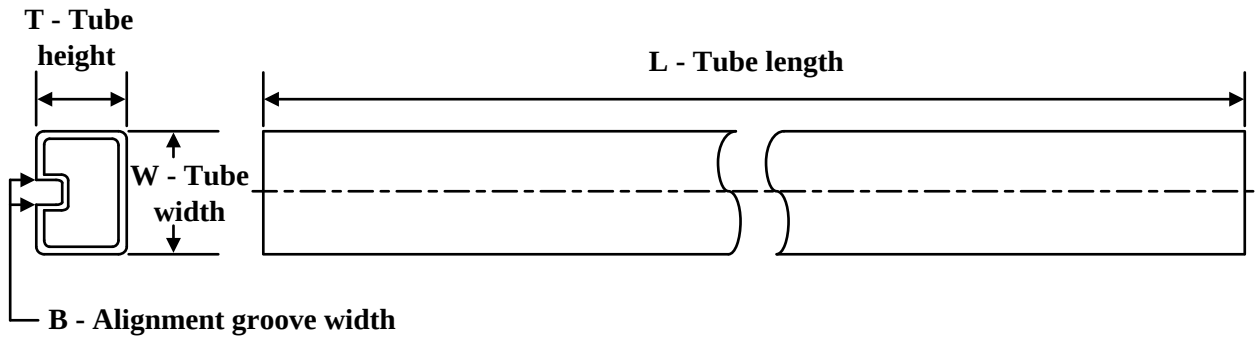
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
MAX3243CDBR	SSOP	DB	28	2000	353.0	353.0	32.0
MAX3243CDWR	SOIC	DW	28	1000	350.0	350.0	66.0
MAX3243CPWR	TSSOP	PW	28	2000	353.0	353.0	32.0
MAX3243IDBR	SSOP	DB	28	2000	353.0	353.0	32.0
MAX3243IDBRG4	SSOP	DB	28	2000	353.0	353.0	32.0
MAX3243IDWR	SOIC	DW	28	1000	350.0	350.0	66.0
MAX3243IDWR1G4	SOIC	DW	28	1000	350.0	350.0	66.0
MAX3243IPWR	TSSOP	PW	28	2000	353.0	353.0	32.0

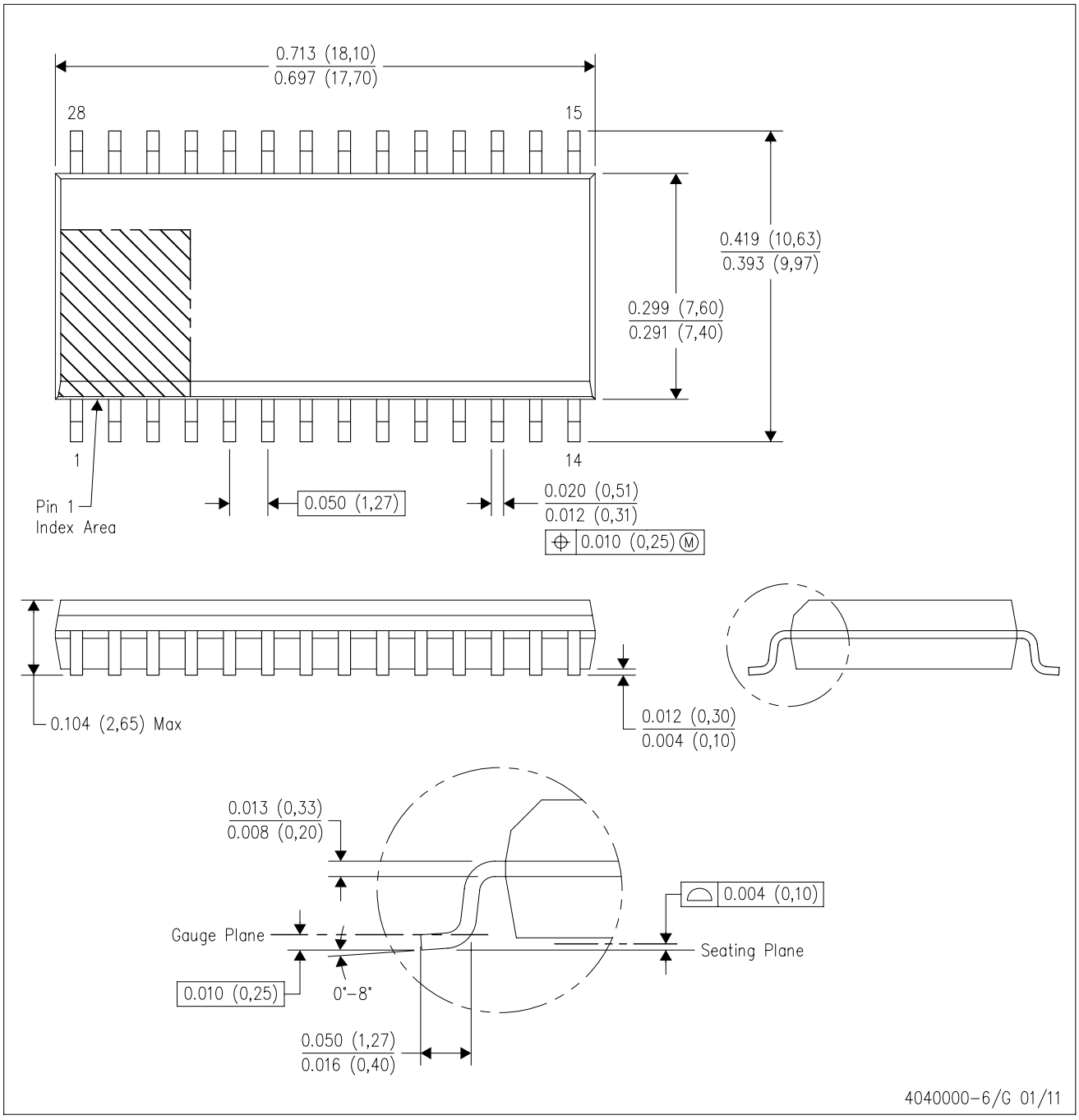
TUBE



*All dimensions are nominal

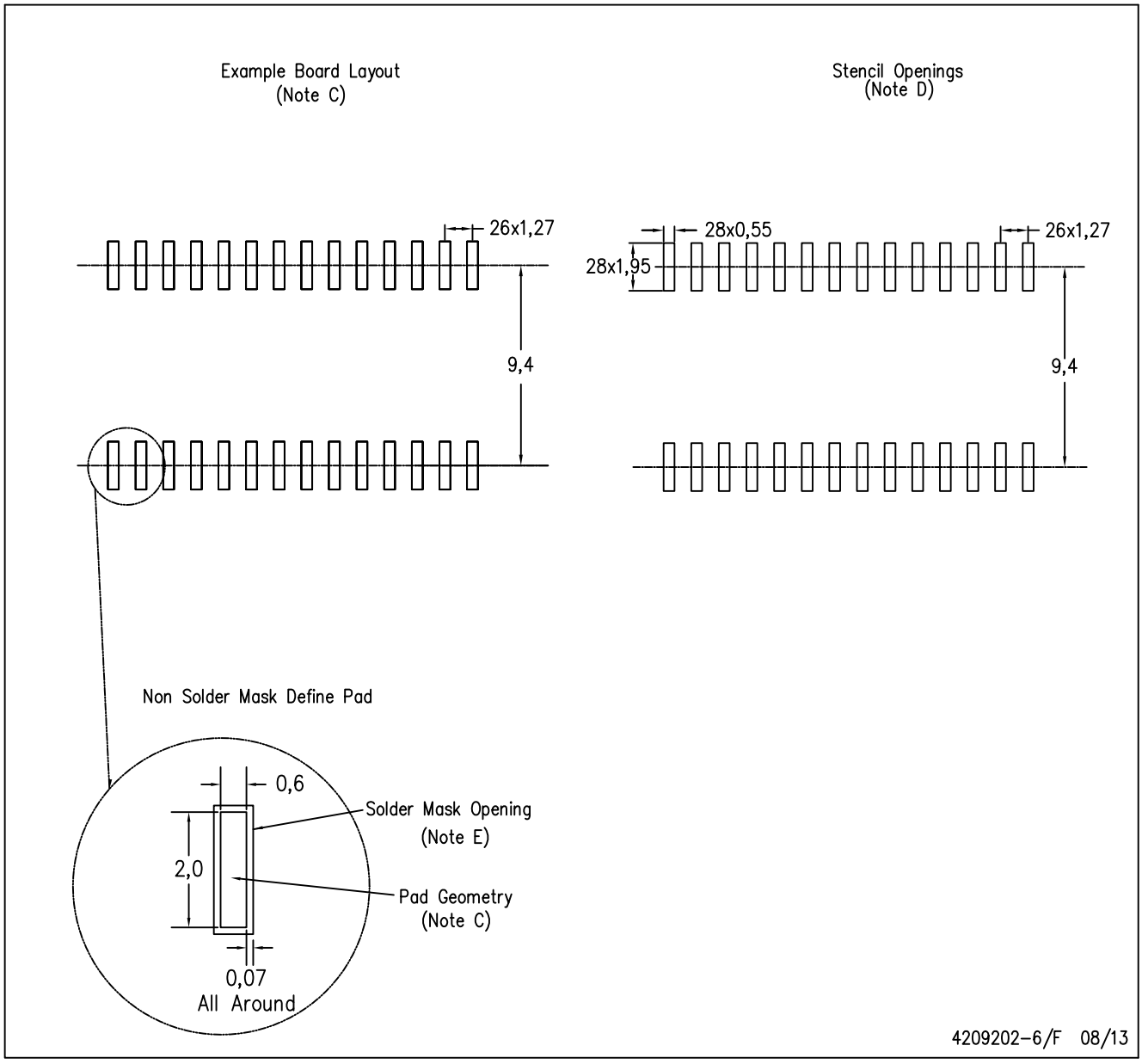
Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
MAX3243IDW	DW	SOIC	28	20	506.98	12.7	4826	6.6
MAX3243IDW.A	DW	SOIC	28	20	506.98	12.7	4826	6.6

DW (R–PDSO–G28) PLASTIC SMALL OUTLINE



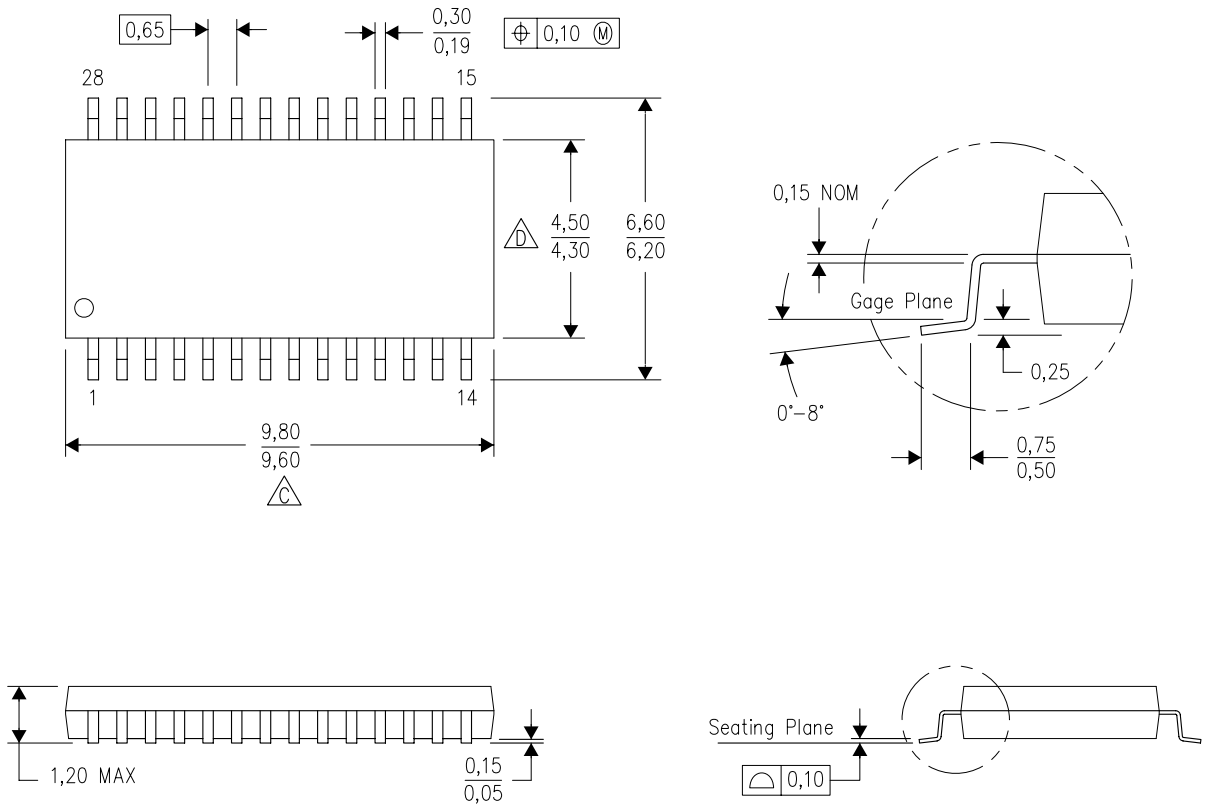
NOTES:
A. All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
D. Falls within JEDEC MS–013 variation AE.

DW (R–PDSO–G28) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Refer to IPC7351 for alternate board design.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

PW (R–PDSO–G28) PLASTIC SMALL OUTLINE



4040064–7/G 02/11

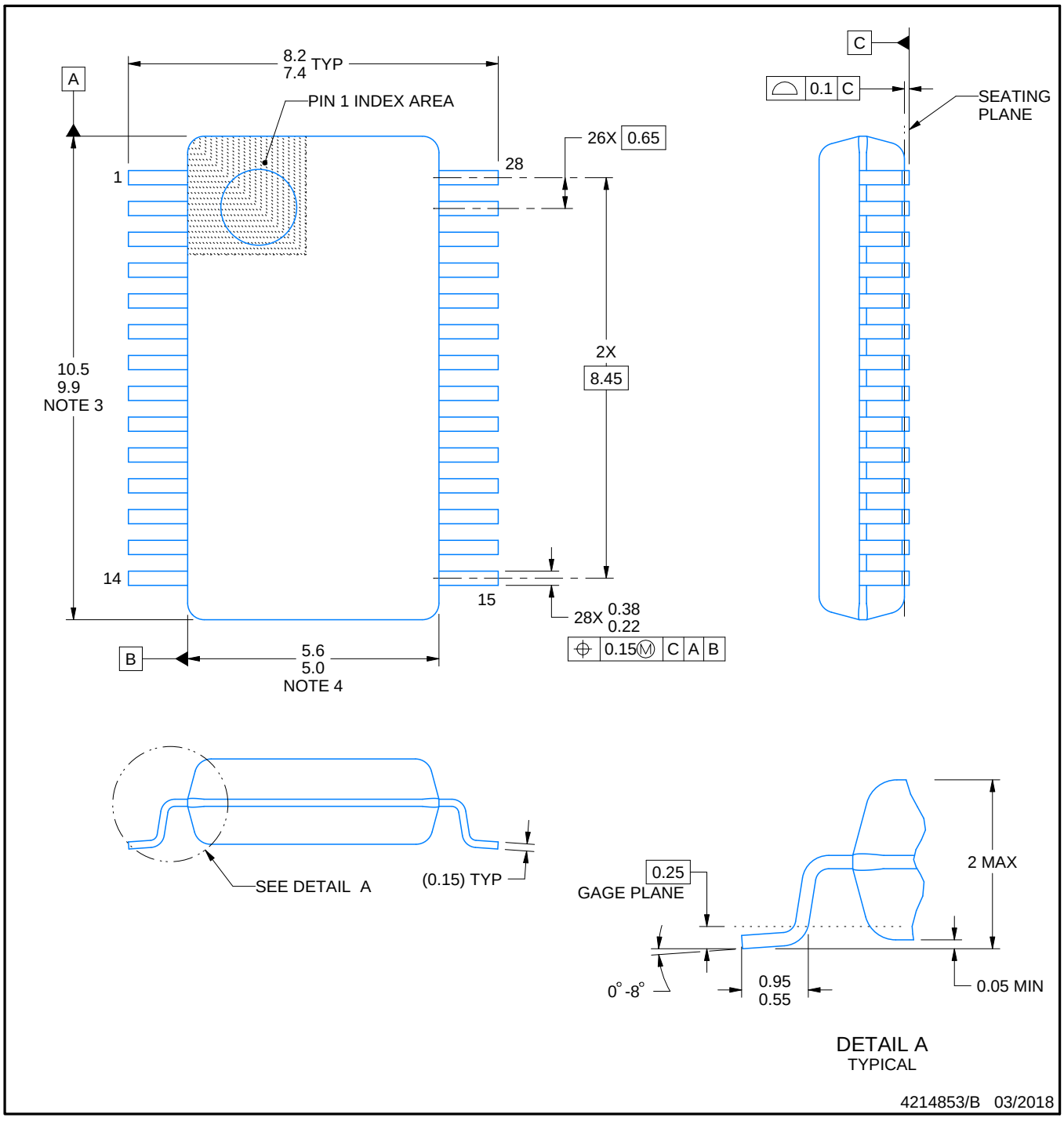
NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
E. Falls within JEDEC MO–153

PACKAGE OUTLINE

DB0028A

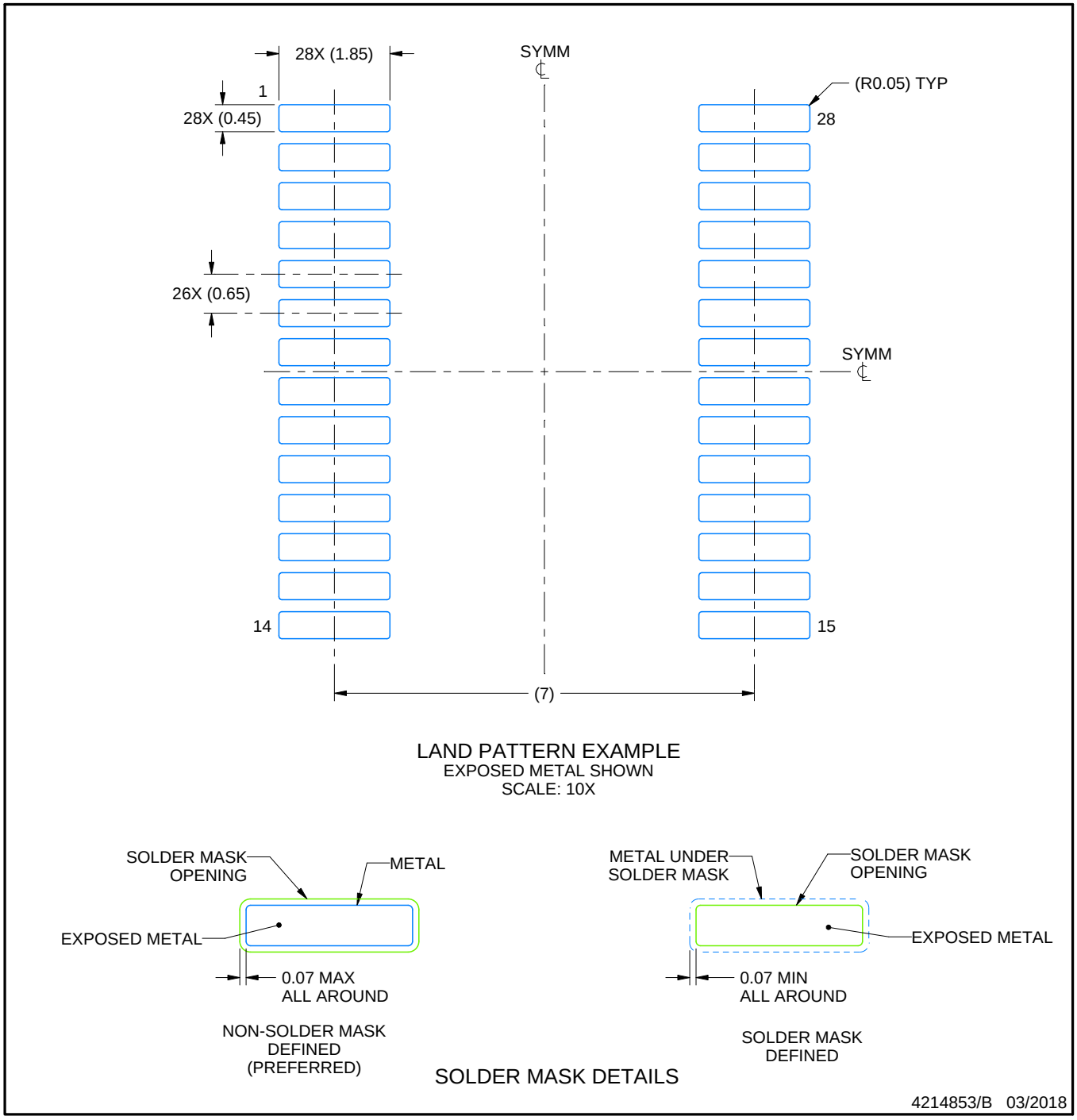
SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



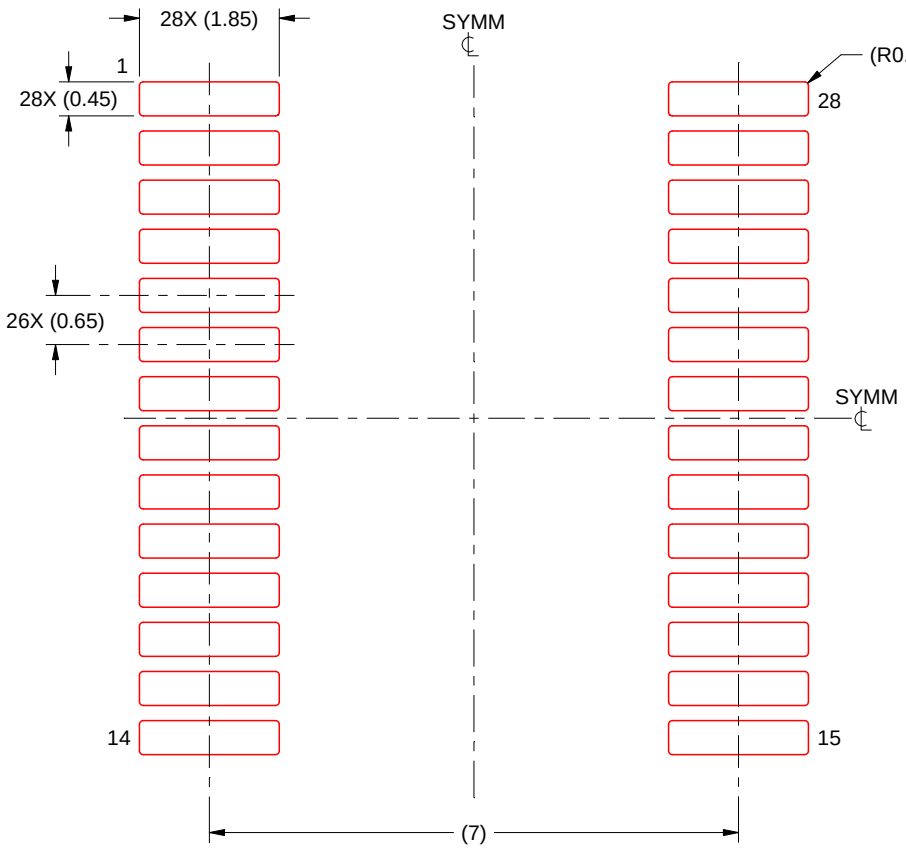
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-150.



NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4214853/B 03/2018

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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Last updated 10/2025