TEXAS INSTRUMENTS

OPA695

SBOS293H – DECEMBER 2003 – REVISED DECEMBER 2015

OPA695 Ultra-Wideband, Current-Feedback Operational Amplifier With Disable

1 Features

- Gain = +2 Bandwidth (1400 MHz)
- Gain = +8 Bandwidth (450 MHz)
- Output Voltage Swing: ±4.2 V
- Ultra-High Slew Rate: 4300 V/µs
- 3RD-Order Intercept: > 40 dBm (f < 50 MHz)
- Low Power: 129 mW
- Low Disabled Power: 0.5 mW
- Packages: SOIC-8, VSSOP-8, SOT23-6

2 Applications

- Very Wideband ADC Drivers
- Low-Cost Precision IF Amplifiers
- Broadband Video Line Drivers
- Portable Instruments
- Active Filters
- ARB Waveform Output Drivers
- OPA685 Performance Upgrades

3 Description

The OPA695 is a high bandwidth, current-feedback operational amplifier that combines an exceptional 4300-V/µs slew rate and a low input voltage noise to deliver a precision, low-cost, high dynamic range intermediate frequency (IF) amplifier. Optimized for high gain operation, the OPA695 is ideally suited to buffering surface acoustic wave (SAW) filters in an IF strip, or delivering high output power at low distortion for cable-modem upstream line drivers. At lower gains, a higher bandwidth of 1400 MHz is achievable, making the OPA695 an excellent video line driver for supporting high-resolution RGB applications.

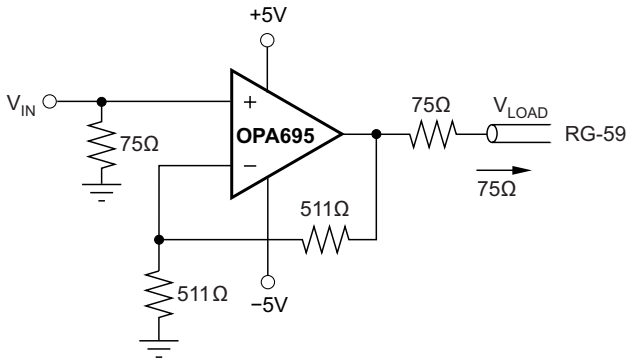
The OPA695 low 12.9-mA supply current is precisely trimmed at +25°C. This trim, along with a low temperature drift, gives low system power over temperature. System power may be further reduced using the optional disable control pin. Leaving this pin open, or holding it HIGH, gives normal operation. If pulled LOW, the OPA695 supply current drops to less than 170 µA. This power-saving feature, along with exceptional single +5-V operation and ultra-small SOT23-6 packaging, make the OPA695 ideal for portable applications.

Device Information(1)

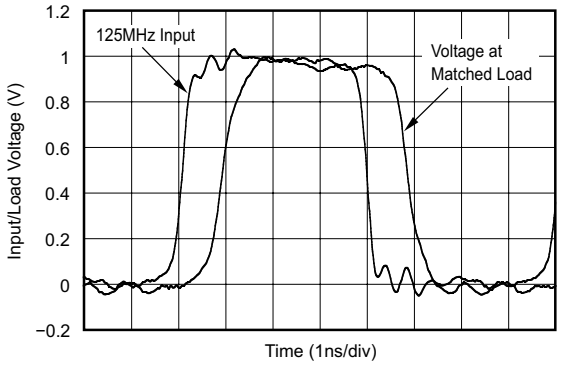
PART NUMBER	PACKAGE	BODY SIZE (NOM)
OPA695	SOT-23 (6)	1.60 mm × 2.90 mm
	VSSOP (8)	3.00 mm × 3.00 mm
	SOIC (8)	3.91 mm × 4.90 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Gain 2V/V Video Line Driver



Gain of +2V/V Video Line Driver Pulse Response



An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision G (April 2009) to Revision H — **Page**

- Added *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section. ... 1
- Removed lead temperature ... 3

Changes from Revision F (July 2006) to Revision G — **Page**

- Added DGK (MSOP-8) package to Package Ordering Information table and to Thermal Resistance specification in the Electrical Characteristics tables. ... 1

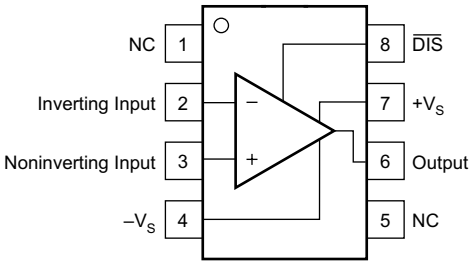
Changes from Revision E (March 2006) to Revision F — **Page**

- Changed Storage Temperature Range from −40°C to +125C to −65°C to +125C. ... 3

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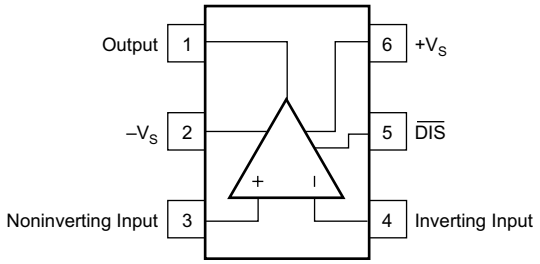
5 Pin Configuration and Functions

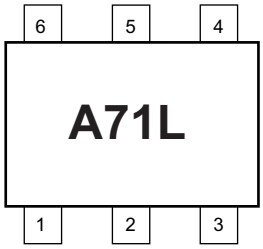
DGK or D Package
8-Pin VSSOP or SOIC
Top View



NC = No Connection

DBV Package
6-Pin SOT-23
Top View





Pin Orientation/Package Marking

Pin Functions

PIN			I/O	DESCRIPTION
VSSOP, SOIC NO.	SOT-23 NO.	NAME		
1, 5	—	NC	—	Not connected
2	4	Inverting input	I	Inverting input
3	3	Non-inverting input	I	Non-inverting input
4	2	$-V_S$	P	Negative supply
6	1	Output	O	Output
7	6	$+V_S$	P	Positive supply
8	5	$\overline{DIS}$	I	Not disable (Enable)

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)

		MIN	MAX	UNIT
	Power supply		±6.5	V
	Internal power dissipation	See *Thermal Analysis*		
	Differential input voltage		±1.2	V
	Input common-mode voltage		$\pm V_S$	V
T_J	Junction temperature		150	°C
T_{stg}	Storage temperature; D, DBV	–65	125	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

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6.2 ESD Ratings

				VALUE	UNIT
OPA695 in DGK or D package					
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001[1]	All pins except pin 2	±1500	V
			Pin 2	±500	
		Charged-device model (CDM), per JEDEC specification JESD22-C101[2]	All pins	±1000	
		Machine Model (MM)	All pins	±100	
OPA695 in DBV package					
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001[1]	All pins except pin 4	±1500	V
			Pin 4	±500	
		Charged-device model (CDM), per JEDEC specification JESD22-C101[2]	All pins	±1000	
		Machine Model (MM)	All pins	±100	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 500-V HBM is possible if necessary precautions are taken.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 250-V CDM is possible if necessary precautions are taken.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_S	Split supply voltage	±2.5	±5	±6	V
V_S	Single supply voltage	5	10	12	V
T_A	Ambient temperature	–40	25	85	°C

6.4 Thermal Information

THERMAL METRIC[1]		OPA695			UNIT
		D (SOIC)	DGK (VSSOP)	DBV (SOT-23)	
		8 PINS	8 PINS	6 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	125	135	150	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	63	81	108	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	58	56	26.4	°C/W
ψ_{JT}	Junction-to-top characterization parameter	12	8.5	15	°C/W
ψ_{JB}	Junction-to-board characterization parameter	57	48	26	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	—	—	—	—

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

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6.5 Electrical Characteristics

R_F = 348 Ω, R_L = 100 Ω to V_S/2, and G = +8, (see Figure 50 for AC performance only), unless otherwise noted.

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT	TEST LEVEL (1)
AC PERFORMANCE (see Gain 2V/V Video Line Driver)								
Small-signal bandwidth (V_O = 0.5 V_{PP})		G = +1, R_F = 523 Ω	25°C		1700		MHz	C
		G = +2, R_F = 511 Ω	25°C		1400		MHz	C
		G = +8, R_F = 402 Ω	25°C (2)	400	450		MHz	B
			0°C to 70°C (3)	380			MHz	B
			–40°C to +85°C (3)	350			MHz	B
		G = +16, R_F = 249 Ω	25°C		350		MHz	C
Bandwidth for 0.2-dB gain flatness		G = +2, V_O = 0.5 V_{PP}, R_F =523 Ω	25°C	320			MHZ	B
Peaking at a gain of +1		R_F = 523 Ω, V_O = 0.5 V_{PP}	25°C (2)		4.6	5.4	dB	B
			0°C to 70°C (3)			5.8	dB	B
			–40°C to +85°C (3)			6	dB	B
Large-signal bandwidth		G = +8, V_O = 4 V_{PP}	25°C		450		MHz	c
Slew Rate		G = –8, V_O = 4-V Step	25°C (2)	3700	4300		V/µs	B
			0°C to 70°C (3)	3600			V/µs	B
			–40°C to +85°C (3)	3500			V/µs	B
		G = +8, V_O = 4-V Step	25°C (2)	2600	2900		V/µs	B
			0°C to 70°C (3)	2500			V/µs	B
			–40°C to +85°C (3)	2400			V/µs	B
Rise-and-fall time		G = +8, V_O = 0.5-V Step	25°C	0.8			ns	C
		G = +8, V_O = 4-V Step	25°C	1			ns	C
Settling time	to 0.02%	G = +8, V_O = 2-V Step	25°C		16		ns	C
	to 0.1%		25°C		10		ns	C
Harmonic distortion (G = +8, f = 10 MHz, V_O = 2 V_{PP})	2nd-harmonic	R_L = 100 Ω	25°C (2)		–65	–62	dBc	B
			0°C to 70°C (3)			–60	dBc	B
			–40°C to +85°C (3)			–59	dBc	B
		R_L ≥ 500 Ω	25°C (2)		–78	–76	dBc	B
			0°C to 70°C (3)			–74	dBc	B
			–40°C to +85°C (3)			–73	dBc	B
	3rd-harmonic	R_L = 100 Ω	25°C (2)		–86	–84	dBc	B
			0°C to 70°C (3)			–75	dBc	B
			–40°C to +85°C (3)			–72	dBc	B
		R_L ≥ 500 Ω	25°C (2)		–86	–82	dBc	B
			0°C to 70°C (3)			–81	dBc	B
			–40°C to +85°C (3)			–80	dBc	B
Input voltage noise		f > 1 MHz	25°C (2)		1.8	2	nV/√Hz	B
			0°C to 70°C (3)			2.7	nV/√Hz	B
			–40°C to +85°C (3)			2.9	nV/√Hz	B
Noninverting input current noise		f > 1 MHz	25°C (2)		18	19	nV/√Hz	B
			0°C to 70°C (3)			21	nV/√Hz	B
			–40°C to +85°C (3)			22	nV/√Hz	B

(1) Test levels: (A) 100% tested at +25°C. Over temperature limits by characterization and simulation. (B) Limits set by characterization and simulation. (C) Typical value only for information.
(2) Junction temperature = ambient for +25°C specifications.
(3) Junction temperature = ambient at low temperature limit; junction temperature = ambient +15°C at high temperature limit for over temperature specifications.

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Electrical Characteristics (continued)

R_F = 348 Ω, R_L = 100 Ω to V_S/2, and G = +8, (see Figure 50 for AC performance only), unless otherwise noted.

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT	TEST LEVEL (1)
Inverting input current noise	f > 1 MHz	25°C (2)		22	24	pA/√Hz	B
		0°C to 70°C (3)			26		
		–40°C to +85°C (3)			27		
Differential gain	G = +2, NTSC, V_O = 1.4 Vp, R_L = 150 Ω	25°C		0.04%			C
Differntial phase	G = +2, NTSC, V_O = 1.4 Vp, R_L = 150 Ω	25°C		0.007		deg	deg
DC PERFORMANCE (4)							
Open-loop transimpedance gain (Z_{OL})	V_O = 0 V, R_L = 100	25°C (2)	45 (5)	85		kΩ	A
		0°C to 70°C (3)	43				
		–40°C to +85°C (3)	41				
Input offset voltage	V_{CM} = 0 V	25°C (2)		±0.3	±3.0 (5)	mV	A
		0°C to 70°C (3)			±3.5		
		–40°C to +85°C (3)			±4		
Average offset voltage drift	V_{CM} = 0 V	0°C to 70°C (3)			±10	µV/°C	B
		–40°C to +85°C (3)			±15		
Noninverting input bias current	V_{CM} = 0 V	25°C (2)		±13	±30 (5)	µA	A
		0°C to 70°C (3)			±37		
		–40°C to +85°C (3)			±41		
Average noninventing input bias current drift	V_{CM} = 0 V	0°C to 70°C (3)			150	µA	A
		–40°C to +85°C (3)			150		
Inverting input bias current	V_{CM} = 0 V	25°C (2)		±20	±60 (5)	µA	A
		0°C to 70°C (3)			±66		
		–40°C to +85°C (3)			±70		
Average inventing bias current drift	V_{CM} = 0 V	0°C to 70°C (3)			±120	nA/°C	B
		–40°C to +85°C (3)			±160		
INPUT							
Common-mode input range (6) (CMIR)	25°C (2)		±3.1 (5)	±3.3		V	A
	0°C to 70°C (3)		±3				
	–40°C to +85°C (3)		±3				
Common-mode rejection ratio (CMRR)	VCM = 0 V	25°C (2)	51 (5)	56		dB	A
		0°C to 70°C (3)	50				
		–40°C to +85°C (3)	50				
Noninverting input impedance	25°C (2)			280 || 1.2		kΩ || pF	C
Inverting input resistance (R_I)	Open-loop	25°C (2)		29		Ω	C
OUTPUT							
Voltage output swing	No load	25°C (2)	±4 (5)	±4.2		V	A
		0°C to 70°C (3)	±3.9				
		–40°C to +85°C (3)	±3.9				
	100-Ω load	25°C (2)	±3.7 (5)	±3.9			
		0°C to 70°C (3)	±3.7				
		–40°C to +85°C (3)	±3.6				

(4) Current is considered positive out-of-node. V_{CM} is the input common-mode voltage.
(5) Limits are tested at +25°C.
(6) Tested < 3 dB below minimum specified CMRR at ± CMIR limits.

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Electrical Characteristics (continued)

R_F = 348 Ω, R_L = 100 Ω to V_S/2, and G = +8, (see Figure 50 for AC performance only), unless otherwise noted.

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT	TEST LEVEL (1)
Current output, sourcing	V_O = 0	25°C (2)	90 (5)	120		mA	A
		0°C to 70°C (3)	80				
		–40°C to +85°C (3)	70				
Current output, sinking	V_O = 0	25°C (2)	90 (5)			mA	A
		0°C to 70°C (3)	–80				
		–40°C to +85°C (3)	–70				
Closed-loop output impedance	G = +8, f = 100 kHz	25°C		0.04		Ω	C
DISABLE (Disabled LOW)							
Power-down supply current (+V_S)	$V_{\overline{DIS}}$ = 0	25°C		–100		µA	A
		25°C (2)		–170 (5)			
		0°C to 70°C (3)		–186			
		–40°C to +85°C (3)		–192			
Disable time	V_{IN} = ±0.25 V_{DC}	25°C		1		µs	C
Enable time	V_{IN} = ±0.25 V_{DC}	25°C		1		ns	C
Off isolation	G = +8, 10 MHz	25°C		70		dB	C
Output capacitance in disable	25°C			4		pF	C
Turn on glitch	G = +2, R_L = 150 Ω, V_{IN} = 0	25°C		±100		mV	C
Turn off glitch	G = +2, R_L = 150 Ω, V_{IN} = 0	25°C		±20		mV	C
Enable voltage	25°C (2)		3.5 (5)	3.3		V	A
	0°C to 70°C (3)		3.6				
	–40°C to +85°C (3)		3.7				
Disable voltage	25°C (2)			1.8	1.7 (5)	V	A
	0°C to 70°C (3)				1.6		
	–40°C to +85°C (3)				1.5		
Control pin input bias current ($\overline{DIS}$)	$V_{\overline{DIS}}$ = 0	25°C (2)		75	130 (5)	µA	A
		0°C to 70°C (3)			143		
		–40°C to +85°C (3)			145		
POWER SUPPLY							
Specified operating voltage	25°C			±5		V	C
Maximum operating voltage range	25°C (2)				±6 (5)	V	A
	0°C to 70°C (3)				±6		
	–40°C to +85°C (3)				±6		
Maximum quiescent	V_S = ±5 V	25°C		12.9		mA	A
		25°C (2)			13.3 (5)		
		0°C to 70°C (3)			13.7		
		–40°C to +85°C (3)			14.1		
Minimum quiescent current	V_S = ±5 V	25°C		12.9		mA	A
		25°C (2)	12.6 (5)				
		0°C to 70°C (3)	11.8				
		–40°C to +85°C (3)	11				
Power-supply rejection radio (–PSRR)	Input referred	25°C		55		dB	A
		25°C (2)	51 (5)				
		0°C to 70°C (3)	48				
		–40°C to +85°C (3)	48				

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Electrical Characteristics (continued)

R_F = 348 Ω, R_L = 100 Ω to V_S/2, and G = +8, (see Figure 50 for AC performance only), unless otherwise noted.

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT	TEST LEVEL (1)
TEMPERATURE RANGE								
Specification: ID, IDBV		25°C		–40 to 85			°C	C
AC PERFORMANCE (see Figure 50)								
Small-signal bandwidth (V_O = 0.5 V_{PP})		G = +1, R_F = 511 Ω	25°C		1400		MHz	C
		G = +2, R_F = 487 Ω	25°C	960				C
		G = +8, R_F = 348 Ω	25°C		395			B
			25°C (2)		980			
			0°C to 70°C (3)		330			
			–40°C to +85°C (3)		300			
		G = +16, R_F = 162 Ω	25°C		235			C
Bandwith for 0.2-dB gain flatness		G = +2, V_O <0.5 V_{PP}, R_F = 487Ω	25°C		230		MHz	B
			25°C (2)	180				
			0°C to 70°C (3)	135				
			–40°C to +85°C (3)	110				
Peaking at a gain of +1		V_O <0.5 V_{PP}, R_F = 511 Ω	25°C	1			dB	B
			25°C (2)			2		
			0°C to 70°C (3)			2.5		
			–40°C to +85°C (3)			3		
Large-signal bandwidth		G = +8, V_O = 2 V_{PP}	25°C		310		MHz	C
Slew rate		G = +8, 2-V Step	25°C		1700		v/µs	B
			25°C (2)	1300				
			0°C to 70°C (3)	1200				
			–40°C to +85°C (3)	1100				
Rise-and-fall-time		G = +8, V_O = 0.5-V Step	25°C		1		ns	C
		G = +8, V_O = 2-V Step	25°C		1			
Settling time	to 0.02%	G = +8, V_O = 2-V Step	25°C		16		ns	C
	to 0.1%	G = +8, V_O = 2-V Step	25°C		10			
Harmonic distortion (G = +8, f = 10 MHz, V_O = 2 V_{PP})	2nd-Harmonic	R_L = 100 Ω to V_S/2	25°C		–62		dBc	B
			25°C (2)			–58		
			0°C to 70°C (3)			–58		
			–40°C to +85°C (3)			–57		
		R_L ≥ 500 Ω to V_S/2	25°C		–70			
			25°C (2)			–66		
			0°C to 70°C (3)			–66		
			–40°C to +85°C (3)			–65		
	3rd-Harmonic	R_L = 100 Ω to V_S	25°C		–66			
			25°C (2)			–64		
			0°C to 70°C (3)			–64		
			–40°C to +85°C (3)			–63		
		R_L ≥ 500 Ω to V_S	25°C		–65			
			25°C (2)			–63		
			0°C to 70°C (3)			–63		
			–40°C to +85°C (3)			–62		

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Electrical Characteristics (continued)

R_F = 348 Ω, R_L = 100 Ω to V_S/2, and G = +8, (see Figure 50 for AC performance only), unless otherwise noted.

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT	TEST LEVEL (1)
Input voltage noise	f > 1 MHz	25°C		1.8		nV/√Hz	B
		25°C (2)			2		
		0°C to 70°C (3)			2.7		
		–40°C to +85°C (3)			2.9		
Noninverting input current noise	f > 1 MHz	25°C		18		nV/√Hz	B
		25°C (2)			19		
		0°C to 70°C (3)			21		
		–40°C to +85°C (3)			22		
Inverting input current noise	f > 1 MHz	25°C		22		pA/√Hz	B
		25°C (2)			24		
		0°C to 70°C (3)			26		
		–40°C to +85°C (3)			27		
DC PERFORMANCE (4)							
Open-loop transimpedance gain (Z_{OL})	V_O = V_S/2, R_L = 100 Ω to V_S/2	25°C		70		kΩ	A
		25°C (2)	40				
		0°C to 70°C (3)	38				
		–40°C to +85°C (3)	38				
Input offset voltage	V_{CM} = V_S/2	25°C		±0.3		mV	A
		25°C (2)			±3 (5)		
		0°C to 70°C (3)			±3.5		
		–40°C to +85°C (3)			±4		
Average offset voltage drift	V_{CM} = V_S	0°C to 70°C (3)			±10	µV/°C	B
		–40°C to +85°C (3)			±15		
Noninventing input bias current	V_{CM} = V_S	25°C		±5		µA	A
		25°C (2)			±40 (5)		
		0°C to 70°C (3)			±45		
		–40°C to +85°C (3)			±50		
Average noninventing input bias current drift	V_{CM} = V_S	0°C to 70°C (3)			±110	nA/°C	B
		–40°C to +85°C (3)			±170		
Inverting input bias current	V_{CM} = V_S	25°C		±5			
		25°C (2)			±60 (5)		
		0°C to 70°C (3)			±66		
		–40°C to +85°C (3)			±70		
Average inverting input bias current drift	V_{CM} = V_S	0°C to 70°C (3)			±120	nA/°C	B
		–40°C to +85°C (3)			±160		
INPUT							
Least positive input voltage (6)	25°C			1.7		V	A
	25°C (2)				1.8 (5)		
	0°C to 70°C (3)				1.9		
	–40°C to +85°C (3)				1.9		
Most positive input voltage (6)	25°C			3.3		V	A
	25°C (2)		3.2 (5)				
	0°C to 70°C (3)		3.1				
	–40°C to +85°C (3)		3.1				

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Electrical Characteristics (continued)

R_F = 348 Ω, R_L = 100 Ω to V_S/2, and G = +8, (see Figure 50 for AC performance only), unless otherwise noted.

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT	TEST LEVEL (1)
Common-mode rejection ratio (CMRR)	V_{CM} = V_S/2	25°C		54		dB	A
		25°C (2)		51 (5)			
		0°C to 70°C (3)		50			
		–40°C to +85°C (3)		50			
Noninverting input impedance	25°C			280 || 1.2		kΩ || pF	C
Inverting input resistance (R_I)	Open-loop	25°C		32		Ω	C
OUTPUT							
Most positive output voltage	No load	25°C		4.2		V	A
		25°C (2)	4.0 (5)				
		0°C to 70°C (3)	3.9				
		–40°C to +85°C (3)	3.8				
	R_L = 100 Ω to V_S/2	25°C		4			
		25°C (2)	3.9 (5)				
		0°C to 70°C (3)	3.8				
		–40°C to +85°C (3)	3.7				
Least positive output voltage	No load	25°C		0.8		V	A
		25°C (2)			1 (5)		
		0°C to 70°C (3)			1.1		
		–40°C to +85°C (3)			1.2		
	R_L = 100 Ω to V_S/2	25°C	1				
		25°C (2)			1.1 (5)		
		0°C to 70°C (3)			1.2		
		–40°C to +85°C (3)			1.3		
Current output, sourcing	V_O = V_S/2	25°C		90		mA	A
		25°C (2)	70 (5)				
		0°C to 70°C (3)	67				
		–40°C to +85°C (3)	66				
Current output, sinking	V_O = V_S/2	25°C		–90		mA	A
		25°C (2)	–70 (5)				
		0°C to 70°C (3)	–67				
		–40°C to +85°C (3)	–66				
Closed-loop output impedance	G = +2, f = 100 kHz			0.05		Ω	C
DISABLE (Disabled LOW)							
Power down supply current (+V_S)	$V_{\overline{DIS}}$ = 0	25°C	–95			μA	C
		25°C (2)		–160			
		0°C to 70°C (3)		–175			
		–40°C to +85°C (3)		–180			
Disable time	25°C			1		μs	C
Enable time	25°C			25		ns	C
Off isolation	G = +8, 10 MHz	25°C		70		dB	C
Output capacitance in disable	25°C			4		pF	C
Tun on glitch	G = +2, R_L = 150 Ω, VIN = V_S /2	25°C		±100		mV	C
Turn off glitch	G = +2, R_L = 150 Ω, V_{IN} = V_S /2	25°C		±20		mV	C

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Electrical Characteristics (continued)

R_F = 348 Ω, R_L = 100 Ω to V_S/2, and G = +8, (see Figure 50 for AC performance only), unless otherwise noted.

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT	TEST LEVEL (1)
Enable voltage	25°C			3.3		V	A
	25°C (2)		3.5 (5)				
	0°C to 70°C (3)		3.6				
	–40°C to +85°C (3)		3.7				
Disable voltage	25°C			1.8		V	A
	25°C (2)				1.7 (5)		
	0°C to 70°C (3)				1.6		
	–40°C to +85°C (3)				1.5		
Control pin input bias current ($\overline{DIS}$)	$V_{\overline{DIS}}$ = 0	25°C		75		µA	C
		25°C (2)		130			
		0°C to 70°C (3)		143			
		–40°C to +85°C (3)		149			
POWER SUPPLY							
Specified single-supply operating voltage	25°C			5		V	C
Max single-supply operating voltage	25°C (2)				12 (5)	V	A
	0°C to 70°C (3)				12		
	–40°C to +85°C (3)				12		
Max quiescent current	V_S = +5 V	25°C		11.4		mA	A
		25°C (2)			12 (5)		
		0°C to 70°C (3)			12.5		
		–40°C to +85°C (3)			12.9		
Min quiescent current	V_S = +5 V	25°C		11.4		mA	A
		25°C (2)	10.9 (5)				
		0°C to 70°C (3)	9.4				
		–40°C to +85°C (3)	9.1				
Power-supply rejection ratio (–PSRR)	Input referred	25°C		56		dB	A
TEMPERATURE RANGE							
Specification: ID, IDBV	25°C			–40 to +85		°C	°C

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6.6 Typical Characteristics

G = +8, R_F = 402 Ω, R_L = 100 Ω, unless otherwise noted.

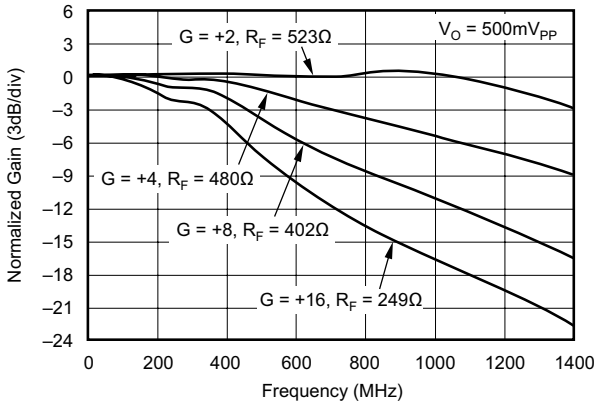


Figure 1. Noninverting Small-Signal Frequency Response

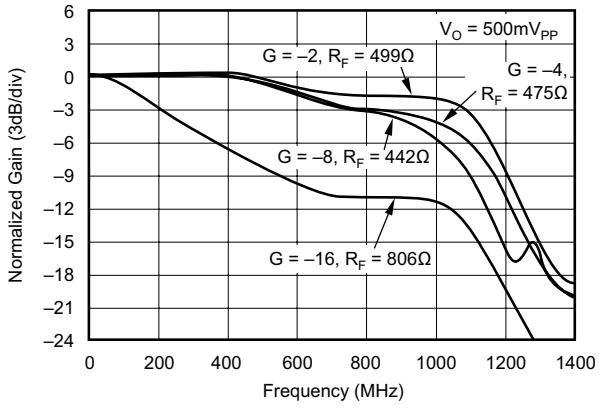


Figure 2. Inverting Small-Signal Frequency Response

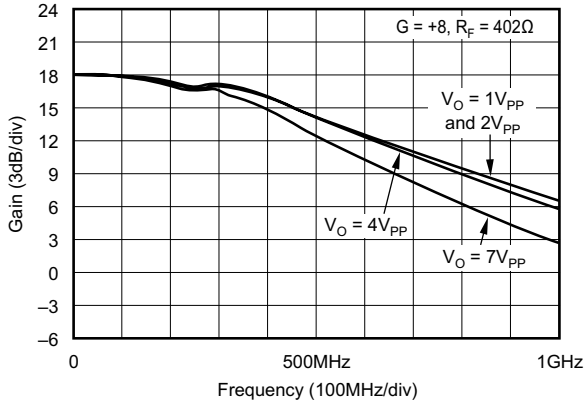


Figure 3. Noninverting Large-Signal Frequency Response

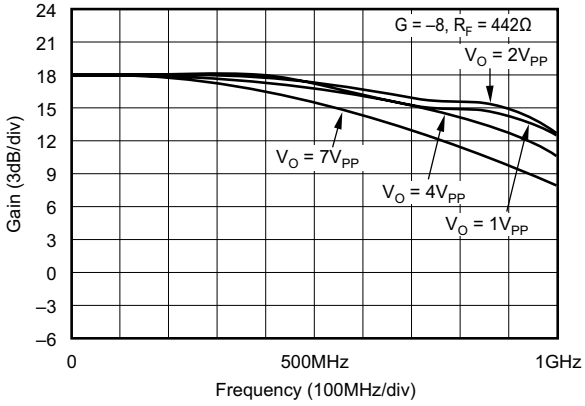


Figure 4. Inverting Large-Signal Frequency Response

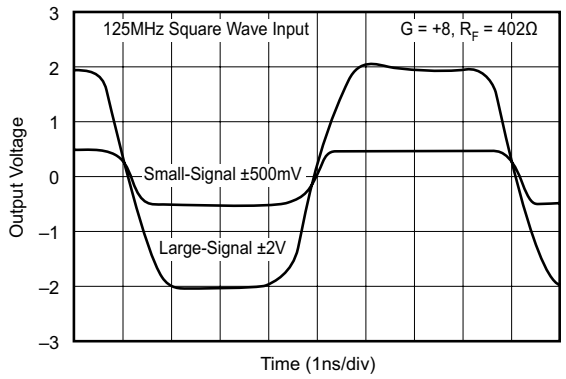


Figure 5. Noninverting Large and Small-Signal Frequency Response

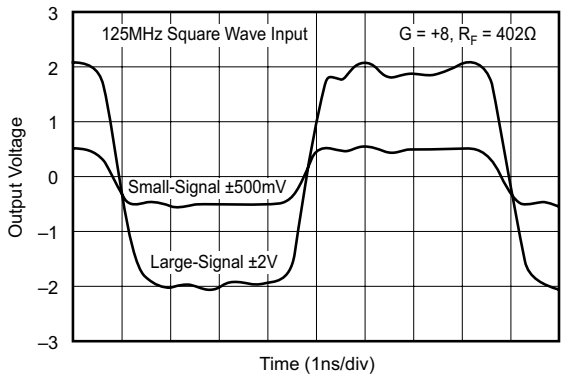


Figure 6. Inverting Large and Small-Signal Frequency Response

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Typical Characteristics (continued)

G = +8, R_F = 402 Ω, R_L = 100 Ω, unless otherwise noted.

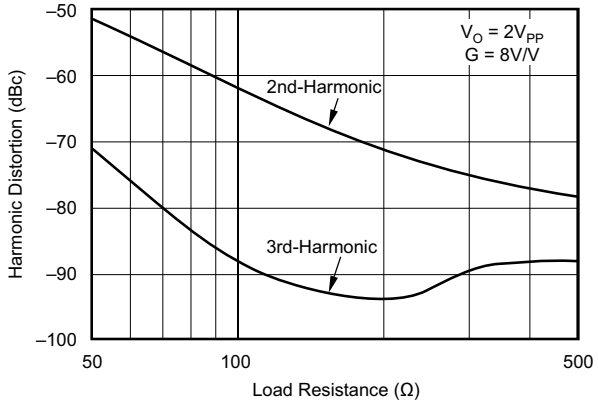


Figure 7. 10-MHz Harmonic Distortion vs Load Resistance

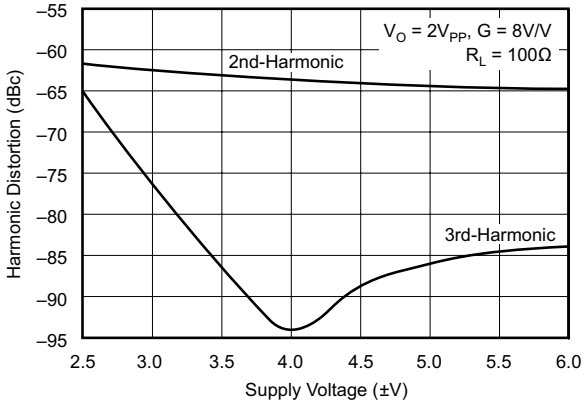


Figure 8. 10-MHz Harmonic Distortion vs Supply Voltage

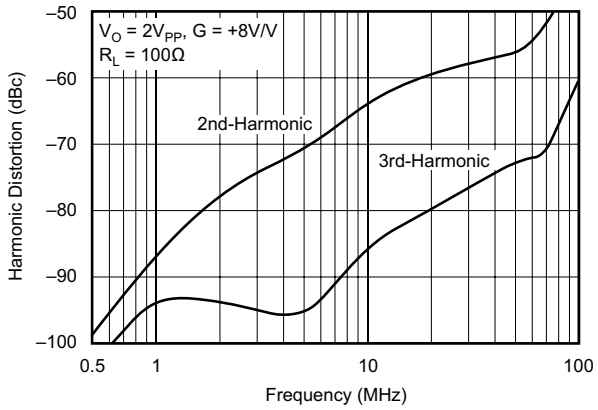


Figure 9. Harmonic Distortion vs Frequency

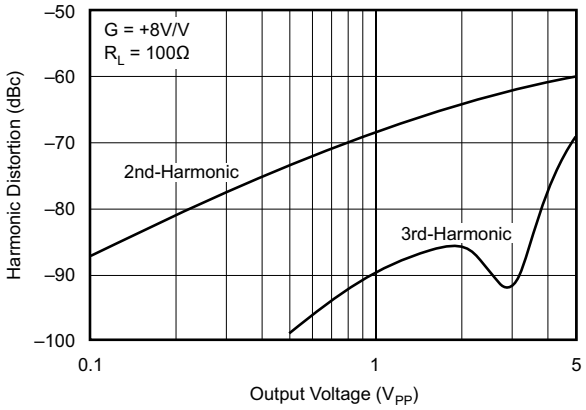


Figure 10. 10-MHz Harmonic Distortion vs Output Voltage

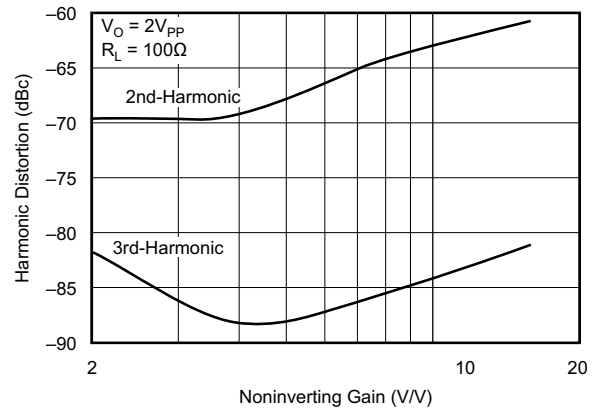


Figure 11. 10-MHz Harmonic Distortion vs Noninverting Gain

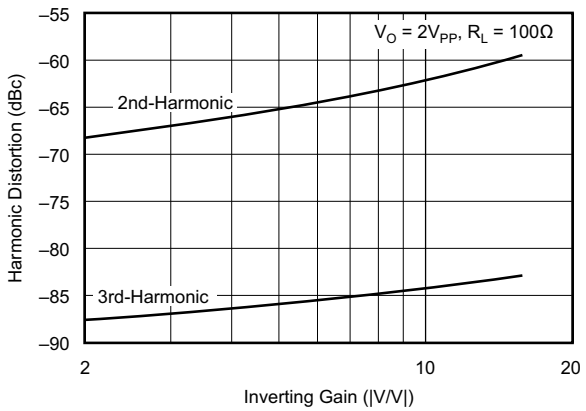


Figure 12. 10-MHz Harmonic Distortion vs Inverting Gain

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Typical Characteristics (continued)

$G = +8$, $R_F = 402\ \Omega$, $R_L = 100\ \Omega$, unless otherwise noted.

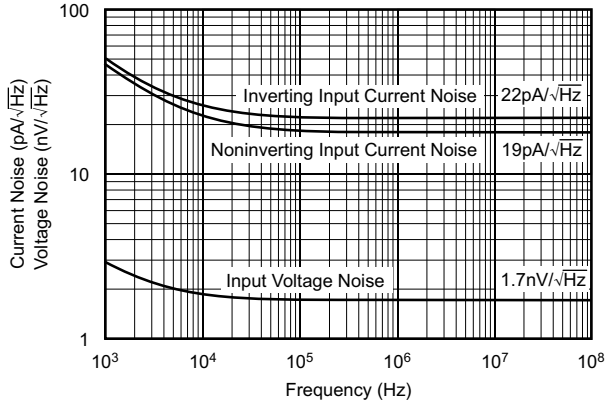


Figure 13. Input Voltage and Current Noise Density

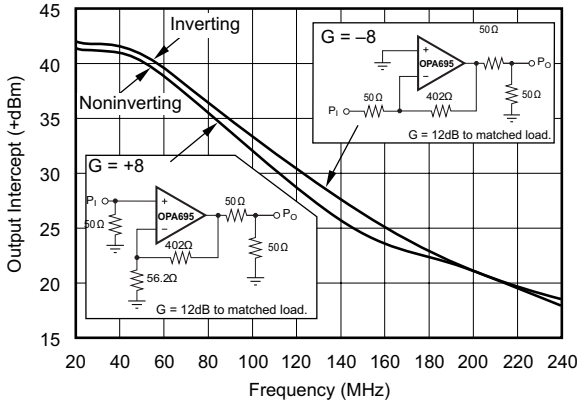


Figure 14. Two-Tone 3rd-Order Intermodulation Intercept ±5 V

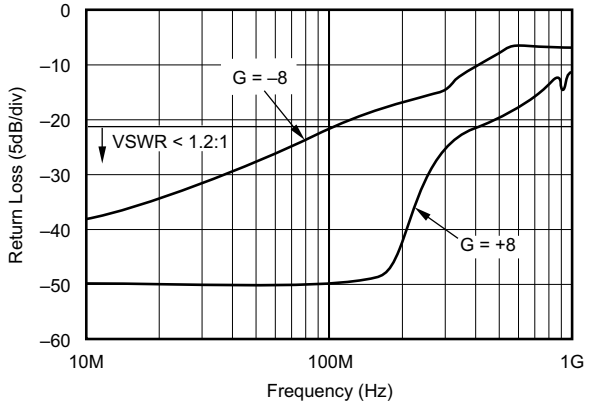


Figure 15. Input Return Loss vs Frequency (S_{11})

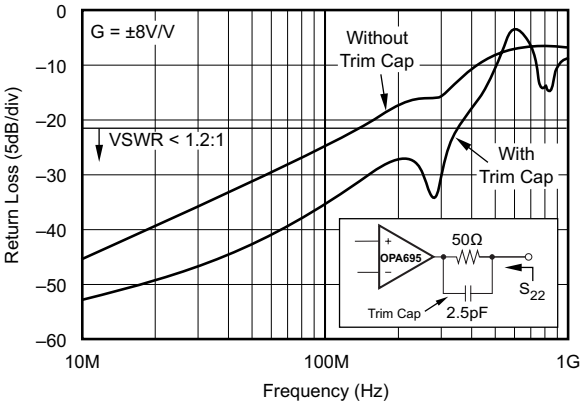


Figure 16. Output Return Loss vs Frequency (S_{22})

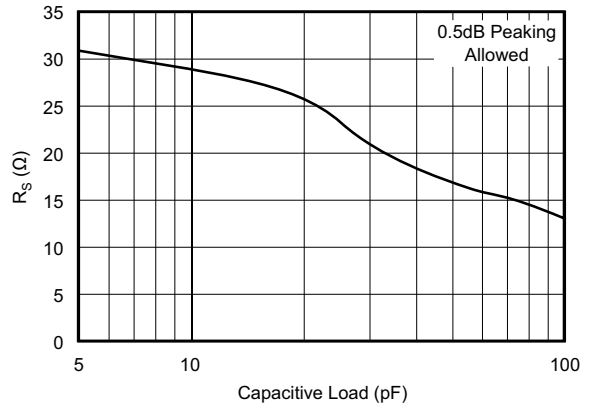


Figure 17. R_S vs Capacitive Load

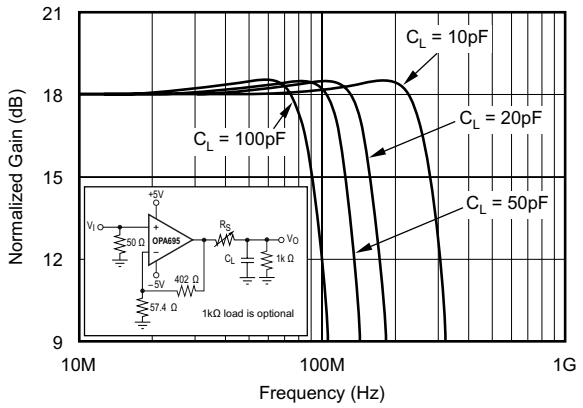


Figure 18. Small-Signal Frequency Response vs Capacitive Load

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Typical Characteristics (continued)

G = +8, R_F = 402 Ω, R_L = 100 Ω, unless otherwise noted.

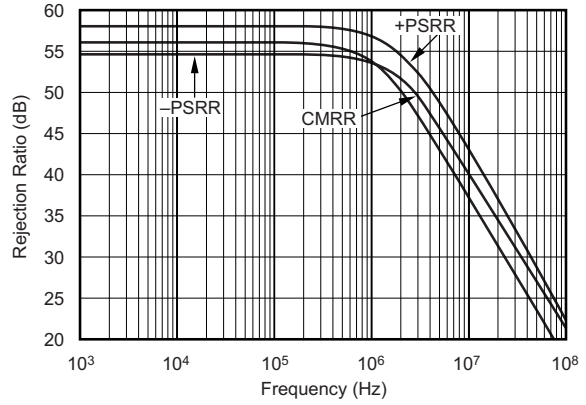


Figure 19. CMRR and PSRR vs Frequency

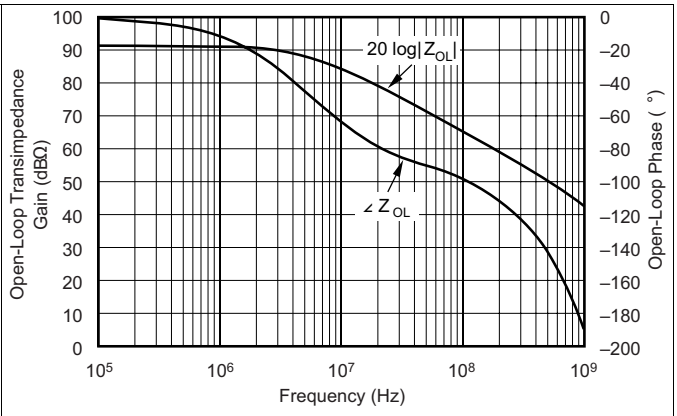


Figure 20. Open-Loop Transimpedance Gain and Phase

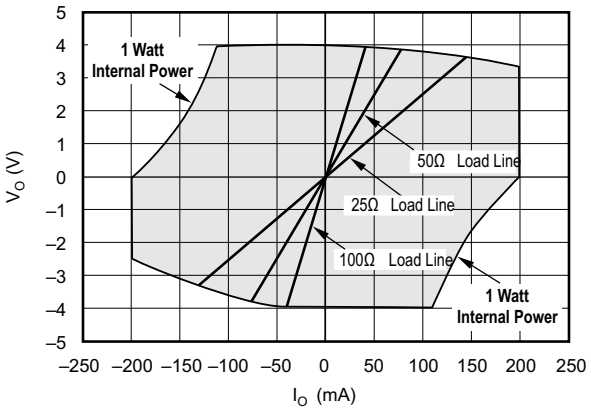


Figure 21. Output Voltage and Current Limitations

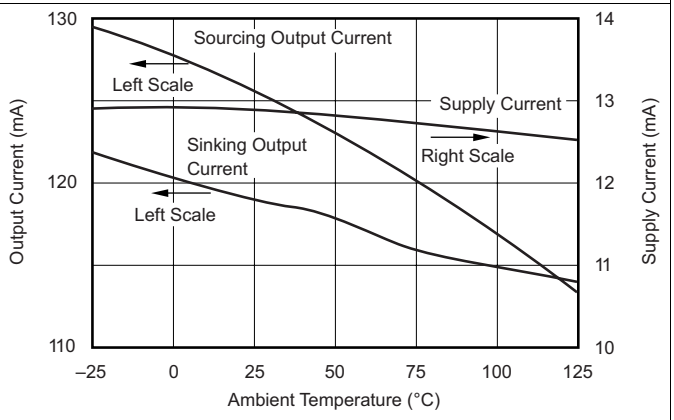


Figure 22. Supply and Output Current vs Temperature

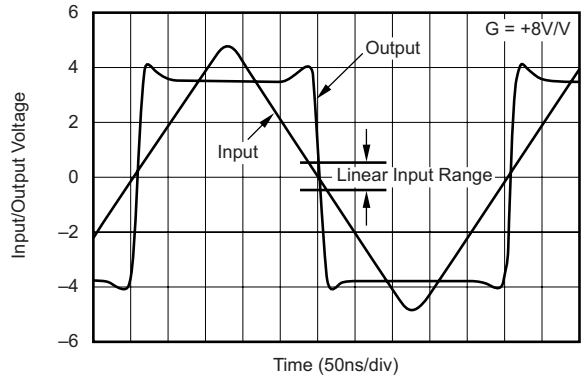


Figure 23. Noninverting Overdrive Recovery

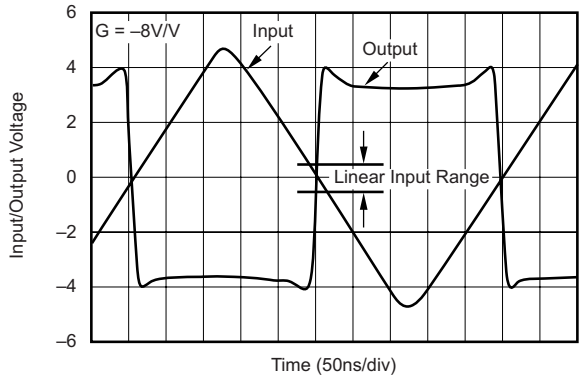


Figure 24. Inverting Overdrive Recovery

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Typical Characteristics (continued)

G = +8, R_F = 402 Ω, R_L = 100 Ω, unless otherwise noted.

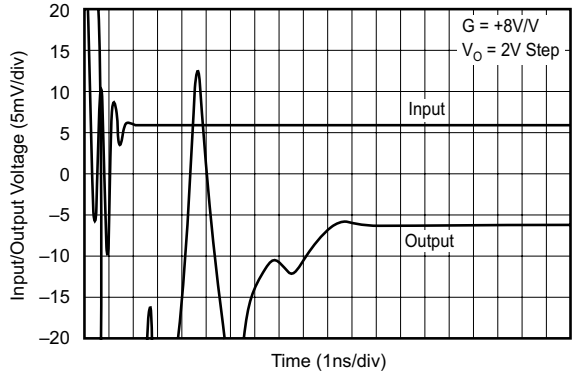


Figure 25. Settling Time

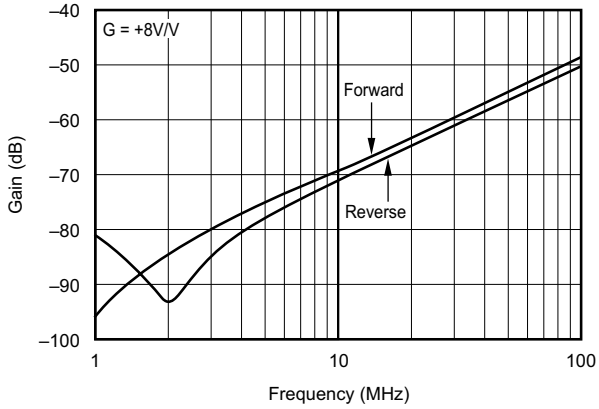


Figure 26. Disabled Feedthrough vs Frequency

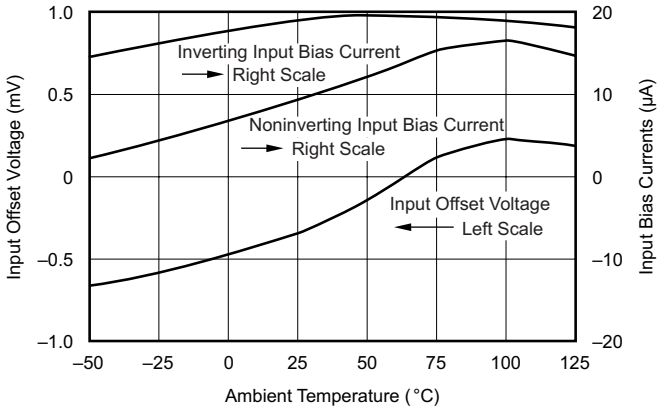


Figure 27. Typical DC Drift Over Temperature

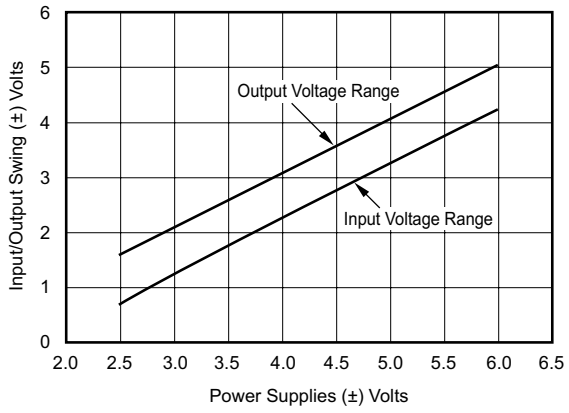


Figure 28. Common-Mode Input and Output Swing vs Supply Voltage

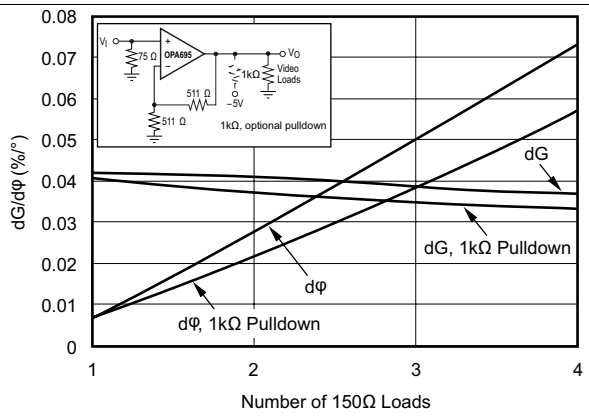


Figure 29. Composite Video dG/dφ

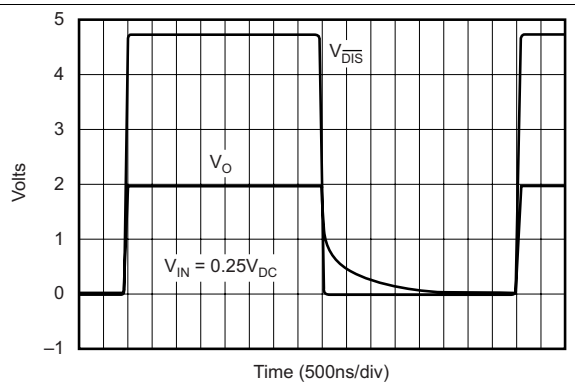
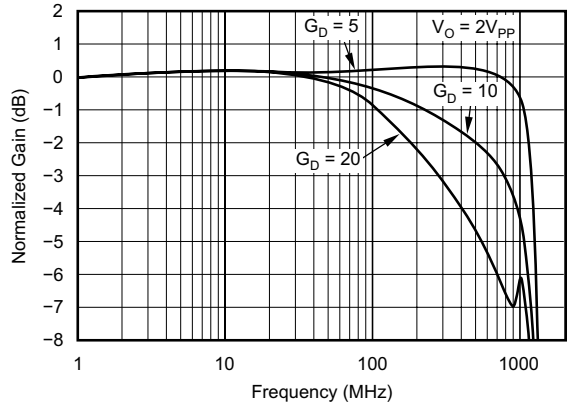


Figure 30. Large-Signal Disable/Enable Response

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Typical Characteristics (continued)

G = +8, R_F = 402 Ω, R_L = 100 Ω, unless otherwise noted.



See Figure 47

Figure 31. Differential Small-Signal Frequency Response

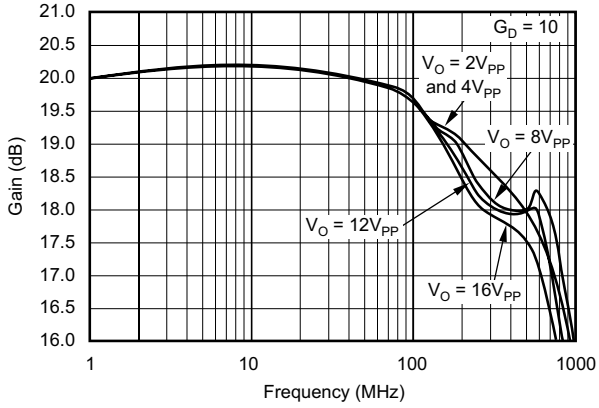


Figure 32. Large-Signal Bandwidth

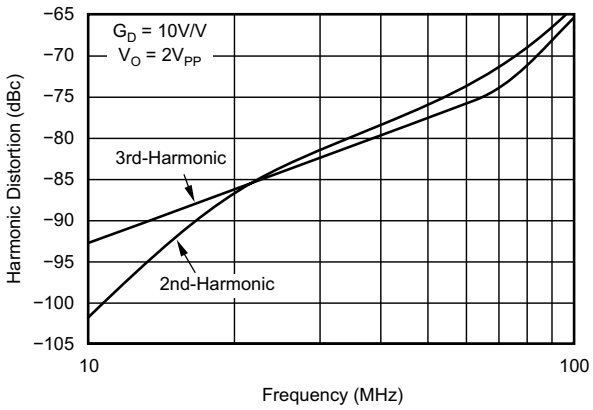


Figure 33. Distortion vs Frequency

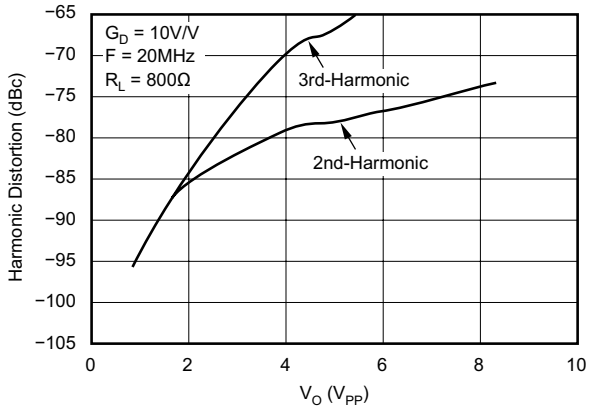


Figure 34. Distortion vs V_{OUT}

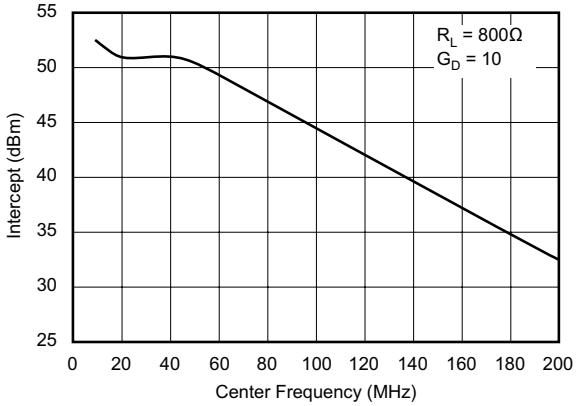


Figure 35. 2-Tone, 3rd-Order Intermodulation Intercept

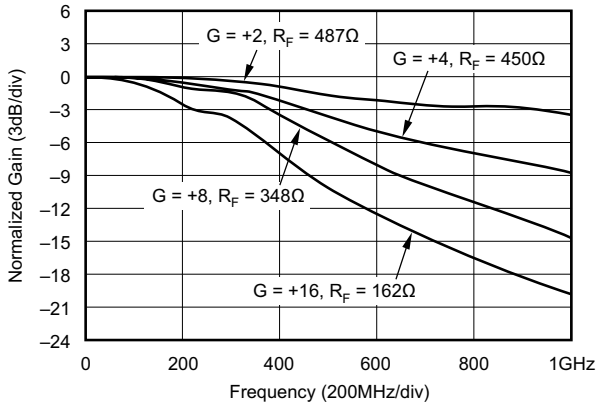


Figure 36. Noninverting Small-Signal Frequency Response

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Typical Characteristics (continued)

G = +8, R_F = 402 Ω, R_L = 100 Ω, unless otherwise noted.

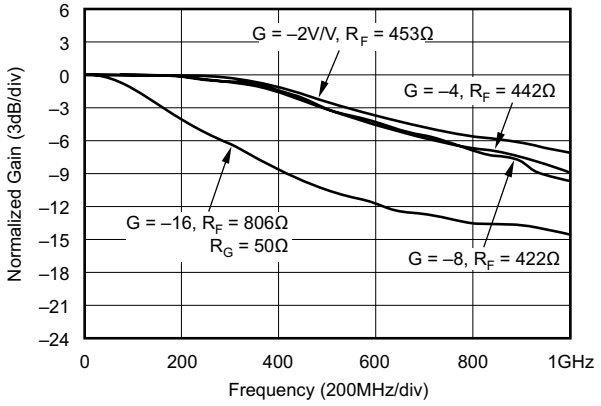


Figure 37. Inverting Small-Signal Frequency Response

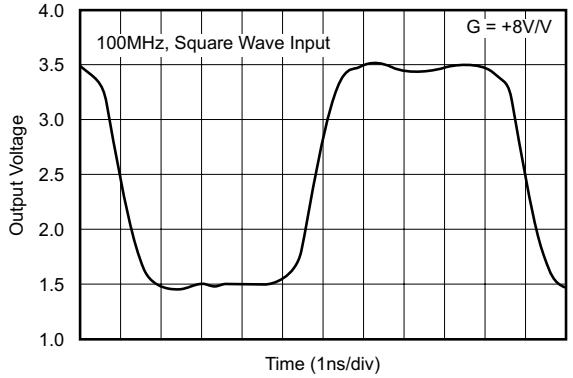


Figure 38. Noninverting Pulse Response

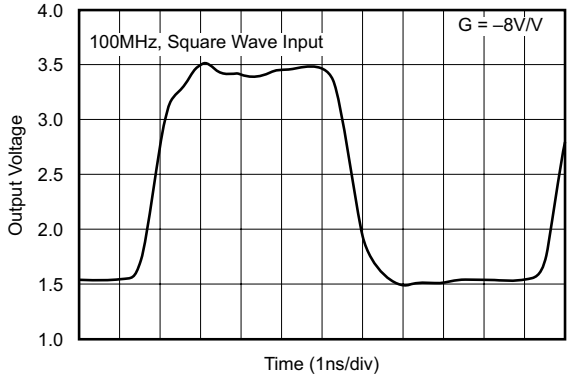


Figure 39. Inverting Pulse Response

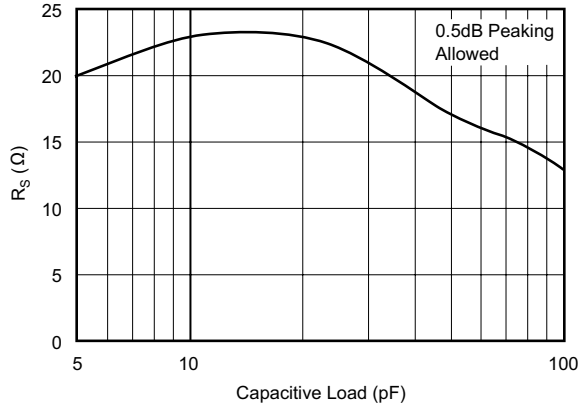


Figure 40. R_S vs Capacitive Load

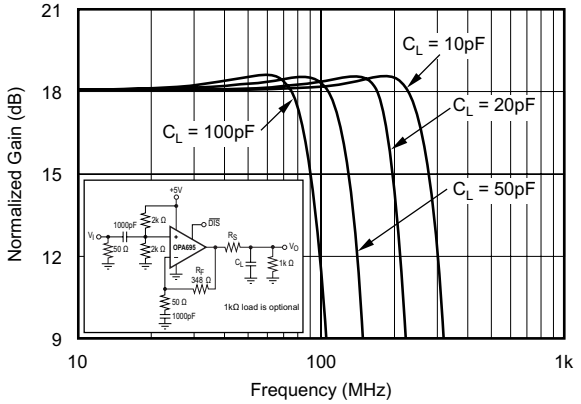


Figure 41. Small-Signal Frequency Response vs Capacitive Load

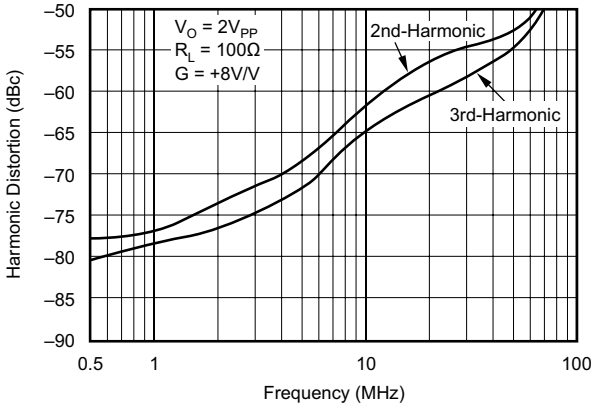


Figure 42. Harmonic Distortion vs Frequency

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Typical Characteristics (continued)

G = +8, R_F = 402 Ω, R_L = 100 Ω, unless otherwise noted.

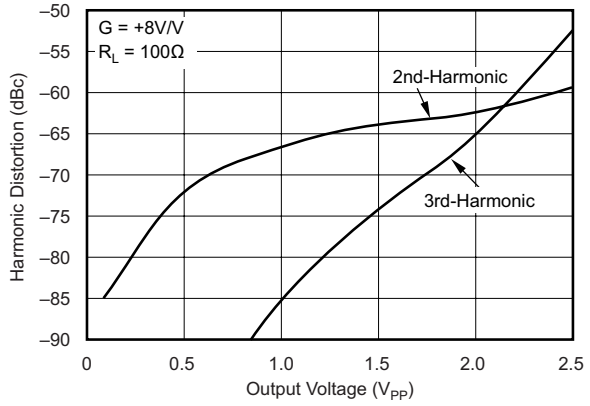


Figure 43. 10-MHz Harmonic Distortion vs Output Voltage

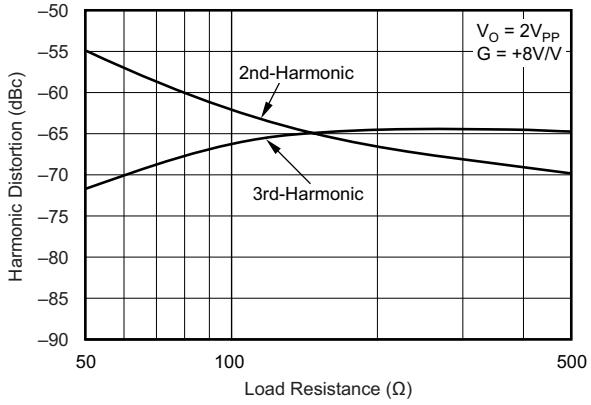


Figure 44. 10-MHz Harmonic Distortion vs Load Resistance

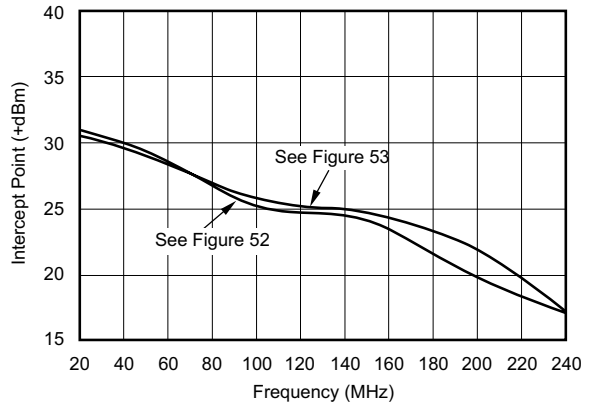


Figure 45. Two-Tone, 3rd-Order Intermodulation Intercept

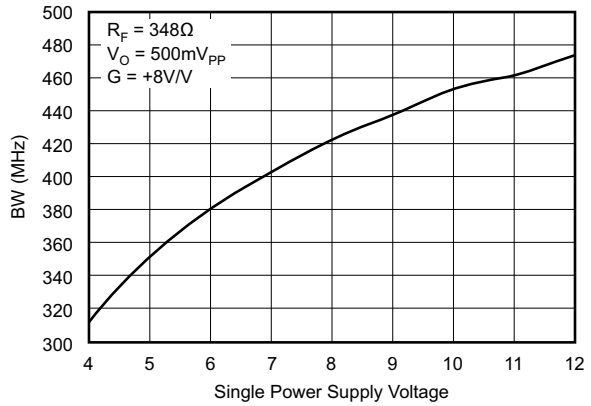


Figure 46. Small-Signal BW vs Single-Supply Voltage

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7 Parameter Measurement Information

7.1 Differential Small Signal Measurement

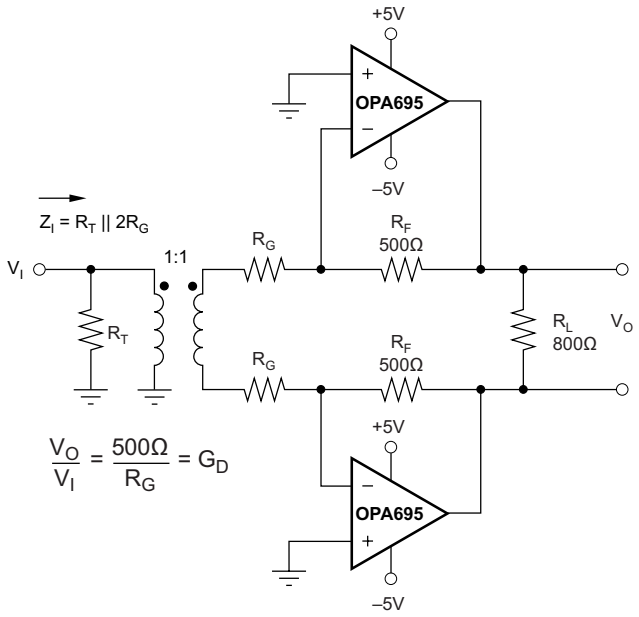


Figure 47. Schematic for Differential Small-Signal Frequency Response

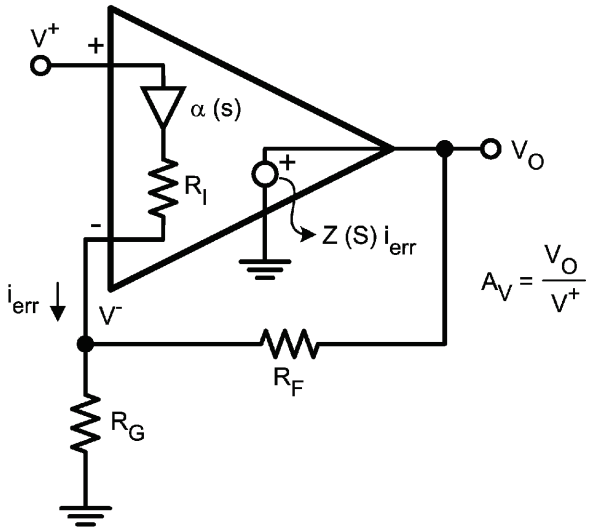
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8 Detailed Description

8.1 Overview

The OPA695, seen below in the *Functional Block Diagram*, is an operational amplifier with time-proven current feedback architecture. Advantages of current feedback include no gain bandwidth product limitations, fast slew rate, high large signal bandwidth and excellent distortion performance at high frequencies and large amplitudes. Common applications for current feedback operational amplifiers include coaxial cable drivers, ADC drivers, video amplifiers and high frequency gain blocks.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Wideband Current Feedback Operation

The OPA695 provides a new level of performance in wideband current feedback operational amplifiers. Nearly constant AC performance over a wide gain range, along with 4300-V/μs slew rate, gives a lower power and cost solution for high-intercept IF amplifier requirements. While optimized at a gain of +8 V/V (12 dB to a matched 50-Ω load) to give 450-MHz bandwidth, applications from gains of 1 to 40 can be supported. As a gain of +2 video line driver, the bandwidth extends to 1.4 GHz with a slew rate to support the highest pixel rates. At gains above 20, the signal bandwidth starts to decrease, but still exceeds 180 MHz up to a gain of 40 V/V (26 dB to a matched 50-Ω load). Single +5-V supply operation is also supported with similar bandwidths but reduced output power capability. For lower speed (< 250-MHz) requirements with higher output powers, consider the OPA691.

Figure 48 shows the DC-coupled, gain of +8 V/V, dual-power supply circuit used as the basis of the ±5-V Specifications and Typical Characteristic curves. For test purposes, the input impedance is set to 50 Ω with a resistor to ground, and the output impedance is set to 50 Ω with a series output resistor. Voltage swings reported in the specifications are taken directly at the input and output pins, while load powers (dBm) are defined at a matched 50-Ω load. For the circuit of Figure 48, the total effective load is 100 Ω || 458 Ω = 82 Ω. The disable control line ($\overline{\text{DIS}}$) is typically left open for normal amplifier operation. The disable line must be asserted low to shut off the OPA695. One optional component is included in Figure 48. In addition to the usual power supply decoupling capacitors to ground, a 0.01-μF capacitor is included between the two power supply pins. In practical PCB layouts, this optional added capacitor typically improves the 2nd-harmonic distortion performance by 3 dB to 6 dB for bipolar supply operation.

Figure 49 shows the DC-coupled, gain of –8 V/V, dual-power supply circuit used as the basis of the Inverting Typical Characteristic curves. Inverting operation offers several performance benefits. Because there is no common-mode signal across the input stage, the slew rate for inverting operation is higher and the distortion performance is slightly improved. An additional input resistor, R_T, is included in Figure 49 to set the input impedance equal to 50 Ω. The parallel combination of R_T and R_G set the input impedance. Both the non-inverting

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Feature Description (continued)

and inverting applications of Figure 48 and Figure 49 benefit from optimizing the feedback resistor (R_F) value for bandwidth (see the discussion in *Setting Resistor Values to Optimize Bandwidth*). The typical design sequence is to select the R_F value for best bandwidth, set R_G for the gain, then set R_T for the desired input impedance. As the gain increases for the inverting configuration, a point is reached where R_G equals 50 Ω, where R_T is removed, and the input match is set by R_G only. With R_G fixed to achieve an input match to 50 Ω, R_F is increased to increase gain. This quickly reduces the achievable bandwidth, as shown by the inverting gain of –16 frequency response in the Typical Characteristic curves. For gains > 10 V/V (14 dB at the matched load), noninverting operation is recommended to maintain broader bandwidth.

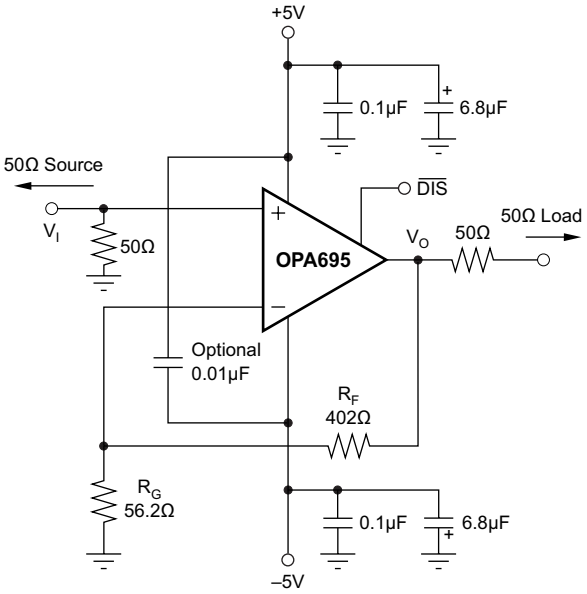


Figure 48. DC-Coupled, G = +8 V/V, Bipolar Supply Specifications and Test Circuit

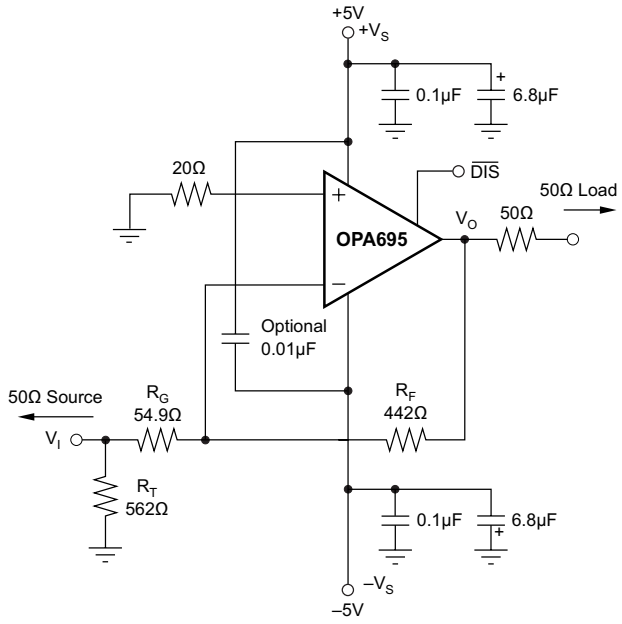


Figure 49. DC-Coupled, G = –8 V/V, Bipolar Supply Specifications and Test Circuit

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Feature Description (continued)

Figure 50 shows the AC-coupled, single +5-V supply, gain of +8 V/V circuit configuration used as a basis for the +5V-only Specifications and Typical Characteristic curves. The key requirement for broadband single-supply operation is to maintain input and output signal swings within the useable voltage ranges at both the input and the output. The circuit of Figure 50 establishes an input midpoint bias using a simple resistive divider from the +5-V supply (two 806-Ω resistors) to the noninverting input. The input signal is then AC-coupled into this midpoint-voltage bias. The input voltage can swing to within 1.6 V of either supply pin, giving a 1.8-V_{PP} input signal range centered between the supply pins. The input impedance matching resistor (57.6 Ω) used in Figure 50 is adjusted to give a 50-Ω input match when the parallel combination of the biasing divider network is included. The gain resistor (R_G) is AC-coupled, giving the circuit a DC gain of +1. This puts the input DC bias voltage (2.5 V) on the output as well. The feedback resistor value has been adjusted from the bipolar supply condition to re-optimize for a flat frequency response in +5 V only, gain of +8 operation (see *Setting Resistor Values to Optimize Bandwidth*). On a single +5-V supply, the output voltage can swing to within 1.0 V of either supply pin while delivering more than 90-mA output current, giving 3-V output swing into 100 Ω (7-dBm maximum at the matched load). The circuit in Figure 50 shows a blocking capacitor driving into a 50-Ω output resistor, then into a 50-Ω load. Alternatively, the blocking capacitor could be removed with the load tied to a supply midpoint, or to ground if the DC current required by this grounded load is acceptable.

Figure 51 shows the AC-coupled, single +5-V supply, gain of –8 V/V circuit configuration used as a basis for the +5V-only Typical Characteristic curves. In this case, the midpoint DC bias on the noninverting input is also de-coupled with an additional 0.1-µF decoupling capacitor. This reduces the source impedance at higher frequencies for the noninverting input bias current noise. This 2.5-V bias on the noninverting input pin appears on the inverting input pin and, because R_G is DC-blocked by the input capacitor, also appears at the output pin. One advantage to inverting operation is that as there is no signal swing across the input stage, higher slew rates and operation to lower supply voltages are possible. To retain a 1-V_{PP} output capability, operation down to a 3-V supply is allowed. At a +3-V supply, the input common mode range is 0 V. However, for the inverting configuration of a current feedback amplifier, wideband operation is retained even with the input stage saturated.

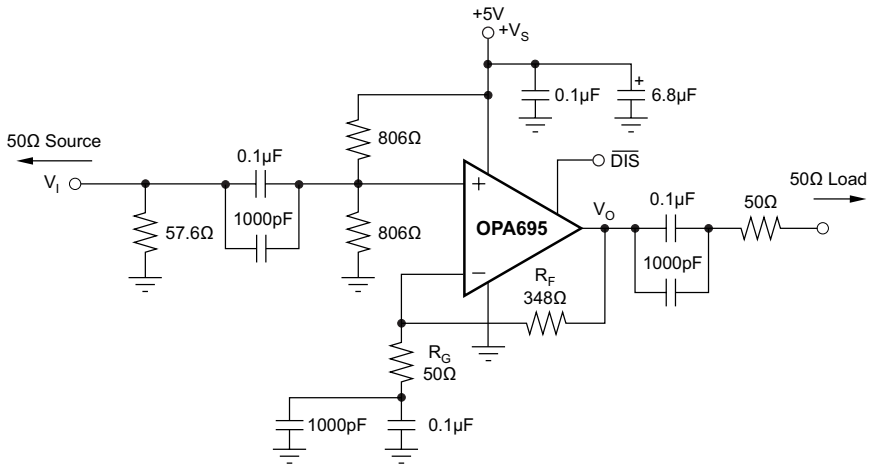


Figure 50. AC-Coupled, G = +8 V/V, Single-Supply Specifications and Test Circuit

Feature Description (continued)

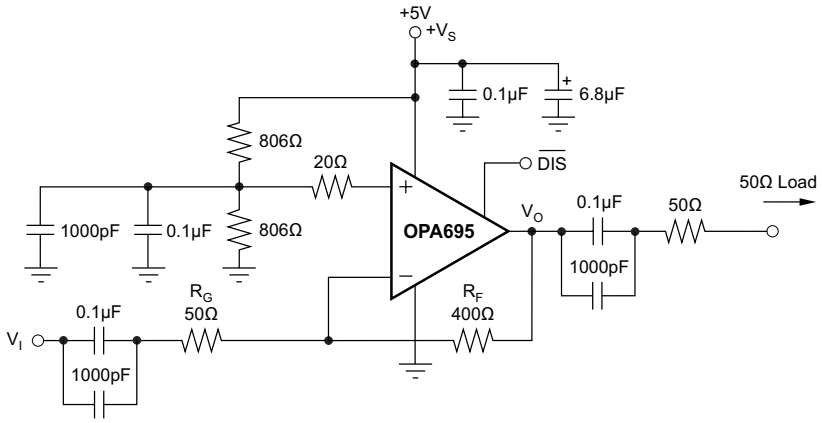


Figure 51. AC-Coupled, G = –8 V/V, Single-Supply Specifications and Test Circuit

The single-supply test circuits of Figure 50 and Figure 51 show +5-V operation. These same circuits can be used over a single-supply range of +5 V to +12 V. Operating on a single +12-V supply, with the Absolute Maximum Supply voltage specification of +13 V, gives adequate design margin for the typical ±5% supply tolerance.

8.3.2 RF Specifications and Applications

The ultra-high, full-power bandwidth and 3rd-order intercept of the OPA695 are ideal for IF amplifier applications. The advantage of a wideband operational amplifier such as the OPA695 include good (and independent) I/O impedance matching, as well as high reverse isolation. A designer accustomed to fixed-gain RF amplifiers will get almost perfect gain accuracy, higher I/O return loss, and 3rd-order intercept points exceeding 30 dBm (up to 110 MHz) using only a 13-mA supply current for the OPA695. Using the considerable design freedom achieved by adjusting the external resistors, the OPA695 can replace a wide range of fixed-gain RF amplifiers with a single part. To understand (in RF amplifier terms) how to take advantage of this, consider first the 4-S parameters (see the example circuits of Figure 48 and Figure 49 on ±5-V supplies, but similar results can be obtained on a single +5-V to +12-V supply).

8.3.3 Input Return Loss (S_{11})

Input return loss is a measure of how closely (over frequency) the input impedance matches the source impedance. This is relatively independent of gain setting for both the noninverting and inverting configurations. The *Typical Characteristics* show the magnitude of S_{11} for the circuits of Figure 48 and Figure 49 through 1 GHz (noninverting gain of +8 and inverting gain of –8 operation, respectively). Noninverting operation offers much better matching to higher frequencies, with the only deviation due to the parasitic input capacitance of the input pin. The noninverting input match is simply set by the resistor to ground on the noninverting input, as the amplifier itself shows a very high input impedance. Inverting operation is also good, but rises more quickly due to loop gain roll-off effects appearing at the inverting node. The inverting mode input match is set by the parallel combination of R_G and R_T in Figure 49, as the inverting amplifier node may be considered a virtual ground. A good, fixed-gain, RF amplifier would have an input, Voltage Standing Wave Ratio (VSWR) < 1.2:1. This corresponds to an S_{11} of –21 dB. The OPA695 exceeds this performance through 100 MHz for the inverting mode of operation, and through 400 MHz for the noninverting mode.

8.3.4 Output Return Loss (S_{22})

Output return loss is a measure of how closely (over frequency) the output impedance matches the load impedance. This is relatively independent of gain setting for both the noninverting and inverting configurations. The output matching impedance, to a first order, is set by adding a series resistor to the low impedance output of the operational amplifier.

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Feature Description (continued)

Because the operational amplifier itself shows a low output impedance that increases with frequency, an improvement in the output match can therefore be obtained by adding a small equalizing capacitor across this output resistor. The *Typical Characteristics* show the measured S_{22} with and without this 2.5-pF capacitor (across the 50-Ω output resistor). Again, a good match for a fixed-gain RF amplifier would give a VSWR of 1.2:1 (S_{22} < –21 dB). The Typical Characteristic curves show that a simple 50-Ω output resistor holds better than –21 dB to 140 MHz, but up to 380 MHz with the tuning capacitor.

8.3.5 Forward Gain (S_{21})

In all high-speed amplifier data sheets, forward gain is the small signal gain plotted over frequency. The difference between noninverting and inverting operation is that the phase of S_{21} starts out at 0° for the noninverting and –180° for the inverting. This initial phase shift for inverting mode is inconsequential to most IF strip applications. The phase of S_{21} was not shown in *Typical Characteristics*, but is linear with frequency and may be accurately modeled as a constant time delay through the amplifier.

The *Typical Characteristics* show S_{21} over a range of signal gains, where the external resistors have been adjusted to re-optimize flatness at each gain setting. Because this is a current feedback operational amplifier, the signal bandwidth can be held relatively constant as the desired gain setting is changed. The plot of the noninverting bandwidth versus gain shows some change in bandwidth versus gain (due to parasitic capacitive effects on the inverting node) with very little change showing up for the inverting mode of operation.

Signal gains are most often referred to as V/V in operational amplifier data sheets. This is the voltage gain from input to output and is set by external resistor ratios. Because the output impedance is set by a physical series resistor, the voltage gain to the matched load is cut in half by this resistor divider. The log gain to the matched load for the noninverting circuit of Figure 48 is:

$$G^{+} = 20\log\frac{1}{2}\left(1+\frac{R_F}{R_G}\right)\text{dB} \quad (1)$$

The log gain to the matched load for the inverting circuit of Figure 49 is:

$$G^{-} = 20\log\frac{1}{2}\left(\frac{R_F}{R_G}\right)\text{dB} \quad (2)$$

The specific resistor values used in Figure 48 and Figure 49 give both a maximally-flat bandwidth and a 12-dB gain to the matched load. The design tables located in the *Noise Figure* section summarize the required resistor values over a range of desired gains for the circuits of Figure 48 and Figure 49.

As the desired signal gain increases, the achievable bandwidths decrease. In the noninverting case, it decreases relatively quickly as shown in *Typical Characteristics*. The inverting configuration holds almost constant bandwidth (with correctly selected external resistor values) until R_G reduces to equal 50 Ω, and remains at that value to satisfy the input impedance matching requirement, with further increases in gain achieved by increasing R_F in Figure 49. The bandwidth then decreases rapidly as shown by the gain of –16 V/V plot in *Typical Characteristics*.

8.3.6 Reverse Isolation (S_{12})

Reverse isolation is a measure of how much power injected into the output pin returns to the source. This is rarely specified for an operational amplifier because operational amplifiers are nearly uni-directional signal devices. Below 300 MHz, the noninverting configuration of Figure 48 gives much better isolation than the inverting of Figure 49. Both are well below 40-dB isolation through 350 MHz.

8.3.7 Limits to Dynamic Range

The next set of considerations for RF amplifier applications are the defined limits to dynamic range. Typical fixed-gain RF amplifiers include:

- –1-dB compression (a measure of maximum output power)
- Two-tone, 3rd-order, output intermodulation intercept (a measure of achievable spurious-free dynamic range)
- Noise figure (a measure of degradation in signal to noise ratio in passing through the amplifier)

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Feature Description (continued)

8.3.7.1 –1-dB Compression

The definition for –1-dB compression power is output power where the actual power is 1 dB less than the input power, plus the log gain. In classic RF amplifiers, this is typically 10 dB less than the 3rd-order intercept. That relationship does not hold for operational amplifiers, as their intercept is improved by loop gain to be far more than 10 dB higher than the –1-dB compression. A simple estimate for –1-dB compression for the OPA695 is the maximum non-slew limited output voltage swing available at the matched load, converted into a power with 1 dB added to satisfy the definition. For the OPA695 on ±5-V supplies, its output will deliver approximately ±4.0 V at the output pin or ±2.0 V at the matched load. The conversion from V_{PP} to power (for a sine wave) is:

$$P_O(\text{dBm}) = 10 \log \left[\frac{\left(\frac{V_{PP}}{2\sqrt{2}}\right)^2}{0.001(50\Omega)} \right] \quad (3)$$

Converting this 4.0-V_{PP} swing at the load to dBm gives 16 dBm; adding 1 dB to this (to satisfy the definition) gives a –1-dB compression of 17 dBm for the OPA695 operating on ±5-V supplies. This is a good estimate for frequencies that require less than the full slew rate of the OPA695.

The maximum frequency of operation given an available slew rate and desired peak output swing (at the output pin for a sine wave) is:

$$F_{MAX} = \frac{\text{Slew Rate}}{2\pi V_p(0.707)} \quad (4)$$

Putting in the 4600-V/µs slew rate available in the inverting mode of operation and the 4.0-V peak output swing at the output pin gives a maximum frequency of 259 MHz. This is the maximum frequency where the –1-dB compression would be 17 dBm at the matched load. Higher useable bandwidths are possible at lower output powers, as shown in the Large Signal Bandwidth curves. As those graphs show, 7-V_{PP} outputs are possible with almost perfect frequency response flatness through 100 MHz for both non-inverting or inverting operation.

8.3.7.2 Two-Tone 3rd-Order Output Intermodulation Intercept (OP_3)

In narrowband IF strips, each amplifier typically feeds into a bandpass filter that attenuates most harmonic distortion terms. The most troublesome remaining distortion is the 3rdorder, two-tone intermodulations that can fall very close (in frequency) to the desired signals and cannot be filtered out. If two test frequencies are defined at $F_O + \Delta F$ and $F_O – \Delta F$, the 3rd-order intermodulation distortion products will fall at $F_O + 3\Delta F$ and $F_O – 3\Delta F$. If the two test power levels (P_T) are equal, the OPA695 produces 3rd-order spurious terms (P_S) at these frequencies, and at a power level below the test power levels given by:

$$P_T – P_S = 2\ (OP_3 – P_T) \quad (5)$$

The 3rd-order intercept plot shown in *Typical Characteristics* shows a very high intercept at low frequencies that decreases with increasing frequency. This intercept is defined at the matched load to allow direct comparison with fixed-gain RF amplifiers. To produce a 2-V_{PP} total two-tone envelope at the matched load, each power level must be 4 dBm at the matched load (1 V_{PP}). Using Equation 5, and the performance curve for inverting operation, at 50 MHz (41.5-dBm intercept) the 3rd-order spurious will be 2 × (41.5 – 4) = 75 dB below these 4-dBm test tones. This is an exceptionally low distortion for an amplifier that only uses 13-mA supply current. Considerable improvement from this level of performance is also possible if the output drives directly into the lighter load of an ADC input.

This very high intercept versus quiescent power is achieved by the high loop gain of the OPA695. This loop gain does, however, decrease with frequency, giving the decreasing OP_3 performance shown in *Typical Characteristics*. Application as an IF amplifier through 200 MHz is possible with output intercepts exceeding 21 dBm at 200 MHz. Intercept performance varies slightly with gain setting, decreasing at higher gains (that is, gains greater than the 8 V/V or 12 dB gain used in the Typical Characteristic curves) and increasing at lower gains.

8.3.7.3 Noise Figure

All fixed-gain RF amplifiers show a very good noise figure (typically < 5 dB). For broadband amplifiers, this is achieved by a low-noise input transistor and an input match set by feedback. This feedback greatly reduces the noise figure for fixed-gain RF amplifiers, but also makes the input match dependent on the load and the output match dependent on the source impedance at the input.

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Feature Description (continued)

The noise figure for an operational amplifier is always higher than for fixed-gain RF amplifiers, due to the more complex internal circuits of an operational amplifier (giving higher input noise voltage and current terms). Also, for simple circuits, the input match is set resistively. What is gained is an almost perfect I/O impedance match, much better load isolation, and very high 3rd-order intercepts versus quiescent power. These higher noise figures can be acceptable if the OPA695 has enough gain preceding it in the IF chain.

Operational amplifier noise figure equations include at least six terms (see *Noise Performance*), due to the external resistors. As a point of reference, the circuit of Figure 48 has an input noise figure of 14 dB, while the inverting configuration of Figure 49 has an input noise figure of 11 dB. At higher gains, it is typical for the inverting noise figure to be slightly better than for an equivalent gain, noninverting configuration. Improve the noise figure for the noninverting configuration of the OPA695 by including a step-up, 1:2 turns ratio transformer at the input. This configuration is shown in Figure 52.

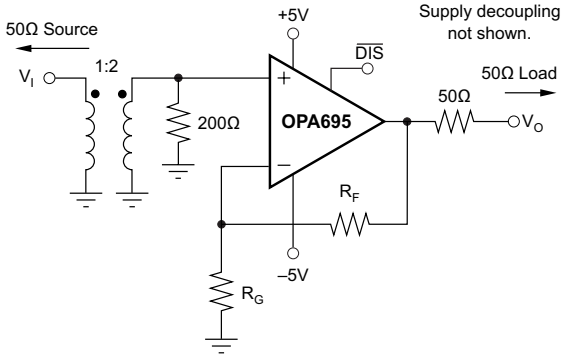


Figure 52. IF Amplifier With Improved Noise Figure

The transformer provides a noiseless voltage gain at the expense of higher source impedance for the OPA695 noninverting input current noise. The input impedance is still set to 50 Ω by the 200-Ω resistor on the transformer secondary. A 1:2 turns ratio transformer will reflect the 200 Ω to the input side as a 50-Ω impedance over the bandwidth of the transformer. Using a 1:2 step-up transformer also reduces the required amplifier gain by 1/2 for any particular desired overall gain.

Table 1, Table 2, and Table 3 summarize the recommended resistor values and resulting noise figures over the desired gain setting for three circuit options for the OPA695 operated as a precision IF amplifier. In each case, R_F and R_G are adjusted for both best bandwidth and required gain.

In all cases, exact computed values for resistors are shown; in an application, pick standard resistor values that are closest to those in the tables.

Table 1. Noninverting Wideband Operational Amplifier

GAIN TO LOAD (dB)	R_F (Ω)	R_G (Ω)	NOISE FIGURE
6	478	159	17.20
7	468	134	16.55
8	458	113	15.95
9	446	96	15.40
10	433	81	14.91
11	419	68	14.47
12	402	57	14.09
13	384	48	13.76
14	363	40	13.23
15	340	33	13.23
16	314	27	13.03
17	284	21	12.86
18	252	16	12.72

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Feature Description (continued)

Table 1. Noninverting Wideband Operational Amplifier (continued)

GAIN TO LOAD (dB)	R_F (Ω)	R_G (Ω)	NOISE FIGURE
19	215	12	12.60
20	174	9	12.51

Table 2. Noninverting With a 1:2 Input Step-Up Transformer

GAIN TO LOAD (dB)	R_F (Ω)	R_G (Ω)	NOISE FIGURE
6	516	518	16.34
7	511	412	15.54
8	506	334	14.78
9	500	275	14.07
10	493	228	13.40
11	486	190	12.78
12	478	160	12.21
13	469	135	11.70
14	458	114	11.25
15	447	96	10.85
16	434	81	10.15
17	419	69	10.21
18	403	58	9.96
19	384	48	9.74
20	364	40	9.57

Table 3. Inverting Wideband RF Amplifier

GAIN TO LOAD (dB)	Optimum R_F (Ω)	R_G (Ω)	Input Match R_T	NOISE FIGURE
6	463.27	116	87	16.94
7	454.61	101	98	16.06
8	444.91	88	114	15.16
9	434.07	77	142	14.23
10	421.95	66	199	13.24
11	408.42	57	380	12.16
12	398.11	50	Infinite	11.03
13	446.68	50	Infinite	10.92
14	501.19	50	Infinite	10.83
15	562.34	50	Infinite	10.75
16	630.96	50	Infinite	10.67
17	707.95	50	Infinite	10.61
18	794.33	50	Infinite	10.55
19	891.25	50	Infinite	10.49
20	1000.00	50	Infinite	10.45

8.4 Device Functional Modes

The OPA695 has two functional modes. The first functional mode is accessed by applying a logic 1 (>3.3 V) to the not Disable (Disable bar) pin. In this mode the amplifier is fully enabled and will draw a supply current of 13 mA.

The second functional mode is the disabled state. The disabled state is accessed by applying a logic 0 (<1.8 V) to the not Disable pin. In this mode, the amplifier is fully disabled and draws a current of only 100 µA.

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9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

9.1.1 SAW Filter Buffer

One common requirement in an IF strip is to buffer the output of a mixer with enough gain to recover the insertion loss of a narrowband SAW filter. Figure 65 shows one possible configuration driving a SAW filter. Figure 53 shows the intercept at the 50-Ω load. Operating in the inverting mode at a voltage gain of –8 V/V, this circuit provides a 50-Ω input match using the gain set resistor, has the feedback optimized for maximum bandwidth (700 MHz in this case), and drives through a 50-Ω output resistor into the matching network at the input of the SAW filter. If the SAW filter gives a 12-dB insertion loss, a net gain of 0 dB to the 50-Ω load at the output of the SAW (which could be the input impedance of the next IF amplifier or mixer) is delivered in the passband of the SAW filter. Using the OPA695 in this application isolates the first mixer from the impedance of the SAW filter and provides very low two-tone, 3rd-order spurious levels in the SAW filter bandwidth. Inverting operation gives the broadest bandwidth up to a gain of –12 V/V (15.6 dB). Noninverting operation gives higher bandwidth at gain settings higher than this, but will also give a slight reduction in intercept and noise figure performance.

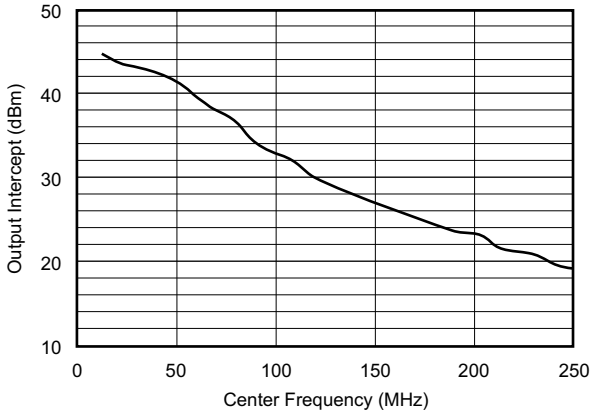


Figure 53. 2-Tone, 3rd-Order Intermodulation Intercept

9.1.2 LO Buffer Amplifier

The OPA695 can also be used to buffer the Local Oscillator (LO) from the mixer. Operating at a voltage gain of +2, the OPA695 provides almost perfect load isolation for the LO, with a net gain of 0 dB to the mixer. Applications through 1.4-GHz LOs may be considered, but best operation would be for LOs < 1.0 GHz at a gain of +2. Gain can also be provided by the OPA695 to drive higher power levels into the mixer. One option for the OPA695 as an LO buffer is shown in Figure 54. Because the OPA695 can drive multiple output loads, two identical LO signals may be delivered to the mixers in a diversity receiver by tapping the output off through two series 50-Ω output resistors. This circuit is set up for a voltage gain of +2 V/V to the output pin for a gain of +1 V/V (0 dB) to the mixers, but could easily be adjusted to deliver higher gains as well.

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Application Information (continued)

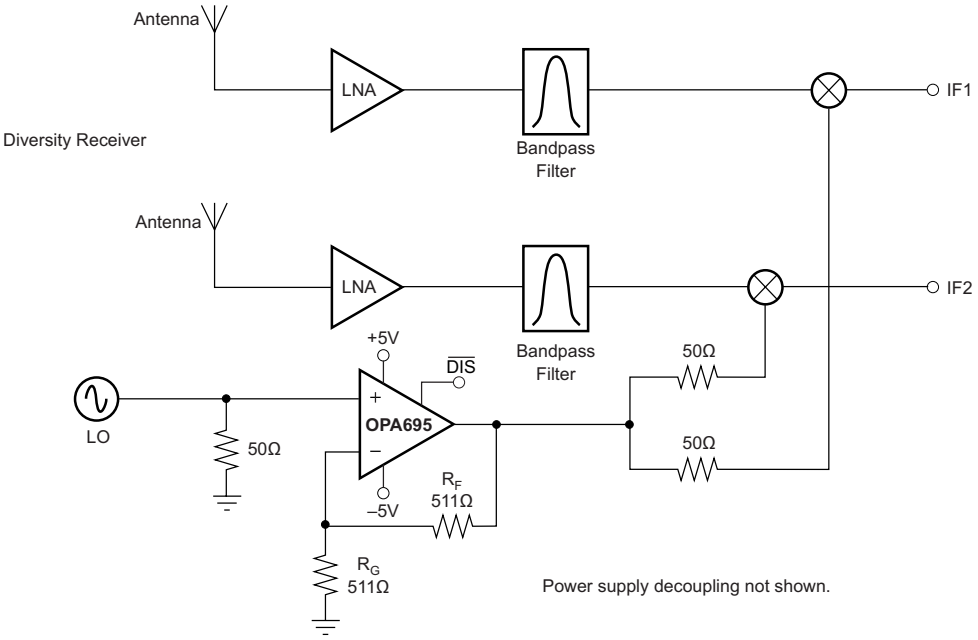


Figure 54. Dual Output LO Buffer

9.1.3 Wideband Cable Driving Applications

The high slew rate and bandwidth of the OPA695 can be used to meet the most demanding cable driving applications.

9.1.3.1 Cable Modem Return Path Driver

The standard cable modem upstream driver is typically required to drive high power over a 5-MHz to 65-MHz bandwidth while delivering < –50-dBc distortion. Highly-integrated solutions (including programmable gain stages) often fall short of this target due to high losses from the amplifier output to the line. The higher gain-operating capability of the OPA695 and its very high slew rate provide a low-cost solution for delivering this signal with the required spurious-free dynamic range. Figure 55 shows one example of using the OPA695 as an upstream driver for a cable modem return path. In this case, the input impedance of the driver is set to 75 Ω by the gain resistor (R_G). The required input level from the adjustable gain stage is significantly reduced by the 15.5-dB gain provided by the OPA695. In this example, the physical 75-Ω output matching resistor, along with the 3-dB loss in the diplexer, attenuate the output swing by 9 dB on the line. In this example, a single +12-V supply was used to achieve the lowest harmonic distortion for the 6-V_{PP} output pin voltage through 65 MHz. Measured performance for this example gave 600-MHz small-signal bandwidth and < –54-dBc distortion through 65 MHz for a 6-V_{PP} output pin voltage swing.

An alternative to this circuit that gives even lower distortion is a differential driver using two OPA695s driving into an output transformer. This can be used either to double the available line power, or to improve distortion by cutting the required output swing in half for each stage. The channel disable required by the MCNS specification must be implemented by using the PGA disable feature. The MCNS disable specification requires that an output impedance match be maintained with the signal channel shut off. The disable feature of the OPA695 is intended principally for power savings and puts the output and inverting input pins into a high impedance mode. This does not maintain the required output-impedance matching. Turning off the signal at the input of Figure 55, while keeping the OPA695 active, maintains the impedance matching while putting very little noise on the line. The line noise in disable for the circuit of Figure 55 (with the PGA source turned off, but still presenting a 75-Ω source impedance) will be a very low 4 nV/√Hz (–157 dBm/Hz) due to the low input noise of the OPA695.

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Application Information (continued)

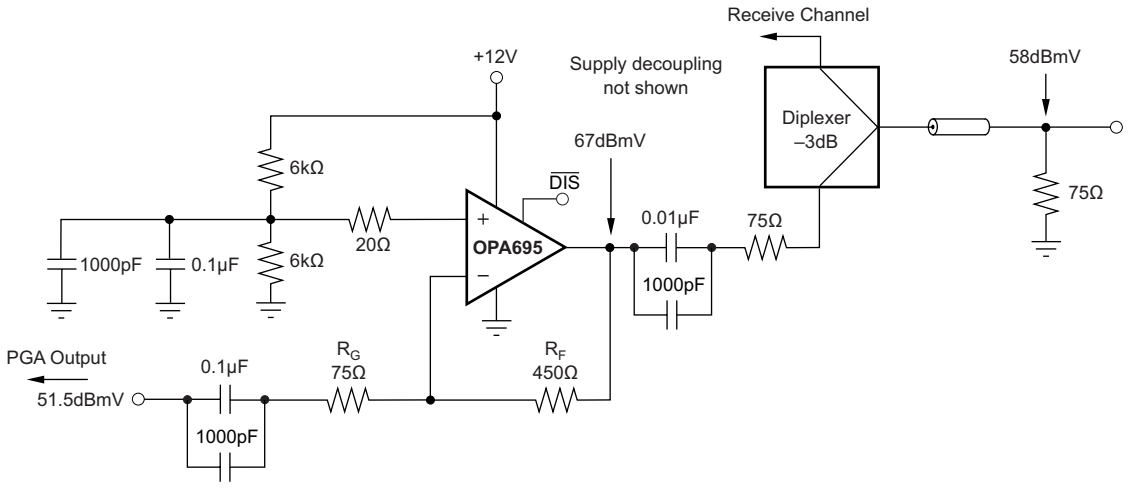


Figure 55. Cable Modem Upstream Driver

9.1.3.2 RGB Video Line Driver

The extremely high bandwidth of the OPA695 operating at a gain of +2 supports the fastest RAMDAC outputs for applications such as auxiliary monitor driving. *Gain 2V/V Video Line Driver* shows measured performance for a 0 → +1-V input square wave at 125 MHz. As a general rule, the required full-power bandwidth for the amplifier must be at least one-half the pixel rate. With its noninverting gain of +2, slew rate of 2900 V/µs, and a 1.4-V_{PP} output pin voltage swing for standard RGB video levels, the OPA695 gives a bandwidth of 600 MHz, which then supports up to 1.26-GHz pixel rates. Figure 56 shows an example where three OPA695s provide an auxiliary monitor output for a highresolution RGB RAMDAC.

An alternative circuit that takes advantage of the higher inverting slew rate of the OPA695 (4300 V/µs) takes the complementary current output from the RAMDAC and converts it to positive video to give a very high, full-power bandwidth RGB line driver. This will give sharper pixel edges than the circuit of Figure 56. Most high-speed DACs are current-steering designs with both an output current signal used for the video, and a complementary output that is typically discarded into a matching resistor. The complementary current output can be used as an auxiliary output if it is inverted, as shown in Figure 57. In the circuit of Figure 57, the complementary current output is terminated by an equivalent 75-Ω impedance (the parallel combination of R_T and R_G) that also provides a current division to reduce the signal current through the feedback resistor, R_F. This allows R_F to be increased to a value which holds a flat frequency response. Since the complementary current output is essentially an inverted video signal, this circuit sets up a white video level at the output of the OPA695 for zero DAC output current (using the 0.77-V DC bias on the noninverting input), then inverts the complementary output current to produce a signal that ranges from this 1.4 V at zero output current down to 0 V at maximum output current level (assuming a 20-mA maximum output current). This gives a very wideband (> 800-MHz) video signal capability.

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Application Information (continued)

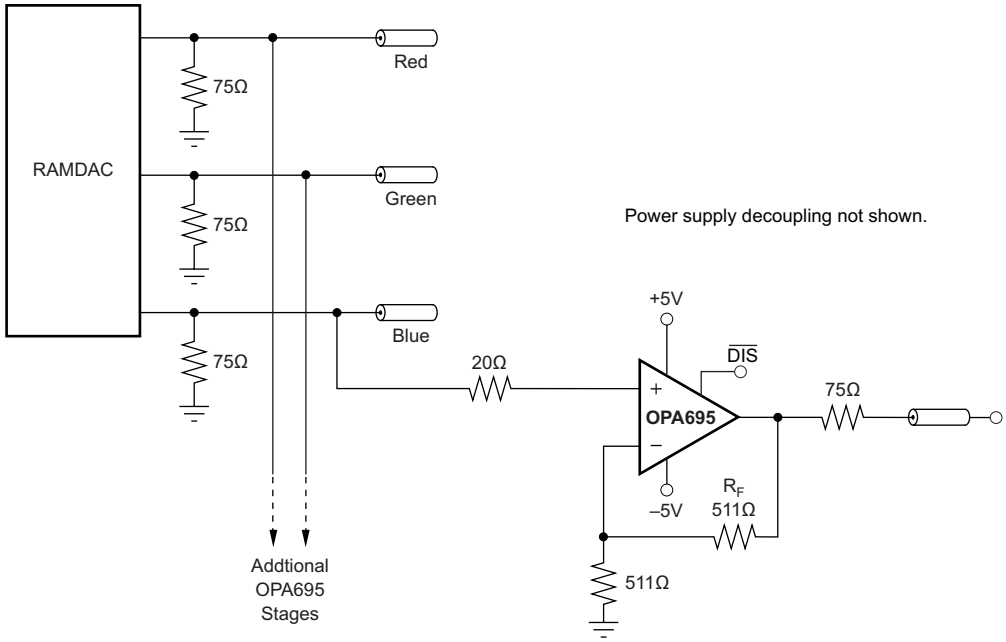


Figure 56. Gain of +2, High-Resolution RGB Monitor Output

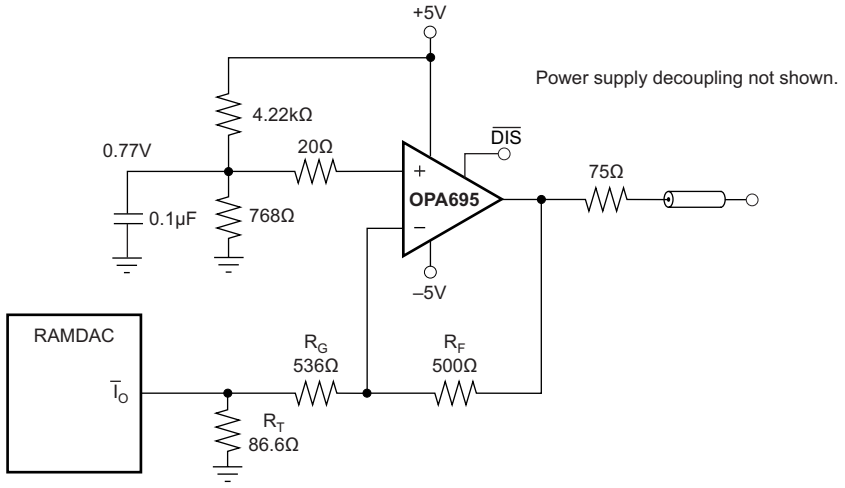


Figure 57. High-Resolution RGB Driver Using DAC Complementary Output Current

9.1.3.3 Arbitrary Waveform Driver

The OPA695 can be used as the output stage for moderate output power arbitrary waveform driver applications. Driving out through a series 50-Ω matching resistor into a 50-Ω matched load allows up to a 4.0-V_{PP} swing at the matched load (15 dBm) when operating the OPA695 on a ±5-V power supply. This level of power is available for gains of either ±8 with a flat response through 100 MHz. When interfacing directly from a complementary current output DAC, consider the circuit of Figure 57, modified for the peak output currents of the particular DAC being considered. Where purely AC-coupled output signals are required from a complementary current output DAC, consider a push-pull output stage using the circuit of Figure 58. The resistor values here have been calculated for a 20-mA peak output current DAC, which produces up to a 5-V_{PP} swing at the matched load (18 dBm). This approach gives higher power at the load, with lower 2nd-harmonic distortion.

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Application Information (continued)

For a 20-mA peak output current DAC, the mid-scale current of 10 mA gives a 2-V DC output common-mode operating voltage, due to the 200-Ω resistor to ground at the outputs. The total AC impedance at each output is 50 Ω, giving a ±0.5-V swing around this 2-V common-mode voltage for the DAC. These resistors also act as a current divider, sending 75% of the DAC output current through the feedback resistor (464 Ω). The blocking capacitor references the OPA695 output voltage to ground, and turns the unipolar DAC output current into a bipolar swing of 0.75 × 20 mA × 464 Ω = 7 V_{PP} at each amplifier output. Each output is exactly 180° out-of-phase from the other, producing double 7 V_{PP} into the matching resistors. To limit the peak output current and improve distortion, the circuit of Figure 58 is set up with a 1.4:1 stepdown transformer. This reflects the 50-Ω load to be 100 Ω at the primary side of the transformer. For the maximum 14-V_{PP} swing across the outputs of the two amplifiers, the matching resistors will drop this to 7 V_{PP} at the input of the transformer, then down to 5-V_{PP} maximum at the 50-Ω load at the output of the transformer. This step-down approach reduces the peak output current to 14 V_P/(200 Ω) = 70 mA.

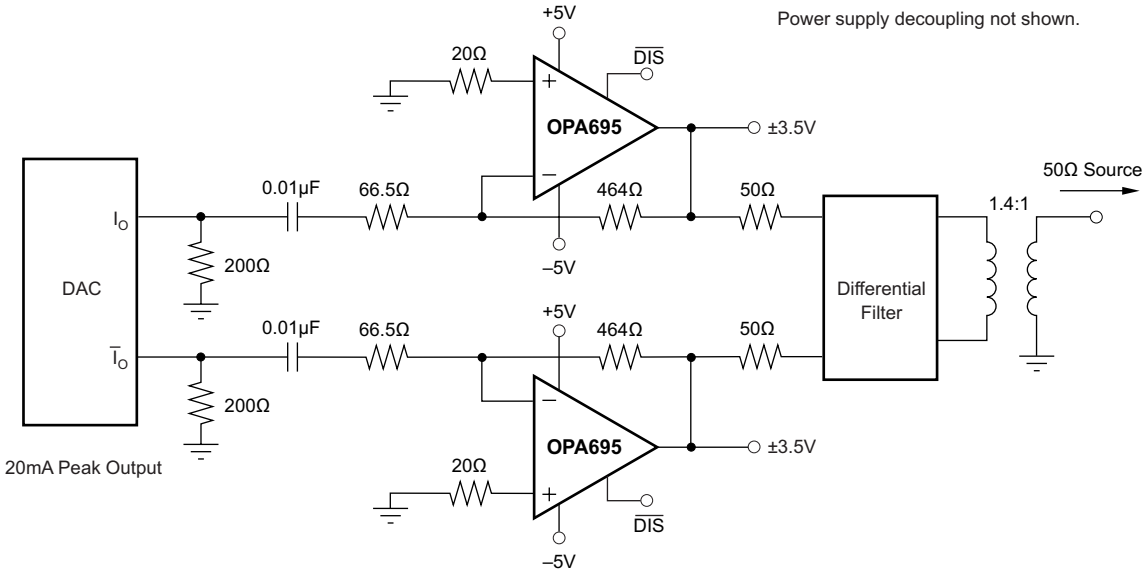


Figure 58. High Power, Wideband AC-Coupled Arbitrary Waveform Driver

9.1.4 Differential I/O Applications

The OPA695 offers very low 3rd-order distortion terms with a dominant 2nd-order distortion for the single amplifier operation. For the lowest distortion, particularly where differential outputs are needed, operating two OPA695s in a differential I/O design suppresses these even-order terms, delivering extremely low harmonic distortion through high frequencies and powers. Differential outputs are often preferred for high performance ADCs, twisted-pair driving, and mixer interfaces. Two basic approaches to differential I/Os are the noninverting or inverting configurations. Because the output is differential, the signal polarity is somewhat meaningless; the noninverting and inverting terminology applies here to where the input is brought into the two OPA695s. Each approach has its advantages and disadvantages. Figure 59 shows a basic starting point for non-inverting differential I/O applications.

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Application Information (continued)

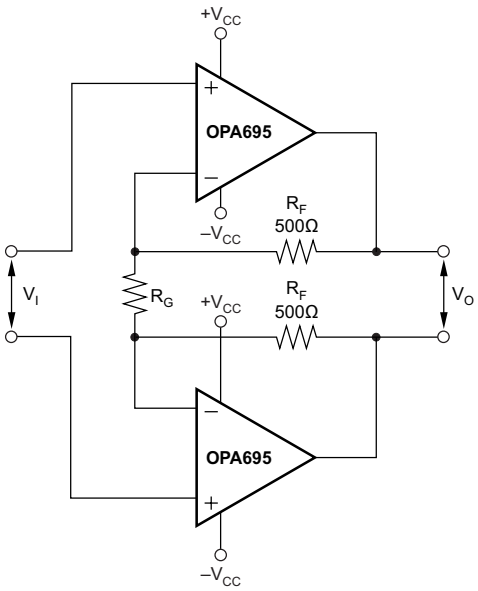


Figure 59. Noninverting Input Differential I/O Amplifier

This approach allows for a source termination impedance independent of the signal gain. For instance, simple differential filters may be included in the signal path right up to the non-inverting inputs without interacting with the gain setting. The differential signal gain for the circuit of Figure 59 is:

$$A_D = 1 + 2 \times R_F/R_G \quad (6)$$

Because the OPA695 is a current feedback amplifier, its bandwidth is principally controlled with the feedback resistor value: Figure 59 shows a typical value of 500 Ω. However, the differential gain may be adjusted with considerable freedom using just the R_G resistor. R_G can be a reactive network providing an isolated shaping to the differential frequency response. AC-coupled applications often include a blocking capacitor in series with R_G. This reduces the gain to 1 at low frequency, rising to the A_D expression shown above at higher frequencies. The noninverting input approach of Figure 59 can be used for higher gains than the inverting input approach, but may have a reduced full-power bandwidth due to the lower slew rate of the OPA695 running a noninverting versus inverting input mode of operation.

Various combinations of single-supply or AC-coupled gain can also be delivered using the basic circuit of Figure 59. Common-mode bias voltages on the two noninverting inputs pass on to the output with a gain of 1, as an equal DC voltage at each inverting node creates no current through R_G. This circuit shows a common-mode gain of 1 from input to output. The source connection must either remove this common-mode signal if it is unnecessary (using an input transformer), or the common-mode voltage at the inputs can set the output common-mode bias. If the low common-mode rejection of this circuit is a problem, the output interface may also be used to reject that common-mode. For instance, most modern differential input ADCs reject common-mode signals well, while a line driver application through a transformer also removes the common-mode signal at the secondary of the transformer.

Figure 60 shows a differential I/O stage configured as an inverting amplifier. In this case, the gain resistors (R_G) become part of the input resistance for the source. This provides a better noise performance than the non-inverting configuration, but limits the flexibility in setting the input impedance separately from the gain.

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Application Information (continued)

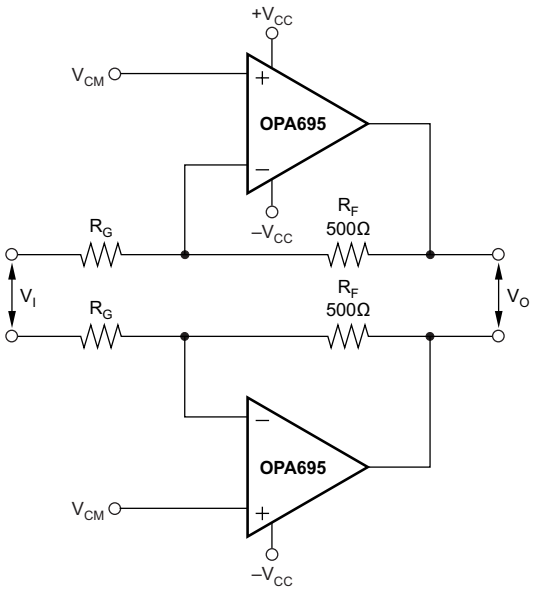


Figure 60. Inverting Input Differential I/O Amplifier

The two noninverting inputs provide an easy common-mode control input, particularly if the source is AC-coupled through either blocking caps or a transformer. In either case, the common-mode input voltages on the two noninverting inputs again have a gain of 1 to the output pins, giving easy common-mode control for single-supply operation. The OPA695 in this configuration constrains the feedback to the 500-Ω region for best frequency response. With R_F fixed, the input resistors may be adjusted to the desired gain, but will also be changing the input impedance. The high-frequency common-mode gain for this circuit from input to output is the same as for the signal gain. Again, if the source might include an undesired common-mode signal, that could be rejected at the input using blocking caps (for low-frequency and DC common-mode) or a transformer coupling. The differential performance plots shown in the Typical Characteristics used the configuration of Figure 60 and an input 1:1 transformer. The differential signal gain in the circuit of Figure 60 is:

$$A_D = R_F/R_G \quad (7)$$

Using this configuration suppresses the 2nd-harmonics, leaving only 3rd-harmonic terms as the limit to output SFDR. The higher slew rate of the inverting configuration also extends the full-power bandwidth and the range of low intermodulation distortion over the performance bandwidth available from the circuit of Figure 59. The Typical Characteristics show that the circuit of Figure 60 operating at an A_D = 10 can deliver a 16 V_{PP} signal with over 500-MHz –3-dB bandwidth. Using Equation 4, this implies a differential output slew of 18000 V/µsec, or 9000 V/µsec at each output. This output slew rate is far higher than specified, and probably due to the lighter load used in the differential tests.

This inverting input differential configuration is suited to high SFDR converter interfaces, specifically narrowband IF channels. The Typical Characteristics show the 2-tone, 3rd-order intermodulation intercept exceeding 45 dBm through 90 MHz. Although this data was taken with an 800-Ω load, the intercept model appears to work for this circuit, treating the power level as if it were into 50 Ω. For example, at 70 MHz, the differential Typical Characteristic plots show a 48 dBm intercept. To predict the 2-tone intermodulation SFDR, assuming a –1-dB below full-scale envelope to a 2-V_{PP} maximum differential input converter, the test power level would be 9 dBm – 6 dBm = 3 dBm for each tone. Putting this into the intercept equation, gives:

$$\Delta dBc = 2 \times (48 - 3) = 90\ dBc \quad (8)$$

The single-tone distortion data shows approximately 72-dB SFDR at 70 MHz for a 2-V_{PP} output into this light 800-Ω load. A modest post filter after the amplifier can reduce these harmonics (2nd at 140 MHz, 3rd at 210 MHz) to the point where the full SFDR to a converter can be in the 85-dB range for a 70-MHz IF operation.

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Application Information (continued)

9.1.5 Operating Suggestions

9.1.5.1 Setting Resistor Values to Optimize Bandwidth

A current-feedback operational amplifier such as the OPA695 can hold an almost constant bandwidth over signal gain settings with the proper adjustment of the external resistor values. This is shown in *Typical Characteristics*. The small-signal bandwidth decreases only slightly with increasing gain. These curves also show that the feedback resistor has been changed for each gain setting. The resistor values on the inverting side of the circuit for a current-feedback operational amplifier can be treated as frequency response compensation elements, while their ratios set the signal gain. Figure 15 shows the analysis circuit for the OPA695 small-signal frequency response.

The key elements of this current feedback operational amplifier model are:

- α ⇒ Buffer gain from the noninverting input to the inverting input.
- R_I ⇒ Buffer output impedance
- i_{ERR} ⇒ Feedback error current signal
- Z(s) ⇒ Frequency-dependent, open-loop transimpedance gain from i_{ERR} to V_O

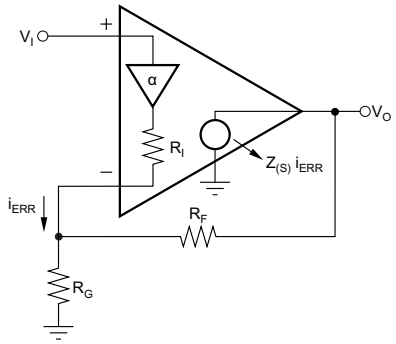


Figure 61. Current-Feedback Transfer Function Analysis Circuit

The buffer gain is typically very close to 1.00 and is normally neglected from signal gain considerations. It will, however, set the CMRR for a single operational amplifier differential amplifier configuration. For the buffer gain α < 1.0, the CMRR = –20 × log (1 – α).

R_I, the buffer output impedance, is a critical portion of the bandwidth control equation. For the OPA695, it is typically about 28 Ω for ±5-V operation, and 31 Ω for single +5-V operation.

A current-feedback operational amplifier senses an error current in the inverting node (as opposed to a differential input error voltage for a voltage-feedback operational amplifier) and passes this on to the output through an internal frequency-dependent transimpedance gain. *Typical Characteristics* show this open-loop transimpedance response. This is analogous to the open-loop voltage gain curve for a voltage-feedback operational amplifier. Developing the transfer function for the circuit of Figure 64 gives Equation 9:

$$\frac{V_O}{V_I} = \frac{\alpha\left(1+\frac{R_F}{R_G}\right)}{1+\frac{R_F+R_I\left(1+\frac{R_F}{R_G}\right)}{Z_{(S)}}} = \frac{\alpha \bullet NG}{1+\frac{R_F+R_I \bullet NG}{Z_{(S)}}}$$

where

- $NC = 1 + R_F/R_G$ = Noise Gain (9)

This is written in a loop gain analysis format, where the errors arising from a non-infinite open-loop gain are shown in the denominator. If Z(s) were infinite over all frequencies, the denominator of Equation 9 would reduce to 1, and the ideal desired signal gain shown in the numerator would be achieved. The fraction in the denominator of Equation 9 determines the frequency response. Equation 10 shows this as the loop gain equation:

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Application Information (continued)

$$\frac{Z_{(S)}}{R_F + R_I \bullet NG} = \text{Loop Gain} \tag{10}$$

If 20 × log (R_F + NG × R_I) were superimposed on the open-loop transimpedance plot, the difference between the two would be the loop gain at a given frequency. Eventually, Z(s) rolls off to equal the denominator of Equation 10, at which point the loop gain has reduced to 1 (and the curves have intersected). This point of equality is where the amplifier closed-loop frequency response given by Equation 9 starts to roll off, and is exactly analogous to the frequency at which the noise gain equals the open-loop voltage gain for a voltage-feedback operational amplifier. The difference is that the total impedance in the denominator of Equation 10 may be controlled separately from the desired signal gain (or NG).

The OPA695 is internally compensated to give a maximally flat frequency response for R_F = 402 Ω at NG = 8 on ±5-V supplies. Evaluating the denominator of Equation 7 (the feedback transimpedance) gives an optimal target of 663 Ω. As the signal gain changes, the contribution of the NG ×R_I term in the feedback transimpedance changes, but the total can be held constant by adjusting R_F. Equation 11 gives an approximate equation for optimum R_F over signal gain:

$$R_F = 663\ \Omega - NG \times R_I \tag{11}$$

As the desired signal gain increases, this equation will eventually predict a negative R_F. A subjective limit to this adjustment can be set by holding R_G to a minimum value of 10 Ω. Lower values will load both the buffer stage at the input and the output stage if R_F gets too low, decreasing the bandwidth. Figure 62 shows the recommended R_F versus NG for both ±5 V and a single +5-V operation. The optimum target feedback impedance for +5-V operation used in Equation 8 is 663 Ω, while the typical buffer output impedance is 32 Ω. The values for R_F versus gain shown are approximately equal to the values used to generate the typical characteristic curves. In some cases, the values used differ slightly from that shown here, in that the values used in the typical characteristics are also correcting for board parasitics not considered in the simplified analysis leading to Equation 11. The values shown in Figure 62 give a good starting point for designs where bandwidth optimization is desired and a flat frequency response is needed.

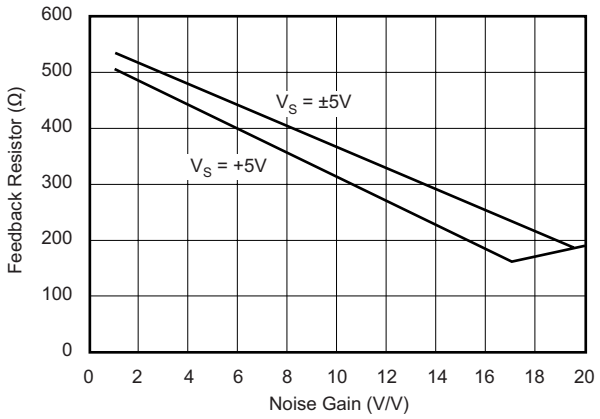


Figure 62. Recommended Feedback Resistor vs Noise Gain

The total impedance presented to the inverting input can adjust the closed-loop signal bandwidth. Inserting a series resistor between the inverting input and the summing junction increases the feedback impedance (denominator of Equation 10), decreasing the bandwidth. The internal buffer output impedance for the OPA695 is slightly influenced by the source impedance looking out of the noninverting input terminal. High source resistors increase R_I, decreasing the bandwidth. For those single-supply applications which develop a midpoint bias at the non-inverting input through high-valued resistors, the decoupling capacitor is essential for power-supply ripple rejection, non-inverting input noise current shunting, and minimizing the high-frequency value for R_I in Figure 61.

Inverting feedback optimization is complicated by the impedance matching requirement at the input, as shown in Figure 49. The resistor values shown in Table 3 must be used in this case.

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Application Information (continued)

9.1.5.2 Output Current and Voltage

The OPA695 provides output voltage and current capabilities consistent with driving doubly-terminated 50-Ω lines. For a 100-Ω load at a gain of +8 (see Figure 48), the total load is the parallel combination of the 100-Ω load and the 456-Ω total feedback network impedance. This 82-Ω load requires no more than 45-mA output current to support the ±3.7-V minimum output voltage swing specified for 100-Ω loads. This is well below the minimum ±90-mA specifications.

The specifications described above, though familiar in the industry, consider voltage and current limits separately. In many applications, it is the voltage × current, or V-I, product which is more relevant to circuit operation. Refer to Figure 21. The X and Y axes of this graph show the zero-voltage output current limit and the zero-current output voltage limit, respectively. The four quadrants provide a more detailed view of the OPA695 output drive capabilities. Superimposing resistor load lines onto the plot shows the available output voltage and current for specific loads.

The minimum specified output voltage and current overtemperature are set by worst-case simulations at the cold temperature extreme. Only at cold startup does the output current and voltage decrease to the numbers shown in the specification tables. As the output transistors deliver power, the junction temperatures increase, decreasing the V_{BE}s (increasing the available output voltage swing) and increasing the current gains (increasing the available output current). In steady-state operation, the available output voltage and current are always be greater than that shown in the over-temperature specifications, because the output stage junction temperatures are higher than the minimum specified operating ambient.

To maintain maximum output-stage linearity, no output short-circuit protection is provided. This is not normally a problem, as most applications include a series-matching resistor at the output that limits the internal power dissipation if the output side of this resistor is shorted to ground. However, shorting the output pin directly to the adjacent positive power supply pin will, in most cases, destroy the amplifier. If additional short-circuit protection is required, consider a small series resistor in the power-supply leads. Under heavy output loads, this reduces the available output voltage swing. A 5-Ω series resistor in each power-supply lead limits the internal power dissipation to less than 1W for an output short circuit, while decreasing the available output voltage swing only 0.25 V for up to 50-mA desired load currents. Always place the 0.1-µF power supply decoupling capacitors directly on the supply pins after these supply current-limiting resistors.

9.1.5.3 Driving Capacitive Loads

One of the most demanding, and yet very common, load conditions for an operational amplifier is capacitive loading. Often, the capacitive load is the input of an A/D converter,including additional external capacitance which may be recommended to improve A/D linearity. A high-speed, high open-loop gain amplifier like the OPA695 can be susceptible to decreased stability and closed-loop response peaking when a capacitive load is placed directly on the output pin. When the open-loop output resistance of the amplifier is considered, this capacitive load introduces an additional pole in the signal path that can decrease the phase margin. Several external solutions to this problem have been suggested. When the primary considerations are frequency response flatness, pulse response fidelity, and distortion, the simplest and most effective solution is to isolate the capacitive load from the feedback loop by inserting a series isolation resistor between the amplifier output and the capacitive load. This does not eliminate the pole from the loop response, but shifts it and adds a zero at a higher frequency. The additional zero acts to cancel the phase lag from the capacitive load pole, thus increasing the phase margin and improving stability.

The typical characteristics show the recommended R_S versus capacitive load and the resulting frequency response at the load. Parasitic capacitive loads greater than 2 pF can begin to degrade the performance of the OPA695. Long PCB traces, unmatched cables, and connections to multiple devices can exceed this value. Always consider this effect carefully and add the recommended series resistor as close as possible to the OPA695 output pin (see *Layout Guidelines*).

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Application Information (continued)

9.1.5.4 Distortion Performance

The OPA695 provides good distortion performance into a 100-Ω load on ±5-V supplies. Compared to other solutions, the OPA695 holds lower distortion at higher frequencies (> 20 MHz). Generally, until the fundamental signal reaches very high frequency or power levels, the 2nd-harmonic dominates the distortion with a negligible 3rd-harmonic component. Focusing on the 2nd-harmonic, increasing the load impedance directly improves distortion: the total load includes the feedback network. In the non-inverting configuration (see Figure 48), this is the sum of R_F + R_G, while in the inverting configuration, it is only R_F. Also, providing an additional supply decoupling capacitor (0.01 µF) between the supply pins (for bipolar operation) improves the 2nd-order distortion slightly (3 dB to 6 dB).

In most operational amplifiers, increasing the output voltage swing directly increases harmonic distortion. The typical performance curves show the 2nd-harmonic increasing at a little less than the expected 2x rate, while the 3rd-harmonic increases at a little less than the expected 3x rate. Where the test power doubles, the difference between it and the 2nd harmonic decreases less than the expected 6 dB, while the difference between it and the 3rd decreases by less than the expected 12 dB.

The OPA695 has extremely low 3rd-order harmonic distortion. This also gives a high 2-tone, 3rd-order intermodulation intercept, as shown in the typical characteristic curves. This intercept curve is defined at the 50-Ω load when driven through a 50-Ω matching resistor to allow direct comparisons to RF MMIC devices, and is shown for both gains of ±8. There is a slight improvement in intercept by operating the OPA695 in the inverting mode. The output matching resistor attenuates the voltage swing from the output pin to the load by 6 dB. If the OPA695 drives directly into the input of a high impedance device, such as an ADC, this 6-dB attenuation is not taken. Under these conditions, the intercept increases by a minimum 6 dBm.

The intercept predicts the intermodulation products for two closely-spaced frequencies. If the two test frequencies, F_1 and F_2, are specified in terms of average and delta frequency, $F_O = (F_1 + F_2)/2$ and $\Delta F = |F_2 – F_1|/2$, the two 3rd-order, close-in spurious tones will appear at $F_O \pm 3 \times \Delta F$. The difference between two equal test-tone power levels and these intermodulation spurious power levels is given by $\Delta dBc = 2 \times (OP_3 – P_O)$, where OP_3 is the intercept taken from the typical characteristic curve and P_O is the power level in dBm at the 50-Ω load for one of the two closely-spaced test frequencies. For example, at 50 MHz, gain of –8, the OPA695 has an intercept of 42 dBm at a matched 50-Ω load. If the full envelope of the two frequencies must be 2 V_{PP}, this requires each tone to be 4 dBm. The 3rd-order intermodulation spurious tones are then 2 × (42 – 4) = 76 dBc below the test-tone power level (–72 dBm). If this same 2-V_{PP} 2-tone envelope were delivered directly into the input of an ADC without the matching loss or the loading of the 50-Ω network, the intercept would increase to at least 48 dBm. With the same signal and gain conditions, but now driving directly into a light load, the 3rd-order spurious tones are then at least 2 × (48 – 4) = 88 dBc below the 4-dBm test-tone power levels centered on 50 MHz. Tests have shown that, in reality, the 3rd-order spurious levels are much lower due to the lighter loading presented by most ADCs.

9.1.5.5 Noise Performance

The OPA695 offers an excellent balance between voltage and current noise terms to achieve low output noise. The inverting current noise (22 pA/√Hz) is lower than most other current-feedback operational amplifiers, while the input voltage noise (1.8 nV/√Hz) is lower than any unity-gain stable, wideband, voltage-feedback operational amplifier. This low-input voltage noise was achieved at the price of a higher noninverting input current noise (18 pA/√Hz). As long as the AC source impedance looking out of the noninverting node is less than 50 Ω, this current noise does not contribute significantly to the total output noise. The operational amplifier input voltage noise and the two input current noise terms combine to give low output noise under a wide variety of operating conditions. Figure 63 shows the operational amplifier noise analysis model with all the noise terms included. In this model, all noise terms are taken to be noise voltage or current density terms in either nV/√Hz or pA/√Hz.

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Application Information (continued)

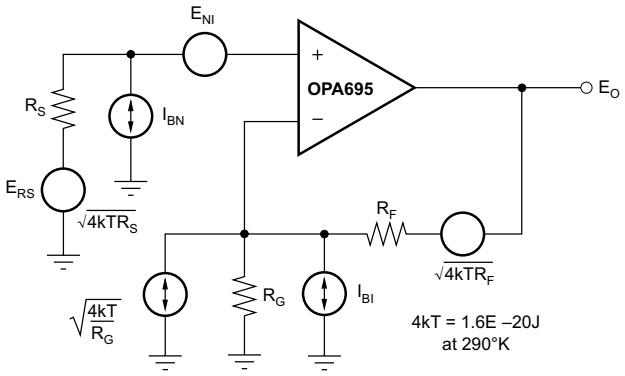


Figure 63. Operational Amplifier Noise Figure Analysis Model

The total output spot-noise voltage can be computed as the square root of the sum of all squared output noise voltage contributors. Equation 12 shows the general form for the output noise voltage using the terms shown in Figure 59.

$$E_O = \sqrt{\left(E_{NI}^2 + \left(I_{BN}R_S\right)^2 + 4kTR_S\right)G_N^2 + \left(I_{BI}R_F\right)^2 + 4kTR_FG_N} \quad (12)$$

Dividing this expression by the noise gain (NG = (1 + R_F/R_G)) gives the equivalent input referred spot-noise voltage at the noninverting input, as shown in Equation 13:

$$E_N = \sqrt{E_{NI}^2 + \left(I_{BN}R_S\right)^2 + 4kTR_S + \left(\frac{I_{BI}R_F}{NG}\right)^2 + \frac{4kTR_F}{NG}} \quad (13)$$

Evaluating these two equations for the OPA695 circuit and component values shown in Figure 48 gives a total output spot-noise voltage of 18.7 nV/√Hz and a total equivalent input spot-noise voltage of 2.3 nV/√Hz. This total input referred spot-noise voltage is higher than the 1.8-nV/√Hz specification for the operational amplifier voltage noise alone. This reflects the noise added to the output by the inverting current noise times the feedback resistor. If the feedback resistor is reduced in high-gain configurations (as suggested previously), the total input referred voltage noise given by Equation 13 just approaches the 1.8 nV/√Hz of the operational amplifier itself. For example, going to a gain of +20 (using R_F = 200 Ω) gives a total input referred noise of 2.0 nV/√Hz.

For a more complete discussion of operational amplifier noise calculation, see TI Application Note, SBOA066, *Noise Analysis for High Speed Op Amps*, available through www.ti.com.

9.1.5.6 DC Accuracy and Offset Control

A current-feedback operational amplifier such as the OPA695 provides exceptional bandwidth in high gains, giving fast pulse settling but only moderate DC accuracy. The typical specifications show an input offset voltage comparable to high-speed voltage-feedback amplifiers; however, the two input bias currents are somewhat higher and are unmatched. Although bias current cancellation techniques are effective with most voltage-feedback operational amplifiers, they do not generally reduce the output DC offset for wideband current-feedback operational amplifiers. Because the two input bias currents are unrelated in both magnitude and polarity, matching the source impedance looking out of each input to reduce their error contribution to the output is ineffective. Evaluating the configuration of Figure 48, using a worst-case +25°C input offset voltage and the two input bias currents, gives a worst-case output offset range equal to:

$$\pm(NG \times V_{OS}) + (I_{BN} \times R_S/2 \times NG) \pm(I_{BI} \times R_F) \quad (14)$$

where

- NG = noninverting signal gain

$$= \pm(8 \times 3.0\ mV) \pm (30\ \mu A \times 25\ \Omega \times 8) \pm(402\ \Omega \times 60\ \mu A)$$

$$= \pm 24\ mV \pm 1.6\ mV \pm 24\ mV$$

$$= \pm 54\ mV$$

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Application Information (continued)

A fine-scale output offset null, or DC operating point adjustment, is often required. Numerous techniques are available for introducing DC offset control into an operational amplifier circuit. Most simple adjustment techniques do not correct for temperature drift.

9.1.5.7 Power Shutdown Operation

The OPA695 provides an optional power shutdown feature that can be used to reduce system power. If the $V_{\overline{DIS}}$ control pin is left unconnected, the OPA695 operates normally. This shutdown is intended only as a power-saving feature. Forward path isolation is effective for small signals. Large signal isolation is not ensured. Using this feature to multiplex two or more outputs together is not recommended. Large signals applied to the shutdown output stages can turn on parasitic devices, degrading signal linearity for the desired channel.

Turn-on time is quick from the shutdown condition, typically < 60 ns. Turn-off time is strongly dependent on the external circuit configuration, but is typically 200 ns for the circuit of Figure 48.

To shut down, the control pin must be asserted low. This logic control is referenced to the positive supply, as shown in the simplified circuit of Figure 64.

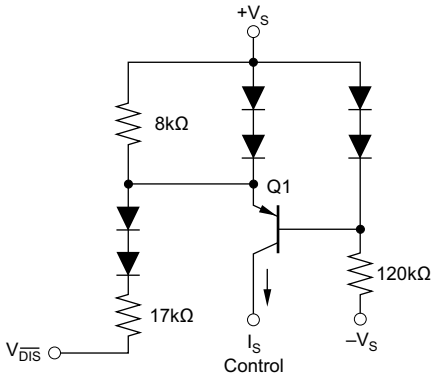


Figure 64. Operational Amplifier Noise Figure Analysis Model

In normal operation, base current to Q1 is provided through the 120-kΩ resistor, while the emitter current through the 8-kΩ resistor sets up a voltage drop that is inadequate to turn on the two diodes in the Q1 emitter. As $V_{\overline{DIS}}$ is pulled low, additional current is pulled through the 8-kΩ resistor, eventually turning on these two diodes (≈ 180 µA). At this point, any further current pulled out of $V_{\overline{DIS}}$ goes through those diodes holding the emitter-base voltage of Q1 at approximately 0 V. This shuts off the collector current out of Q1, turning the amplifier off. The supply current in the shutdown mode is only that required to operate the circuit of Figure 64.

When disabled, the output and input nodes go to a high impedance state. If the OPA695 is operating in a gain of +1, this will show a very high impedance (3 pF || 1 MΩ) at the output and exceptional signal isolation. If operating at a gain greater than +1, the total feedback network resistance ($R_F + R_G$) appears as the impedance looking back into the output, but the circuit will still show very high forward and reverse isolation. If configured as an inverting amplifier, the input and output are connected through the feedback network resistance ($R_F + R_G$), giving relatively poor input to output isolation.

9.1.5.8 Thermal Analysis

The OPA695 does not require external heatsinking for most applications. Maximum desired junction temperature sets the maximum allowed internal power dissipation as described below. In no case should the maximum junction temperature be allowed to exceed 150°C.

Operating junction temperature (T_J) is given by $T_A + P_D \times \theta_{JA}$. The total internal power dissipation (P_D) is the sum of quiescent power (P_{DQ}) and additional power dissipated in the output stage (P_{DL}) to deliver load power. Quiescent power is simply the specified no-load supply current times the total supply voltage across the part. P_{DL} depends on the required output signal and load. However, for a grounded resistive load, P_{DL} would be at a maximum when the output is fixed at a voltage equal to one-half of either supply voltage (for equal bipolar supplies). Under this condition, $P_{DL} = V_S\ 2/(4 \times R_L)$, where R_L includes feedback network loading.

Note that it is the power in the output stage and not into the load that determines internal power dissipation.

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Application Information (continued)

As an absolute worst-case example, compute the maximum T_J using an OPA695IDBV (SOT23-6 package) in the circuit of Figure 48 operating at the maximum specified ambient temperature of +85°C and driving a grounded 100-Ω load.

$$P_D = 10\ V \times 14.1\ mA + 52/(4 \times (100\ \Omega \parallel 458\ \Omega)) = 217\ mW \quad (15)$$

$$\text{Maximum } T_J = +85°C + (0.22\ W \times 150°C/W) = 118°C \quad (16)$$

This maximum operating junction temperature is well below most system level targets. Most applications are lower as an absolute worst-case output stage power was assumed in this calculation.

9.2 Typical Application

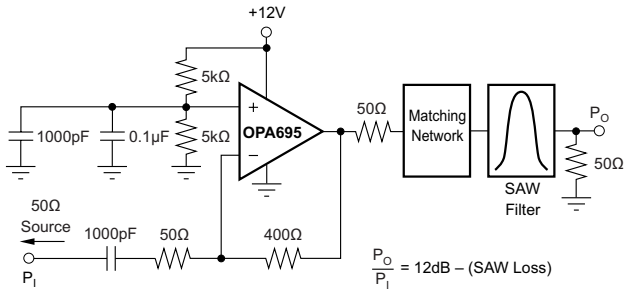


Figure 65. IF Amplifier Driving SAW Filter

9.2.1 Design Requirements

9.2.1.1 Saw Filter Buffer

One common requirement in an IF strip is to buffer the output of a mixer with enough gain to recover the insertion loss of a narrowband SAW filter. Figure 65 shows one possible configuration driving a SAW filter. Figure 53 shows the intercept at the 50-Ω load. Operating in the inverting mode at a voltage gain of –8 V/V, this circuit provides a 50-Ω input match using the gain set resistor, has the feedback optimized for maximum bandwidth (700 MHz in this case), and drives through a 50-Ω output resistor into the matching network at the input of the SAW filter. If the SAW filter gives a 12-dB insertion loss, a net gain of 0 dB to the 50-Ω load at the output of the SAW (which could be the input impedance of the next IF amplifier or mixer) is delivered in the passband of the SAW filter. Using the OPA695 in this application isolates the first mixer from the impedance of the SAW filter and provides very low two-tone, 3rd-order spurious levels in the SAW filter bandwidth. Inverting operation gives the broadest bandwidth up to a gain of –12 V/V (15.6 dB). Noninverting operation gives higher bandwidth at gain settings higher than this, but will also give a slight reduction in intercept and noise figure performance.

9.2.2 Detailed Design Procedure

The design procedure begins with calculating the required signal gain and signal swing. Once the gain and swing requirements are determined the appropriate amplifier is selected along with the required supply voltage. Due to the input impedance of 50 Ω the gain and the input impedance require a feedback resistor value of 400 Ω.

In this application the supply voltage is 12 V single ended. In order to provide the proper DC operating point it is necessary to apply a mid supply voltage to the non inverting input. This is accomplished by using a resistive voltage divider composed of two 1% precision 5-kΩ resistors along with two ceramic bypass capacitors. These components provide an accurate and low AC impedance reference voltage for the non inverting input. The inverting input requires only an AC coupling capacitor to isolate the 6 V operating voltage from the signal source. In this example a ceramic 1000-pF capacitor is used.

The circuit shown in Figure 65 shows an output resistor value of 50 Ω. This resistor will need to be adjusted to accommodate the SAW input impedance. Additional L/C components may be required as well, consult the SAW manufacturer's design guidelines for more details.

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Typical Application (continued)

9.2.3 Application Curve

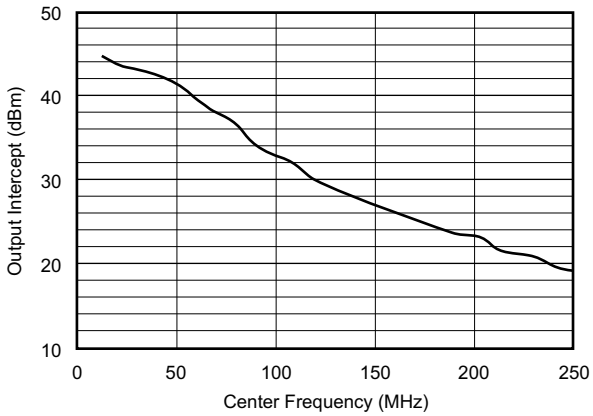


Figure 66. 2-Tone, 3rd-Order Intermodulation Intercept

10 Power Supply Recommendations

High-speed amplifiers require low inductance power supply traces and low ESR bypass capacitors. When possible both power and ground planes must be used in the printed circuit board design and the power plane must be adjacent to the ground plane in the board stack-up. The power supply voltage must be centered on the desired amplifier output voltage, so for ground referenced output signals, split supplies are required. The power supply voltage must be from 5 V to 12 V.

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11 Layout

11.1 Layout Guidelines

Achieving optimum performance with a high-frequency amplifier like the OPA695 requires careful attention to board layout parasitics and external component types. Recommendations that will optimize performance include:

- **Minimize parasitic capacitance to any AC ground for all of the signal I/O pins.** Parasitic capacitance on the output and inverting input pins can cause instability; on the non-inverting input, it can react with the source impedance to cause unintentional bandlimiting. To reduce unwanted capacitance, a window around the signal I/O pins must be opened in all of the ground and power planes around those pins. Otherwise, ground and power planes must be unbroken elsewhere on the board.
- **Minimize the distance (< 0.25") from the power supply pins to high frequency 0.1-µF decoupling capacitors.** At the device pins, the ground and power plane layout must not be in close proximity to the signal I/O pins. Avoid narrow power and ground traces to minimize inductance between the pins and the decoupling capacitors. The power-supply connections must always be decoupled with these capacitors. An optional supply-decoupling capacitor across the two power supplies (for bipolar operation) improves 2nd-harmonic distortion performance. Larger (2.2 µF to 6.8 µF) decoupling capacitors, effective at a lower frequency, must also be used on the main supply pins. These may be placed somewhat farther from the device, and may be shared among several devices in the same area of the PCB.
- **Careful selection and placement of external components will preserve the high frequency performance of the OPA695.** Resistors must be a low reactance type. Surface-mount resistors work best and allow a tighter overall layout. Metal-film and carbon composition, axially-leaded resistors can also provide good high frequency performance. Keep their leads and PCB trace length as short as possible. Never use wirewound-type resistors in a high frequency application. Because the output pin and inverting input pin are the most sensitive to parasitic capacitance, always position the feedback and series output resistor, if any, as close as possible to the output pin. Other network components, such as noninverting input termination resistors, must also be placed close to the package. Where double-side component mounting is allowed, place the feedback resistor directly under the package on the other side of the board between the output and inverting input pins. The frequency response is primarily determined by the feedback resistor value. Increasing its value reduces the bandwidth, while decreasing it gives a more peaked frequency response. The 402-Ω feedback resistor (used in the typical performance specifications at a gain of +8 on ±5-V supplies) is a good starting point for design. Note that a 523-Ω feedback resistor, rather than a direct short, is required for the unity gain follower application. A current-feedback operational amplifier requires a feedback resistor, even in the unity gain follower configuration, to control stability.
- **Connections to other wideband devices on the board may be made with short direct traces or through onboard transmission lines.** For short connections, consider the trace and the input to the next device as a lumped capacitive load. Relatively wide traces (50 mils to 100 mils) must be used, preferably with ground and power planes opened up around them. Estimate the total capacitive load and set R_S from the plot of Figure 40. Low parasitic capacitive loads (< 5 pF) may not need an R_S as the OPA695 is nominally compensated to operate with a 2-pF parasitic load. If a long trace is required, and the 6-dB signal loss intrinsic to a doubly-terminated transmission line is acceptable, implement a matched impedance transmission line using microstrip or stripline techniques (consult an ECL design handbook for microstrip and stripline layout techniques). A 50-Ω environment is usually not necessary on board. In fact, a higher impedance environment improves distortion, as shown in the distortion versus load plots. With a characteristic board trace impedance defined (based on board material and trace dimensions), use a matching series resistor into the trace from the output of the OPA695. Also use terminating shunt resistor at the input of the destination device. Remember that the terminating impedance will be the parallel combination of the shunt resistor and the input impedance of the destination device; this total effective impedance must be set to match the trace impedance. The high output voltage and current capability of the OPA695 allows multiple destination devices to be handled as separate transmission lines, each with their own series and shunt terminations. If the 6-dB attenuation of a doubly-terminated transmission line is unacceptable, a long trace can be series-terminated at the source end only. Treat the trace as a capacitive load in this case, and set the series resistor value as shown in the plot of Figure 40. This will not preserve signal integrity as well as a doubly-terminated line. If the input impedance of the destination device is low, there will be some signal attenuation due to the voltage divider formed by the series output into the terminating impedance.
- **Socketing a high-speed part like the OPA695 is not recommended.** The additional lead length and pin-to-pin capacitance introduced by the socket can create a troublesome parasitic network, which can make it almost impossible to achieve a smooth, stable frequency response. Best results are obtained by soldering the OPA695 directly onto the board.

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Layout Guidelines (continued)

11.1.1 Input and ESD Protection

The OPA695 is built using a very high-speed, complementary bipolar process. The internal junction breakdown voltages are relatively low for these small geometry devices. These breakdowns are reflected in the *Absolute Maximum Ratings* where an absolute maximum ±6.5-V supply is reported. All device pins have limited ESD protection using internal diodes to the power supplies, as shown in Figure 67.

These diodes also provide moderate protection to input overdrive voltages above the supplies. The protection diodes can typically support 30-mA continuous current. Where higher currents are possible (for example, in systems with ±15-V supply parts driving into the OPA695), current-limiting series resistors must be added into the two inputs. Keep these resistor values as low as possible as high values degrade both noise performance and frequency response.

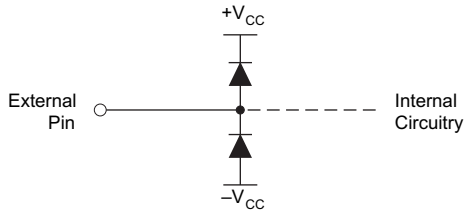


Figure 67. Internal ESD Protection

11.2 Layout Example

As detailed in *Layout Guidelines* and illustrated in Figure 68, the input termination resistor, output resistor and bypass capacitors must be placed close to the amplifier. Power and ground planes are placed under the amplifier, but must be removed under the input and output pins as shown in Figure 68.

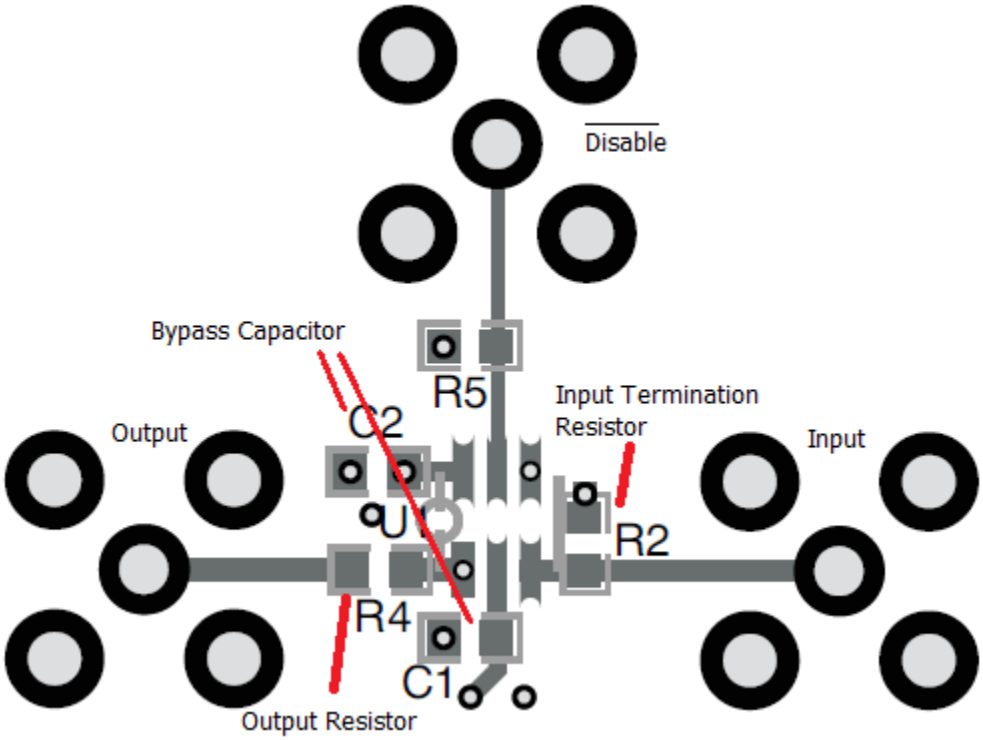


Figure 68. SBOS293 Layout

12 Device and Documentation Support

12.1 Device Support

12.1.1 Design-In Tools

12.1.1.1 Demonstration Fixtures

Two printed circuit boards (PCBs) are available to assist in the initial evaluation of circuit performance using the OPA695 in its two package options. Both of these are offered free of charge as unpopulated PCBs, delivered with a user's guide. The summary information for these fixtures is shown in Table 4.

Table 4. Demonstration Boards

PRODUCT	PACKAGE	ORDERING NUMBER	USER'S GUIDE LITERATURE NUMBER
OPA695ID	VSSOP-8	DEM-OPA-SO-1B	SBOU026
OPA691IDBV	SOT23-6	DEM-OPA-SOT-1B	SBOU027

The demonstration fixtures can be requested at the Texas Instruments web site (www.ti.com) through the OPA695 product folder.

12.2 Documentation Support

12.2.1 Related Documentation

For related documentation, see the following:

- *Absolute Maximum Ratings for Soldering*, SNOA549
- *Current Feedback Op Amp Applications Circuit Guide, Application Note OA--07*, SNOA365
- *Frequent Faux Pas in Applying Wideband Current Feedback Amplifiers, Application Note OA-15*, SNOA367
- *Noise Analysis for Comlinear Amplifiers, Application Note OA-12*, SNOA375
- *Semiconductor and IC Package Thermal Metrics*, SPRA953

12.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.4 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

12.5 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

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13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
OPA695ID	LIFEBUY	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	OPA 695	
OPA695IDBVR	ACTIVE	SOT-23	DBV	6	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	A71L	Samples
OPA695IDBVT	LIFEBUY	SOT-23	DBV	6	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	A71L	
OPA695IDBVTG4	LIFEBUY	SOT-23	DBV	6	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	A71L	
OPA695IDG4	LIFEBUY	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	OPA 695	
OPA695IDGKR	LIFEBUY	VSSOP	DGK	8	2500	RoHS & Green	Call TI | NIPDAUAG	Level-2-260C-1 YEAR	-40 to 85	695	
OPA695IDGKT	LIFEBUY	VSSOP	DGK	8	250	RoHS & Green	Call TI | NIPDAUAG	Level-2-260C-1 YEAR	-40 to 85	695	
OPA695IDR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	OPA 695	Samples
OPA695IDRG4	LIFEBUY	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	OPA 695	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

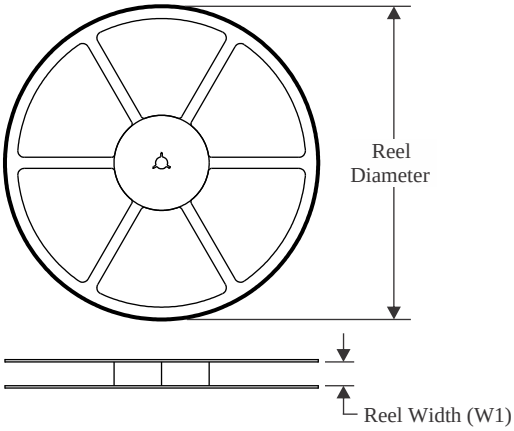
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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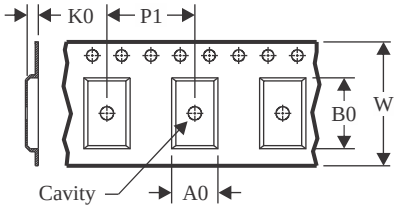
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

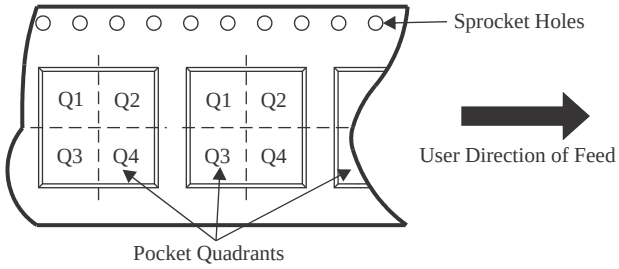


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

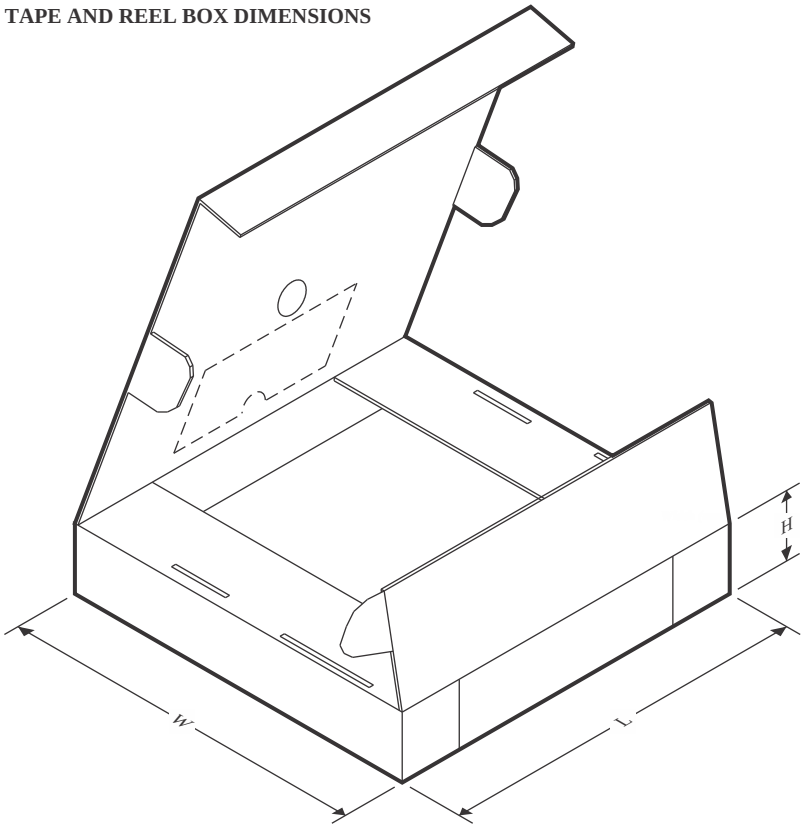
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
OPA695IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

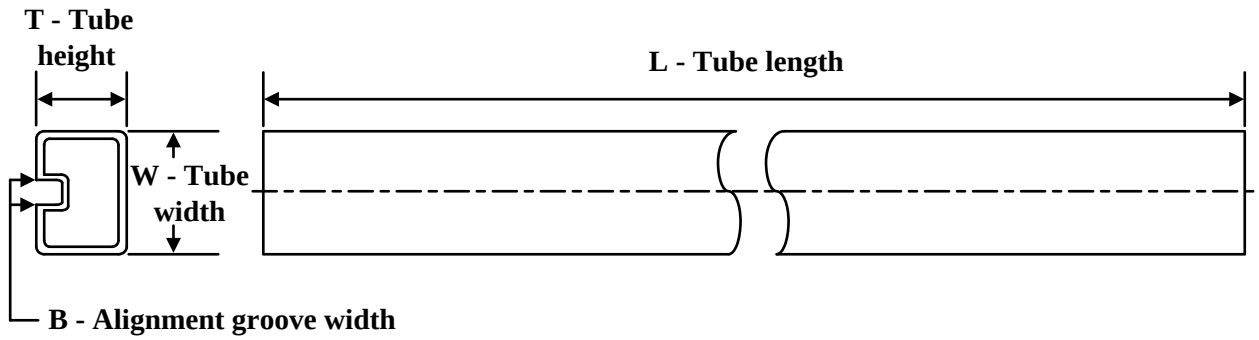
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
OPA695IDR	SOIC	D	8	2500	356.0	356.0	35.0

TUBE



*All dimensions are nominal

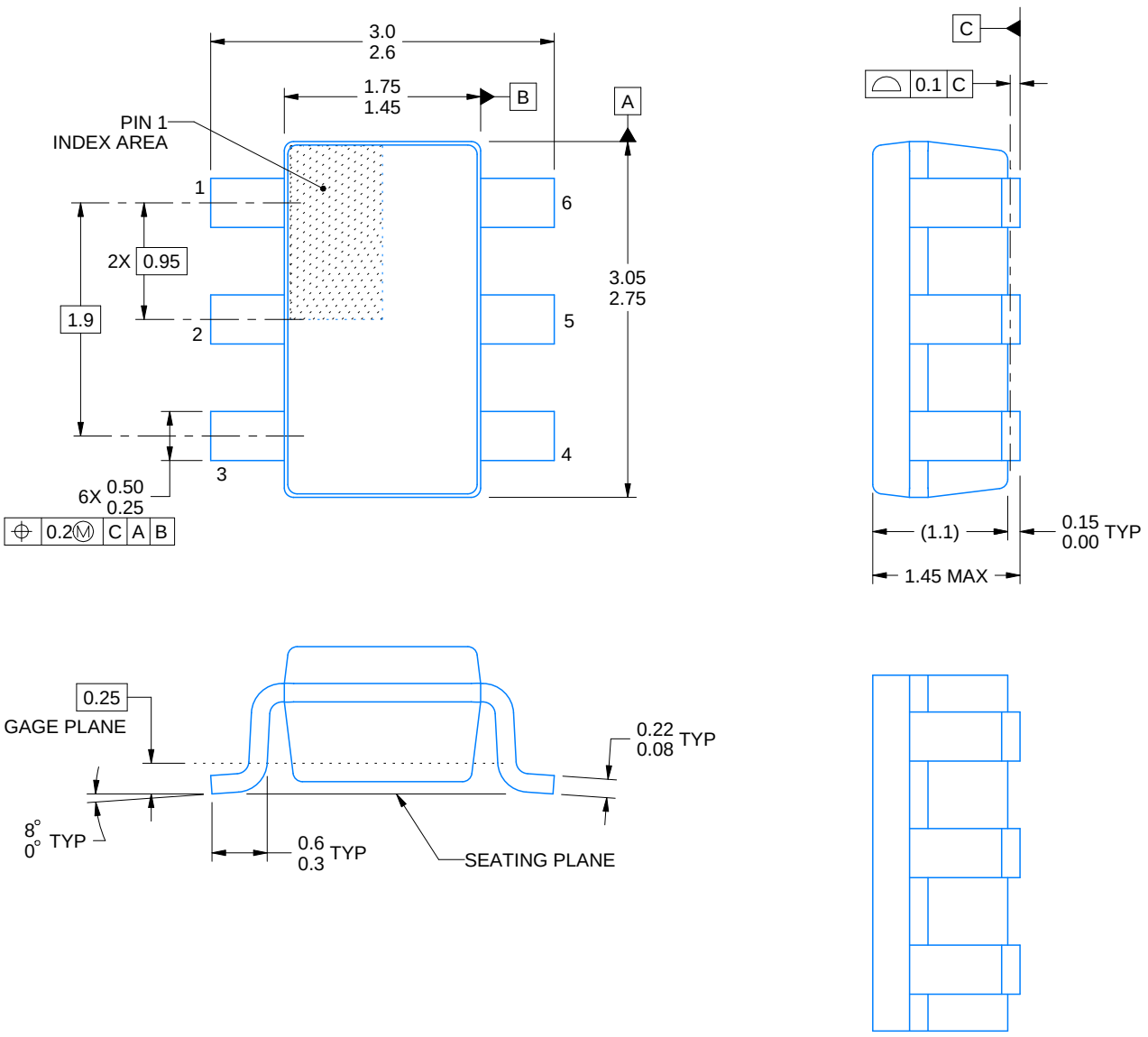
Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
OPA695ID	D	SOIC	8	75	506.6	8	3940	4.32
OPA695IDG4	D	SOIC	8	75	506.6	8	3940	4.32

PACKAGE OUTLINE

DBV0006A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR

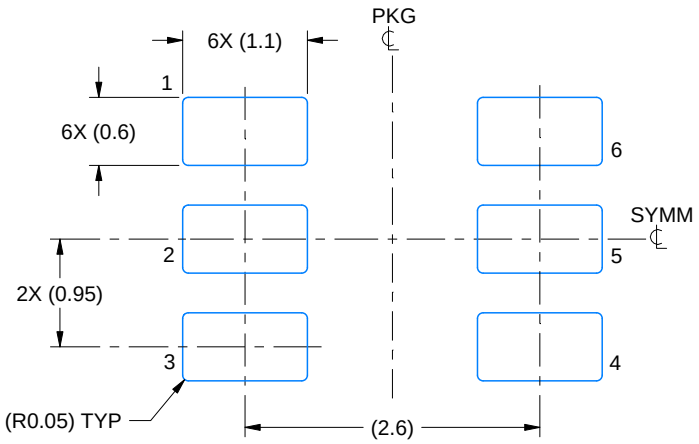


ALTERNATIVE PACKAGE SINGULATION VIEW

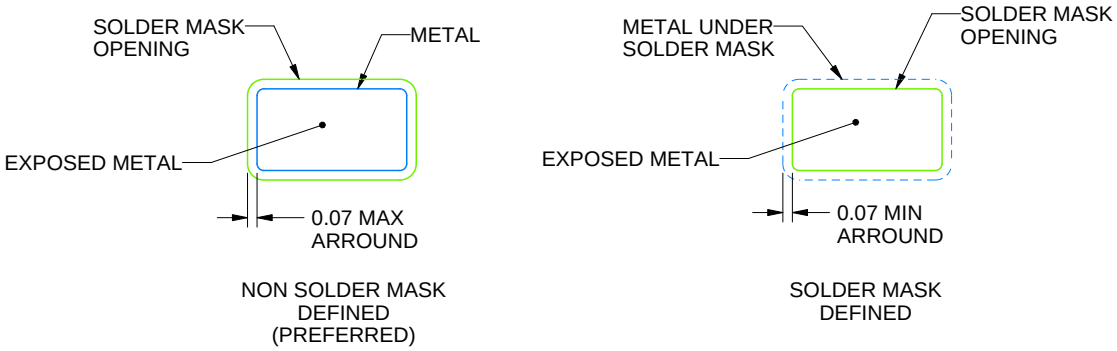
4214840/E 02/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.25 per side.
4. Leads 1,2,3 may be wider than leads 4,5,6 for package orientation.
5. Refernce JEDEC MO-178.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

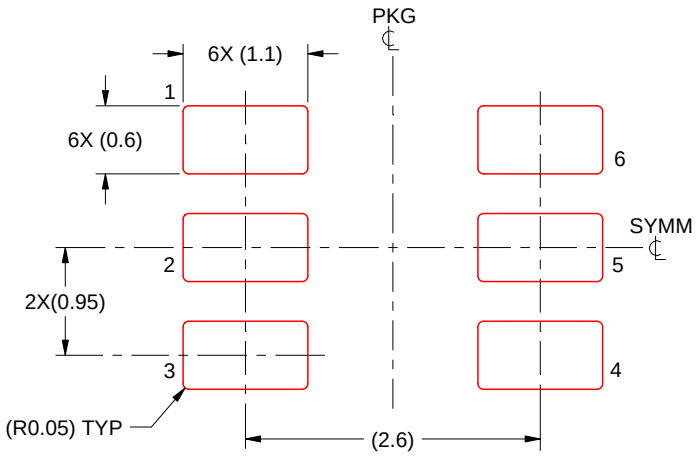


SOLDER MASK DETAILS

4214840/E 02/2024

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

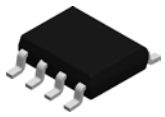


SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214840/E 02/2024

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

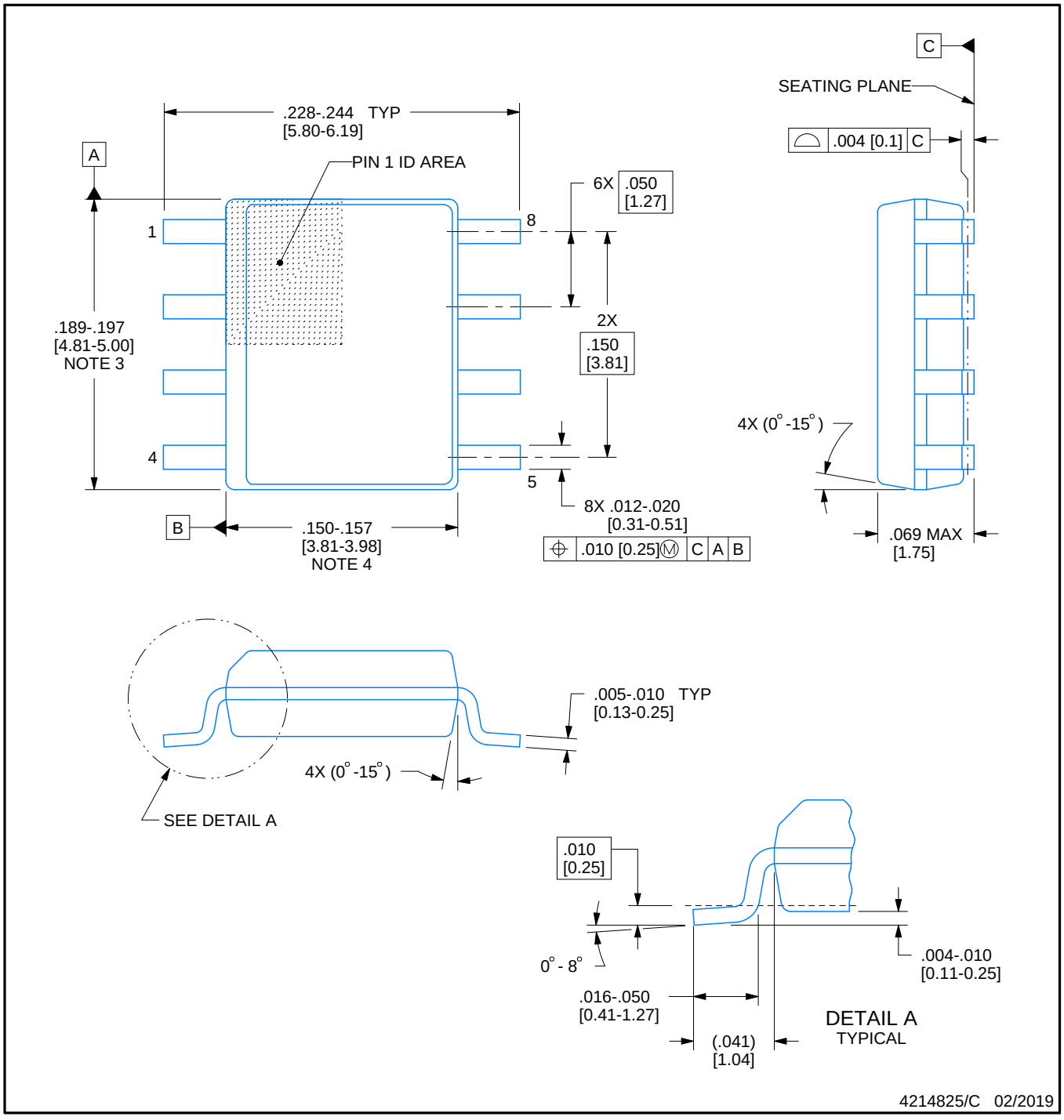


PACKAGE OUTLINE

D0008A

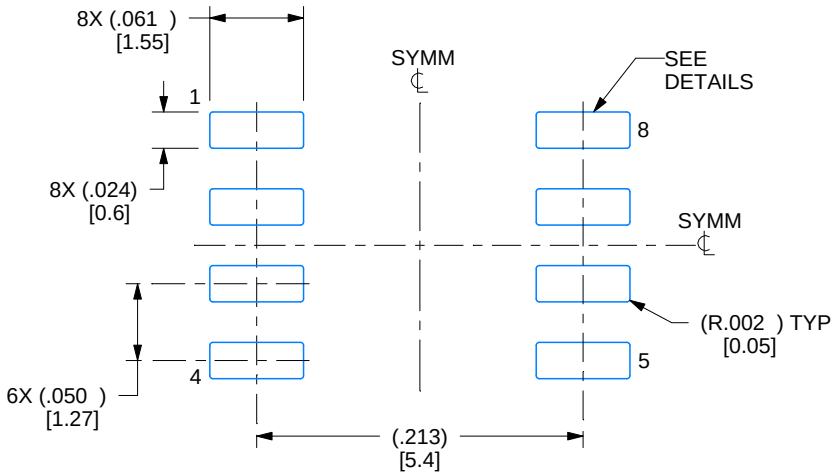
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

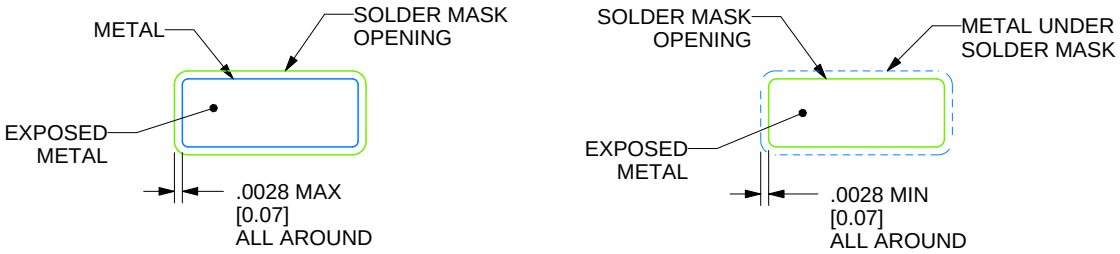


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

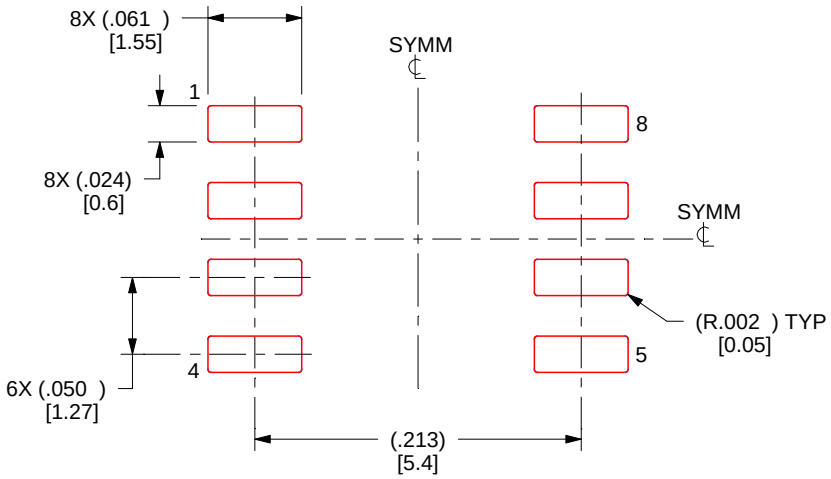
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



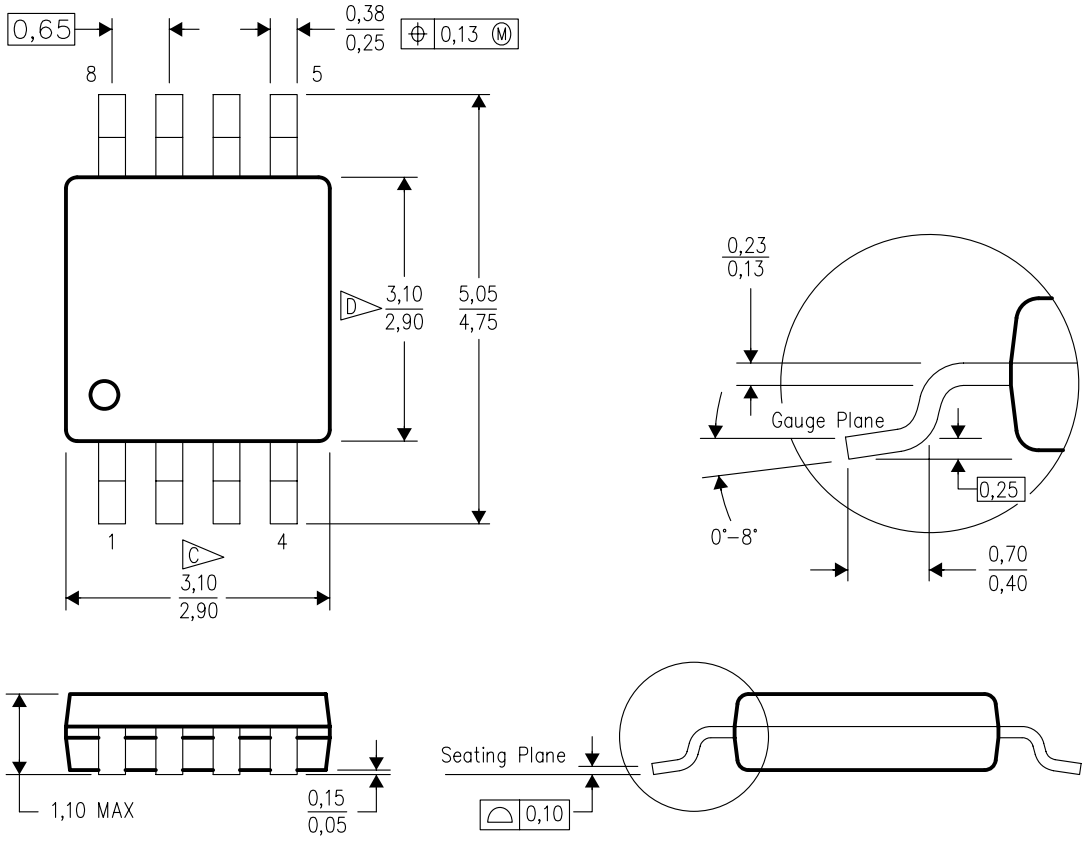
SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

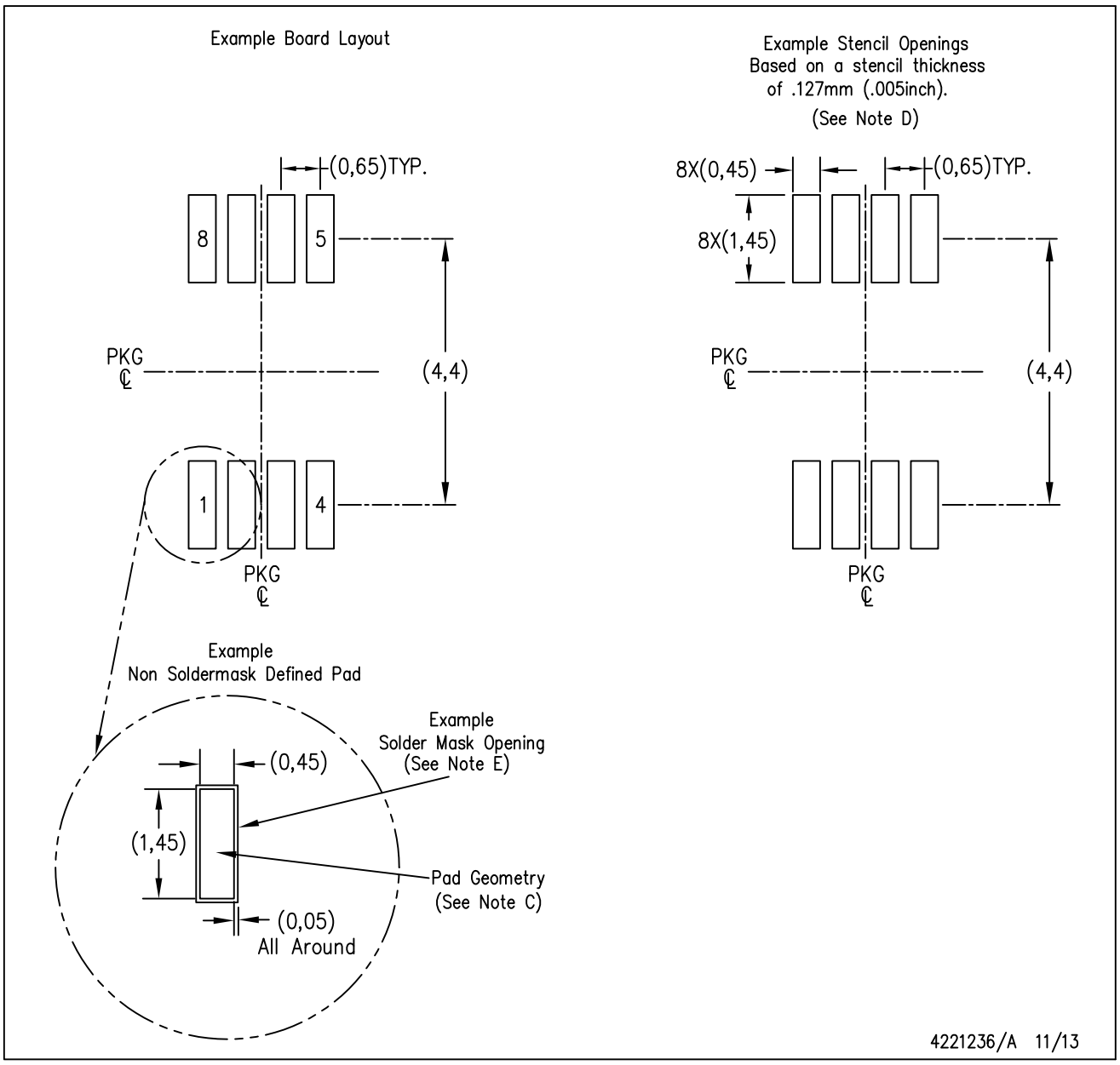
DGK (S–PDSO–G8) PLASTIC SMALL–OUTLINE PACKAGE



4073329/E 05/06

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
E. Falls within JEDEC MO–187 variation AA, except interlead flash.

DGK (S–PDSO–G8) PLASTIC SMALL OUTLINE PACKAGE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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