

SN74AC14-Q1 Automotive Hex Schmitt-Trigger Inverter

1 Features

- Qualified for automotive applications
- 2V to 6V V_{CC} operation
- Inputs accept voltages to 6V

2 Description

This Schmitt-trigger device contain six independent inverters. They perform the Boolean function $Y = \bar{A}$.

Package Information

PART NUMBER	PACKAGE ⁽¹⁾	PACKAGE SIZE ⁽²⁾	BODY SIZE ⁽³⁾
SN74AC14-Q1	BQA (WQFN, 14)	3.00mm × 2.50mm	3.00mm × 2.50mm
	PW (TSSOP, 14)	5mm x 6.4mm	5.00mm x 4.4mm

- (1) For more information, see [Section 10](#).
- (2) The package size (length × width) is a nominal value and includes pins, where applicable.
- (3) The body size (length × width) is a nominal value and does not include pins.



Logic Diagram
Each Inverter (Positive Logic)



Table of Contents

1 Features	1	6.3 Device Functional Modes.....	8
2 Description	1	7 Application and Implementation	9
3 Pin Configuration and Functions	3	7.1 Power Supply Recommendations.....	9
4 Specifications	4	7.2 Layout.....	9
4.1 Absolute Maximum Ratings.....	4	8 Device and Documentation Support	10
4.2 Recommend Operating Conditions.....	4	8.1 Documentation Support.....	10
4.3 Thermal Information.....	4	8.2 Receiving Notification of Documentation Updates...	10
4.4 Electrical Characteristics.....	5	8.3 Support Resources.....	10
4.5 Switching Characteristics, $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$	5	8.4 Trademarks.....	10
4.6 Switching Characteristics, $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$	5	8.5 Electrostatic Discharge Caution.....	10
4.7 Operating Characteristics.....	6	8.6 Glossary.....	10
5 Parameter Measurement Information	7	9 Revision History	10
6 Detailed Description	8	10 Mechanical, Packaging, and Orderable Information	11
6.1 Overview.....	8		
6.2 Functional Block Diagram.....	8		

3 Pin Configuration and Functions

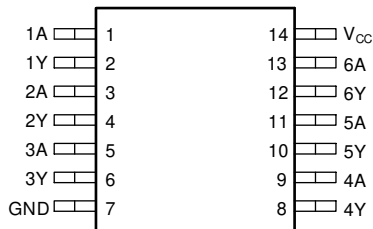


Figure 3-1. PW Package, 14-Pin TSSOP (Top View)

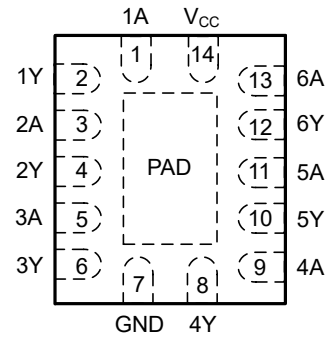


Figure 3-2. BQA Package, 14-Pin WQFN (Top View)

PIN		I/O	DESCRIPTION
NAME	N.O.		
1A	1	Input	Channel 1, Input A
1Y	2	Output	Channel 1, Output Y
2A	3	Input	Channel 2, Input A
2Y	4	Output	Channel 2, Output Y
3A	5	Input	Channel 3, Input A
3Y	6	Output	Channel 3, Output Y
GND	7	—	Ground
4Y	8	Output	Channel 4, Output Y
4A	9	Input	Channel 4, Input A
5Y	10	Output	Channel 5, Output Y
5A	11	Input	Channel 5, Input A
6Y	12	Output	Channel 6, Output Y
6A	13	Input	Channel 6, Input A
V _{cc}	14	—	Positive Supply
NC		—	Not internally connected
Thermal Pad ⁽¹⁾		—	The thermal pad can be connected to GND or left floating. Do not connect to any other signal or supply.

(1) BQA package only.

4 Specifications

4.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

		MIN	MAX	UNIT
V _{CC}	Supply voltage range	-0.5	7	V
V _I ⁽²⁾	Input voltage range	-0.5	V _{CC} + 0.5	V
V _O ⁽²⁾	Output voltage range	-0.5	V _{CC} + 0.5	V
I _{IK}	Input clamp current	(V _I < 0 or V _I > V _{CC})		±20 mA
I _{OK}	Output clamp current	(V _O < 0 or V _O > V _{CC})		±20 mA
I _O	Continuous output current	(V _O = 0 to V _{CC})		±50 mA
	Continuous current through V _{CC} or GND			±200 mA
T _{stg}	Storage temperature range	-65	150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

4.2 Recommend Operating Conditions

over recommended operating free-air temperature range (unless otherwise noted)⁽¹⁾

		MIN	MAX	UNIT
V _{CC}	Supply voltage	2	6	V
V _I	Input voltage	0	V _{CC}	V
V _O	Output voltage	0	V _{CC}	V
I _{OH}	High-level output current	V _{CC} = 3 V		-12 mA
		V _{CC} = 4.5 V		-24
		V _{CC} = 5.5 V		-24
I _{OL}	Low-level output current	V _{CC} = 3 V		12 mA
		V _{CC} = 4.5 V		24
		V _{CC} = 5.5 V		24
T _A	Operating free-air temperature	-40	125	°C

- (1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number [SCBA004](#).

4.3 Thermal Information

THERMAL METRIC ⁽¹⁾	SN74AC14-Q1		UNIT	
	BQA (WQFN)	PW (TSSOP)		
	14 PINS	14 PINS		
R _{θJA}	Junction-to-ambient thermal resistance	93.4	148	°C/W

- (1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

4.4 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	T _A = 25°C			MIN	MAX	UNIT
			MIN	TYP	MAX			
V _{T+} Positive-going threshold		3 V	0.8	1.8	2.2	0.8	2.2	V
		4.5 V	1.5	2.6	3.2	1.5	3.2	
		5.5 V	1.6	3.2	3.9	1.6	3.9	
V _{T-} Negative-going threshold		3 V	0.5	0.8	1	0.5	1.2	V
		4.5 V	0.9	1.4	1.8	0.9	1.8	
		5.5 V	1.1	1.8	2.3	1.1	2.3	
ΔV _T Hysteresis (V _{T+} - V _{T-})		3 V	0.3	1	1.2	0.3	1.2	V
		4.5 V	0.4	1.2	1.4	0.4	1.4	
		5.5 V	0.5	1.4	1.6	0.5	1.6	
V _{OH}	I _{OH} = -50 μA	3 V	2.9			2.9		V
		4.5 V	4.4			4.4		
		5.5 V	5.4			5.4		
	I _{OH} = -12 mA	3 V	2.56			2.4		
		4.5 V	3.86			3.7		
		5.5 V	4.86			4.7		
V _{OL}	I _{OL} = 50 μA	3 V	0.1			0.1		V
		4.5 V	0.1			0.1		
		5.5 V	0.1			0.1		
	I _{OL} = 12 mA	3 V	0.36			0.5		
		4.5 V	0.36			0.5		
		5.5 V	0.36			0.5		
I _I	V _I = V _{CC} or GND	5.5 V	±0.1			±1		μA
I _{CC}	V _I = V _{CC} or GND, I _O = 0	5.5 V	2			40		μA
C _i	V _I = V _{CC} or GND	5 V	4.5					pF

4.5 Switching Characteristics, V_{CC} = 5 V ± 0.5 V

over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see [Load Circuit and Voltage Waveforms](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T _A = 25°C			MIN	MAX	UNIT
			MIN	TYP	MAX			
t _{PLH}	A	Y	1.5	5	10	1.5	12	ns
t _{PHL}			1.5	5	8.5	1.5	10	

4.6 Switching Characteristics, V_{CC} = 3.3 V ± 0.3 V

over recommended operating free-air temperature range, V_{CC} = 3.3 V ± 0.3 V (unless otherwise noted) (see [Load Circuit and Voltage Waveforms](#))

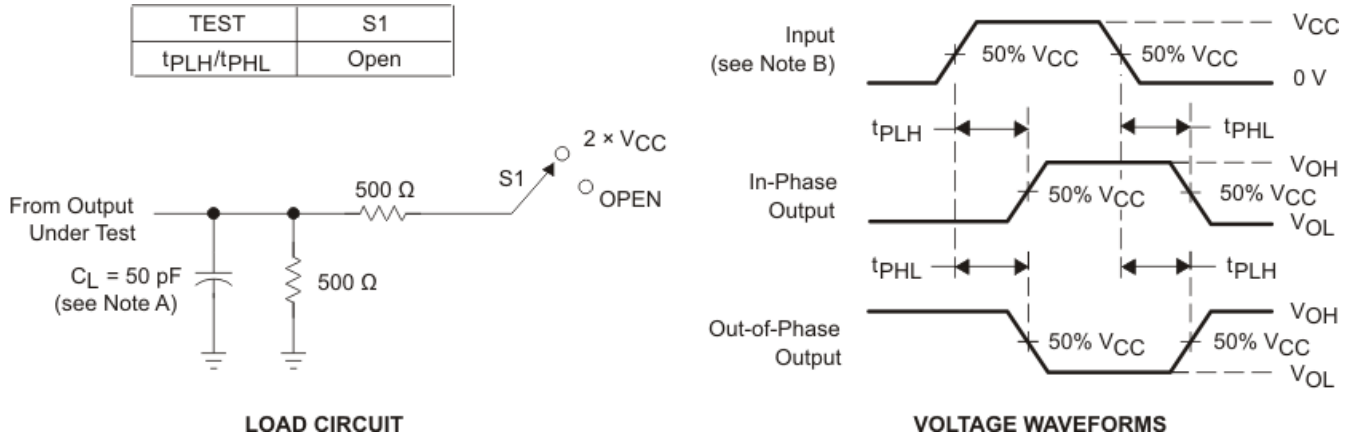
PARAMETER	FROM (INPUT)	TO (OUTPUT)	T _A = 25°C			MIN	MAX	UNIT
			MIN	TYP	MAX			
t _{PLH}	A	Y	1.5	6	13.5	1.0	16	ns
t _{PHL}			1.5	6	11.5	1.0	14	

4.7 Operating Characteristics

$V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$

PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance	$C_L = 50\text{ pF}$, $f = 1\text{ MHz}$	30	pF

5 Parameter Measurement Information



- A. C_L includes probe and jig capacitance.
- B. All input pulses are supplied by generators having the following characteristics: $PRR \leq 1 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 2.5 \text{ ns}$, $t_f \leq 2.5 \text{ ns}$.
- C. The outputs are measured one at a time with one input transition per measurement.

Figure 5-1. Load Circuit and Voltage Waveforms

6 Detailed Description

6.1 Overview

This Schmitt-trigger device contains six independent inverters. They perform the Boolean function $Y = \overline{A}$. Because of the Schmitt action, they have different input threshold levels for positive-going (V_{T+}) and for negative-going (V_{T-}) signals.

These circuits are temperature compensated and can be triggered from the slowest of input ramps and still give clean, jitter-free output signals. They also have a greater noise margin than conventional inverters.

6.2 Functional Block Diagram



**Figure 6-1. Logic Diagram
Each Inverter (Positive Logic)**

6.3 Device Functional Modes

Table 6-1. Function Table

INPUT	OUTPUT
A	Y
H	L
L	H

7 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

7.1 Power Supply Recommendations

The power supply can be any voltage between the MIN and MAX supply voltage rating located in the [Section 4.2](#).

Each V_{CC} pin should have a good bypass capacitor to prevent power disturbance. For devices with a single supply, $0.1\mu\text{F}$ is recommended; if there are multiple V_{CC} pins, then $0.01\mu\text{F}$ or $0.022\mu\text{F}$ is recommended for each power pin. It is acceptable to parallel multiple bypass caps to reject different frequencies of noise. A $0.1\mu\text{F}$ and a $1\mu\text{F}$ are commonly used in parallel. The bypass capacitor should be installed as close to the power pin as possible for best results.

7.2 Layout

7.2.1 Layout Guidelines

When using multiple bit logic devices, inputs should not float. In many cases, functions or parts of functions of digital logic devices are unused. Some examples are when only two inputs of a triple-input AND gate are used, or when only 3 of the 4-buffer gates are used. Such input pins should not be left unconnected because the undefined voltages at the outside connections result in undefined operational states.

Specified in [Section 7.2.2](#) are rules that must be observed under all circumstances. All unused inputs of digital logic devices must be connected to a high or low bias to prevent them from floating. The logic level that should be applied to any particular unused input depends on the function of the device. Generally they will be tied to GND or V_{CC} , whichever makes more sense or is more convenient. It is acceptable to float outputs unless the part is a transceiver. If the transceiver has an output enable pin, it will disable the outputs section of the part when asserted. This will not disable the input section of the I/Os so they also cannot float when disabled.

7.2.2 Layout Example

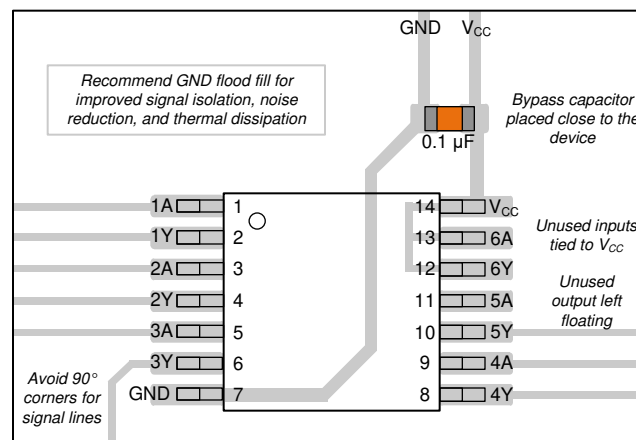


Figure 7-1. Example Layout for the SN74AC14-Q1

8 Device and Documentation Support

8.1 Documentation Support

8.1.1 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 8-1. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
SN74AC14-Q1	Click here	Click here	Click here	Click here	Click here

8.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

8.3 Support Resources

[TI E2E™ support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

8.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.

All trademarks are the property of their respective owners.

8.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

8.6 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

9 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (May 2023) to Revision B (July 2024)	Page
• Added BQA package size to <i>Package Information</i> table, Pin Configuration and Functions section, and <i>Thermal Information</i> table.....	1
• Added package size to <i>Package Information</i> table.....	1
• Updated R θ JA values: PW = 113 to 148, all values in °C/W.....	4
• Updated <i>Layout Example</i> image.....	9
<hr/>	
Changes from Revision * (June 2011) to Revision A (May 2023)	Page
• Added <i>Package Information</i> table, <i>Pin Functions</i> table, and <i>Thermal Information</i> table.....	1

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74AC14QPWRQ1	ACTIVE	TSSOP	PW	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AC14Q	Samples
SN74AC14WBQARQ1	ACTIVE	WQFN	BQA	14	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AC14Q	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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OTHER QUALIFIED VERSIONS OF SN74AC14-Q1 :

- Catalog : [SN74AC14](#)
- Military : [SN54AC14](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74AC14QPWRQ1	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74AC14QPWRQ1	TSSOP	PW	14	2000	356.0	356.0	35.0

GENERIC PACKAGE VIEW

BQA 14

WQFN - 0.8 mm max height

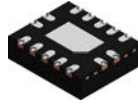
2.5 x 3, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



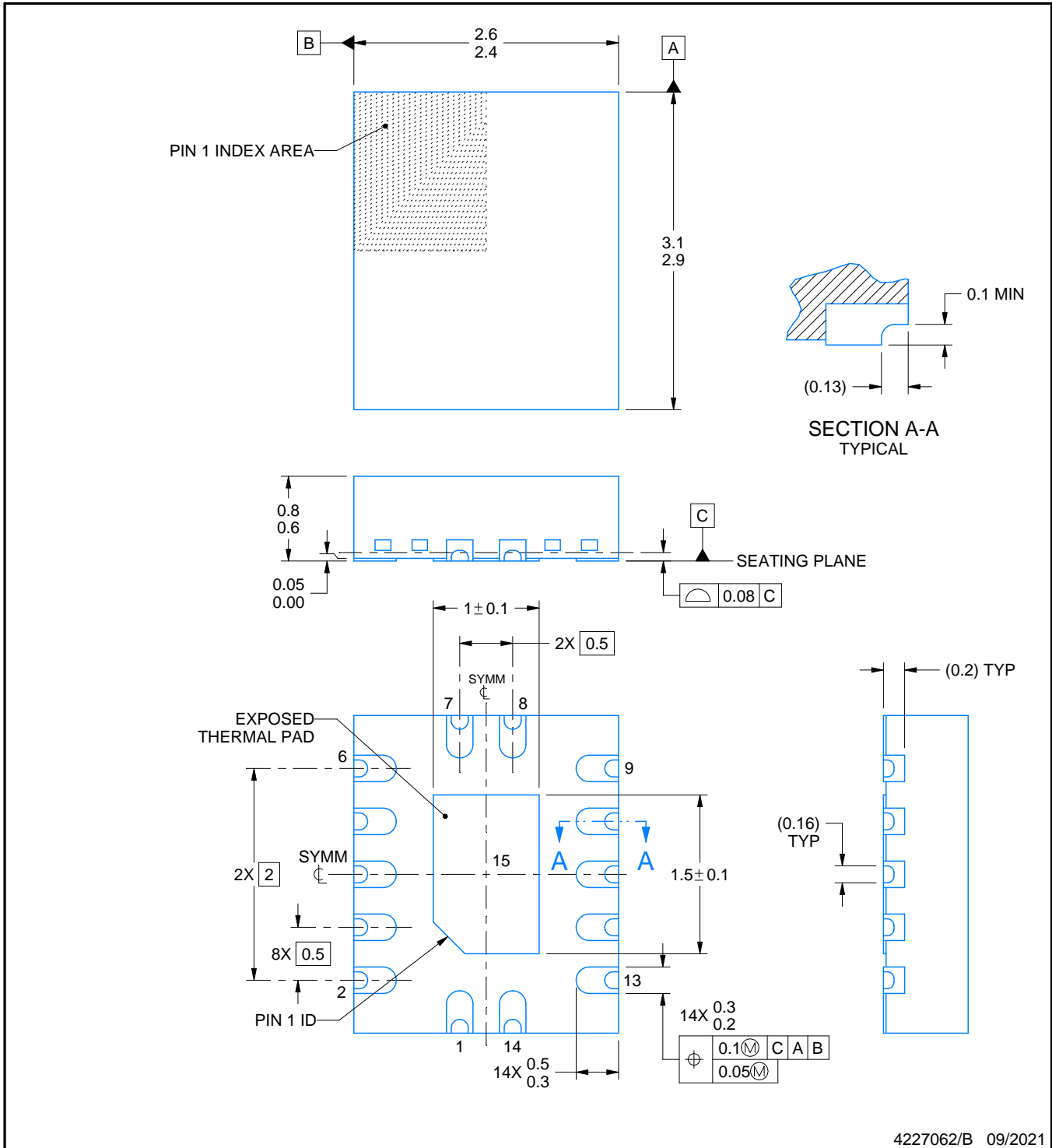
BQA0014B



PACKAGE OUTLINE

WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



NOTES:

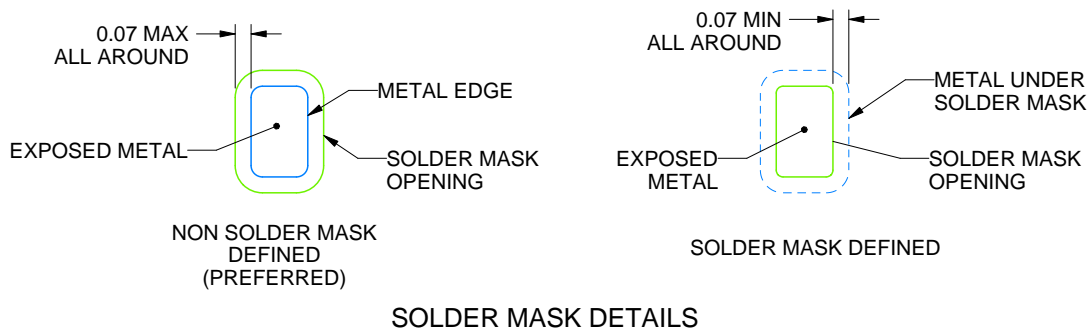
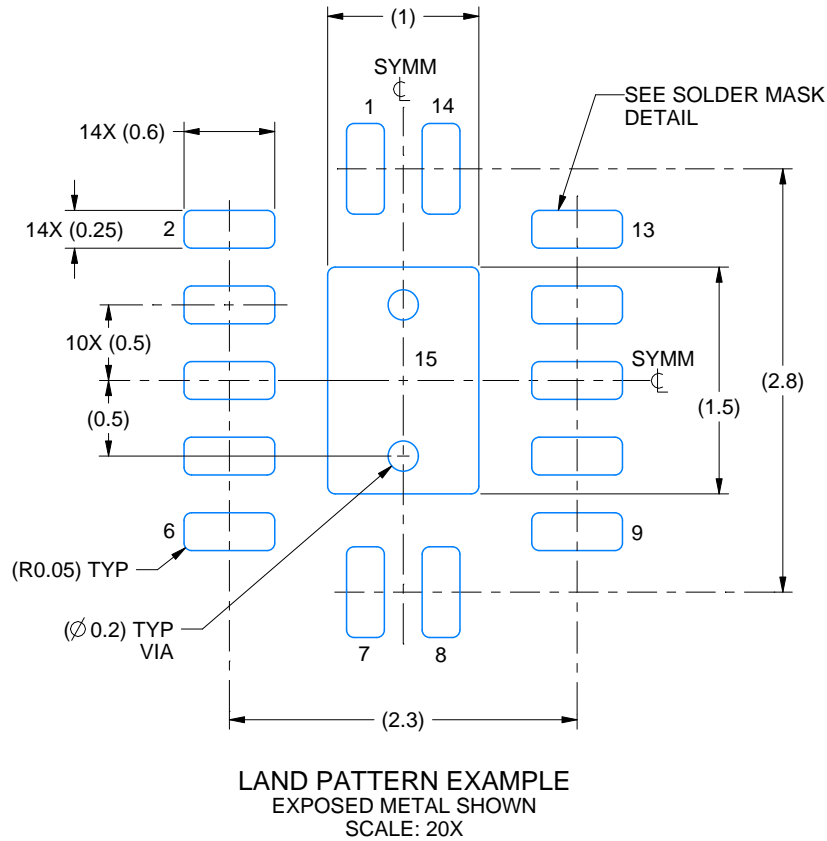
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

EXAMPLE BOARD LAYOUT

BQA0014B

WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



4227062/B 09/2021

NOTES: (continued)

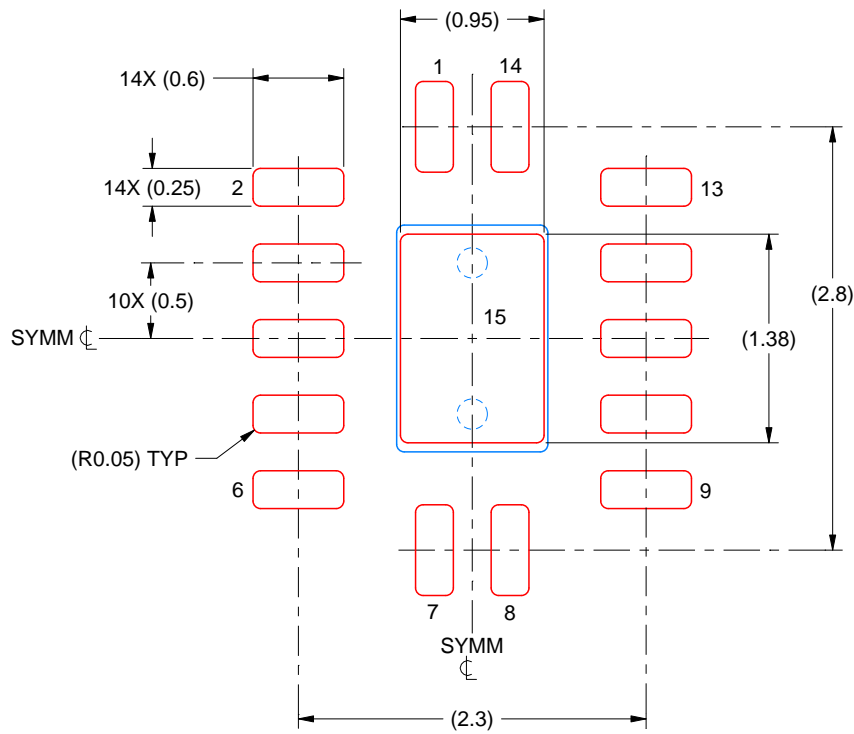
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/sluea271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

BQA0014B

WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 MM THICK STENCIL
SCALE: 20X

EXPOSED PAD 15
87% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE

4227062/B 09/2021

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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