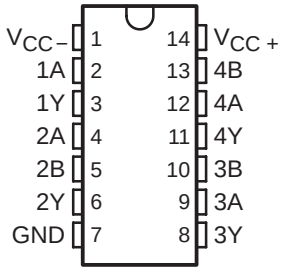
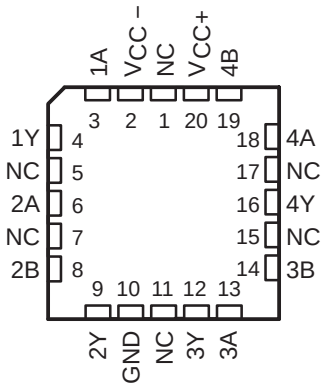
- **Meet or Exceed the Requirements of ANSI TIA/EIA-232-E and ITU Recommendation V.28**
- **Current-Limited Output: 10 mA Typical**
- **Power-Off Output Impedance: 300 Ω Minimum**
- **Slew Rate Control by Load Capacitor**
- **Flexible Supply-Voltage Range**
- **Input Compatible With Most TTL Circuits**

SN55188 . . . J OR W PACKAGE
SN75188 . . . D, N, OR NS PACKAGE
MC1488 . . . N PACKAGE
(TOP VIEW)



SN55188 . . . FK PACKAGE
(TOP VIEW)



NC − No internal connection

description/ordering information

The MC1488, SN55188, and SN75188 are monolithic quadruple line drivers designed to interface data terminal equipment with data communications equipment in conformance with ANSI TIA/EIA-232-E, using a diode in series with each supply-voltage terminal as shown under typical applications.

The SN55188 is characterized for operation over the full military temperature range of −55°C to 125°C. The MC1488 and SN75188 are characterized for operation from 0°C to 70°C.

ORDERING INFORMATION

T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
0°C to 70°C	PDIP (N)	Tube of 25	MC1488N	MC1488N
		Tube of 25	SN75188N	SN75188N
	SOIC (D)	Tube of 50	SN75188D	SN75188
		Reel of 2500	SN75188DR	
	SOP (NS)	Reel of 2000	SN75188NSR	SN75188
−55°C to 125°C	CDIP (J)	Tube of 25	SN55188J	SN55188J
			SNJ55188J	SNJ55188J
	CFP (W)	Tube of 150	SNJ55188W	SNJ55188W
	LCCC (FK)	Tube of 55	SNJ55188FK	SNJ55188FK

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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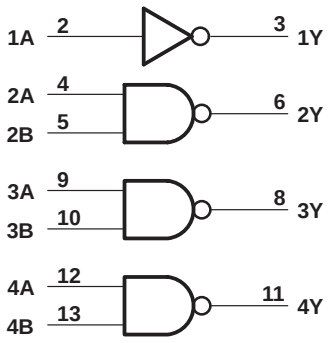
On products compliant to MIL-PRF-38535, all parameters are tested unless otherwise noted. On all other products, production processing does not necessarily include testing of all parameters.

FUNCTION TABLE
(drivers 2−4)

A	B	Y
H	H	L
L	X	H
X	L	H

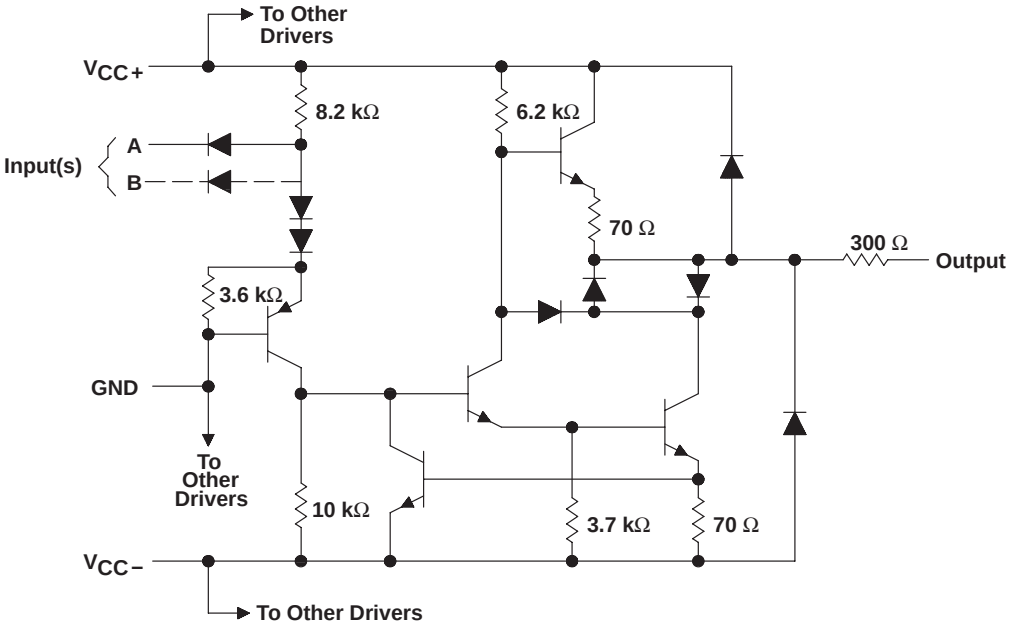
H = high level, L = low level,
X = irrelevant

logic diagram (positive logic)



Positive logic
$Y = \overline{A}$ (driver 1)
$Y = \overline{AB}$ or $\overline{A} + \overline{B}$ (drivers 2 thru 4)

schematic (each driver)



Resistor values shown are nominal.

absolute maximum ratings over operating free-air temperature (unless otherwise noted)†

Supply voltage, V_{CC+} at (or below) 25°C free-air temperature (see Notes 1 and 2) . . . . . 15 V
Supply voltage, V_{CC-} at (or below) 25°C free-air temperature (see Notes 1 and 2) . . . . . −15 V
Input voltage, V_I . . . . . −15 V to 7 V
Output voltage, V_O . . . . . −15 V to 15 V
Continuous total power dissipation (see Note 2) . . . . . See Dissipation Rating Table
Package thermal impedance, θ_{JA} (see Notes 3 and 4): D package . . . . . 86°C/W
N package . . . . . 80°C/W
NS package . . . . . 76°C/W
Operating virtual junction temperature, T_J . . . . . 150°C
Case temperature for 60 seconds, FK package . . . . . 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: J or W package . . . . . 300°C
Storage temperature range, T_{stg} . . . . . −65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values are with respect to the network ground terminal.
2. For operation above 25°C free-air temperature, refer to the maximum supply voltage curve, Figure 6. In the J package, SN55188 chips are alloy mounted.
3. Maximum power dissipation is a function of $T_J(max)$, θ_{JA}, and T_A. The maximum allowable power dissipation at any allowable ambient temperature is $P_D = (T_J(max) - T_A)/\theta_{JA}$. Selecting the maximum of 150°C can affect reliability.
4. The package thermal impedance is calculated in accordance with JESD 51-7.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 125°C$ POWER RATING
FK	1375 mW	11.0 mW/°C	880 mW	275 mW
J	1375 mW	11.0 mW/°C	880 mW	275 mW
W	1000 mW	8.0 mW/°C	640 mW	200 mW

recommended operating conditions

		SN55188			MC1488, SN75188			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC+}	Supply voltage	7.5	9	15	7.5	9	15	V
V_{CC-}	Supply voltage	−7.5	−9	−15	−7.5	−9	−15	V
V_{IH}	High-level input voltage	1.9			1.9			V
V_{IL}	Low-level input voltage			0.8			0.8	V
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over operating free-air temperature range, $V_{CC\pm}$ = ±9 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN55188			MC1488, SN75188			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{OH}	High-level output voltage	V_{IL} = 0.8 V, R_L = 3 kΩ	V_{CC+} = 9 V, V_{CC-} = −9 V	6	7		6	7		V
			V_{CC+} = 13.2 V, V_{CC-} = −13.2 V	9	10.5		9	10.5		
V_{OL}	Low-level output voltage	V_{IH} = 1.9 V, R_L = 3 kΩ	V_{CC+} = 9 V, V_{CC-} = −9 V		−7‡	−6		−7	−6	V
			V_{CC+} = 13.2 V, V_{CC-} = −13.2 V		−10.5‡	−9		−10.5	−9	
I_{IH}	High-level input current	V_I = 5 V				10			10	μA
I_{IL}	Low-level input current	V_I = 0			−1	−1.6		−1	−1.6	mA
$I_{OS(H)}$	Short-circuit output current at high level§	V_I = 0.8 V,	V_O = 0	−4.6	−9	−13.5	−6	−9	−12	mA
$I_{OS(L)}$	Short-circuit output current at low level§	V_I = 1.9 V,	V_O = 0	4.6	9	13.5	6	9	12	mA
r_o	Output resistance, power off	V_{CC+} = 0, V_O = −2 V to 2 V	V_{CC-} = 0,	300			300			Ω
I_{CC+}	Supply current from V_{CC+}	V_{CC+} = 9 V, No load	All inputs at 1.9 V		15	20		15	20	mA
			All inputs at 0.8 V		4.5	6		4.5	6	
		V_{CC+} = 12 V, No load	All inputs at 1.9 V		19	25		19	25	
			All inputs at 0.8 V		5.5	7		5.5	7	
		V_{CC+} = 15 V, No load, T_A = 25°C	All inputs at 1.9 V			34			34	
			All inputs at 0.8 V			12			12	
I_{CC-}	Supply current from I_{CC-}	V_{CC-} = −9 V, No load	All inputs at 1.9 V		−13	−17		−13	−17	mA
			All inputs at 0.8 V			−0.5			−0.015	
		V_{CC-} = −12 V, No load	All inputs at 1.9 V		−18	−23		−18	−23	
			All inputs at 0.8 V			−0.5			−0.015	
		V_{CC-} = −15 V, No load, T_A = 25°C	All inputs at 1.9 V			−34			−34	
			All inputs at 0.8 V			−2.5			−2.5	
P_D	Total power dissipation	V_{CC+} = 9 V, No load	V_{CC-} = −9 V,			333			333	mW
		V_{CC+} = 12 V, No load	V_{CC-} = −12 V,			576			576	

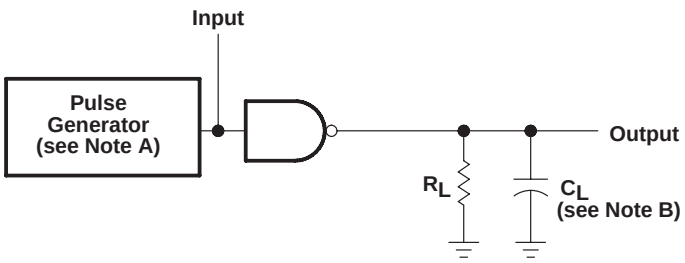
† All typical values are at T_A = 25°C.
‡ The algebraic convention, in which the less positive (more negative) limit is designated as minimum, is used in this data sheet for logic voltage levels only, e.g., if −6 V is a maximum, the typical value is a more negative voltage.
§ Not more than one output should be shorted at a time.

switching characteristics, $V_{CC\pm}$ = ±9 V, T_A = 25°C

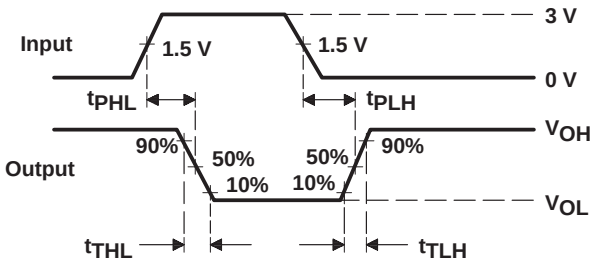
PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low- to high-level output	R_L = 3 kΩ, See Figure 1	C_L = 15 pF,		220	350	ns
t_{PHL}	Propagation delay time, high- to low-level output				100	175	ns
t_{TLH}	Transition time, low- to high-level output†				55	100	ns
t_{THL}	Transition time, high- to low-level output†				45	75	ns
t_{TLH}	Transition time, low- to high-level output‡	R_L = 3 kΩ to 7 kΩ, See Figure 1	C_L = 2500 pF,		2.5		µs
t_{THL}	Transition time, high- to low-level output‡				3.0		µs

† Measured between 10% and 90% points of output waveform
‡ Measured between 3 V and −3 V points on the output waveform (TIA/EIA-232-E conditions)

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT



VOLTAGE WAVEFORMS

NOTES: A. The pulse generator has the following characteristics: t_W = 0.5 µs, PRR ≤ 1 MHz, Z_O = 50 Ω.
B. C_L includes probe and jig capacitance.

Figure 1. Test Circuit and Voltage Waveforms

TYPICAL CHARACTERISTICS†

VOLTAGE TRANSFER CHARACTERISTICS

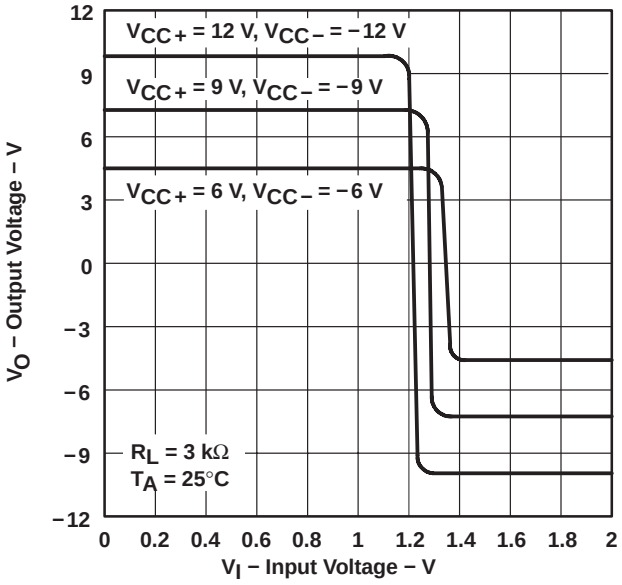


Figure 2

OUPUT CURRENT
vs
OUTPUT VOLTAGE

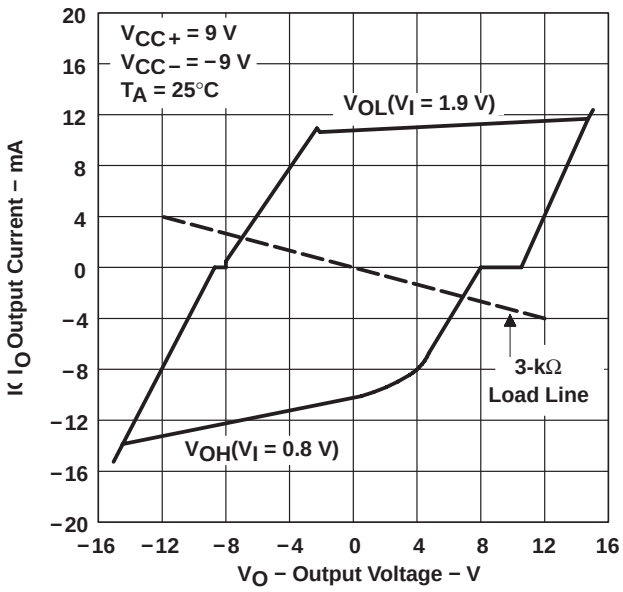


Figure 3

SHORT-CIRCUT OUTPUT CURRENT
vs
FREE-AIR TEMPERATURE

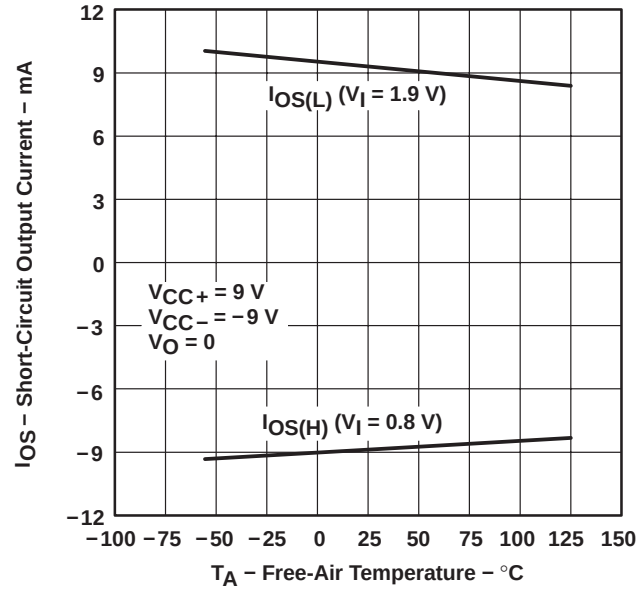


Figure 4

SLEW RATE
vs
LOAD CAPACITANCE

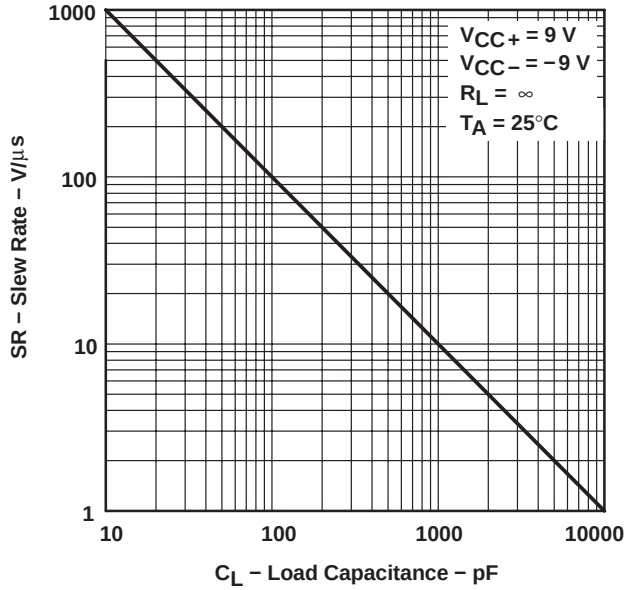


Figure 5

† Data for temperatures below 0°C and above 70°C are applicable to SN55188 circuit only.

THERMAL INFORMATION†

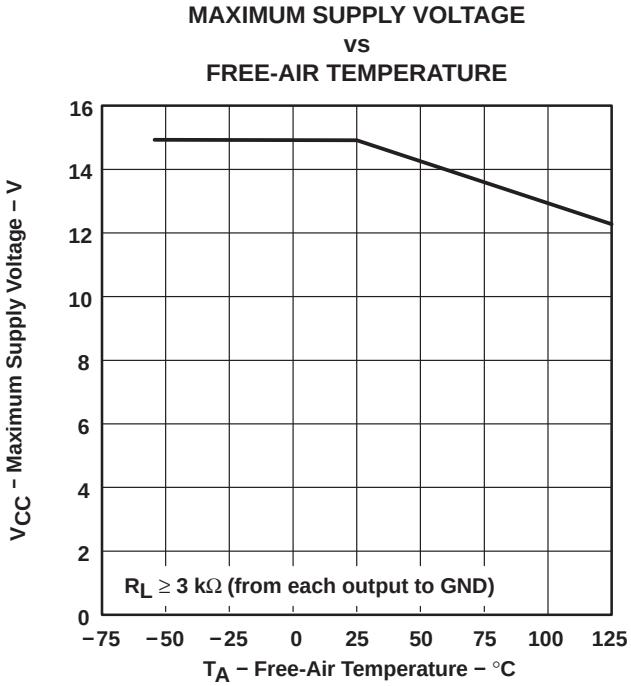


Figure 6

† Data for temperatures below 0°C and above 70°C are applicable to the SN55188 circuit only.

APPLICATION INFORMATION

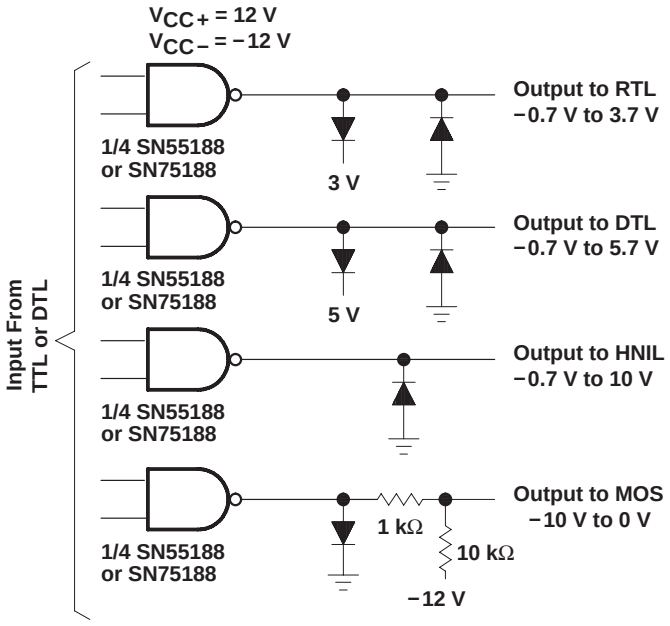
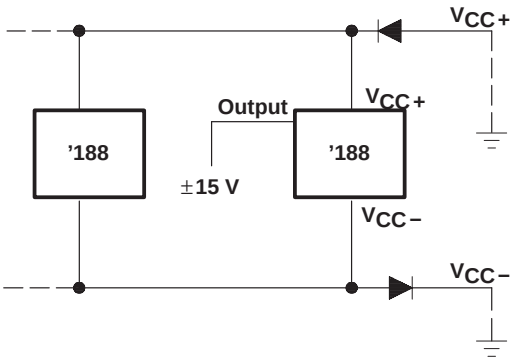


Figure 7. Logic Translator Applications



Diodes placed in series with the V_{CC+} and V_{CC-} leads protect the SN55188/SN75188 in the fault condition in which the device outputs are shorted to ±15 V, and the power supplies are at low voltage and provide low-impedance paths to ground.

Figure 8. Power-Supply Protection to Meet Power-Off Fault Conditions of ANSI TIA/EIA-232-E

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
5962-86889012A	Active	Production	LCCC (FK) | 20	55 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-86889012A SNJ55188FK
5962-8688901CA	Active	Production	CDIP (J) | 14	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-8688901CA SNJ55188J
5962-8688901DA	Active	Production	CFP (W) | 14	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-8688901DA SNJ55188W
MC1488N	Obsolete	Production	PDIP (N) | 14	-	-	Call TI	Call TI	0 to 70	MC1488N
SN55188J	Active	Production	CDIP (J) | 14	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	SN55188J
SN55188J.A	Active	Production	CDIP (J) | 14	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	SN55188J
SN75188D	Obsolete	Production	SOIC (D) | 14	-	-	Call TI	Call TI	0 to 70	SN75188
SN75188DR	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	SN75188
SN75188DR.A	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	SN75188
SN75188N	Active	Production	PDIP (N) | 14	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	SN75188N
SN75188N.A	Active	Production	PDIP (N) | 14	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	SN75188N
SN75188NSR	Active	Production	SOP (NS) | 14	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	SN75188
SN75188NSR.A	Active	Production	SOP (NS) | 14	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	SN75188
SNJ55188FK	Active	Production	LCCC (FK) | 20	55 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-86889012A SNJ55188FK
SNJ55188FK.A	Active	Production	LCCC (FK) | 20	55 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-86889012A SNJ55188FK
SNJ55188J	Active	Production	CDIP (J) | 14	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-8688901CA SNJ55188J
SNJ55188J.A	Active	Production	CDIP (J) | 14	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-8688901CA SNJ55188J
SNJ55188W	Active	Production	CFP (W) | 14	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-8688901DA SNJ55188W

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SNJ55188W.A	Active	Production	CFP (W) | 14	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-8688901DA SNJ55188W

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF SN55188, SN75188 :

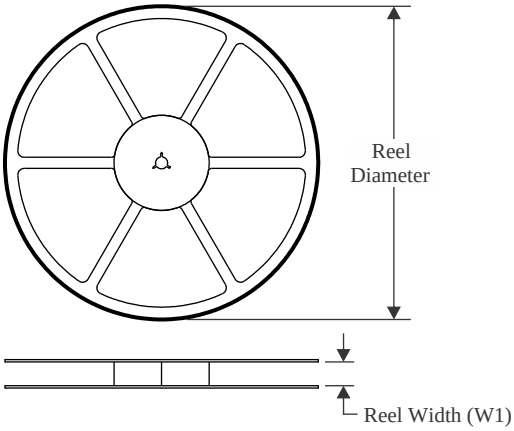
- Catalog : SN75188
- Military : SN55188

NOTE: Qualified Version Definitions:

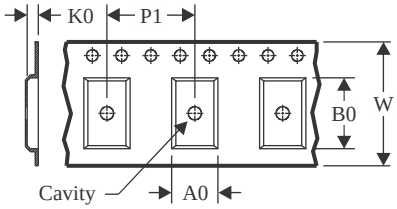
- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION

REEL DIMENSIONS

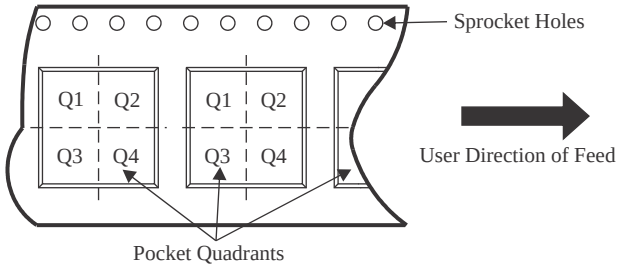


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

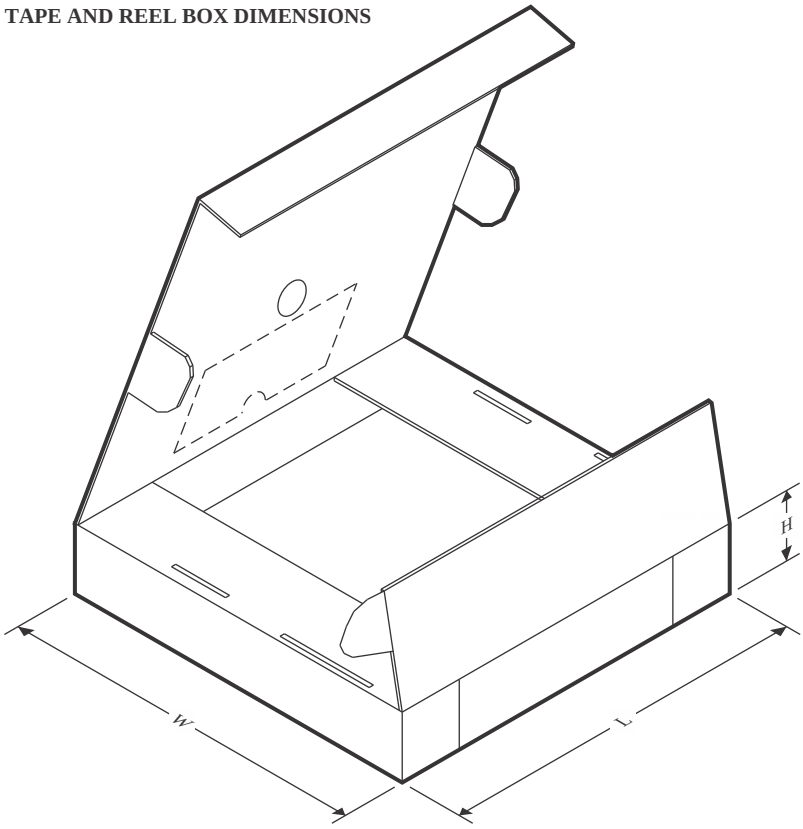
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN75188DR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN75188NSR	SOP	NS	14	2000	330.0	16.4	8.1	10.4	2.5	12.0	16.0	Q1

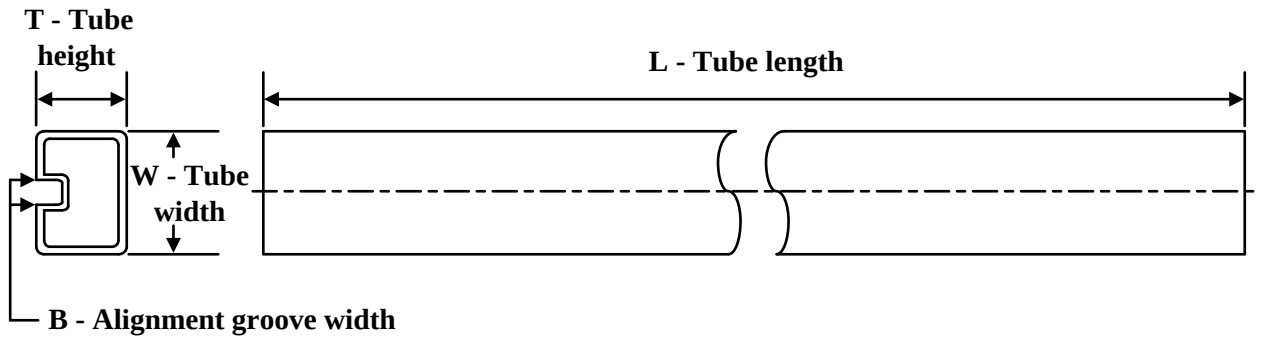
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

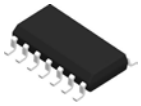
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN75188DR	SOIC	D	14	2500	353.0	353.0	32.0
SN75188NSR	SOP	NS	14	2000	353.0	353.0	32.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
5962-86889012A	FK	LCCC	20	55	506.98	12.06	2030	NA
5962-8688901DA	W	CFP	14	25	506.98	26.16	6220	NA
SN75188N	N	PDIP	14	25	506	13.97	11230	4.32
SN75188N	N	PDIP	14	25	506	13.97	11230	4.32
SN75188N.A	N	PDIP	14	25	506	13.97	11230	4.32
SN75188N.A	N	PDIP	14	25	506	13.97	11230	4.32
SNJ55188FK	FK	LCCC	20	55	506.98	12.06	2030	NA
SNJ55188FK.A	FK	LCCC	20	55	506.98	12.06	2030	NA
SNJ55188W	W	CFP	14	25	506.98	26.16	6220	NA
SNJ55188W.A	W	CFP	14	25	506.98	26.16	6220	NA

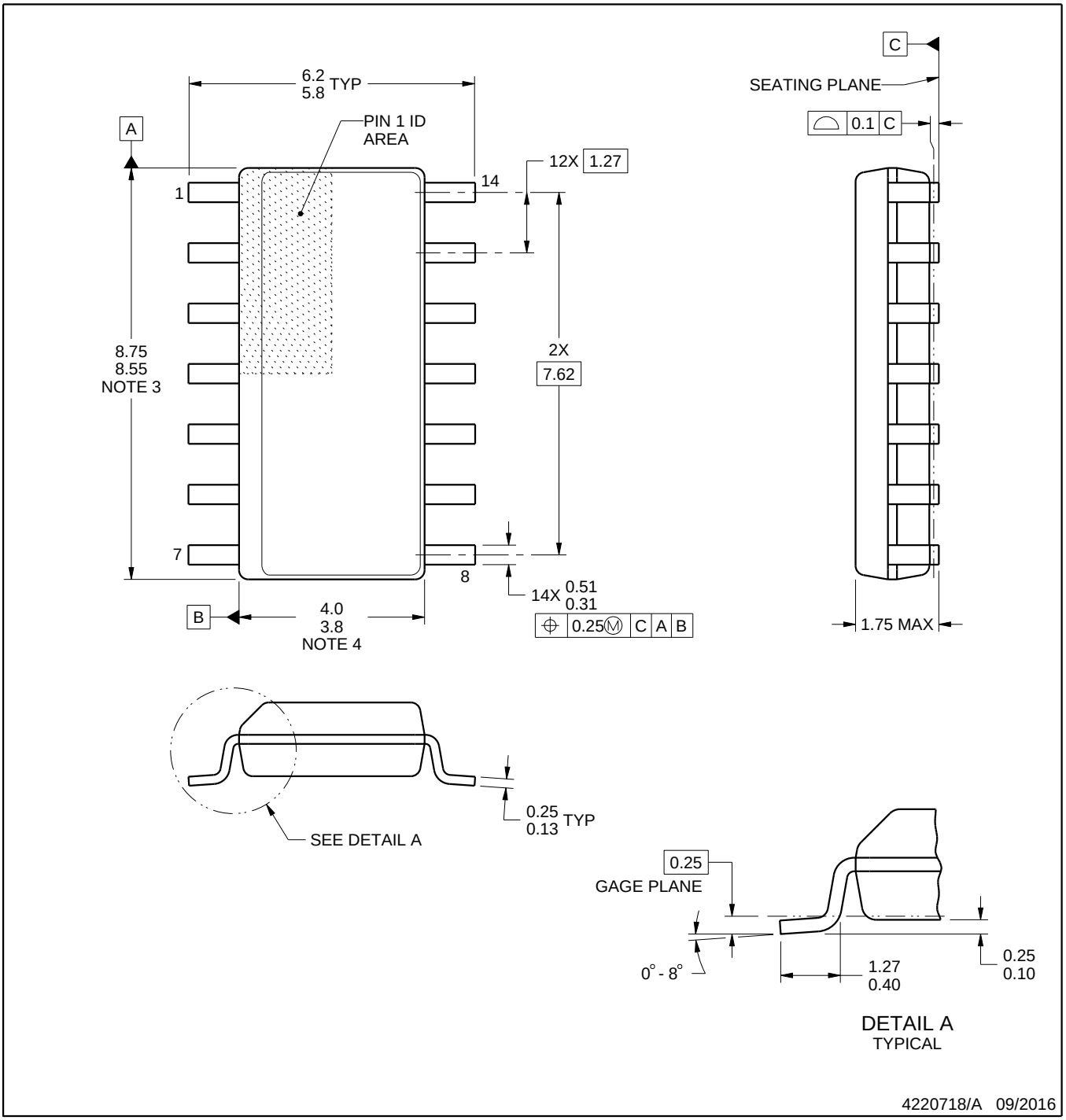


PACKAGE OUTLINE

D0014A

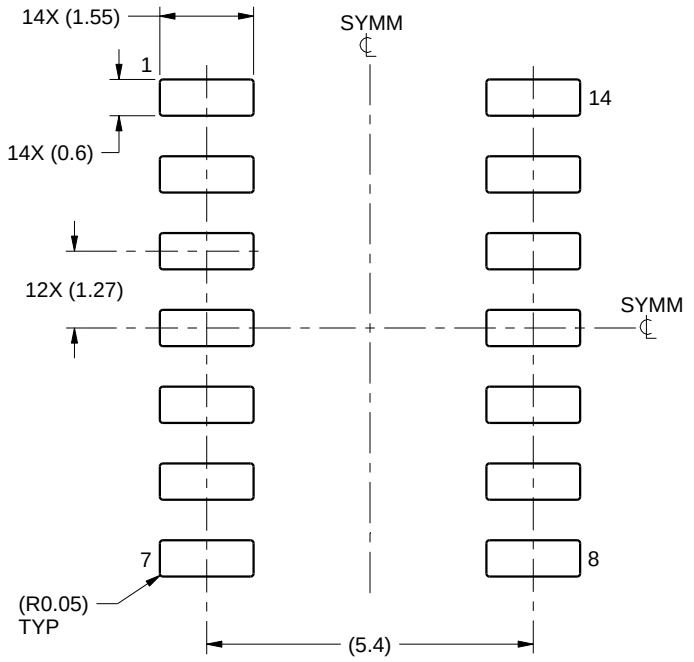
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

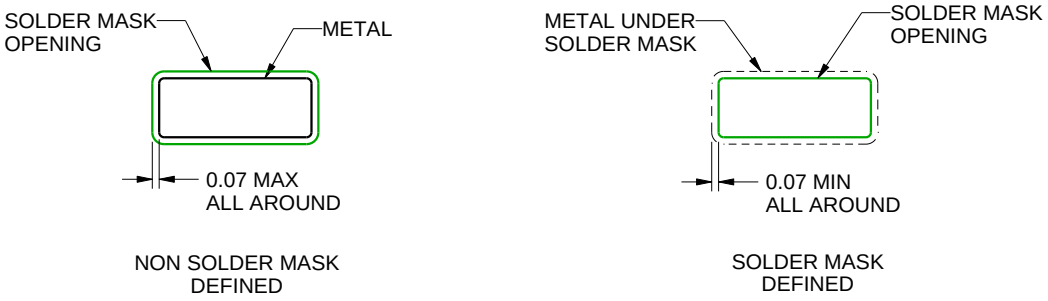


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm, per side.
5. Reference JEDEC registration MS-012, variation AB.



LAND PATTERN EXAMPLE
SCALE:8X



SOLDER MASK DETAILS

4220718/A 09/2016

NOTES: (continued)

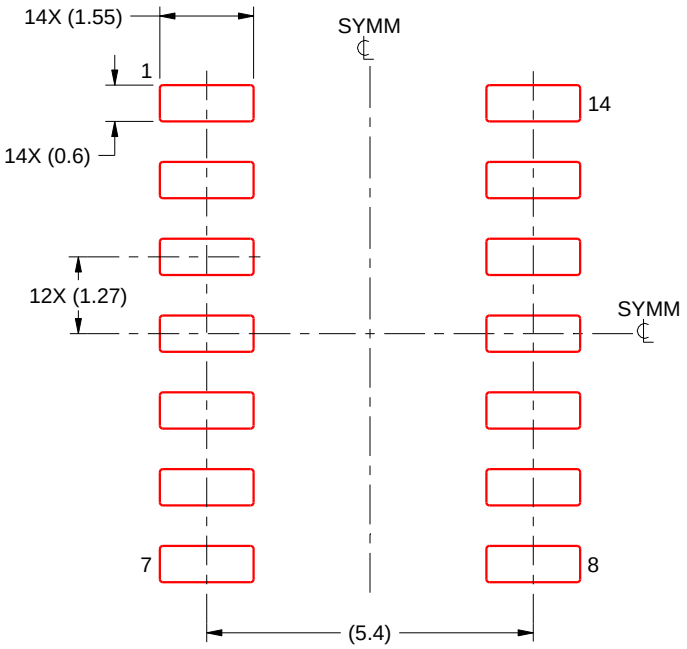
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:8X

4220718/A 09/2016

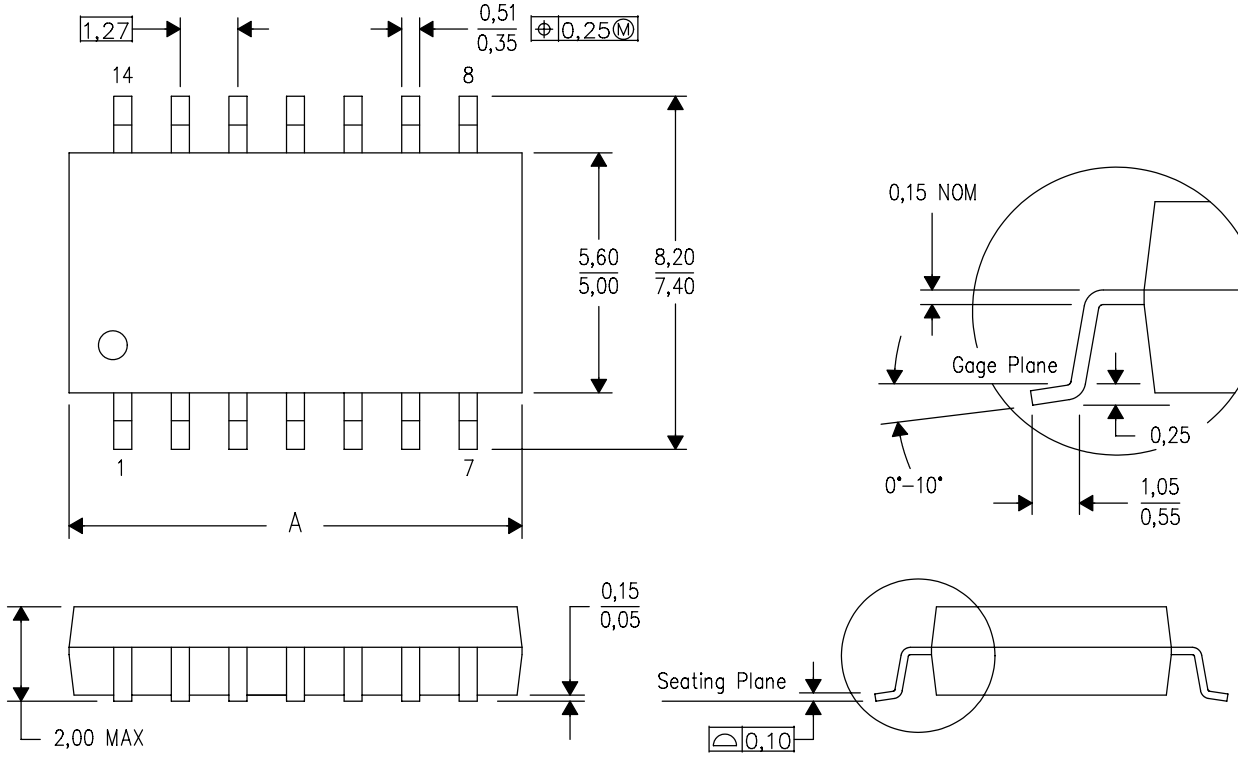
NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

MECHANICAL DATA

NS (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14-PINS SHOWN

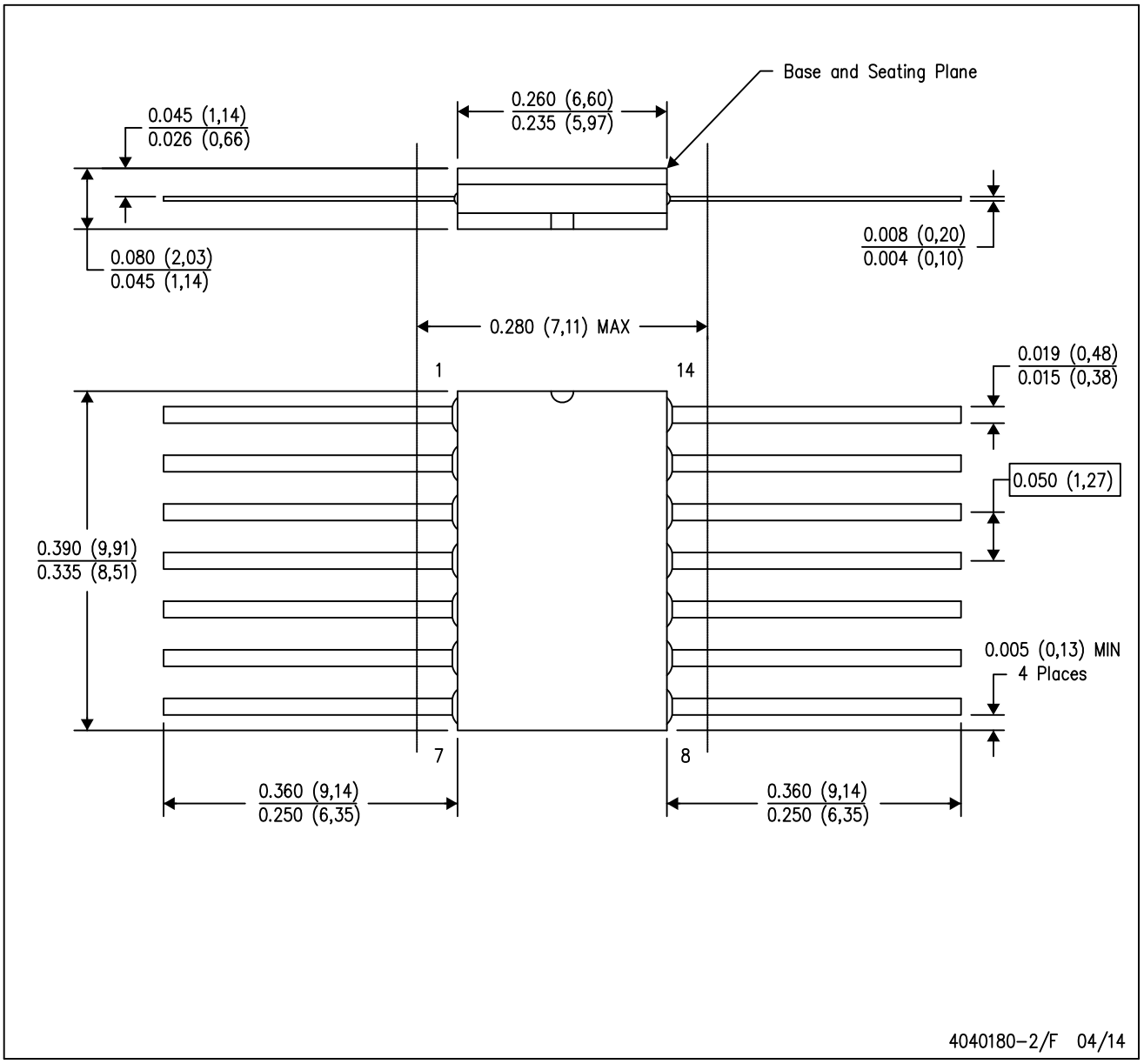


DIM \ PINS **	14	16	20	24
A MAX	10,50	10,50	12,90	15,30
A MIN	9,90	9,90	12,30	14,70

4040062/C 03/03

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

W (R–GDFP–F14) CERAMIC DUAL FLATPACK



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only.
E. Falls within MIL STD 1835 GDFP1–F14

GENERIC PACKAGE VIEW

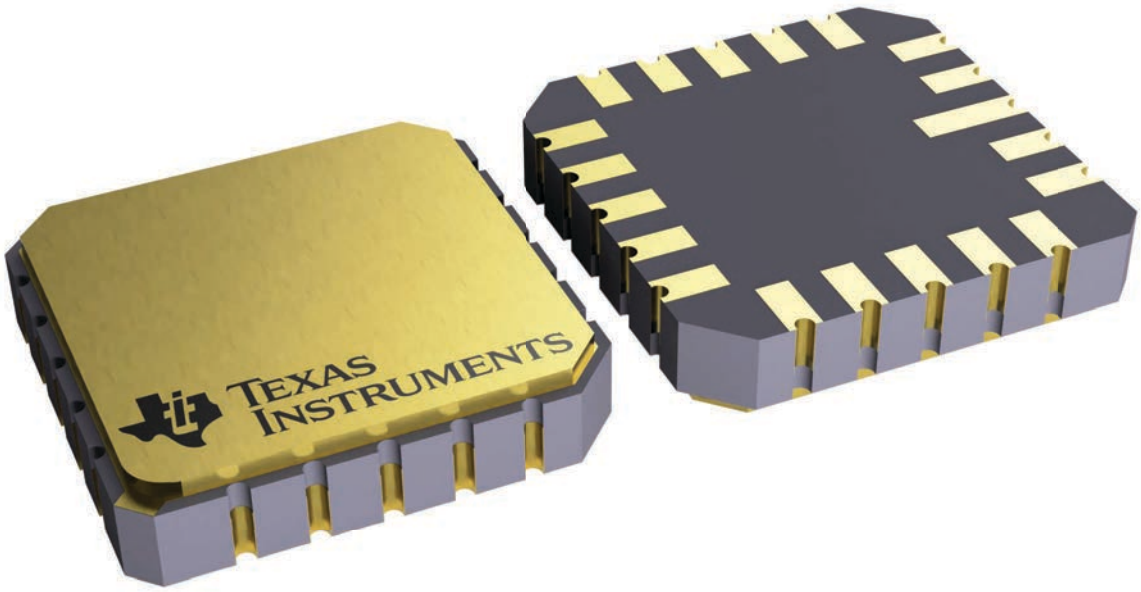
FK 20

LCCC - 2.03 mm max height

8.89 x 8.89, 1.27 mm pitch

LEADLESS CERAMIC CHIP CARRIER

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

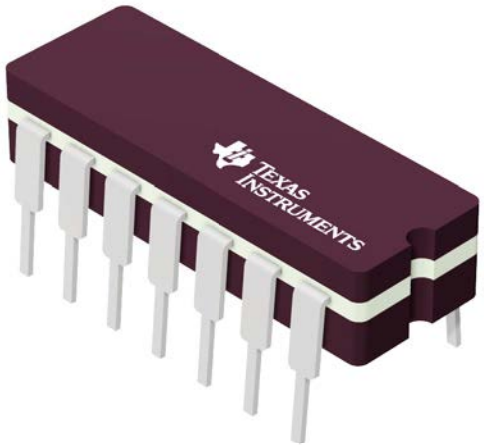


4229370VA\

GENERIC PACKAGE VIEW

J 14 CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

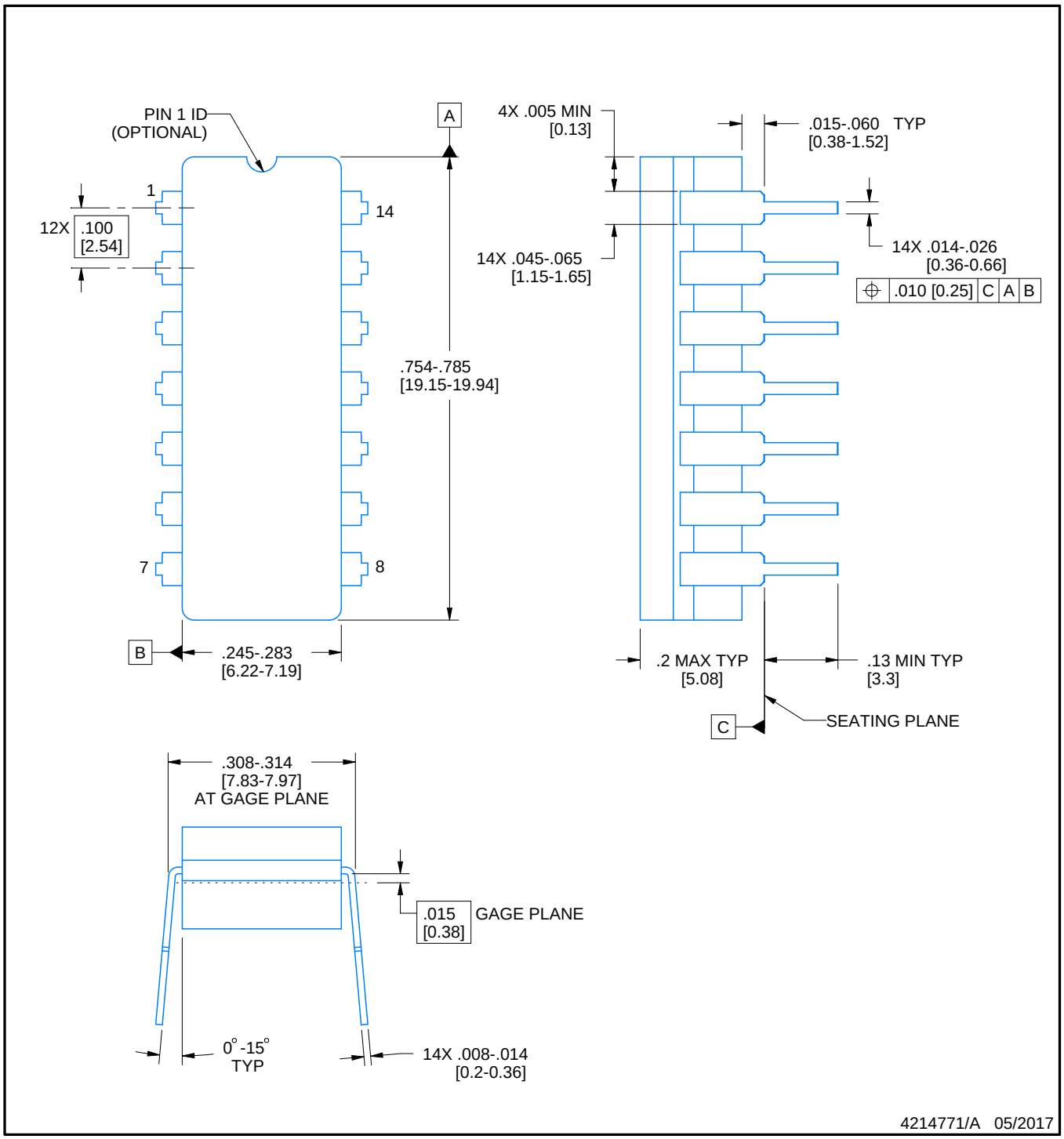
4040083-5/G

PACKAGE OUTLINE

J0014A

CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



NOTES:

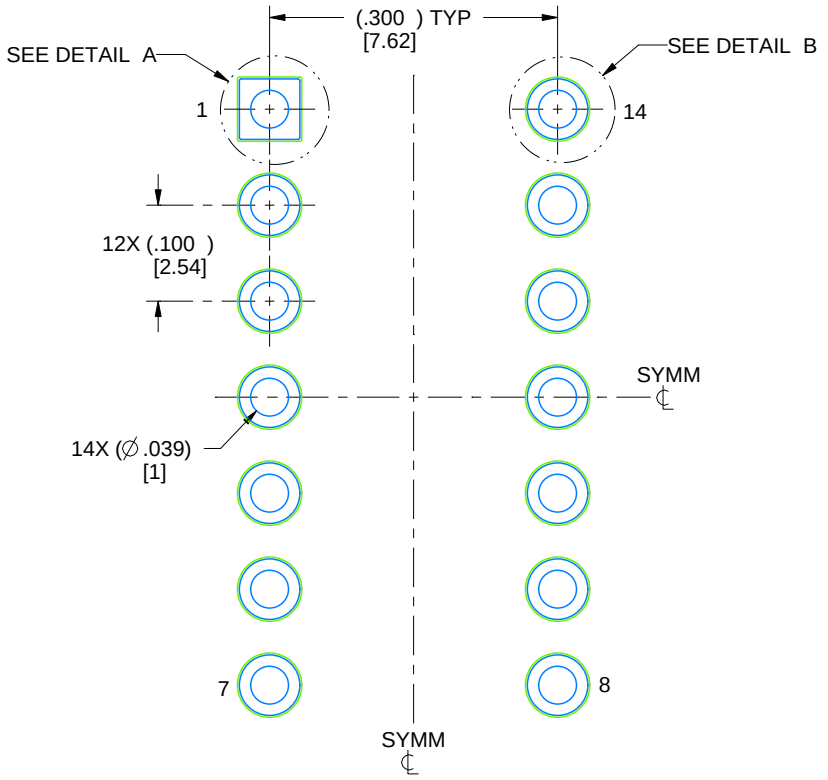
1. All controlling linear dimensions are in inches. Dimensions in brackets are in millimeters. Any dimension in brackets or parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This package is hermitically sealed with a ceramic lid using glass frit.
4. Index point is provided on cap for terminal identification only and on press ceramic glass frit seal only.
5. Falls within MIL-STD-1835 and GDIP1-T14.

EXAMPLE BOARD LAYOUT

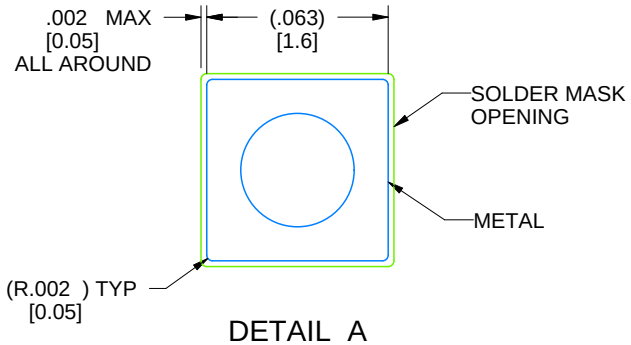
J0014A

CDIP - 5.08 mm max height

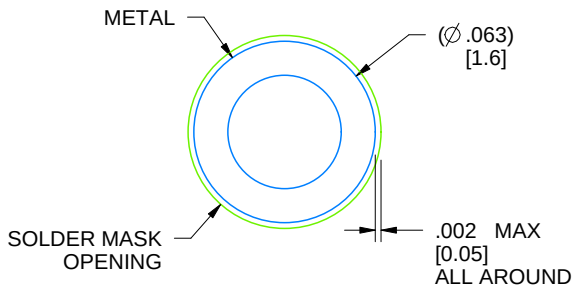
CERAMIC DUAL IN LINE PACKAGE



LAND PATTERN EXAMPLE
NON-SOLDER MASK DEFINED
SCALE: 5X



DETAIL A
SCALE: 15X



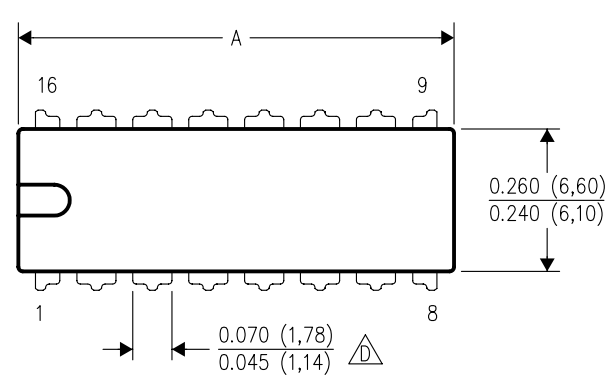
DETAIL B
13X, SCALE: 15X

4214771/A 05/2017

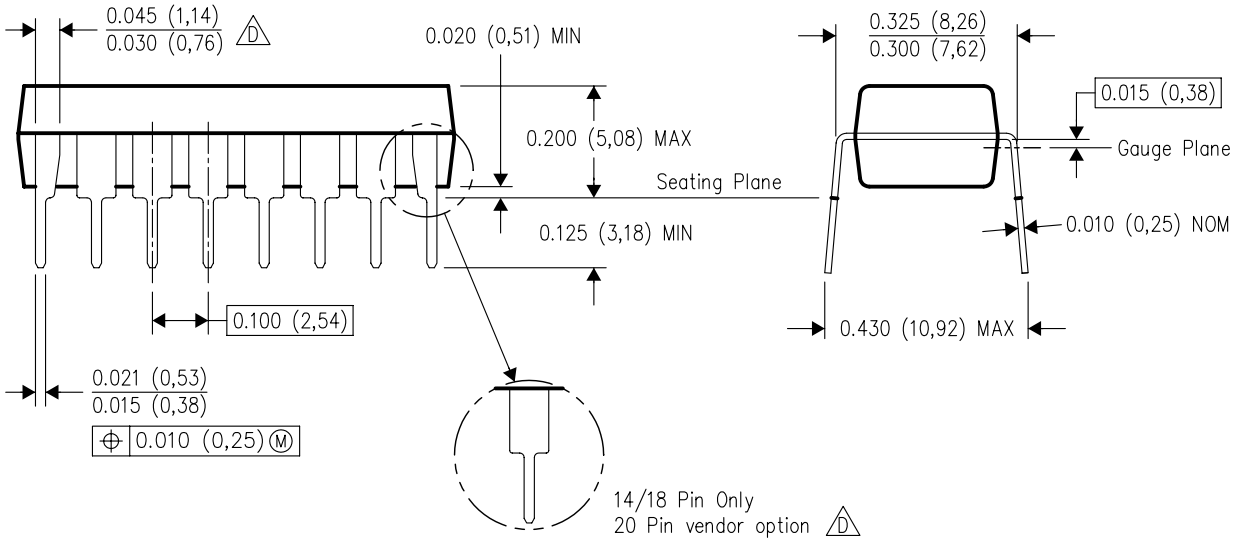
N (R–PDIP–T**)

PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN



DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS–001 VARIATION (C)	AA	BB	AC	AD



4040049/E 12/2002

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

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