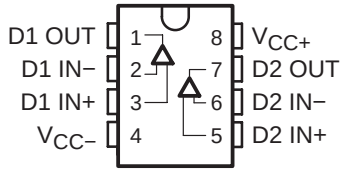
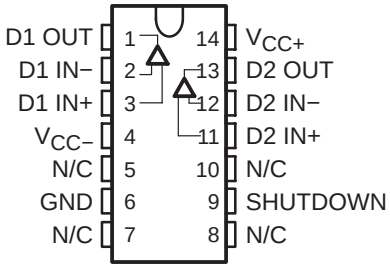
- **Remote Terminal ADSL Line Driver**
  - **Ideal for Both Full Rate ADSL and G.Lite**
  - **Compatible With 1:2 Transformer Ratio**
- **Wide Supply Voltage Range +5 V to +14 V**
  - **Ideal for Single Supply +12-V Operation**
- **Low 2.1 pA/$\sqrt{\text{Hz}}$ Noninverting Current Noise**
  - **Reduces Noise Feedback Through Hybrid Into Downstream Channel**
- **Wide Output Swing**
  - **18.4 Vpp Differential Output Voltage, R_L = 50 Ω, 12-V Single Supply**
- **High Output Current**
  - **275 mA (typ)**
- **High Speed**
  - **100 MHz (−3 dB, G=1, 12-V Single Supply)**
  - **600 V/μs Slew Rate (G = 4, 12-V Single Supply)**
- **Low Distortion, Single-Ended, G = 4**
  - **−72 dBc (250 kHz, 2 Vpp, 25 Ω load)**
  - **−78 dBc (250 kHz, 2 Vpp, 100 Ω load)**
- **Low Power Shutdown (THS6093)**
  - **300 μA Total Standby Current**
- **Thermal Shutdown and Short Circuit Protection**
- **Standard SOIC, SOIC PowerPAD™, and TSSOP PowerPAD™ Package**
- **Evaluation Module Available**

THS6092
SOIC (D) AND
SOIC PowerPAD™ (DDA) PACKAGE
(TOP VIEW)

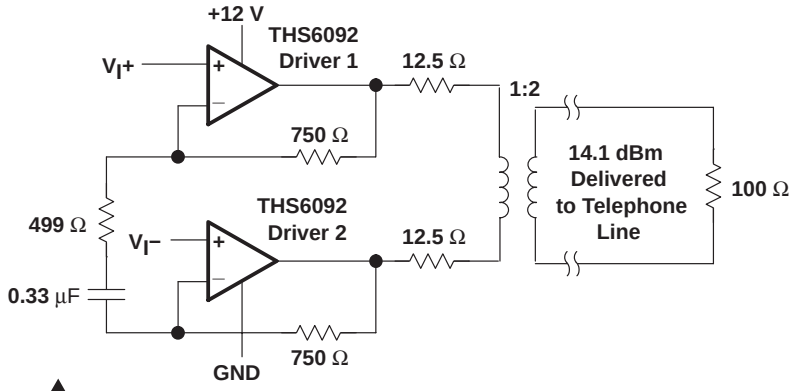


THS6093
SOIC (D) AND
TSSOP PowerPAD™ (PWP) PACKAGE
(TOP VIEW)



description

The THS6092/3 is a high-speed line driver ideal for driving signals from the remote terminal to the central office in asymmetrical digital subscriber line (ADSL) applications. It can operate from a single +12-V supply voltage while drawing only 7.3 mA of supply current per channel. It offers low –72 dBc total harmonic distortion driving a 25-Ω load (2 Vpp). The THS6092/3 offers a high 18.4-Vpp differential output swing across a 50-Ω load from a single +12-V supply. The THS6093 features a low-power shutdown mode, consuming only 300 μA quiescent current per channel. The THS6092/3 is packaged in a standard SOIC, SOIC PowerPAD™, and TSSOP PowerPAD™ package.



RELATED PRODUCTS

DEVICE	DESCRIPTION
THS6042/3	350-mA, ±12 ADSL CPE line driver
THS6052/3	175-mA, ±12 V ADSL CPE line driver
OPA2677	380-mA, +12 V ADSL CPE line driver
THS6062	Low noise ADSL receiver

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PowerPAD is a trademark of Texas Instruments.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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AVAILABLE OPTIONS

T_A	PACKAGED DEVICE				EVALUATION MODULES
	SOIC-8† (D)	SOIC-8† PowerPAD (DDA)	SOIC-14† (D)	TSSOP-14† PowerPAD (PWP)	
0°C to 70°C	THS6092CD	THS6092CDDA	THS6093CD	THS6093CPWP	THS6092EVM THS6093EVM
−40°C to 85°C	THS6092ID	THS6092IDDA	THS6093ID	THS6093IPWP	—

† All packages are available taped and reeled. Add an R-suffix to the device type (i.e., THS6092IDR).

absolute maximum ratings over operating free-air temperature (unless otherwise noted)†

Supply voltage, V_{CC+} to V_{CC-} . . . . . 14.7 V
Input voltage . . . . . ± V_{CC}
Output current (see Note 1) . . . . . 350 mA
Differential input voltage . . . . . ± 3 V
Maximum junction temperature . . . . . 150°C
Total power dissipation at (or below) 25°C free-air temperature . . . . . See Dissipation Ratings Table
Operating free-air temperature, T_A: Commercial . . . . . 0°C to 70°C
Industrial . . . . . −40°C to 85°C
Storage temperature, T_{stg} : Commercial . . . . . −65°C to 125°C
Industrial . . . . . −65°C to 125°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 300°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The THS6092 and THS6093 may incorporate a PowerPAD™ on the underside of the chip. This acts as a heatsink and must be connected to a thermally dissipating plane for proper power dissipation. Failure to do so may result in exceeding the maximum junction temperature which could permanently damage the device. See TI Technical Brief SLMA002 for more information about utilizing the PowerPAD™ thermally enhanced package.

DISSIPATION RATING TABLE

PACKAGE	θ_{JA}	θ_{JC}	T_A = 25°C§ POWER RATING	T_A = 70°C§ POWER RATING	T_A = 85°C§ POWER RATING
D-8	95°C/W‡	38.3°C/W‡	1.1 W	0.63 W	0.47 W
DDA	45.8°C/W	9.2°C/W	2.3 W	1.31 W	0.98 W
D-14	66.6°C/W‡	26.9°C/W‡	1.6 W	0.90 W	0.68 W
PWP	37.5°C/W	1.4°C/W	2.8 W	1.60 W	1.20 W

‡ This data was taken using the JEDEC proposed high-K test PCB. For the JEDEC low-K test PCB, the Θ_{JA} is168°C/W for the D−8 package and 122.3°C/W for the D−14 package.

§ Power rating is determined with a junction temperature of 130°C. This is the point where distortion starts to substantially increase. Thermal management of the final PCB should strive to keep the junction temperature at or below 125°C for best performance.

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC+} to V_{CC-}	Dual supply	±2.5		±7	V
	Single supply	+5		+14	
Operating free-air temperature, T_A	C-suffix	0		70	°C
	I-suffix	−40		85	

electrical characteristics over recommended operating free-air temperature range, T_A = 25°C, V_{CC+} = 12 V, V_{CC-} = GND, $R_{FEEDBACK}$ = 750 Ω, R_L = 25 Ω (unless otherwise noted)

dynamic performance

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
BW	Small-signal bandwidth (−3 dB) G=1	V_{CC} = 12 V		100		MHz
		V_{CC} = 5 V		90		
SR	Slew rate (see Note 2)	V_{CC} = 12 V		600		V/μs
		V_{CC} = 5 V		400		

NOTE 2: Slew rate is defined from the 25% to the 75% output levels.

noise/distortion performance

PARAMETER			TEST CONDITIONS		MIN	TYP	MAX	UNIT
THD	Total harmonic distortion (single-ended configuration)		Gain = 4, R_L = 25 Ω, V_{CC} = 5 V, f = 250 kHz	$V_{O(pp)}$ = 2 V		−70		dBc
			Gain = 4, R_L = 25 Ω, V_{CC} = 12 V, f = 250 kHz	$V_{O(pp)}$= 2 V		−72		
				$V_{O(pp)}$= 7 V		−68		
V_n	Input voltage noise		V_{CC} = 12 V, 5 V, f = 10 kHz			2.1		nV/√Hz
I_n	Input current noise	+Input	V_{CC} = 12 V, 5 V, f = 10 kHz			2.1		pA/√Hz
		−Input				10.9		
X_T	Crosstalk		f = 250 kHz, G = 4, V_O = 2 Vpp, R_L= 25 Ω	V_{CC} = 5 V		−65		dBc
				V_{CC} = 12 V		−63		

dc performance

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{OS}	Input offset voltage	V_{CC} = 12 V, 5 V	T_A = 25°C		6	16	mV
			T_A = full range			21	
	Differential offset voltage		T_A = 25°C		1	6	
			T_A = full range			8	
	Offset drift		T_A = full range		20		μV/°C
I_{IB}	− Input bias current	V_{CC} = 12 V, 5 V	T_A = 25°C		3	10	μA
			T_A = full range			12	
	+ Input bias current		T_A = 25°C		1	6	
			T_A = full range			7	
	Differential input bias current		T_A = 25°C		3	10	
			T_A = full range			12	
Z_{OL}	Open loop transimpedance	R_L = 1 kΩ	V_{CC} = 12 V, 5 V		0.9		MΩ

electrical characteristics over recommended operating free-air temperature range, T_A = 25°C, V_{CC+} = 12 V, V_{CC-} = GND, $R_{FEEDBACK}$ = 750 Ω, R_L = 25 Ω (unless otherwise noted) (continued)

input characteristics

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{ICR}	Input common-mode voltage range	V_{CC} = 5 V	T_A = 25°C	1.5 to 3.5	1.1 to 3.9		V
			T_A = full range	1.6 to 3.4			
		V_{CC} = 12 V	T_A = 25°C	2.3 to 9.7	1.8 to 10.2		
			T_A = full range	2.4 to 9.6			
CMRR	Common-mode rejection ratio	V_{CC} = 5 V	T_A = 25°C	56	63		dB
			T_A = full range	54			
		V_{CC} = 12 V	T_A = 25°C	50	56		
			T_A = full range	48			
R_I	Input resistance	+ Input			1		MΩ
		−Input			15		Ω
C_I	Input capacitance				2		pF

output characteristics

PARAMETER			TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_O	Output voltage swing	Single ended 100 mV overdrive	R_L = 25 Ω	V_{CC} = 5 V	1.4 to 3.6	1.1 to 3.9		V
				V_{CC} = 12 V	1.9 to 10.1	1.4 to 10.6		
			R_L = 100 Ω	V_{CC} = 5 V	1.3 to 3.7	1.05 to 3.95		
				V_{CC} = 12 V	1.5 to 10.5	1.1 to 10.9		
I_O	Output current		R_L = 3.6 Ω,	V_{CC} = 5 V		240		mA
			R_L = 10 Ω,	V_{CC} = 12 V	240	275		
I_{SC}	Short-circuit current		R_L = 0 Ω,	V_{CC} = 12 V		325		mA
	Output resistance		Open loop			15		Ω

power supply

PARAMETER			TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{CC}	Operating range	Dual supply			±2.25		±7	V
		Single supply			4.5		14	
I_{CC}	Quiescent current (each driver)		V_{CC} = 5 V	T_A = 25°C		6.7	8.8	mA
				T_A = full range			10	
			V_{CC} = 12 V	T_A = 25°C		7.3	9.5	mA
				T_A = full range			10.5	
PSRR	Power supply rejection ratio		V_{CC} = 5 V	T_A = 25°C	-54	−58		dB
				T_A = full range	-46	−		
			V_{CC} = 12 V	T_A = 25°C	-58	−70		
				T_A = full range	-50			

electrical characteristics over recommended operating free-air temperature range, T_A = 25°C, V_{CC+} = 12 V, V_{CC-} = GND, $R_{FEEDBACK}$ = 750 Ω, R_L = 25 Ω (unless otherwise noted) (continued)

shutdown characteristics (THS6093 only)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{IL(SHDN)}$	Shutdown pin voltage for power up	V_{CC} = 12 V, GND = 6 V (GND Pin as Reference)			0.8	V
$V_{IH(SHDN)}$	Shutdown pin voltage for power down	V_{CC} = 12 V, GND = 6 V (GND Pin as Reference)	2			V
$I_{CC(SHDN)}$	Total quiescent current when in shutdown state	V_{SHDN} = 8 V, V_{GND} = 6 V, V_{CC} = 12 V		0.3	0.7	mA
t_{DIS}	Disable time (see Note 3)	V_{CC} = 12 V		0.2		µs
t_{EN}	Enable time (see Note 3)	V_{CC} = 12 V		0.5		µs
$I_{IL(SHDN)}$	Shutdown pin input bias current for power up	V_{SHDN} = 6 V, V_{GND} = 6 V, V_{CC} = 12 V		40	100	µA
$I_{IH(SHDN)}$	Shutdown pin input bias current for power down	V_{SHDN} = 9.3 V, V_{GND} = 6 V, V_{CC} = 12 V		50	100	µA

NOTE 3: Disable/enable time is defined as the time from when the shutdown signal is applied to the SHDN pin to when the supply current has reached half of its final value.

APPLICATION INFORMATION

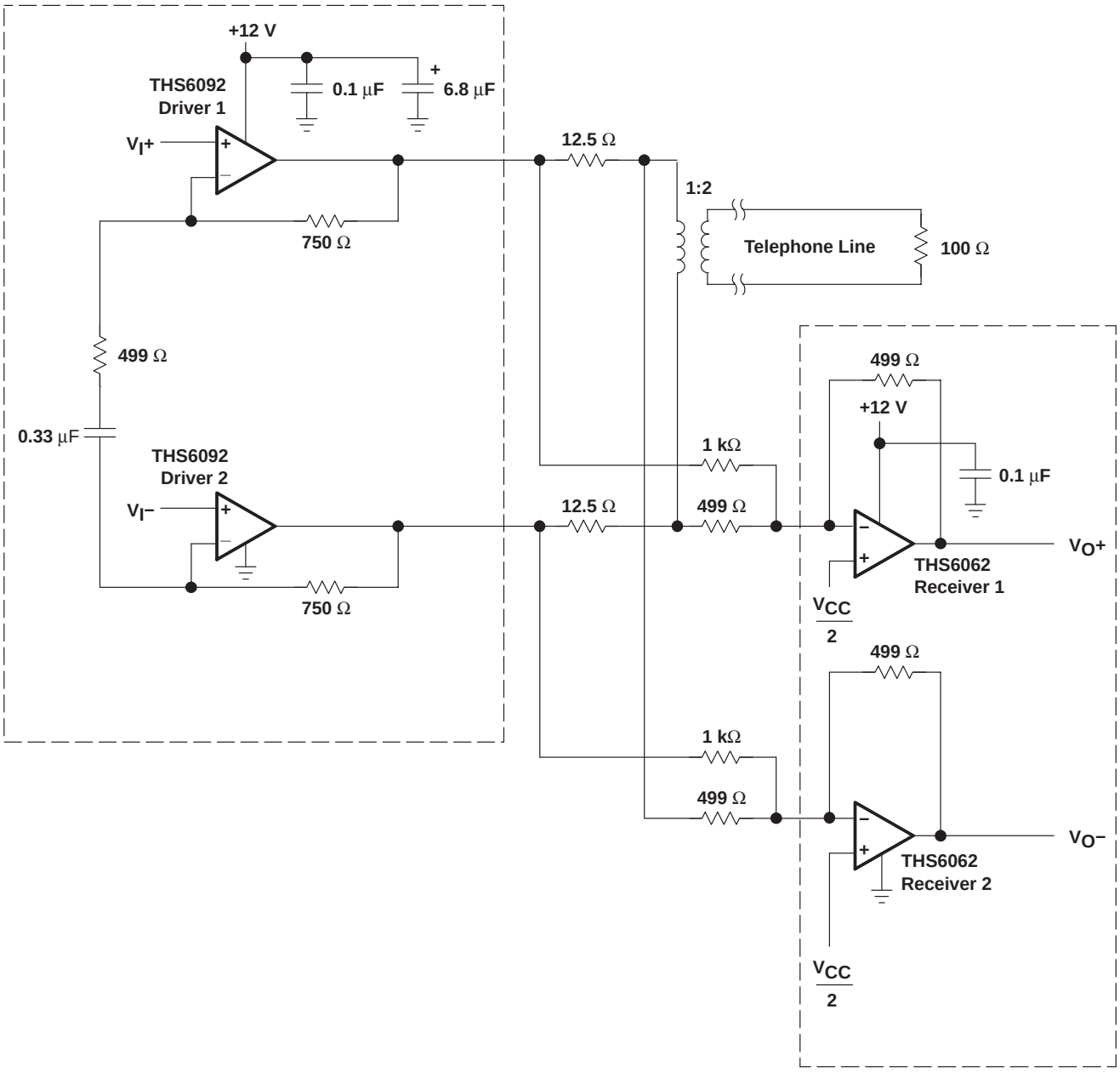

Figure 1. THS6092 ADSL Application With 1:2 Transformer Ratio

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
THS6092ID	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	6092I
THS6092ID.A	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	6092I
THS6093CPWPR	Active	Production	HTSSOP (PWP) | 14	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	0 to 70	HS6093C
THS6093CPWPR.A	Active	Production	HTSSOP (PWP) | 14	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	0 to 70	HS6093C
THS6093IPWP	Active	Production	HTSSOP (PWP) | 14	90 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	HS6093I
THS6093IPWP.A	Active	Production	HTSSOP (PWP) | 14	90 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	HS6093I
THS6093IPWPR	Active	Production	HTSSOP (PWP) | 14	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	HS6093I
THS6093IPWPR.A	Active	Production	HTSSOP (PWP) | 14	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	HS6093I

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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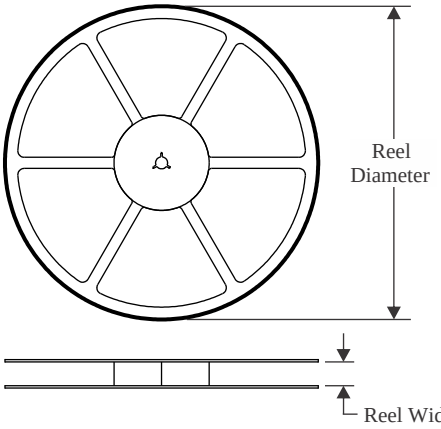
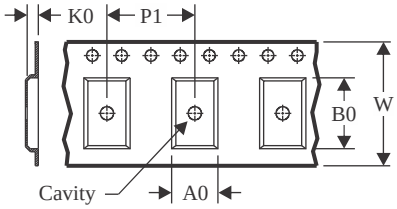
TAPE AND REEL INFORMATION

REEL DIMENSIONS

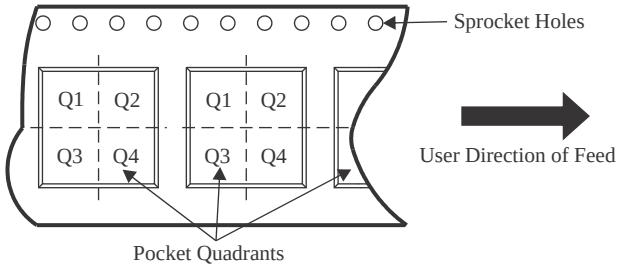


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

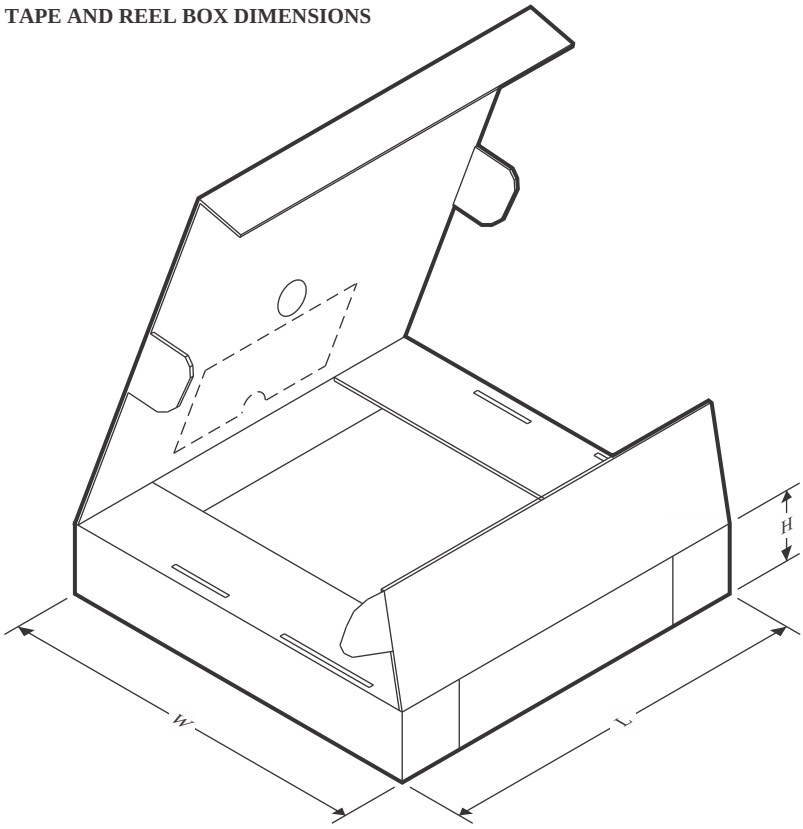
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
THS6093CPWPR	HTSSOP	PWP	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
THS6093IPWPR	HTSSOP	PWP	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

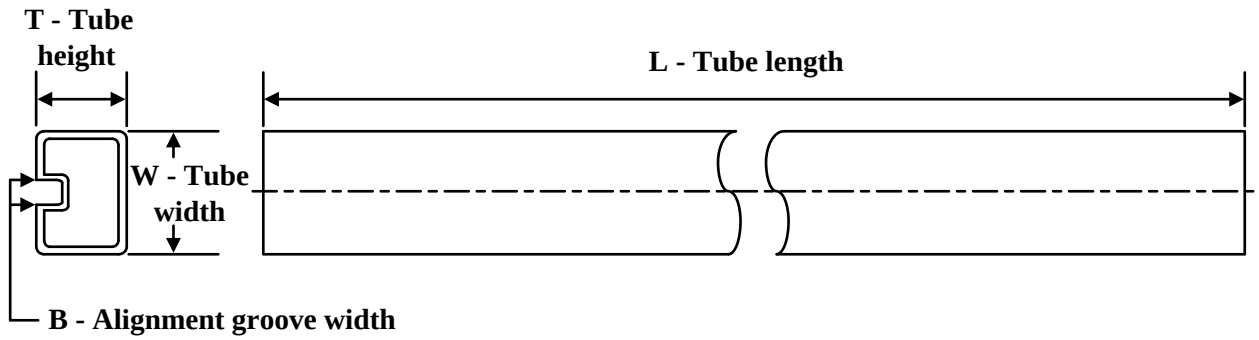
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
THS6093CPWPR	HTSSOP	PWP	14	2000	350.0	350.0	43.0
THS6093IPWPR	HTSSOP	PWP	14	2000	350.0	350.0	43.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
THS6092ID	D	SOIC	8	75	505.46	6.76	3810	4
THS6092ID.A	D	SOIC	8	75	505.46	6.76	3810	4
THS6093IPWP	PWP	HTSSOP	14	90	530	10.2	3600	3.5
THS6093IPWP.A	PWP	HTSSOP	14	90	530	10.2	3600	3.5

GENERIC PACKAGE VIEW

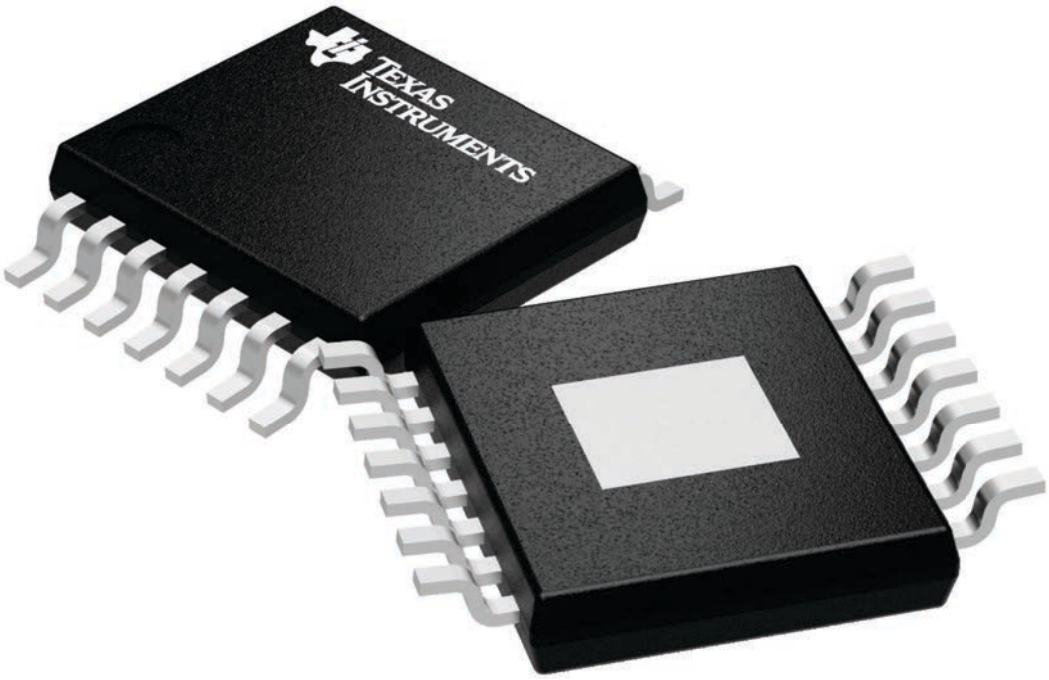
PWP 14

PowerPAD TSSOP - 1.2 mm max height

4.4 x 5.0, 0.65 mm pitch

PLASTIC SMALL OUTLINE

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



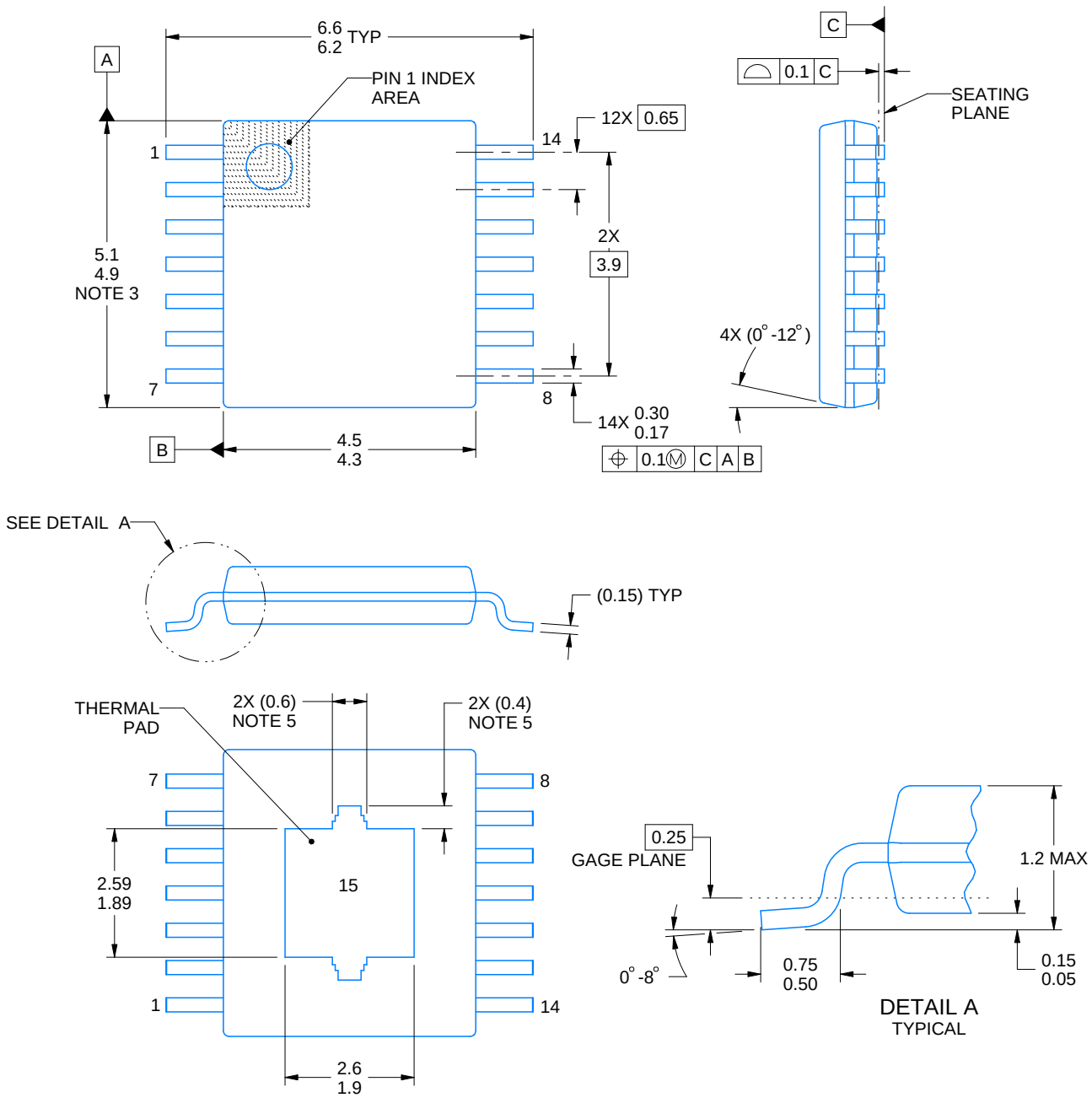
4224995/A

PACKAGE OUTLINE

PWP0014K

PowerPAD™ TSSOP - 1.2 mm max height

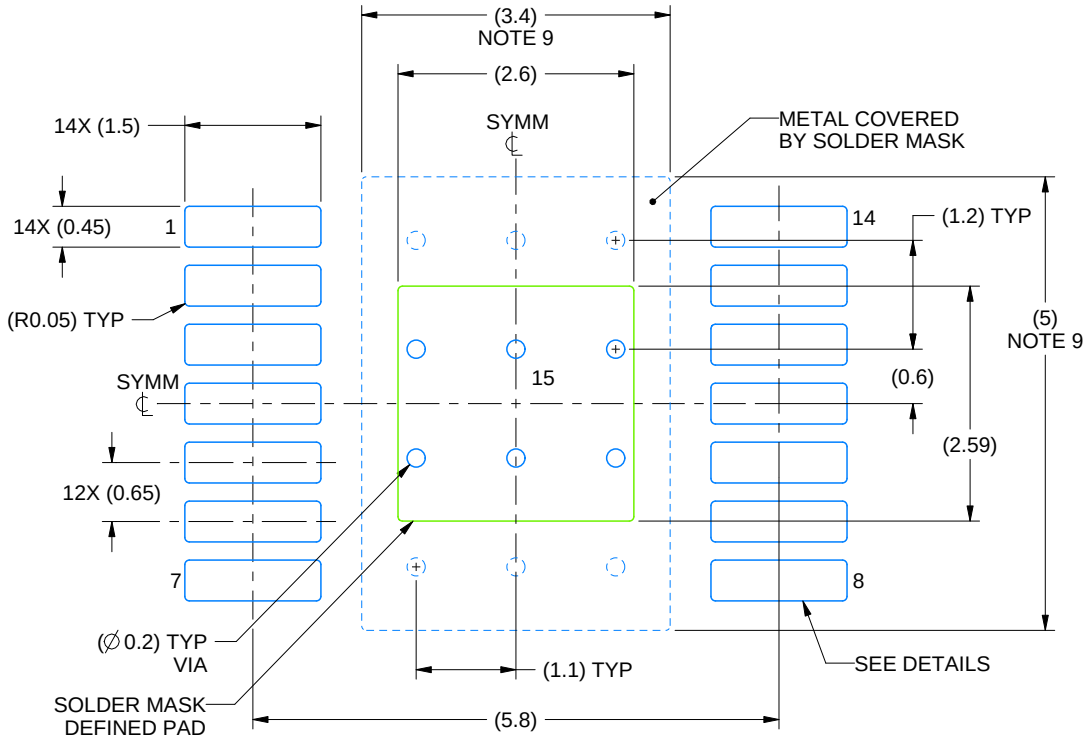
SMALL OUTLINE PACKAGE



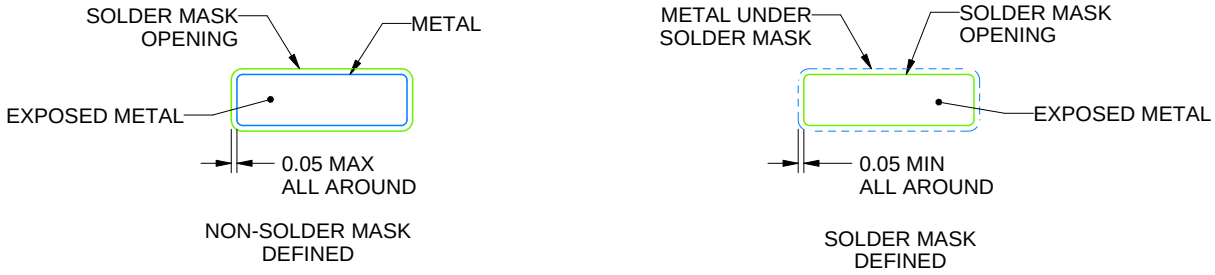
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-153.
5. Features may differ or may not be present.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 12X



SOLDER MASK DETAILS

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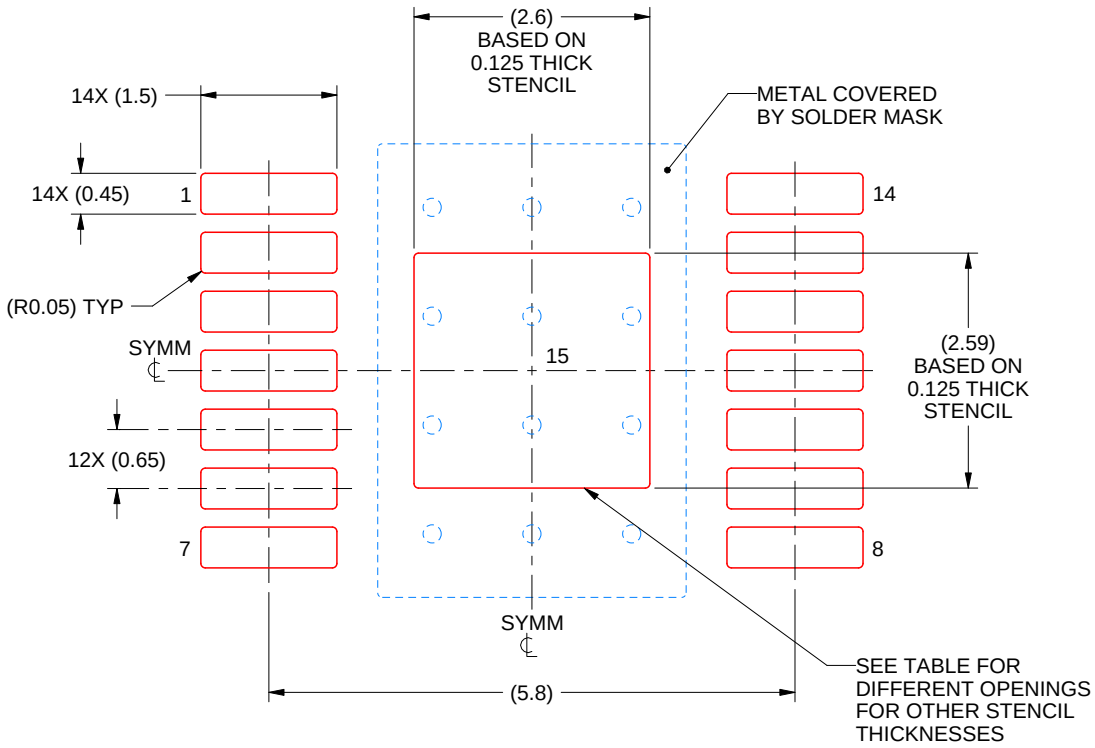
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
9. Size of metal pad may vary due to creepage requirement.
10. Vias are optional depending on application, refer to device data sheet. It is recommended that vias under paste be filled, plugged or tented.



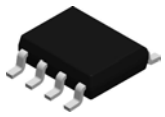
SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 12X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	2.91 X 2.90
0.125	2.60 X 2.59 (SHOWN)
0.15	2.37 X 2.36
0.175	2.20 X 2.19

4229706/B 12/2023

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

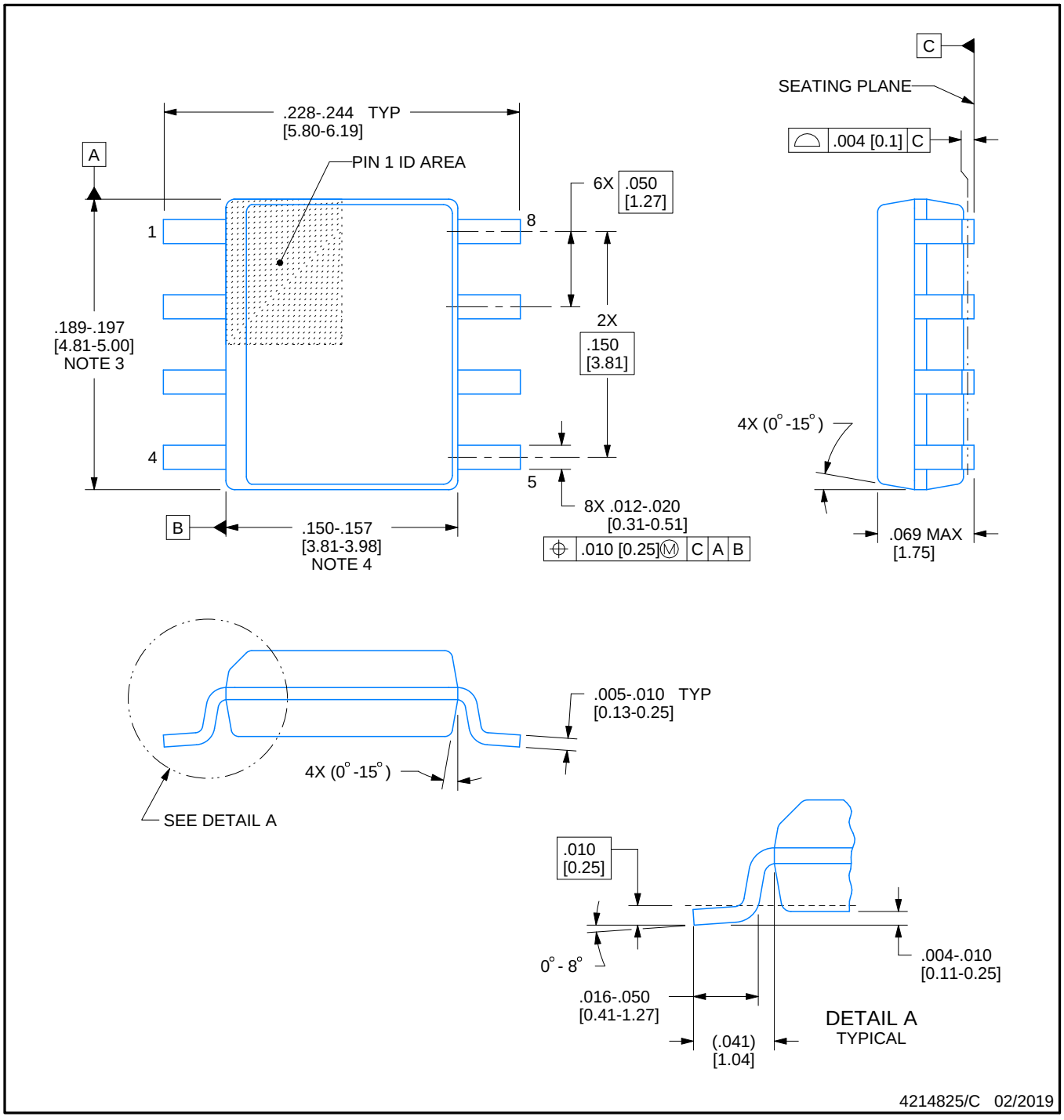


PACKAGE OUTLINE

D0008A

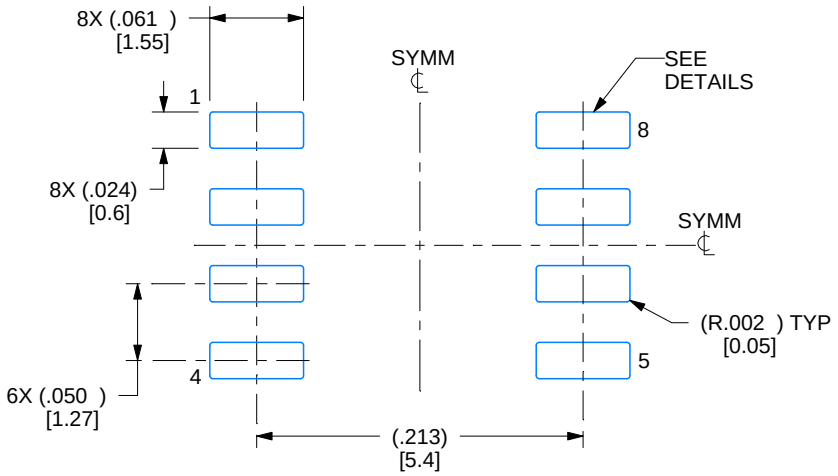
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

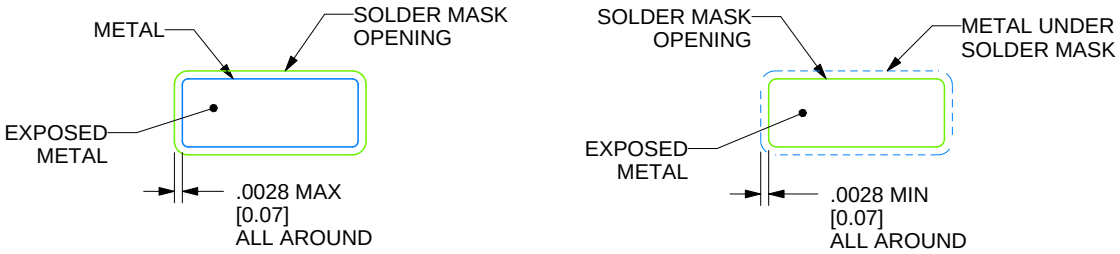


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

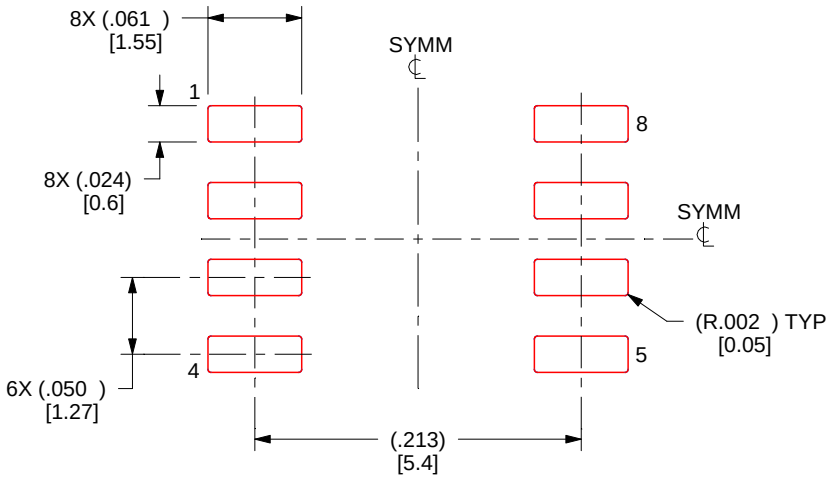
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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