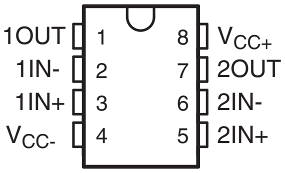
Excalibur™ LOW-NOISE HIGH-SPEED PRECISION OPERATIONAL AMPLIFIER

FEATURES

- **Qualified for Automotive Applications**
- **Low Noise**
  - **10 Hz: 15 nV/$\sqrt{\text{Hz}}$**
  - **1 kHz: 10.5 nV/$\sqrt{\text{Hz}}$**
- **10000-pF Load Capability**
- **20-mA Short-Circuit Output Current (Min)**
- **27-V/μs Slew Rate (Min)**
- **High Gain-Bandwidth Product: 5.9 MHz**
- **Single or Split Supply: 4 V to 44 V**
- **Fast Settling Time**
  - **340 ns to 0.1%**
  - **400 ns to 0.01%**
- **Large Output Swing:**
  V_{CC-} + 0.1 V to V_{CC+} – 1 V

D PACKAGE
(TOP VIEW)



DESCRIPTION/ORDERING INFORMATION

The TLE2142 device is a high-performance, internally compensated operational amplifier built using the Texas Instruments complementary bipolar Excalibur™ process. It is a pin-compatible upgrade to standard industry products.

The design incorporates an input stage that simultaneously achieves low audio-band noise of 10.5 nV/$\sqrt{\text{Hz}}$ with a 10-Hz 1/f corner and symmetrical 40-V/μs slew rate typically with loads up to 800 pF. The resulting low distortion and high power bandwidth are important in high-fidelity audio applications. A fast settling time of 340 ns to 0.1% of a 10-V step with a 2-kΩ/100-pF load is useful in fast actuator/positioning drivers. Under similar test conditions, settling time to 0.01% is 400 ns.

The device is stable with capacitive loads up to 10 nF, although the 6-MHz bandwidth decreases to 1.8 MHz at this high loading level. As such, the TLE2142 is useful for low-droop sample-and-holds and direct buffering of long cables, including 4-mA to 20-mA current loops.

The special design also exhibits an improved insensitivity to inherent integrated circuit component mismatches as is evidenced by a 500-μV maximum offset voltage and 1.7-μV/°C typical drift. Minimum common-mode rejection ratio and supply-voltage rejection ratio are 85 dB and 90 dB, respectively.

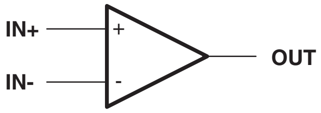
Device performance is relatively independent of supply voltage over the ±2-V to ±22-V range. Inputs can operate between V_{CC-} – 0.3 V to V_{CC+} – 1.8 V without inducing phase reversal, although excessive input current may flow out of each input exceeding the lower common-mode input range. The all-npn output stage provides a nearly rail-to-rail output swing of V_{CC-} + 0.1 V to V_{CC+} – 1 V under light current-loading conditions. The device can sustain shorts to either supply, because output current is internally limited, but care must be taken to ensure that maximum package power dissipation is not exceeded.

The TLE2142 can also be used as a comparator. Differential inputs of $V_{CC\pm}$ can be maintained without damage to the device. Open-loop propagation delay with TTL supply levels is typically 200 ns. This gives a good indication as to output stage saturation recovery when the device is driven beyond the limits of recommended output swing.

The TLE2142 device is available in industry-standard 8-pin small-outline (D) packages. The device is characterized for operation from –40°C to 125°C.

Excalibur is a trademark of Texas Instruments.

SYMBOL (EACH AMPLIFIER)

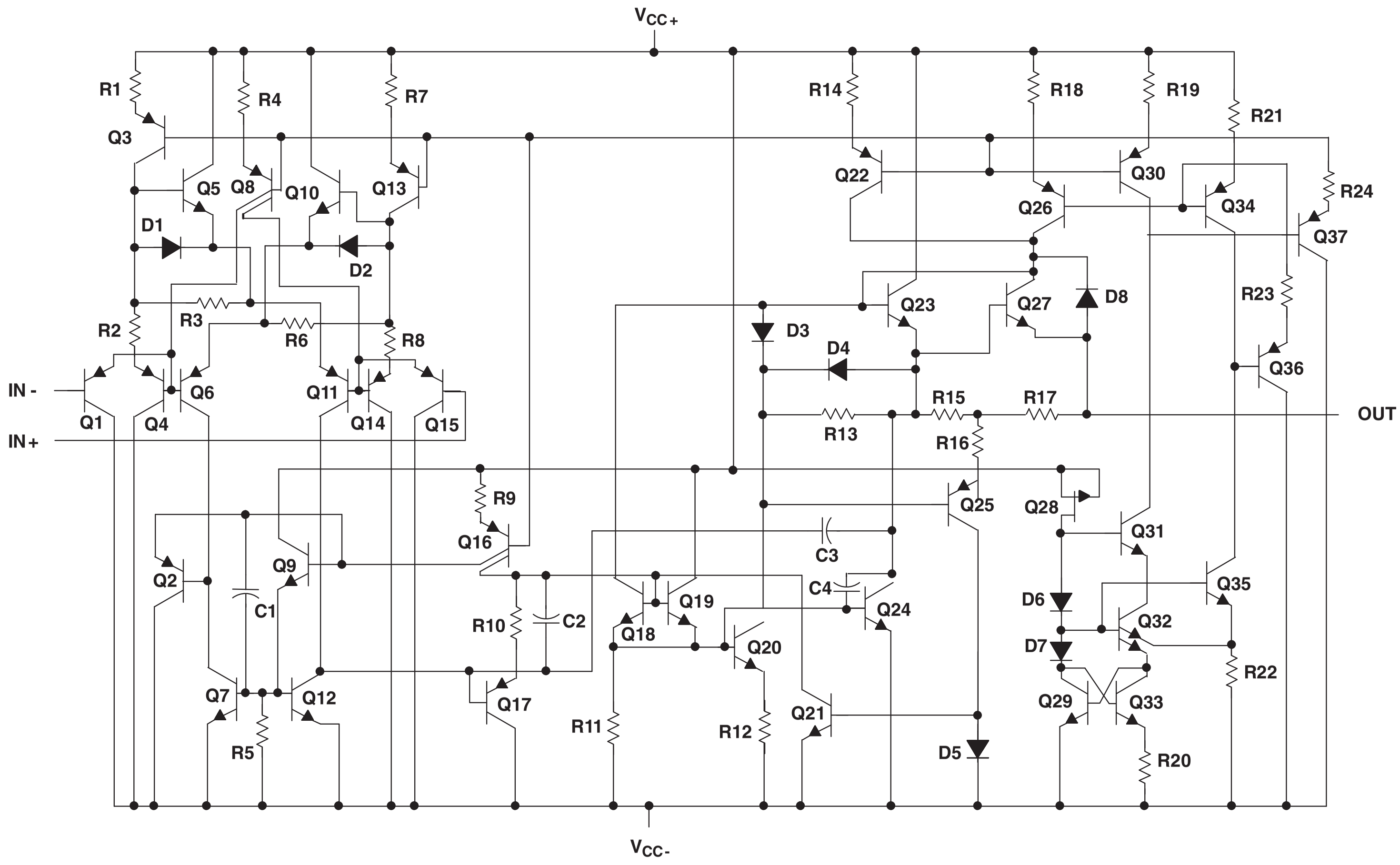


ORDERING INFORMATION(1)

T_A	PACKAGE(2)		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 125°C	SOIC – D	Reel of 2500	TLE2142QDRQ1	2142Q

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.
(2) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.

EQUIVALENT SCHEMATIC



DEVICE COMPONENT COUNT

COMPONENT	TLE2142
Transistors	65
Resistors	43
Diodes	14
Capacitors	8
Epi-FET	1

ABSOLUTE MAXIMUM RATINGS[1]

over operating free-air temperature range (unless otherwise noted)

V_{CC+}	Supply voltage[2]	22 V
$V_{CC–}$	Supply voltage	–22 V
V_{ID}	Differential input voltage[3]	±44 V
V_I	Input voltage range (any input)	V_{CC+} to ($V_{CC–}$ – 0.3) V
I_I	Input current (each input)	±1 mA
I_O	Output current	±80 mA
	Total current into V_{CC+}	80 mA
	Total current out of $V_{CC–}$	80 mA
	Duration of short-circuit current at (or below) 25°C[4]	Unlimited
θ_{JA}	Package thermal impedance[5][6]	97.1°C/W
T_A	Operating free-air temperature range	–40°C to 125°C
T_{stg}	Storage temperature range	–65°C to 150°C
	Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C
ESD	Electrostatic discharge rating, Human-body model	500 V

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values, except differential voltages, are with respect to the midpoint between V_{CC+} and $V_{CC–}$.
(3) Differential voltages are at IN+ with respect to IN–. Excessive current flows, if input, are brought below $V_{CC–}$ – 0.3 V.
(4) The output may be shorted to either supply. Temperature and/or supply voltages must be limited to ensure that the maximum dissipation rating is not exceeded.
(5) Maximum power dissipation is a function of T_J(max), θ_{JA}, and T_A. The maximum allowable power dissipation at any allowable ambient temperature is $P_D = (T_J(max) – T_A)/\theta_{JA}$. Operating at the absolute maximum T_J of 150°C can affect reliability.
(6) The package thermal impedance is calculated in accordance with JESD 51-7.

RECOMMENDED OPERATING CONDITIONS

			MIN	MAX	UNIT
$V_{CC±}$	Supply voltage		±2	±22	V
V_{IC}	Common-mode input voltage	V_{CC} = 5 V	0	2.7	V
		$V_{CC±}$ = ±15 V	–15	12.7	
T_A	Operating free-air temperature		–40	125	°C

ELECTRICAL CHARACTERISTICS

V_{CC} = 5 V, at specified free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A(1)	MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	V_O = 2.5 V, R_S = 50 Ω, V_{IC} = 2.5 V	25°C		220	1900	μV
			Full range			2600	
α_{VIO}	Temperature coefficient of input offset voltage	V_O = 2.5 V, R_S = 50 Ω, V_{IC} = 2.5 V	Full range		1.7		μV/°C
I_{IO}	Input offset current	V_O = 2.5 V, R_S = 50 Ω, V_{IC} = 2.5 V	25°C		8	100	nA
			Full range			200	
I_{IB}	Input bias current	V_O = 2.5 V, R_S = 50 Ω, V_{IC} = 2.5 V	25°C		–0.8	–2	μA
			Full range			–2.3	
V_{ICR}	Common-mode input voltage range	R_S = 50 Ω	25°C	0 to 3	–0.3 to 3.2		V
			Full range	0 to 2.7	–0.3 to 2.9		
V_{OH}	High-level output voltage	I_{OH} = –150 μA	25°C	3.9	4.1		V
		I_{OH} = –1.5 mA		3.8	4		
		I_{OH} = –15 mA		3.4	3.7		
		I_{OH} = –100 μA	Full range	3.75			
		I_{OH} = –1 mA		3.65			
		I_{OH} = –10 mA		3.45			
V_{OL}	Low-level output voltage	I_{OL} = 150 μA	25°C		75	125	mV
		I_{OL} = 1.5 mA			150	225	
		I_{OL} = 15 mA			1.2	1.4	V
		I_{OL} = 100 μA	Full range			200	mV
		I_{OL} = 1 mA				250	
		I_{OL} = 10 mA				1.25	V
A_{VD}	Large-signal differential voltage amplification	V_{IC} = ±2.5 V, R_L = 2 kΩ, V_O = 1 V to -1.5 V	25°C	50	220		V/mV
			Full range	5			
r_i	Input resistance		25°C		70		MΩ
c_i	Input capacitance		25°C		2.5		pF
z_o	Open-loop output impedance	f = 1 MHz	25°C		30		Ω
CMRR	Common-mode rejection ratio	V_{IC} = V_{ICR}(min), R_S = 50 Ω	25°C	85	118		dB
			Full range	80			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm}/\Delta V_{IO}$)	$V_{CC\pm}$ = ±2.5 V to ±15 V, R_S = 50 Ω	25°C	90	106		dB
			Full range	85			
I_{CC}	Supply current	V_O = 2.5 V, No load, V_{IC} = 2.5 V	25°C		6.6	8.8	mA
			Full range			9.2	

(1) Full range is –40°C to 125°C.

OPERATING CHARACTERISTICS

V_{CC} = 5 V, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
SR+	Positive slew rate	A_{VD} = –1, R_L = 2 kΩ[1], C_L = 500 pF			45		V/µs
SR–	Negative slew rate	A_{VD} = –1, R_L = 2 kΩ[1], C_L = 500 pF			42		V/µs
t_s	Settling time	A_{VD} = –1, 2.5-V step	To 0.1%		0.16		µs
			To 0.01%		0.22		
V_n	Equivalent input noise voltage	R_S = 20 Ω	f = 10 Hz		15		nV/√Hz
			f = 1 kHz		10.5		
$V_{n(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 1 Hz			0.48		µV
		f = 0.1 Hz to 10 Hz			0.51		
I_n	Equivalent input noise current	f = 10 Hz			1.92		pA/√Hz
		f = 1 kHz			0.5		
THD+N	Total harmonic distortion plus noise	V_O = 1 V to 3 V, R_L = 2 kΩ[1], A_{VD} = 2, f = 10 kHz			0.0052		%
B_1	Unity-gain bandwidth	R_L = 2 kΩ[1], C_L = 100 pF			5.9		MHz
	Gain-bandwidth product	R_L = 2 kΩ[1], C_L = 100 pF, f = 100 kHz			5.8		MHz
BOM	Maximum output-swing bandwidth	$V_{O(PP)}$ = 2 V, R_L = 2 kΩ[1], A_{VD} = 1, C_L = 100 pF			660		kHz
ϕ_m	Phase margin at unity gain	R_L = 2 kΩ[1], C_L = 100 pF			57		°

(1) R_L terminated at 2.5 V.

ELECTRICAL CHARACTERISTICS

V_{CC} = ±15 V, at specified free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A (1)	MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	$V_{IC} = 0$, $R_S = 50\ \Omega$		25°C		290	1200	µV
				Full range			2000	
α_{VIO}	Temperature coefficient of input offset voltage	$V_{IC} = 0$, $R_S = 50\ \Omega$		Full range		1.7		µV/°C
I_{IO}	Input offset current	$V_{IC} = 0$, $R_S = 50\ \Omega$		25°C		7	100	nA
				Full range			250	
I_{IB}	Input bias current	$V_{IC} = 0$, $R_S = 50\ \Omega$		25°C		–0.7	–1.5	µA
				Full range			–1.8	
V_{ICR}	Common-mode input voltage range	$R_S = 50\ \Omega$		25°C	–15 to 13	–15.3 to 13.2		V
				Full range	–15 to 12.7	–15.3 to 12.9		
V_{OM+}	Maximum positive peak output voltage swing	I_O = –150 µA		25°C	13.8	14.1		V
		I_O = –1.5 mA			13.7	14		
		I_O = –15 mA			13.3	13.7		
		I_O = –100 µA		Full range	13.7			
		I_O = –1 mA			13.6			
		I_O = –10 mA			13.3			
$V_{OM–}$	Maximum negative peak output voltage swing	I_O = 150 µA		25°C	–14.7	–14.9		V
		I_O = 1.5 mA			–14.5	–14.8		
		I_O = 15 mA			–13.4	–13.8		
		I_O = 100 µA		Full range	–14.6			
		I_O = 1 mA			–14.5			
		I_O = 10 mA			–13.4			
A_{VD}	Large-signal differential voltage amplification	V_O = ±10 V, R_L = 2 kΩ		25°C	100	450		V/mV
				Full range	20			
r_i	Input resistance			25°C		65		MΩ
c_i	Input capacitance			25°C		2.5		pF
z_o	Open-loop output impedance	f = 1 MHz		25°C		30		Ω
CMRR	Common-mode rejection ratio	$V_{IC} = V_{ICR}$(min), $R_S = 50\ \Omega$		25°C	85	108		dB
				Full range	80			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm}/\Delta V_{IO}$)	$V_{CC\pm}$ = ±2.5 V to ±15 V, $R_S = 50\ \Omega$		25°C	90	106		dB
				Full range	85			
I_{OS}	Short-circuit output current	$V_O = 0$	V_{ID} = 1 V	25°C	–25	–50		mA
			V_{ID} = –1 V		20	31		
I_{CC}	Supply current	V_O = 0, No load, V_{IC} = 2.5 V		25°C		6.9	9	mA
				Full range			9.4	

(1) Full range is –40°C to 125°C.

OPERATING CHARACTERISTICS

V_{CC} = ±15 V, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
SR+	Positive slew rate	A_{VD} = –1, R_L = 2 kΩ, C_L = 100 pF		27	45		V/µs
SR–	Negative slew rate	A_{VD} = –1, R_L = 2 kΩ, C_L = 100 pF		27	42		V/µs
t_s	Settling time	A_{VD} = –1, 10-V step	To 0.1%		0.34		µs
			To 0.01%		0.4		
V_n	Equivalent input noise voltage	R_S = 20 Ω	f = 10 Hz		15		$nV/\sqrt{Hz}$
			f = 1 kHz		10.5		
$V_{n(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 1 Hz			0.48		µV
		f = 0.1 Hz to 10 Hz			0.51		
I_n	Equivalent input noise current	f = 10 Hz			1.89		$pA/\sqrt{Hz}$
		f = 1 kHz			0.47		
THD+N	Total harmonic distortion plus noise	$V_{O(PP)}$ = 20 V, R_L = 2 kΩ, A_{VD} = 10, f = 10 kHz			0.01		%
B_1	Unity-gain bandwidth	R_L = 2 kΩ, C_L = 100 pF			6		MHz
	Gain-bandwidth product	R_L = 2 kΩ, C_L = 100 pF, f = 100 kHz			5.9		MHz
BOM	Maximum output-swing bandwidth	$V_{O(PP)}$ = 20 V, A_{VD} = 1, R_L = 2 kΩ, C_L = 100 pF			668		kHz
ϕ_m	Phase margin at unity gain	R_L = 2 kΩ, C_L = 100 pF			58		°

TYPICAL CHARACTERISTICS

Table of Graphs

V_{IO}	Input offset voltage		Distribution	Figure 1
I_{IO}	Input offset current		vs Free-air temperature	Figure 2
I_{IB}	Input bias current		vs Common-mode input voltage	Figure 3
			vs Free-air temperature	Figure 4
V_{OM+}	Maximum positive peak output voltage		vs Supply voltage	Figure 5
			vs Free-air temperature	Figure 6
			vs Output current	Figure 7
			vs Settling time	Figure 9
$V_{OM–}$	Maximum negative peak output voltage		vs Supply voltage	Figure 5
			vs Free-air temperature	Figure 6
			vs Output current	Figure 8
			vs Settling time	Figure 9
$V_{O(PP)}$	Maximum peak-to-peak output voltage		vs Frequency	Figure 10
V_{OH}	High-level output voltage		vs Output current	Figure 11
V_{OL}	Low-level output voltage		vs Output current	Figure 12
	Phase shift		vs Frequency	Figure 13
A_{VD}	Large-signal differential voltage amplification		vs Frequency	Figure 13
			vs Free-air temperature	Figure 14
z_o	Closed-loop output impedance		vs Frequency	Figure 15
I_{OS}	Short-circuit output current		vs Free-air temperature	Figure 16
CMRR	Common-mode rejection ratio		vs Frequency	Figure 17
			vs Free-air temperature	Figure 18
k_{SVR}	Supply-voltage rejection ratio		vs Frequency	Figure 19
			vs Free-air temperature	Figure 20
I_{CC}	Supply current		vs Supply voltage	Figure 21
			vs Free-air temperature	Figure 22
V_n	Equivalent input noise voltage		vs Frequency	Figure 23
V_n	Input noise voltage		Over a 10-second period	Figure 24
I_n	Noise current		vs Frequency	Figure 25
THD+N	Total harmonic distortion plus noise		vs Frequency	Figure 26
SR	Slew rate		vs Free-air temperature	Figure 27
			vs Load capacitance	Figure 28
	Pulse response	Noninverting large signal	vs Time	Figure 29
		Inverting large signal	vs Time	Figure 30
		Small signal	vs Time	Figure 31
B_1	Unity-gain bandwidth		vs Load capacitance	Figure 32
	Gain margin		vs Load capacitance	Figure 33
ϕ_m	Phase margin		vs Load capacitance	Figure 34

TLE2142
DISTRIBUTION OF
INPUT OFFSET VOLTAGE

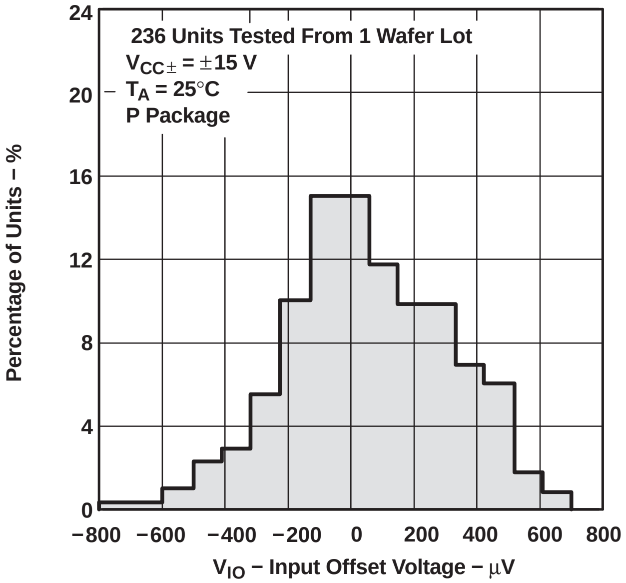


Figure 1.

INPUT OFFSET CURRENT
vs
FREE-AIR TEMPERATURE

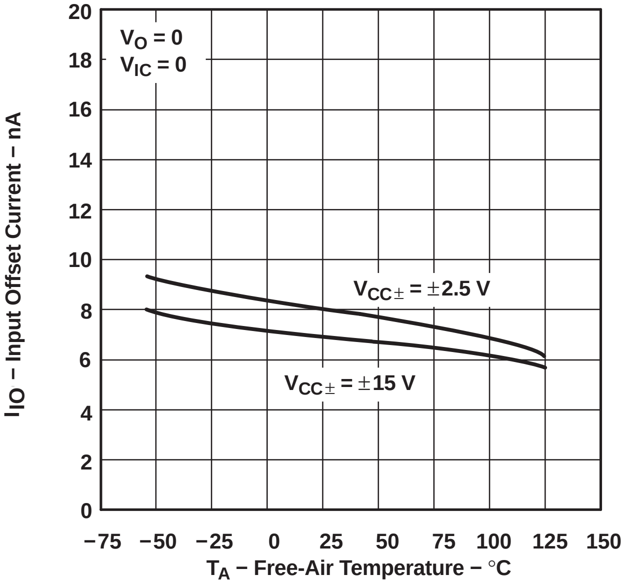


Figure 2.

INPUT BIAS CURRENT
vs
COMMON-MODE INPUT VOLTAGE

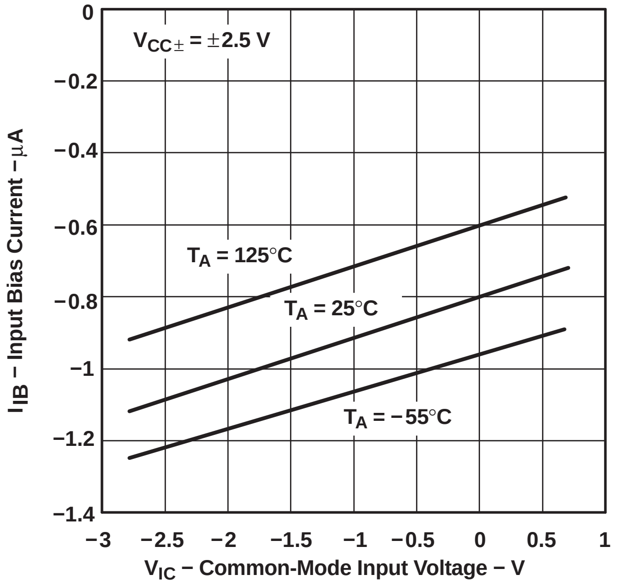


Figure 3.

INPUT BIAS CURRENT
vs
FREE-AIR TEMPERATURE

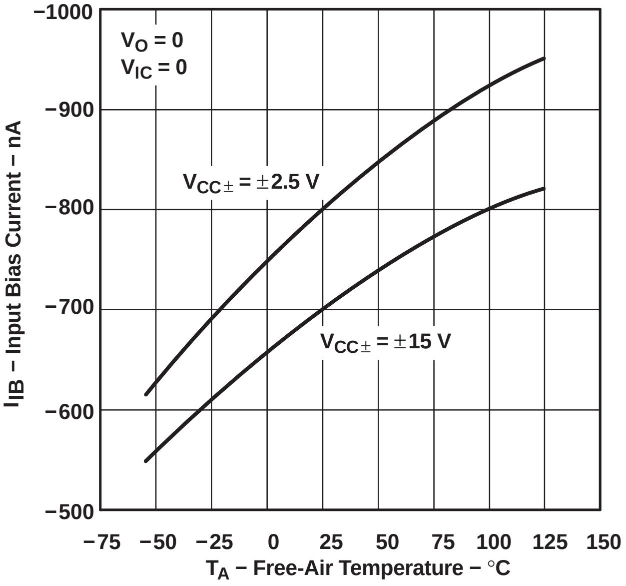


Figure 4.

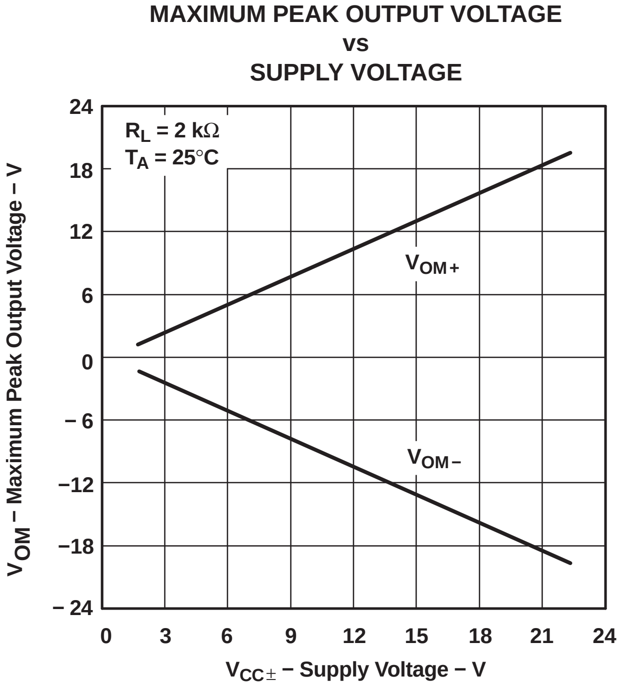


Figure 5.

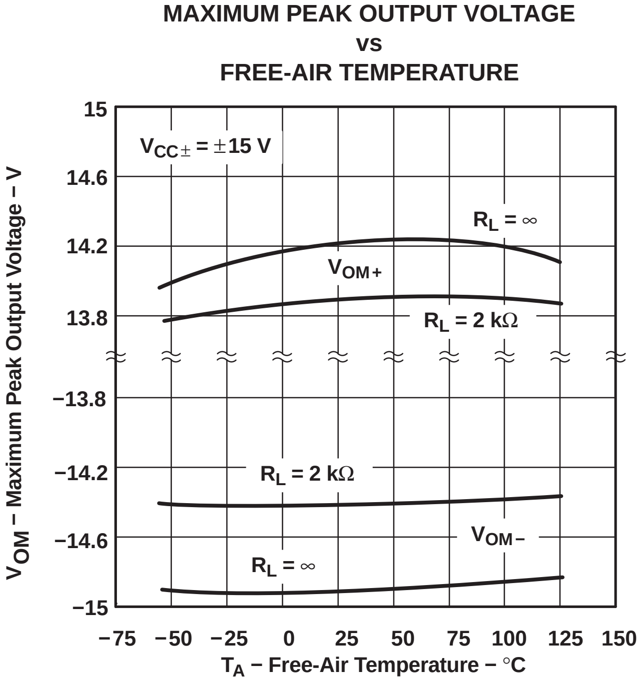


Figure 6.

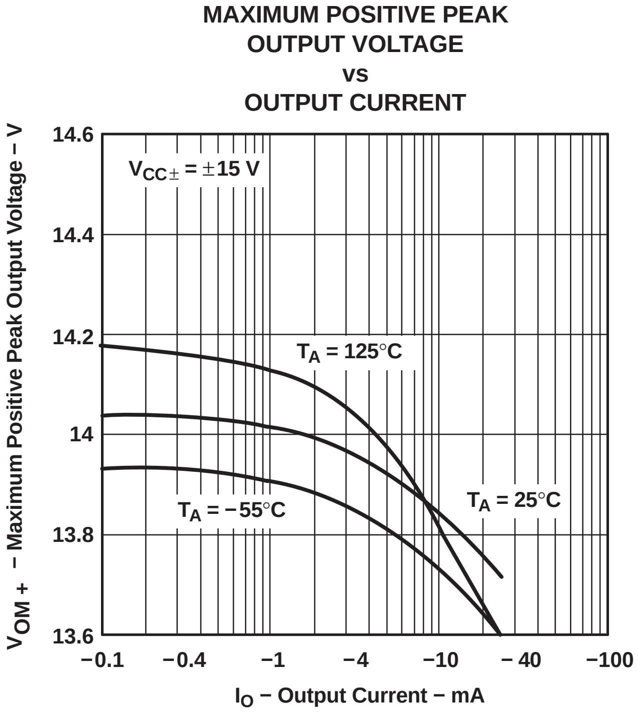


Figure 7.

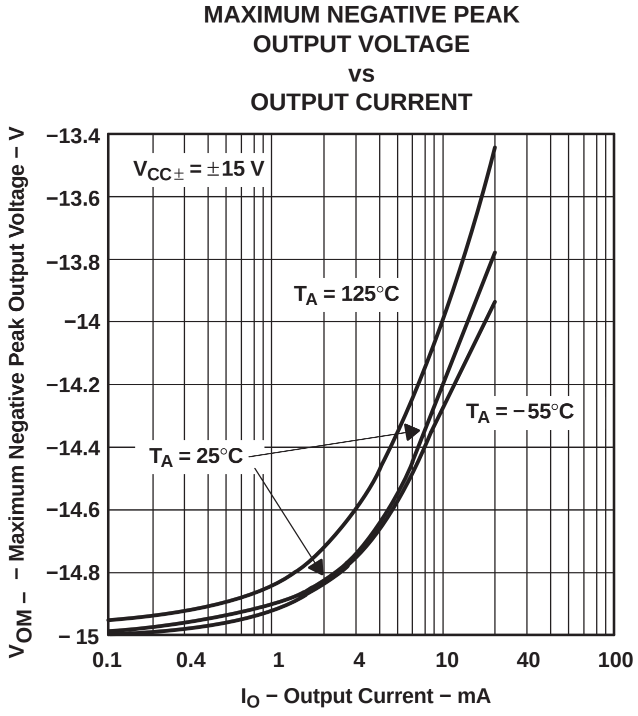


Figure 8.

**MAXIMUM PEAK OUTPUT VOLTAGE
vs
SETTLING TIME**

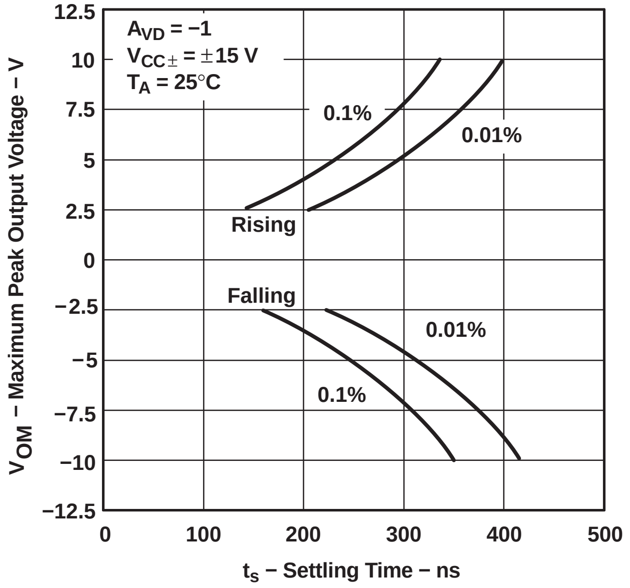


Figure 9.

**MAXIMUM PEAK-TO-PEAK
OUTPUT VOLTAGE
vs
FREQUENCY**

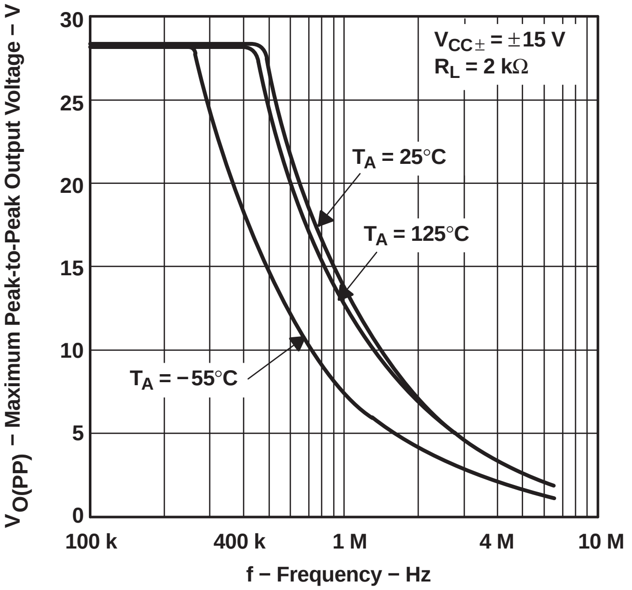


Figure 10.

**HIGH-LEVEL OUTPUT VOLTAGE
vs
OUTPUT CURRENT**

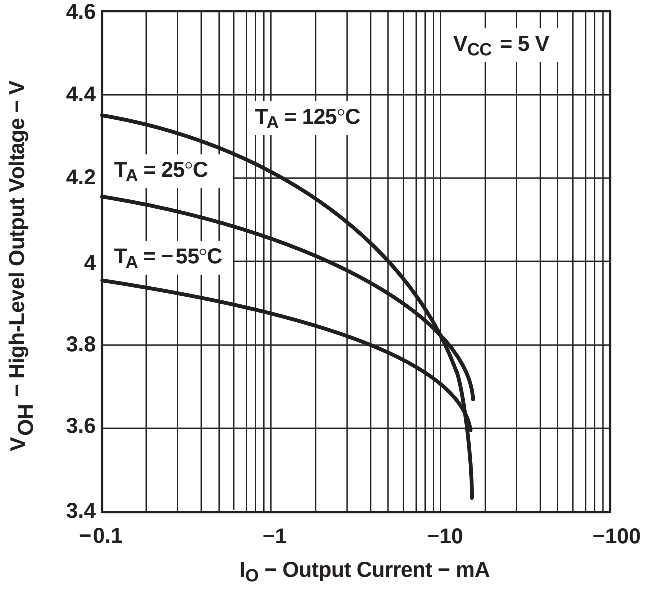


Figure 11.

**LOW-LEVEL OUTPUT VOLTAGE
vs
OUTPUT CURRENT**

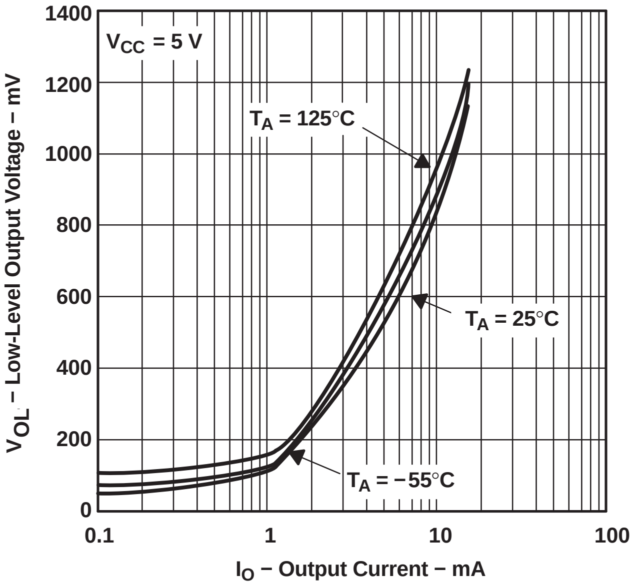


Figure 12.

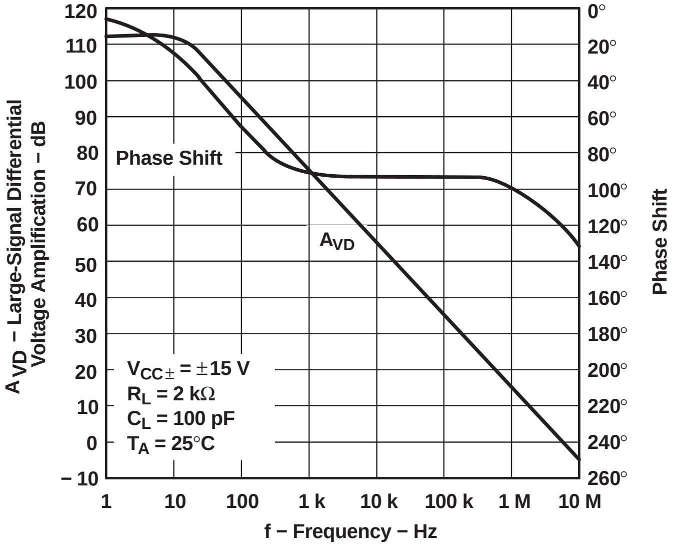

LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION AND PHASE SHIFT vs FREQUENCY

Figure 13.

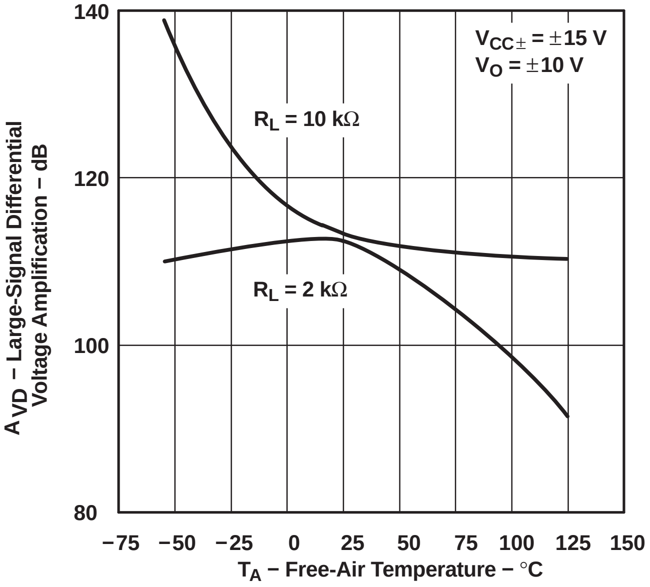

LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION vs FREE-AIR TEMPERATURE

Figure 14.

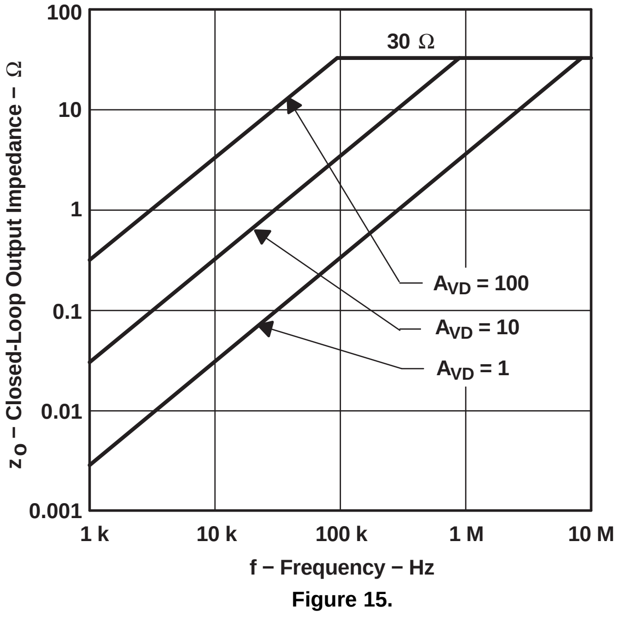

CLOSED-LOOP OUTPUT IMPEDANCE vs FREQUENCY

Figure 15.

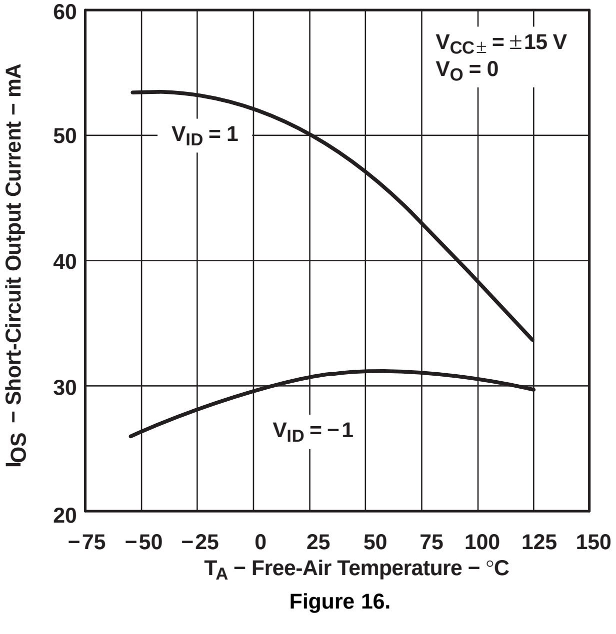

SHORT-CIRCUIT OUTPUT CURRENT vs FREE-AIR TEMPERATURE

Figure 16.

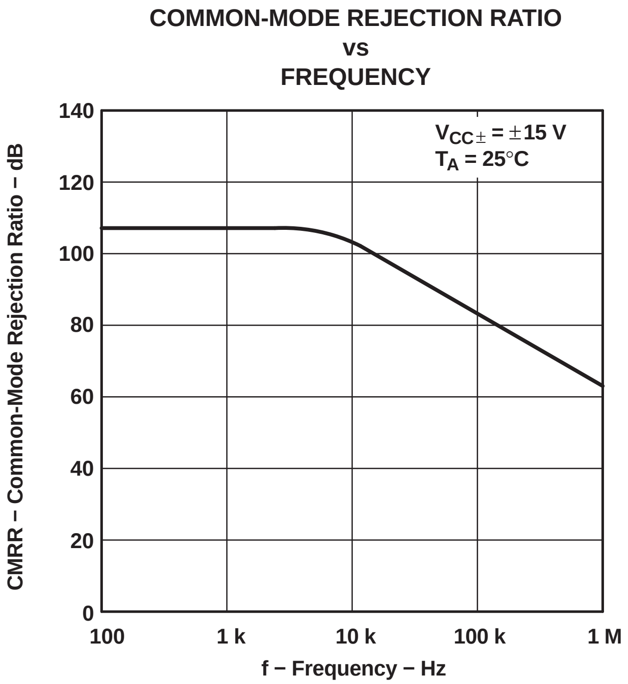


Figure 17.

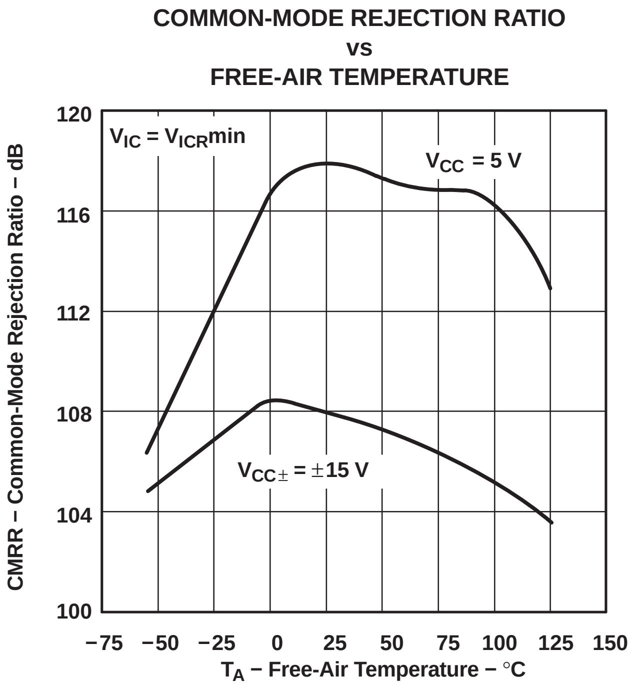


Figure 18.

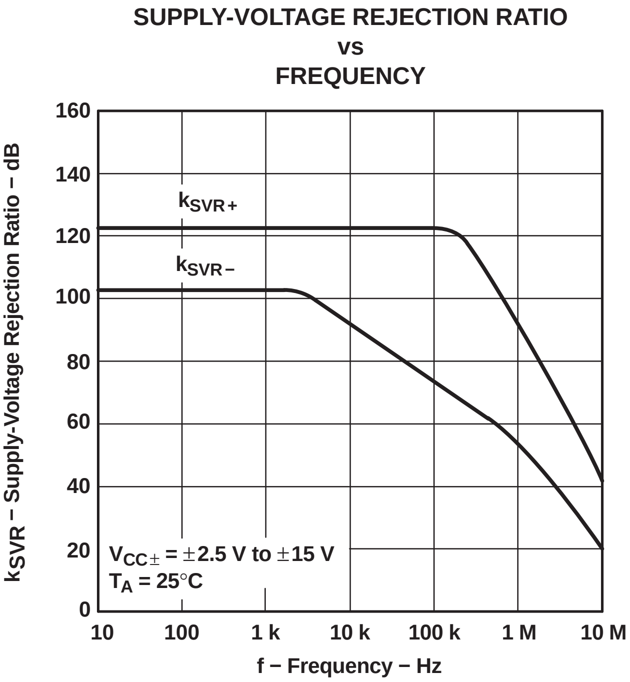
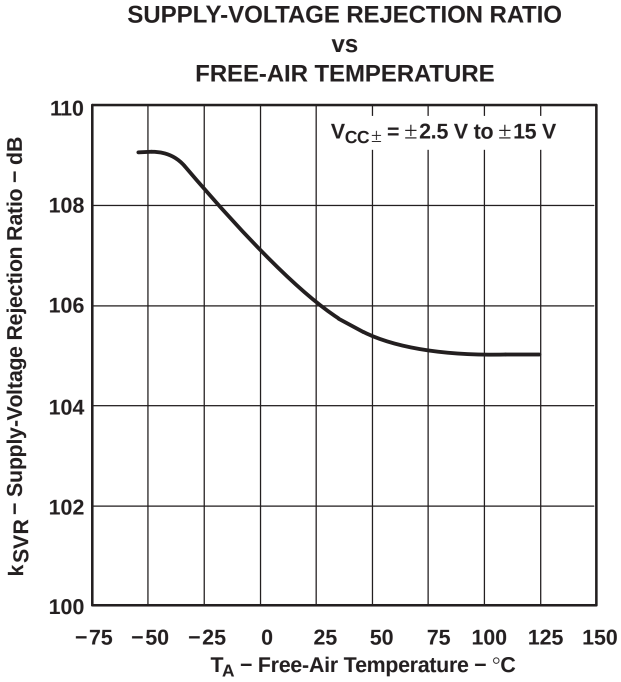


Figure 19.



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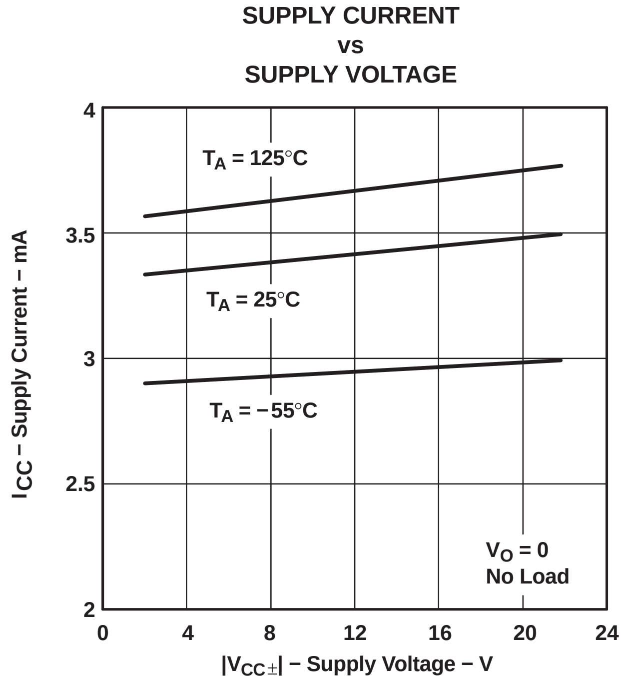
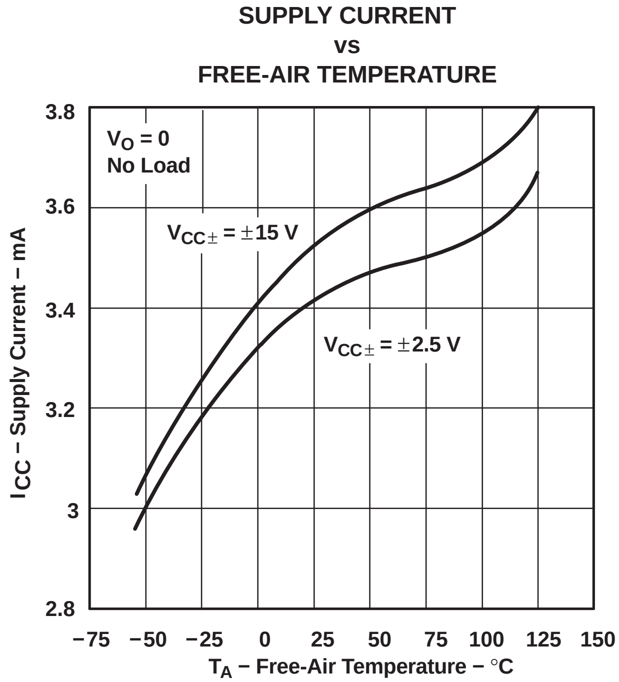


Figure 21.



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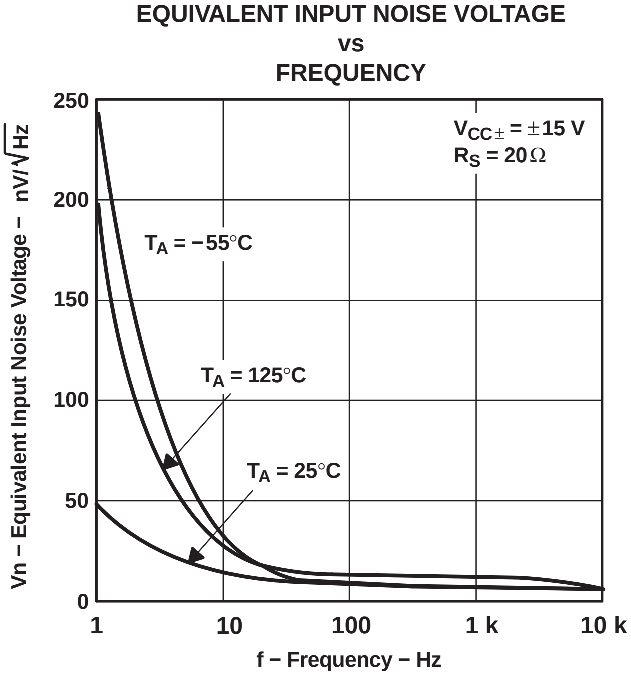

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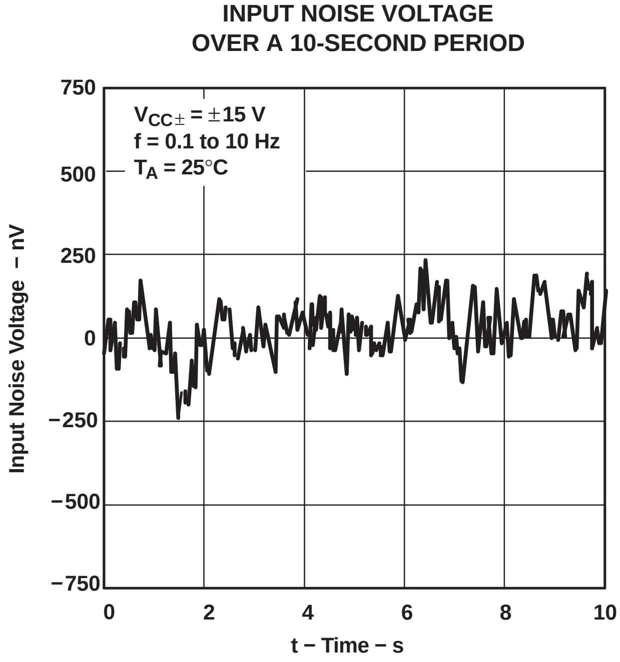

Figure 24.

NOISE CURRENT
vs
FREQUENCY

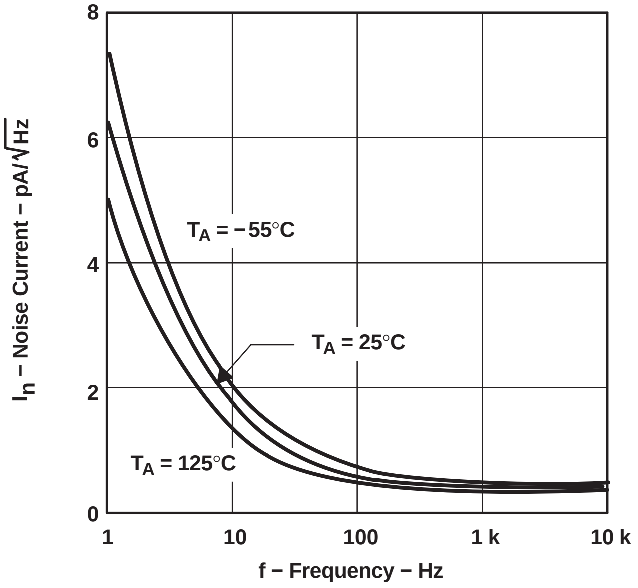

Figure 25.

TOTAL HARMONIC DISTORTION
PLUS NOISE
vs
FREQUENCY

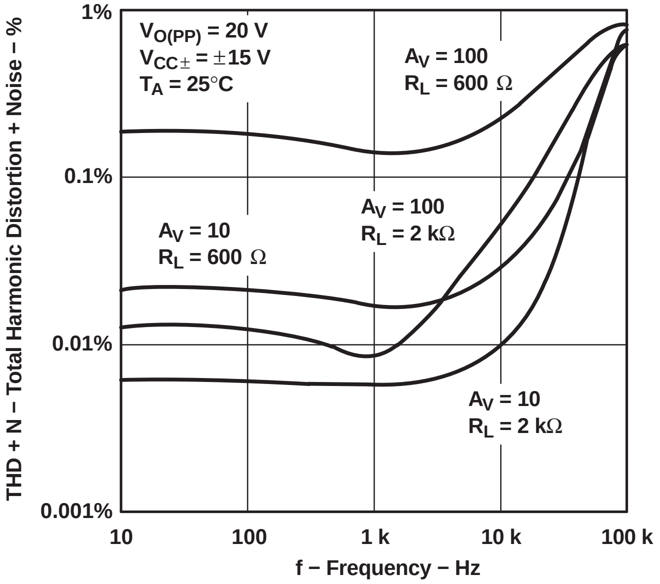

Figure 26.

SLEW RATE
vs
FREE-AIR TEMPERATURE

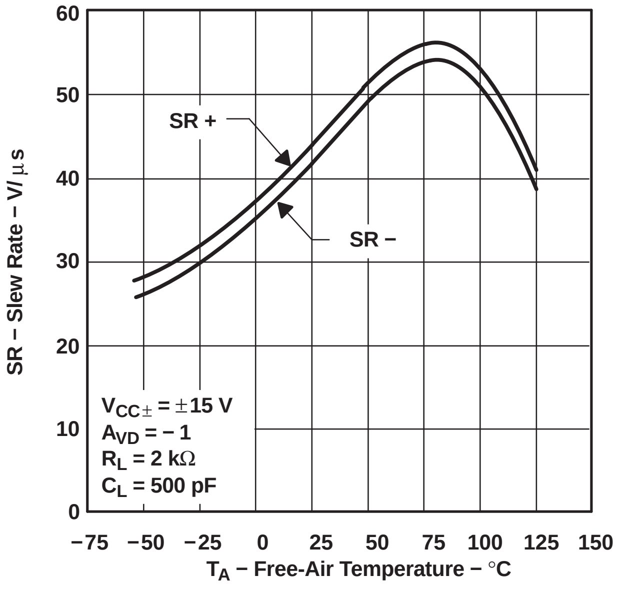

Figure 27.

SLEW RATE
vs
LOAD CAPACITANCE

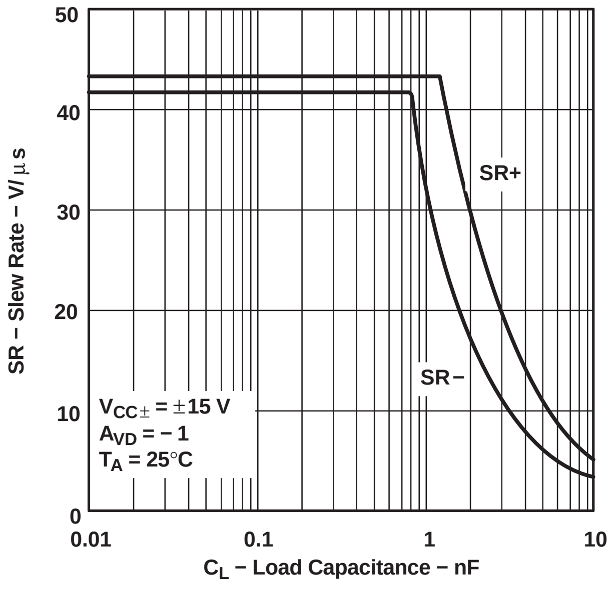

Figure 28.

NONINVERTING LARGE-SIGNAL PULSE RESPONSE

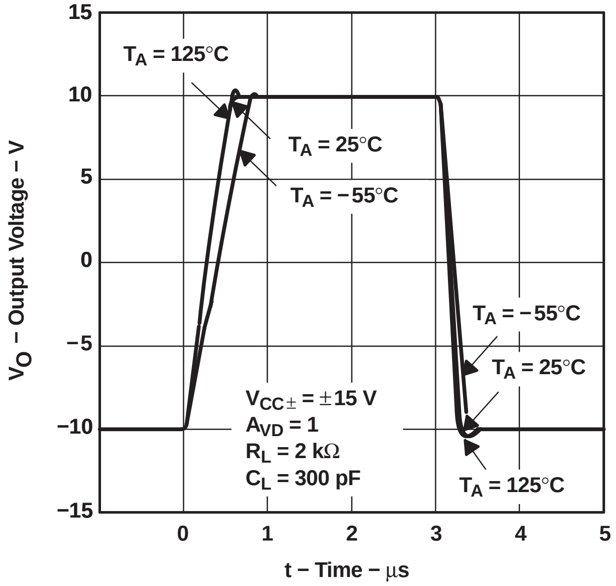

Figure 29.

INVERTING LARGE-SIGNAL PULSE RESPONSE

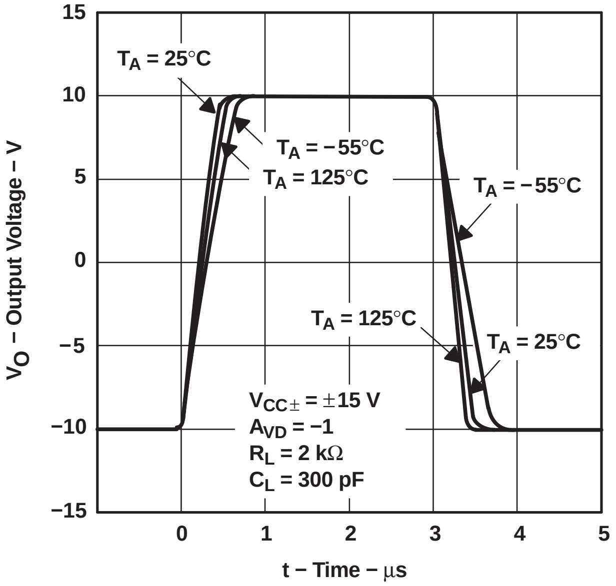

Figure 30.

SMALL-SIGNAL PULSE RESPONSE

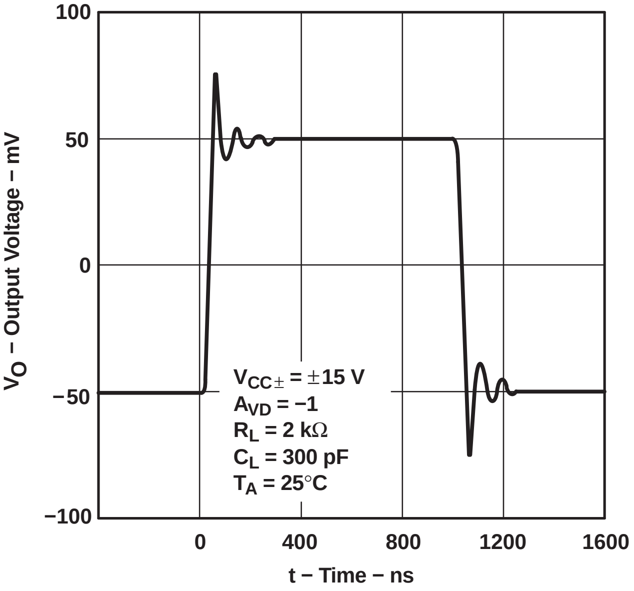

Figure 31.

UNITY-GAIN BANDWIDTH vs LOAD CAPACITANCE

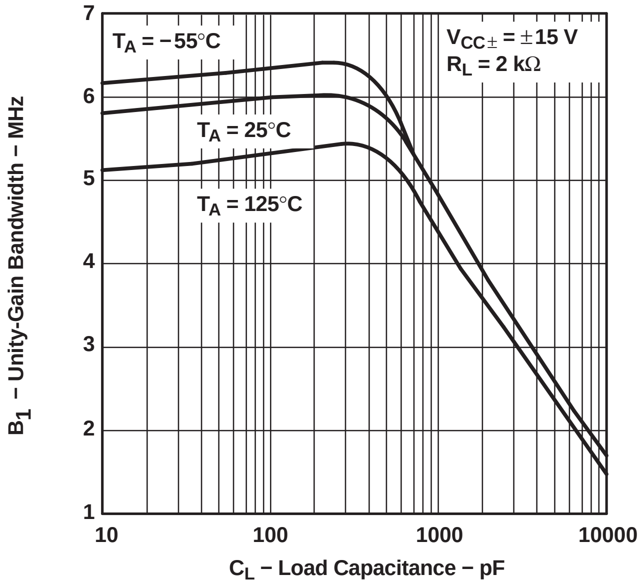

Figure 32.

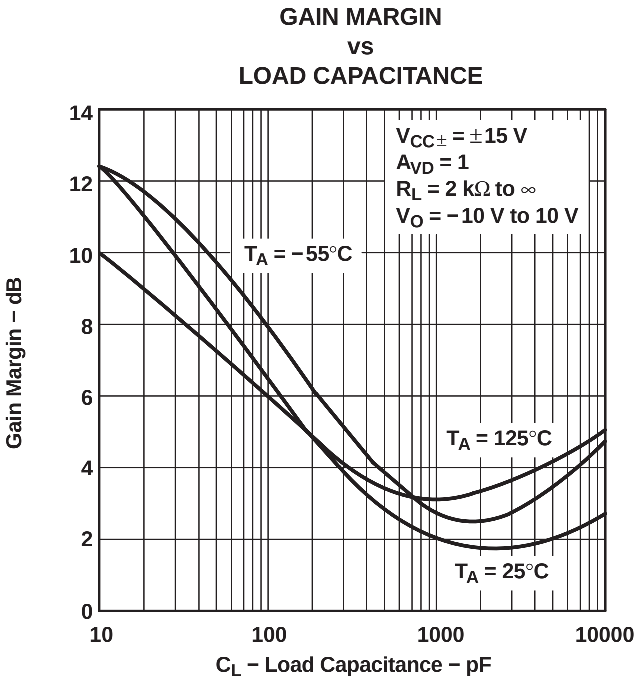

Figure 33.

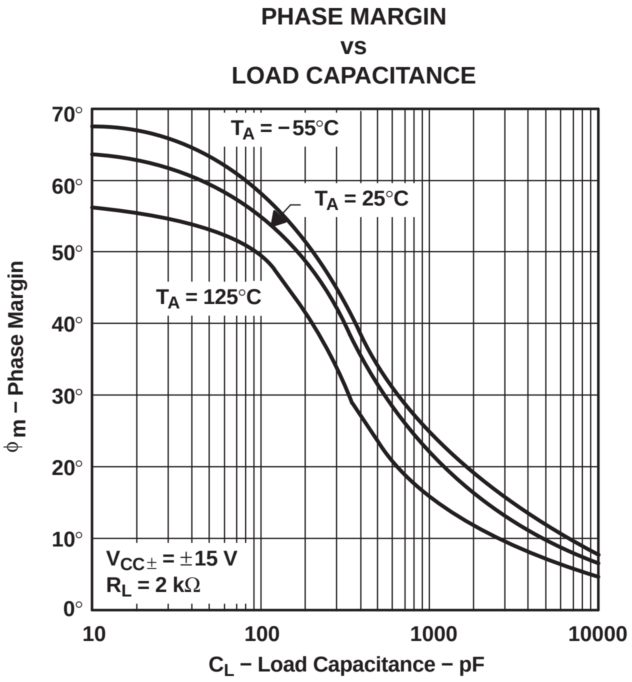

Figure 34.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TLE2142QDRQ1	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2142Q	Samples

[1] The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

[2] **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

[3] MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

[4] There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

[5] Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

[6] Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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OTHER QUALIFIED VERSIONS OF TLE2142-Q1 :

- Catalog: TLE2142
- Military: TLE2142M

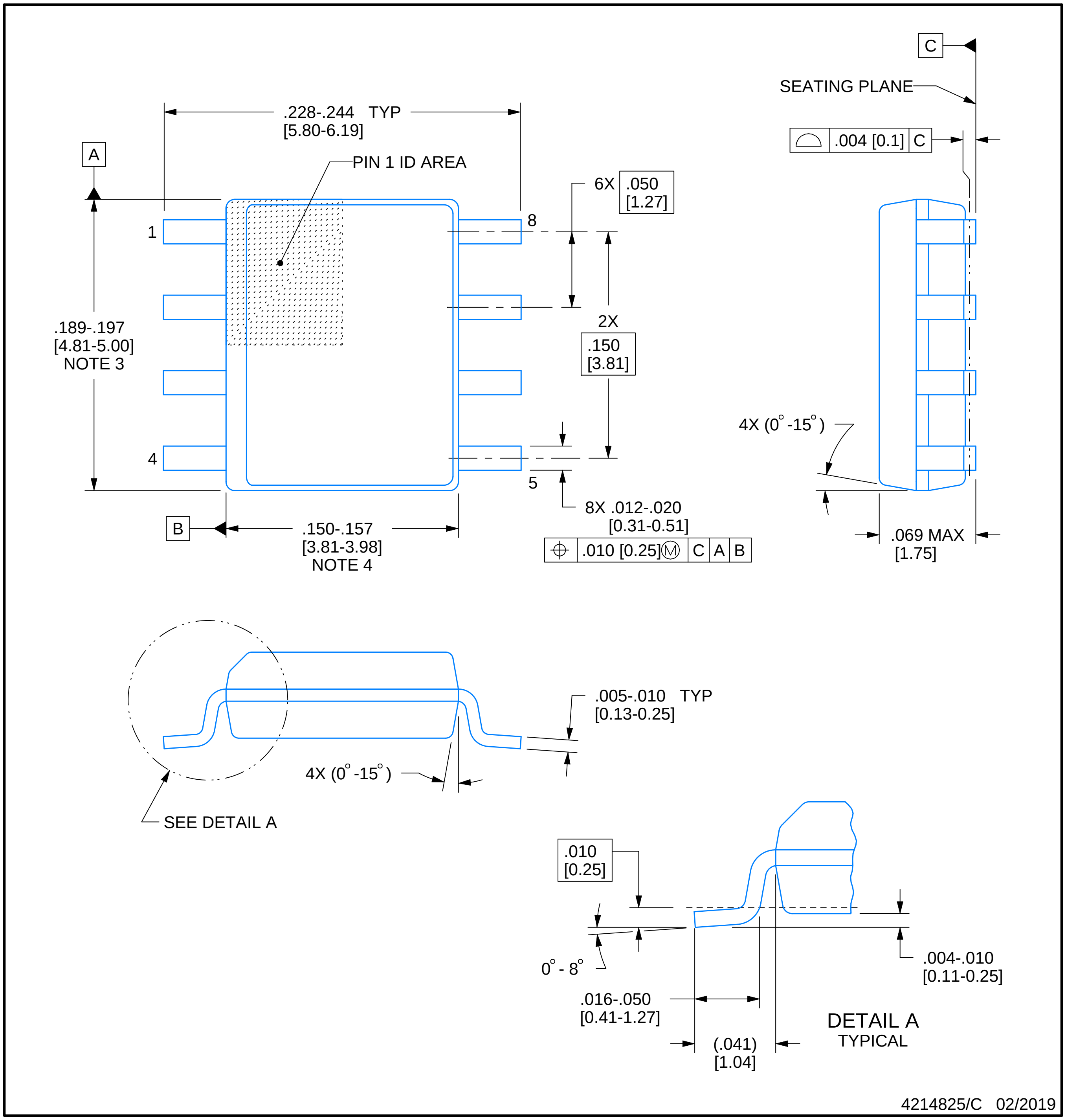
NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

PACKAGE OUTLINE

SOIC - 1.75 mm max height

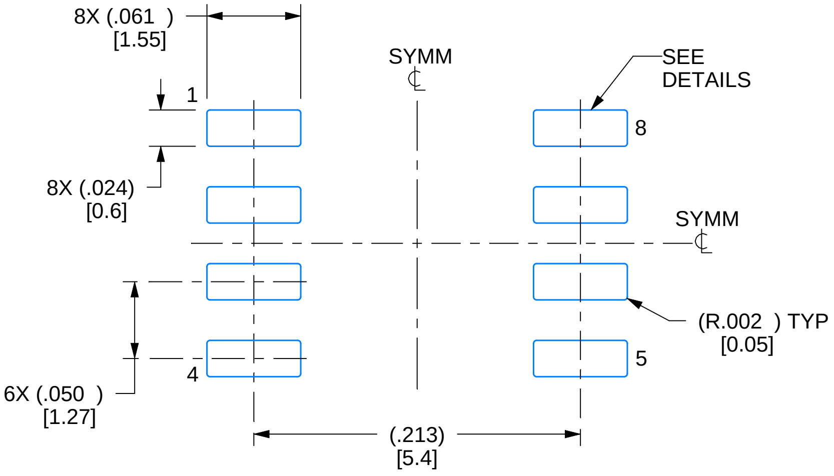
SMALL OUTLINE INTEGRATED CIRCUIT



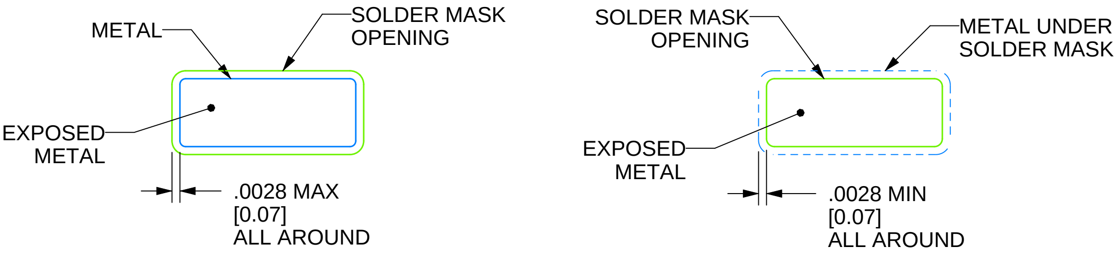
4214825/C 02/2019

NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



NON SOLDER MASK DEFINED

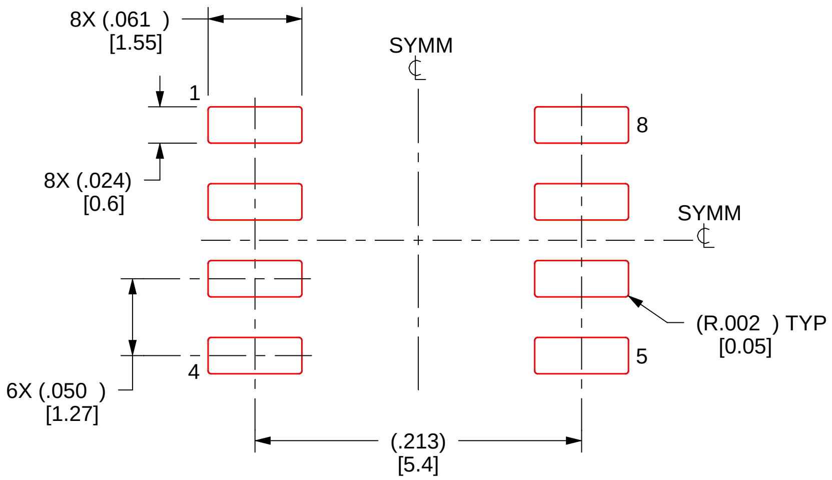
SOLDER MASK DEFINED

SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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